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Implementation of a Novel Variable Structure Nearest Level Modulation on Cascaded H-Bridge Multilevel Inverter

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ABSTRACT The output voltage of a Multilevel Inverter (MLI) can be controlled using various low and high frequency modulation strategy. Apart from meeting the load voltage demand, the modulation strategy also tries to reduce the harmonics present in the output voltage waveform. In this paper, a novel modulation strategy, a Variable Structure Nearest Level Modulation (VSNLM) has been proposed with the objective to reduce the Total Harmonic Distortion (THD) thus giving better output voltage quality and smoother control. The development of the mathematical model and subsequent analysis has been carried out. Moreover, the proposed modulation scheme has been implemented on 7, 9, 11, and 13 level Cascaded H Bridge inverter and a generalized mathematical model of the proposed scheme has been developed. A comparison of the proposed strategy with the conventional NLC is presented in the paper. The results confirm the superior performance of proposed strategy in terms of THD. Experimental results have also been presented for validation.

INDEX TERMS Nearest level control (NLC), variable structure nearest level modulation (VSNLM), total harmonic distortion (THD).

I. INTRODUCTION

The integration of renewable energy sources into the existing power system network had resulted in the increased reliability of the overall system. Solar and wind energy are the two leading contributors in the area of renewable energy. The integration of solar energy with the system requires the use of inverters which are basically dc to ac converters. Multilevel inverters are being used quite frequently in these applications owing to their special features such as less harmonic distortion, increased reliability, reduced interference. Apart from this, MLIs are also used in various other applications such as HVDC, drives, marine propulsion, FACTS etc. The conventional 2-level converter is not suitable for use in the mentioned applications as it has various drawbacks such as more harmonic distortion, reduced efficiency, less power quality etc. Keeping these points in consideration, the MLIs have served as a viable alternative to be used in various applications some of which are already mentioned here. Starting from the conventional MLI structures which are Flying Capacitor (FC), Neutral-Point Clamped (NPC) and Cascaded H-Bridge (CHB) MLIs, the development in this field has reached manifolds. Within a short span of time, lot of new MLI topologies were proposed by the researchers working in this area.

The modulation techniques are the basic building blocks in any MLI topology. In fact, it can be treated as a separate area of research to propose novel modulation technique which

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can be implemented in any topology in order to fulfill certain criteria. Modulation means controlling the power electronic switches in a manner intended to produce the desired output voltage waveform. Various modulation techniques are proposed in the literature to achieve a voltage waveform with improved power-quality. The resultant waveform has a lower value of THD. The efficiency of the MLI depends upon the modulation techniques. Broadly the modulation techniques for MLI can be divided into high frequency and low frequency. The high-frequency techniques eliminate the lower order harmonics and shift the other harmonics in the higher side-bands thus leading to a simpler filter design. The high-frequency (HF) reference-based techniques use a carrier wave of high frequency which is compared with a reference signal for the generation of switching pulses. Usually, the reference signal is a sinusoidal wave which is compared with high frequency triangular or trapezoidal wave. Based on the selection of reference the PWM methods can be classified as sinusoidal PWM (SPWM) and trapezoidal PWM. Some other reference-based PWM methods are third harmonic injection, 60° PWM [1]–[4]. The modified PWM techniques are used to eliminate particular harmonics in the output voltage waveform. To increase the RMS value of output voltage trapezoidal reference is sometimes used but SPWM remains the most popular choice. Based on the selection of carrier, HF modulation techniques can be level-shifted and phase-shifted PWM methods. These techniques utilize several carriers wave which differs either in-phase or levels. The phase-shifted PWM has an additional advantage of better distribution of power in the cells [5] along with reduced distortion in output voltage. Another HF scheme is space vector modulation however for the increased number of voltage levels, the scheme becomes complex and is difficult to implement.

The advantages of using Low frequency (LF) modulation techniques over the high-frequency methods are reduction in switching losses, low stress on switches, low cooling requirement as less heat is generated, better device utilization and increase in converter efficiency. Popular Low-frequency modulation techniques are selective harmonic elimination (SHE), [6] space vector control (SVC) [7] and nearest level control (NLC). The SVC is suitable for the higher number of levels which will minimise the space error of vectors with reference vector. In the SVC algorithm, a particular harmonic cannot be eliminated as can be done in the SHE algorithm. Using the SHE algorithm particular low order harmonics can be eliminated by appropriately determining the switching angles. A set of non-linear transcendental equations have to be solved in order to get switching angles. These equations can be solved by using any suitable heuristic algorithm. The SHE algorithm works well for open-loop operation but the algorithm cannot be implemented in real-time. Moreover, the technique is also heavily dependent on the modulation index. In the NLC technique, [8]–[11] the nearest voltage is level is generated by comparing a sinusoidal reference with constant carriers. The NLC is suitable for higher number of levels and in comparison to the SHE algorithm, its digital implementation is simple. In [12] and [13] the conventional NLC is modified by the authors for modular multilevel converters. As compared with the conventional NLC method the THD in output voltage and current is low. It is to be mentioned that modified NLC algorithms are not general and can only be applied to specific MLI topologies. In [14] a fundamental modulation technique using selective harmonic elimination (SHE) is proposed by the authors to generate 11 levels of voltage. The proposed technique works well for low modulation indices. In [15] a new modulation technique that combines the advantage of both level shifted and phase-shifted PWM techniques are proposed. The proposed technique has the advantage of equal power distribution in modules [16] as well as low THD in output voltage. The authors in [17] have proposed an 11 level MLI topology that utilizes SHE for the removal of lower-order odd harmonics. A projectile target algorithm is used to solve the non-linear transcendental equations. The results are verified through real-time hardware in loop simulations. Some more topologies which utilize SHE modulation technique are discussed in [18]–[21]. A comprehensive review of different modulation techniques for traction purposes is presented in [22]. When the number of levels are low, NLC can easily applied in comparison to SHE. However, for low number of levels, the performance of conventional NLC deteriorates and the THD in output voltage is high. Model predictive control is used to implement modified NLC in a modular multilevel converter proposed in [23]. In [24] a control method based on SPWM is used to balance and minimize the deviations in the capacitor voltage of a 4 level MLI. The SPWM is simple to implement however, the THD obtained is 24.7% [24] which is high as per IEEE-standards. Phase shifted PWM modulation technique is used in [25] to generate a staircase voltage waveform for a cascaded MLI topology. In [26] an improved NLC method for MLI is proposed and it is found that for the same number of sub modules the number of level increases which reduces the THD in the output voltage. In [27] a hybrid modulation technique based on PWM and Pulse amplitude modulation for grid connected inverter is proposed by authors. The proposed hybrid modulation technique results in increased efficiency of the converter. 15-levels are generated in [28] using NLC switching technique.

This paper explains and implements a novel variable structure nearest level modulation scheme for controlling the output voltage waveform of a Multilevel Inverter. The features of the proposed scheme are:

1. Mathematical model developed to minimize the THD at a particular modulation index.
2. Generalization extended for 'N' levels.
3. Incorporate the good feature of NLC while providing optimal THD operation
4. Ease of implementation

Section II deals with the implementing the proposed modulation scheme on the CHB inverter for different number of levels. Section III discusses the developed mathematical

TABLE 1. 7-level switching sequence.

ON Switches	OFF switches	Vo
1, 4, 6 and 8	2, 3, 5 and 7	V
2, 4, 5 and 8	1, 3, 6 and 7	2V
1, 4, 5 and 8	2, 3, 6 and 7	3V
2, 4, 6 and 8	1, 3, 5 and 7	0
2, 3, 6 and 8	1, 4, 5 and 7	-V
2, 4, 6 and 7	1, 3, 5 and 8	-2V
2, 3, 6 and 7	1, 4, 5 and 8	-3V

TABLE 2. 9-level switching sequence.

ON Switches	OFF switches	Vo
1, 4, 6 and 8	2, 3, 5 and 7	V
2, 3, 5 and 8	1, 4, 6 and 7	2V
2, 4, 5 and 8	1, 3, 6 and 7	3V
1, 3, 5 and 8	2, 4, 6 and 8	4V
2, 4, 6 and 8	1, 3, 5 and 7	0
2, 3, 6 and 8	1, 4, 5 and 7	-V
1, 4, 6 and 7	2, 3, 5 and 8	-2V
2, 4, 6 and 7	1, 3, 5 and 8	-3V
2, 3, 6 and 7	1, 4, 5 and 8	-4V

TABLE 3. 11-level switching sequence.

ON Switches	OFF switches	Vo
1,4,6,8,10 and 12	2,3,5,7,9 and 11	V
2,4,5,8,10 and 12	1,3,6,7,9 and 11	2V
1,4,5,8,10 and 12	2,3,6,7,9 and 11	3V
2,4,5,8,9 and 12	1,3,6,7,10 and 11	4V
1,4,5,8,9 and 12	2,3,6,7,10 and 11	5V
2,4,6,8,10 and 12	1,3,5,7,9 and 11	0
2,3,6,8,10 and 12	1,4,5,7,9 and 11	-V
2,4,6,7,10 and 12	1,3,5,8,9 and 11	-2V
2,3,6,7,10 and 12	1,4,5,8,9 and 11	-3V
2,4,6,7,10 and 11	1,3,5,8, 9 and 12	-4V
2,3,6,7,10 and 11	1,4,5,8 9 and 12	-5V

analysis and explanation of the VSNLM strategy. The analysis is done for 7,9,11 and 13-level outputs. To justify the merits of the proposed method its comparison has been done with conventional NLC and it is shown in section IV of the paper. The experimental implementation and results of the proposed scheme has been done and the obtained results has been shown and explained in section V. Finally, section VI contains the conclusion.

II. IMPLEMENTATION OF THE PROPOSED STRATEGY ON CHB

The generalized circuit structure of cascaded h-bridge (CHB) inverter has been shown in Fig. 1(a). One unit of h-bridge contains one dc source and 4 switches. For 'k' number of units, we can obtain the structure for 7-level, 9-level, 11-level and 13-level CHB by selecting different values of V_k. The switching sequences are presented in Table 1, 2, 3 and 4.

TABLE 4. 13-level switching sequence.

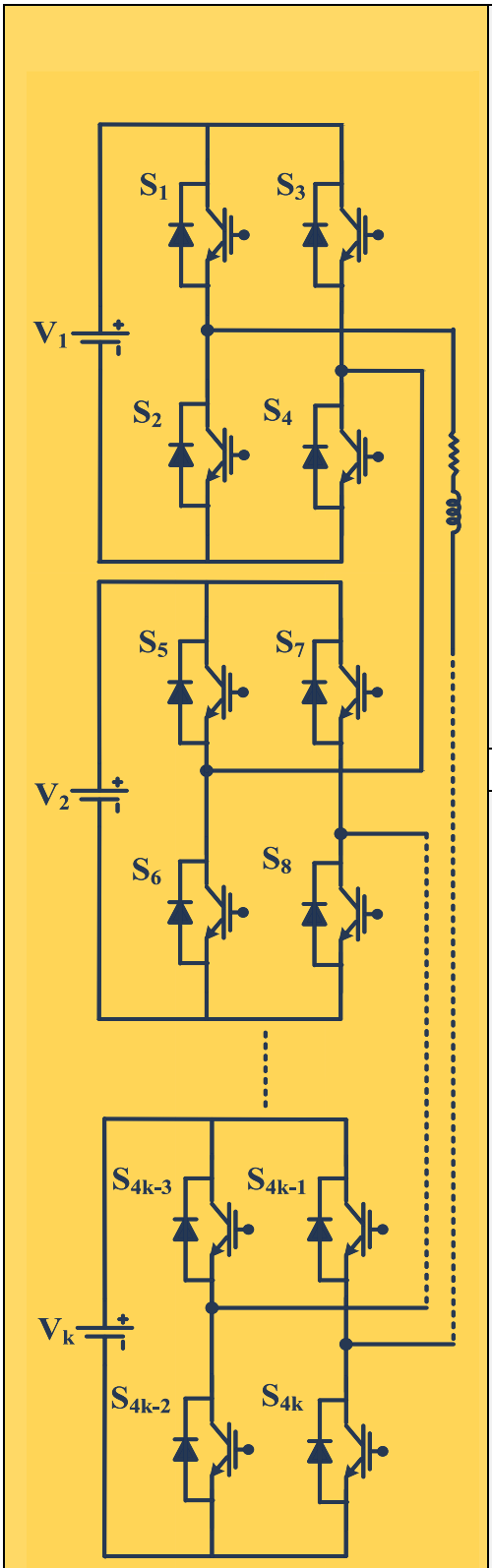
ON Switches	OFF switches	Vo
1,4,6,8,10 and 12	2,3,5,7,9 and 11	V
2,4,5,8,10 and 12	1,3,6,7,9 and 11	2V
1,4,5,8,10 and 12	2,3,6,7,9 and 11	3V
1,4,6,8,9 and 12	2,3,5,7,10 and 11	4V
2,4,5,8,9 and 12	1,3,6,7,10 and 11	5V
1,4,5,8,9 and 12	2,3,6,7,10 and 11	6V
2,4,6,8,10 and 12	1,3,5,7,9 and 11	0
2,3,6,8,10 and 12	1,4,5,7,9 and 11	-V
2,4,6,7,10 and 12	1,3,5,8,9 and 11	-2V
2,3,6,7,10 and 12	1,4,5,8,9 and 11	-3V
2,3,6,8,10 and 11	1,4,5,7,9 and 12	-4V
2,4,6,7,10 and 11	1,3,5,8,9 and 12	-5V
2,3,6,7,10 and 11	1,4,5,8,9 and 12	-6V

The proposed VSNLM strategy is implemented on the 7-level, 9-level, 11-level and 13-level CHB. 7-level and 9-level CHB inverters can be implemented by using 2 H-bridge units. The magnitude of dc sources are $V_1 = V$ and $V_2 = 2V$ whereas in 9-level CHB the required magnitude of dc sources are $V_1 = V$ and $V_2 = 3V$. 3 units are required for 11-level and 13-level CHB inverters respectively and hence there will be 3 dc sources. In 11-level CHB, dc sources are $V_1 = V$, $V_2 = V_3 = 2V$. However, in 13-level, the dc sources of magnitudes $V_1 = V$, $V_2 = 2V$ and $V_3 = 3V$ have to be used.

III. PROPOSED VARIABLE STRUCTURE NEAREST LEVEL MODULATION (VSNLM) STRATEGY

In this section, proposed variable structure nearest level modulation has been discussed. The implementation scheme for 7, 9, 11 and 13-levels CHB inverter has been developed. The equations pertaining to proposed modulation scheme for minimum THD operation has also been developed with the help of MATLAB codes shown in Fig. 1(b) – 1(e).

In the conventional nearest level control modulation strategy, the level changes once the reference sinusoidal wave value $\frac{n-1}{2} msin(\omega t)$, where m is the modulation index and n is the output voltage levels, crosses the constant dc values of 0.5, 1.5 (1+0.5), 2.5 (2+0.5), 3.5 (3+0.5), ... $\frac{n-1}{2} + 0.5$ respectively. When $\frac{n-1}{2} msin(\omega t)$ increases and becomes greater than 0.5, the switching state of the MLI changes and the output voltage level changes from 0 to V. The level changes from V to 2V when the reference wave $\frac{n-1}{2} msin(\omega t)$ becomes greater than 1.5 and switching state corresponding to 2V is triggered. Similarly all the output levels are generated. The NLC implementation strategy is shown in Fig. 2 (a). In the proposed variable structure nearest level modulation strategy, the constant dc value of 0.5 (in case of conventional NLM) is replaced by a variable parameter $'g'$. The value of g can vary from 0 to 1 (Although there is a lower limit on g for each level generation which is discussed in the next subsection). Then a code is executed to find the value of g corresponding to each m (in step size of 0.01), which would result in minimum THD. The waveform for the implementation of the VSNLM is shown in Fig. 2 (b). The generalized expression for THD



(a)

Start
Clear Workspace
initialize $j = 0$
$for\ m = \frac{2}{3} : 0.01 : 1$
Execute the Following Instructions
$i = 0$
$j = j + 1$
$s(j) = m$
$for\ b = 0 : 0.001 : 3m - 2$
Execute the following instructions
$i = i + 1;$
$g(i) = b$
$\alpha_1(i) = \sin^{-1}\frac{g(i)}{4m}$
$\alpha_2(i) = \sin^{-1}\frac{1 + g(i)}{4m}$
$\alpha_3(i) = \sin^{-1}\frac{2 + g(i)}{4m}$
$THD(i) = Expression\ \mathrm{A}$
end
$A(j) = \min(T)$
$M(j) = 0.001 * find(T == A(j))$
$plot(M, s)$

end

(b)

Start
Clear Workspace
initialize $j = 0$
$for\ m = \frac{3}{4} : 0.01 : 1$
Execute the Following Instructions
$i = 0$
$j = j + 1$
$s(j) = m$
$for\ b = 0 : 0.001 : 4m - 3$
Execute the following instructions
$i = i + 1;$
$g(i) = b$
$\alpha_1(i) = \sin^{-1}\frac{g(i)}{4m}$
$\alpha_2(i) = \sin^{-1}\frac{1 + g(i)}{4m}$
$\alpha_3(i) = \sin^{-1}\frac{2 + g(i)}{4m}$
$\alpha_4(i) = \sin^{-1}\frac{3 + g(i)}{4m}$
$THD(i) = Expression\ \mathrm{B}$
end
$A(j) = \min(T)$
$M(j) = 0.001 * find(T == A(j))$
$plot(M, s)$

end

(c)

Start
Clear Workspace
initialize $j = 0$
$for\ m = \frac{4}{5} : 0.01 : 1$
Execute the Following Instructions
$i = 0$
$j = j + 1$
$s(j) = m$
$for\ b = 0 : 0.001 : 5m - 4$
Execute the following instructions
$i = i + 1;$
$g(i) = b$
$\alpha_1(i) = \sin^{-1}\frac{g(i)}{4m}$
$\alpha_2(i) = \sin^{-1}\frac{1 + g(i)}{4m}$
$\alpha_3(i) = \sin^{-1}\frac{2 + g(i)}{4m}$
$\alpha_4(i) = \sin^{-1}\frac{3 + g(i)}{4m}$
$\alpha_5(i) = \sin^{-1}\frac{4 + g(i)}{4m}$
$THD(i) = Expression\ C$
end
$A(j) = \min(T)$
$M(j) = 0.001 * find(T == A(j))$
$plot(M, s)$

end

(d)

Start
Clear Workspace
initialize $j = 0$
$for\ m = \frac{5}{6} : 0.01 : 1$
Execute the Following Instructions
$i = 0$
$j = j + 1$
$s(j) = m$
$for\ b = 0 : 0.001 : 6m - 5$
Execute the following instructions
$i = i + 1;$
$g(i) = b$
$\alpha_1(i) = \sin^{-1}\frac{g(i)}{4m}$
$\alpha_2(i) = \sin^{-1}\frac{1 + g(i)}{4m}$
$\alpha_3(i) = \sin^{-1}\frac{2 + g(i)}{4m}$
$\alpha_4(i) = \sin^{-1}\frac{3 + g(i)}{4m}$
$\alpha_5(i) = \sin^{-1}\frac{4 + g(i)}{4m}$
$\alpha_6(i) = \sin^{-1}\frac{5 + g(i)}{4m}$
$THD(i) = Expression\ D$
end
$A(j) = \min(T)$
$M(j) = 0.001 * find(T == A(j))$
$plot(M, s)$
end

(e)

FIGURE 1. (a) Circuit diagram of an N level CHBMLI. (b) Pseudo code obtaining (m, g) relation for a 7 Level CHBMLI. (c) Pseudo code obtaining (m, g) relation for a 9 Level CHBMLI. (d) Pseudo code obtaining (m, g) relation for a 11 Level CHBMLI. (e) Pseudo code obtaining (m, g) relation for a 13 Level CHBMLI.

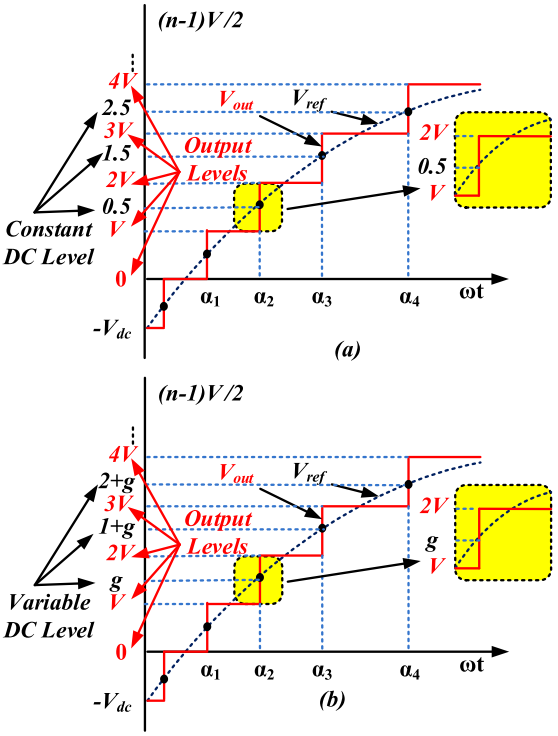


FIGURE 2. (a) Implementation of an n level CHBMLI using with the NLC scheme. (b) Implementation of an n level CHBMLI using with the VSNLM scheme.

has been taken from [29]. The THD expression for 7, 9, 11, and 13 can be obtained from the general expression and is given by expressions (A) to (D), as shown at the bottom of the page. The inbuilt function (''min'') from the MATLAB library has been taken to find the value of g where minimum THD in the output voltage is observed. These data sets of (m, g) is then plotted to obtain the mathematical relation between (m, g).

A. 7-LEVEL OUTPUT

The set of equations for implementing the VSNLM scheme are given by eq. (1) - eq. (3).

$$3msin\,(\alpha_1) = g \tag{1}$$

$$3msin\,(\alpha_2) = 1 + g \tag{2}$$

$$3msin\,(\alpha_3) = 2 + g \tag{3}$$

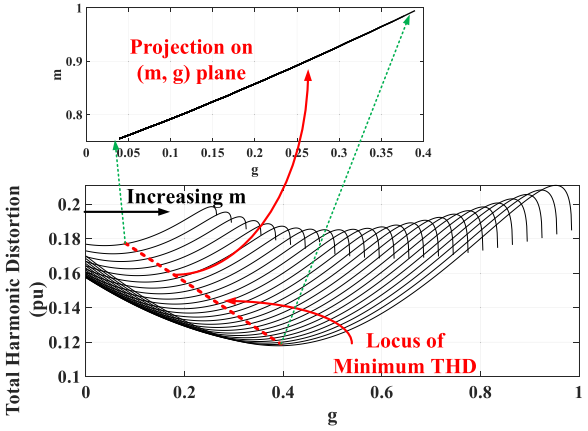


FIGURE 3. Obtaining the relation between the optimal (m, g) pair for 7 level when m varies from 2/3 to 1 in step of 0.01.

Here, $\alpha_i (i = 1, 2, 3)$ are the switching angles and g is the variable DC level of the VSNLM. Its value varies from 0 – 1.

The THD expression given in eq. (A)-(D) has been taken from [29] and calculated for harmonics upto 49. For a given value of modulation index m, g could be found out by minimizing THD expression given in eq. (A). Consequently, for all values of m between (0, 1), corresponding values of g is obtained for minimum THD. The set of (m, g) points can be used to obtain the relation between m and g (Fig. 3), which is given by the Eq. (4) and Eq. (5)

$$g = 1.37m - 0.97(for\ m > \frac{2}{3}) \tag{4}$$

$$g = 1.38m - 0.52(for \frac{1}{3} < m < \frac{2}{3}) \tag{5}$$

Eq. (5) results when the levels in the output decreases to five because of lower value of modulation index. Constraints in the brackets after the eq. (4) and (5) has been obtained from the eq. (6) and (7) respectively.

$3m > 3msin\,(\alpha_3)$ $(sin\,(\alpha_3)$ is less than 1)

$or 3m > 2 + g (From\ eq.1)$

$or 3m > 2$ (As maximum value of g could be 1)

$$or\ m > \frac{2}{3} \tag{6}$$

Also from eq.(1)

$g < 3m\,(sin\,(\alpha_1)$ is less than 1)

$$THD_{7L} = \sqrt{\left(\frac{\pi^2}{8}\right).\frac{9V_{dc}^2 - \frac{2}{\pi}\left[\alpha_1 V_{dc}^2 + 3\alpha_2 V_{dc}^2 + 5\alpha_3 V_{dc}^2\right]}{(V_{dc}cos\alpha_1 + V_{dc}cos\alpha_2 + V_{dc}cos\alpha_3)^2} - 1} \tag{A}$$

$$THD_{9L} = \sqrt{\left(\frac{\pi^2}{8}\right).\frac{16V_{dc}^2 - \frac{2}{\pi}\left[\alpha_1 V_{dc}^2 + 3\alpha_2 V_{dc}^2 + 5\alpha_3 V_{dc}^2 + 7\alpha_4 V_{dc}^2\right]}{(V_{dc}cos\alpha_1 + V_{dc}cos\alpha_2 + V_{dc}cos\alpha_3 + V_{dc}cos\alpha_4)^2} - 1} \tag{B}$$

$$THD_{11L} = \sqrt{\left(\frac{\pi^2}{8}\right).\frac{25V_{dc}^2 - \frac{2}{\pi}\left[\alpha_1 V_{dc}^2 + 3\alpha_2 V_{dc}^2 + 5\alpha_3 V_{dc}^2 + 7\alpha_4 V_{dc}^2 + 9\alpha_5 V_{dc}^2\right]}{(V_{dc}cos\alpha_1 + V_{dc}cos\alpha_2 + V_{dc}cos\alpha_3 + V_{dc}cos\alpha_4 + V_{dc}cos\alpha_5)^2} - 1} \tag{C}$$

$$THD_{13L} = \sqrt{\left(\frac{\pi^2}{8}\right).\frac{36V_{dc}^2 - \frac{2}{\pi}\left[\alpha_1 V_{dc}^2 + 3\alpha_2 V_{dc}^2 + 5\alpha_3 V_{dc}^2 + 7\alpha_4 V_{dc}^2 + 9\alpha_5 V_{dc}^2 + +11\alpha_6 V_{dc}^2\right]}{(V_{dc}cos\alpha_1 + V_{dc}cos\alpha_2 + V_{dc}cos\alpha_3 + V_{dc}cos\alpha_4 + V_{dc}cos\alpha_5 + V_{dc}cos\alpha_6)^2} - 1} \tag{D}$$

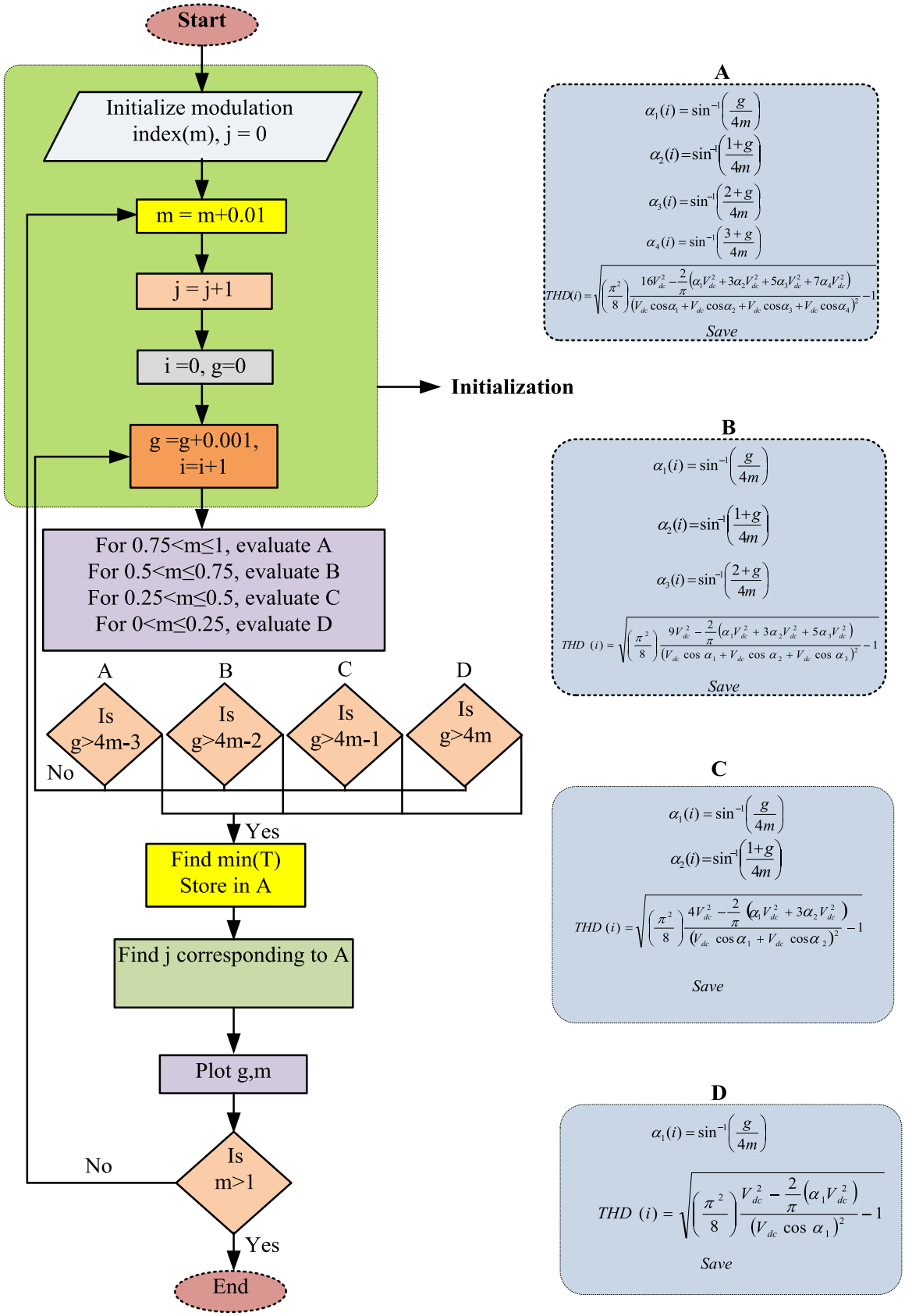


FIGURE 4. VSNLM Flowchart for 9-level output.

Hence $3m > 1$ (As maximum value of g is 1)

$$\text{Or } m > \frac{1}{3} \tag{7}$$

Eq. (6) and (7) put constraint on the values of g and m

Pseudo code for obtaining the $f(g) = m$ with the constraints of eq. (6) and (7) has been shown in Fig.1 (b).

B. 9-LEVEL OUTPUT

The set of equations for implementing the VSNLM scheme are given by eq. (8) – (12).

$$4msin(\alpha_1) = g \tag{8}$$
$$4msin(\alpha_2) = 1 + g \tag{9}$$
$$4msin(\alpha_3) = 2 + g \tag{10}$$
$$4msin(\alpha_4) = 3 + g \tag{11}$$

For a given value of m, g could be found out by minimizing THD expression given in eq. (B). Consequently, for all values of m between (0, 1), corresponding values of g is obtained for minimum THD. The set of (m, g) points can be used to obtain the relation between m and g, which is given by eq.(12)-(15).

$$g = 2m - 1.58 \left(\text{for m} > \frac{3}{4}\right) \tag{12}$$
$$g = 1.887m - 1.01 \left(\text{for} \frac{1}{2} < \text{m} < \frac{3}{4}\right) \tag{13}$$
$$g = 1.818m - 0.518 \left(for \frac{1}{4} < m < \frac{1}{2}\right) \tag{14}$$
$$g = 1.613m - 0.0064 \left(\text{form} < \frac{1}{4}\right) \tag{15}$$

Constraint in eq. (12) in the brackets can be obtained from 16.

$4m > 4msin(\alpha_4)$ ($sin(\alpha_4)$ is less than 1)

or $4m > 3 + g$(*From eq.*11)

or $4m > 3$ (As maximum value of g could be 1)

$$or\ m > \frac{3}{4} \tag{16}$$

Also from eq. (8)

$g < 4m$ ($sin(\alpha_1)$ is less than 1)

Hence $4m > 1$ (As maximum value of g is 1)

$$\text{Or } m > \frac{1}{4} \tag{17}$$

Similarly other constraints can be found out. Eq. (16) and (17) put constraint on the values of g corresponding to m. Eq. (13-(15) are for the modulation index defined in the brackets as levels in output voltage reduces to 7, 5, 3 respectively.

Pseudo code for obtaining the $f(g) = m$ with the constraints of eq. (16) and (17) has been depicted in Fig. 1(c).

The flowchart for the implementation of the scheme discussed in the paper for 9-level output has been shown in Fig. 4.

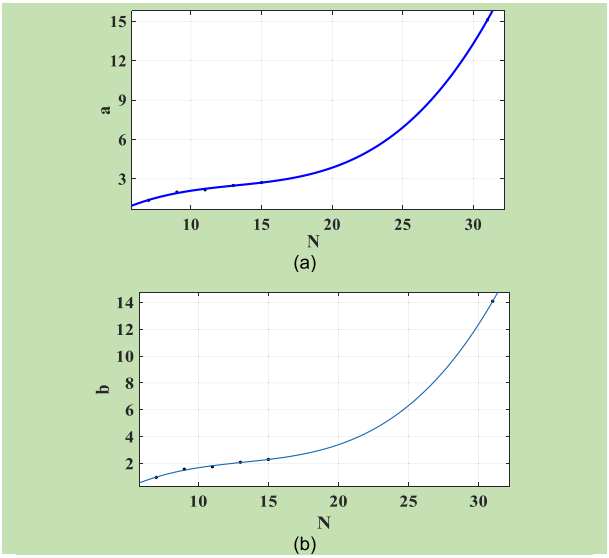


FIGURE 5. Variation of (a) parameter 'a' (b) parameter 'b' against N.

C. 11-LEVEL OUTPUT

The set of equations for implementing the VSNLC scheme are given by eq.(18)-(22).

$$5msin(\alpha_1) = g \tag{18}$$
$$5msin(\alpha_2) = 1 + g \tag{19}$$
$$5msin(\alpha_3) = 2 + g \tag{20}$$
$$5msin(\alpha_4) = 3 + g \tag{21}$$
$$5msin(\alpha_5) = 4 + g \tag{22}$$

For a given value of m, g could be found out by minimizing THD expression as given by eq. (C). Consequently, for all values of m between (0, 1), corresponding values of g is obtained for minimum THD. The set of (m, g) points can be used to obtain the relation between m and g, which is given by the eq. (23)-(25)

$$g = 2.17m - 1.76 \left(for\ m > \frac{4}{5}\right) \tag{23}$$
$$g = 2.27m - 1.41 \left(for \frac{3}{5} < m < \frac{4}{5}\right) \tag{24}$$
$$g = 2.38m - 1.02 \left(for \frac{2}{5} < m < \frac{3}{5}\right) \tag{25}$$

Constraint in eq. (23) in the brackets can be obtained from 26.

$5m > 5msin(\alpha_5)$ ($sin(\alpha_3)$ is less than 1)

or $5m > 4 + g$(*From Eq.*22)

or $5m > 4$ (As maximum value of g could be 1)

$$or\ m > \frac{4}{5} \tag{26}$$

Also from eq. (18)

$g < 5m$ ($sin(\alpha_1)$ is less than 1)

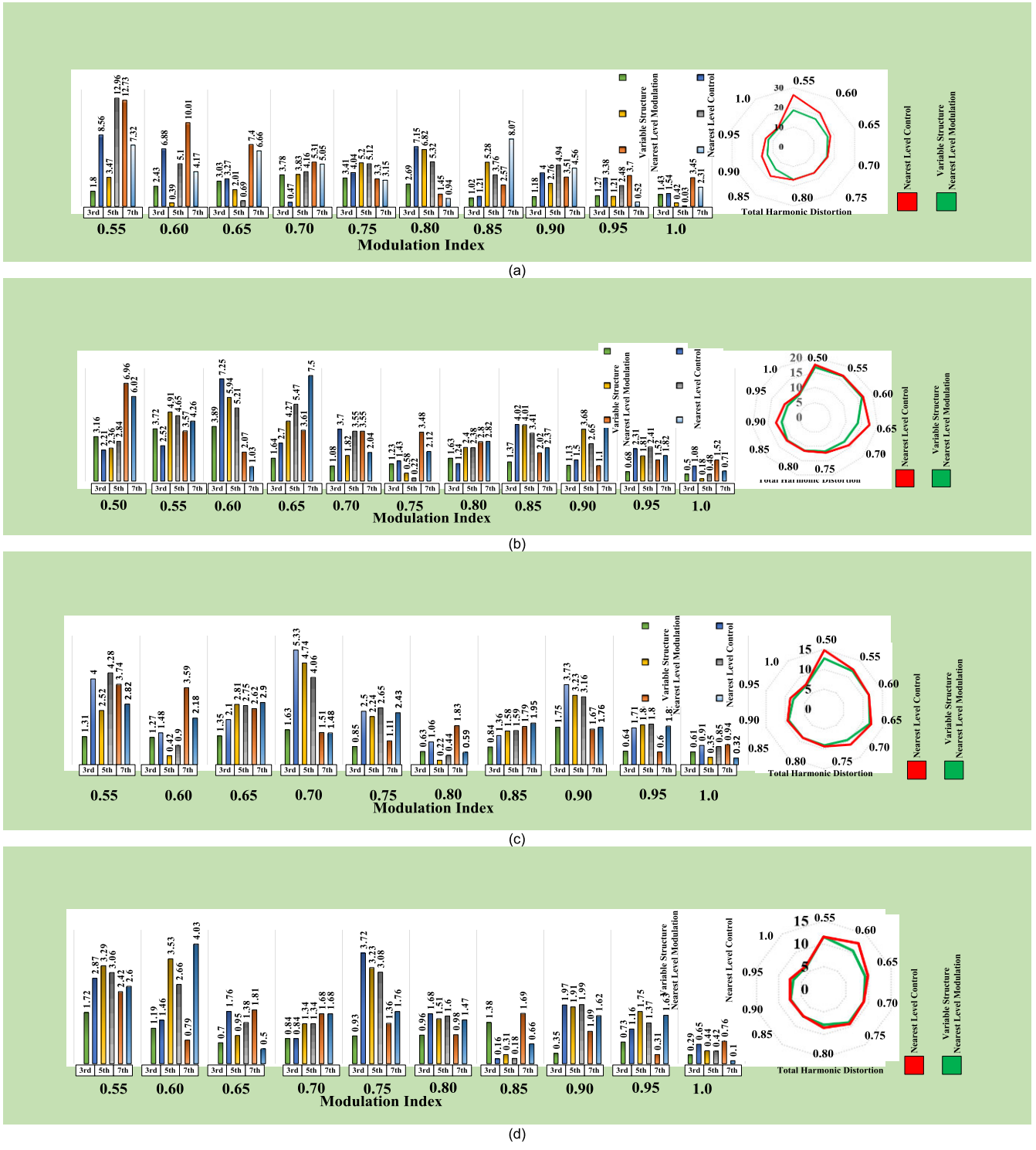


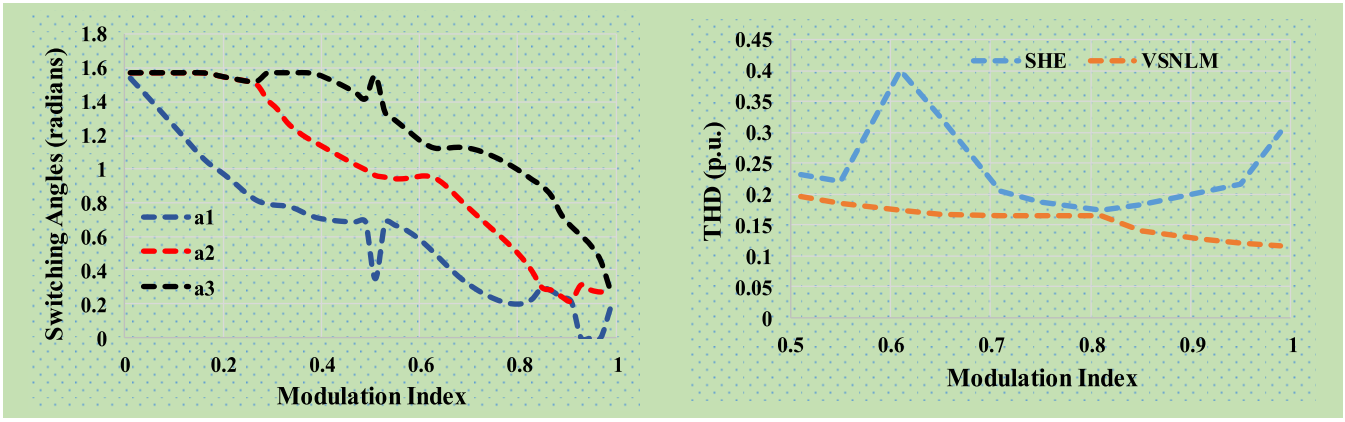
FIGURE 6. Comparative analysis of the proposed strategy.

Hence $5m > 1$ (As maximum value of g is 1)

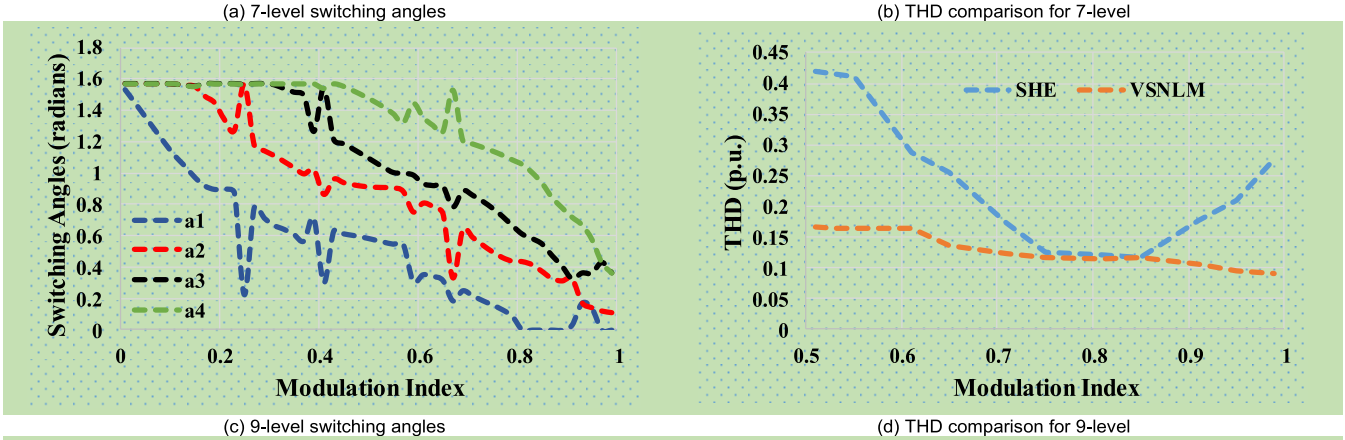
$$\text{Or } m > \frac{1}{5} \tag{27}$$

Similarly other constraints can be found out. Eq. (26) and (27) put constraint on the values of g corresponding to m.

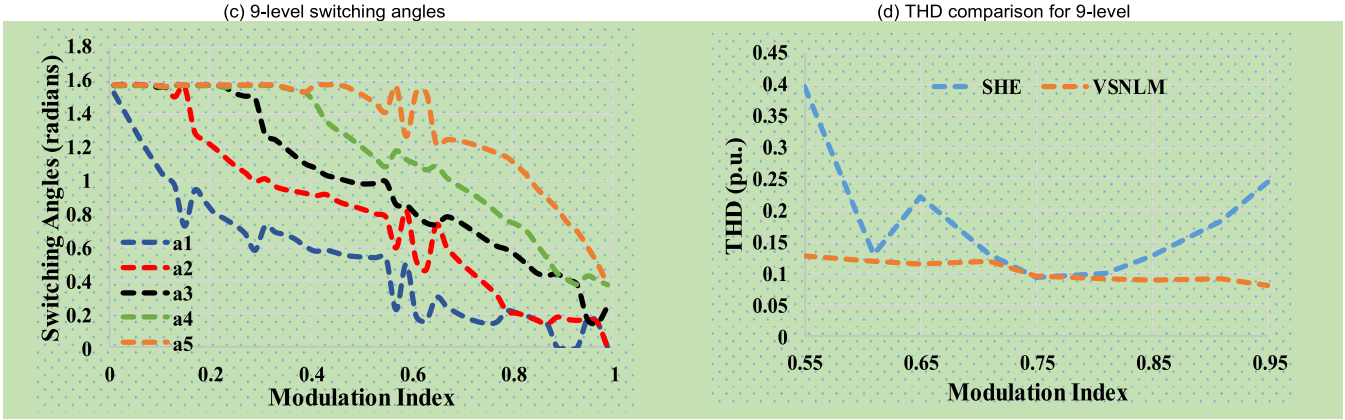
Eq. (24) - (25) are for the modulation index defined in the brackets as levels in output voltage reduces to 9, 7 respectively. Pseudo code for obtaining the $f(g) = m$ with the constraints of eq. (26) and (27) is presented in Fig. 1(d).



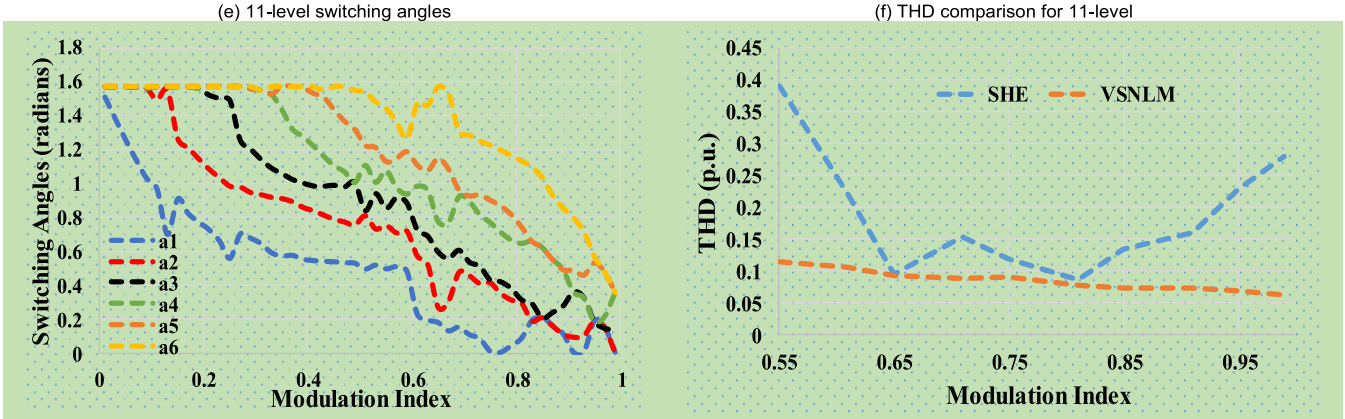
(a) 7-level switching angles (b) THD comparison for 7-level



(c) 9-level switching angles (d) THD comparison for 9-level



(e) 11-level switching angles (f) THD comparison for 11-level



(g) 13-level switching angles (h) THD comparison for 13-level

FIGURE 7. Comparison of SHEPWM with proposed VSNLM.

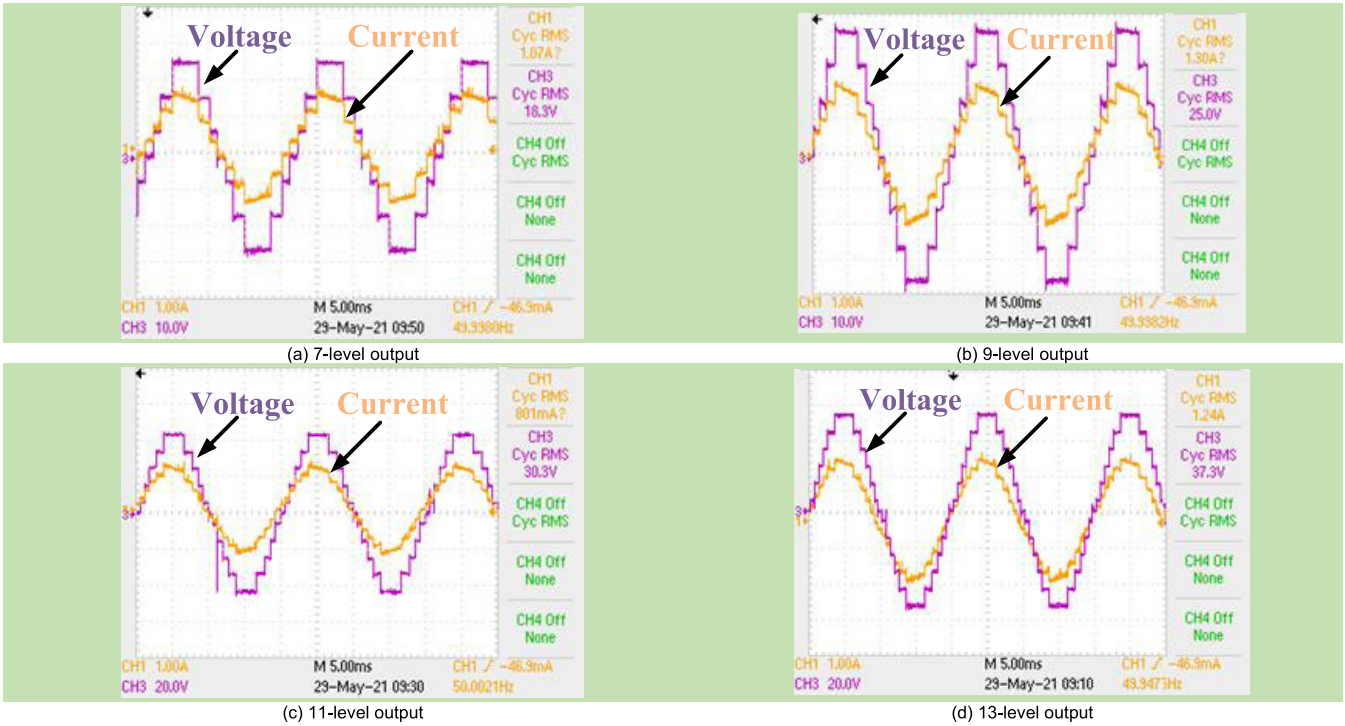


FIGURE 8. Load voltage and current waveforms.

D. 13-LEVEL OUTPUT

The set of equations for implementing the VSNLM scheme are given by eq. (28)-(33).

$$6msin\,(\alpha_1) = g \tag{28}$$
$$6msin\,(\alpha_2) = 1 + g \tag{29}$$
$$6msin\,(\alpha_3) = 2 + g \tag{30}$$
$$6msin\,(\alpha_4) = 3 + g \tag{31}$$
$$6msin\,(\alpha_5) = 4 + g \tag{32}$$
$$6msin\,(\alpha_6) = 5 + g \tag{33}$$

For a given value of m, g could be found out by minimizing THD expression given by Eq. (D). Consequently, for all values of m between (0, 1), corresponding values of g is obtained for minimum THD. The set of (m, g) points can be used to obtain the relation between m and g, which is given by the eq. (34)-(37).

$$g = 2.5m - 2.1\left(for\ m > \frac{5}{6}\right) \tag{34}$$
$$g = 2.63m - 1.79(for \frac{2}{3} < m < \frac{5}{6}) \tag{35}$$
$$g = 2.78m - 1.44\left(for \frac{1}{2} < m < \frac{2}{3}\right) \tag{36}$$
$$g = 2.85m - 1.02\left(for \frac{1}{3} < m < \frac{1}{2}\right) \tag{37}$$

Constraint in eq. (34) in the brackets can be obtained from (38).

$6m > 6msin\,(\alpha_6)$ ($sin\,(\alpha_6)$ is less than 1)
$or\ 6m > 5 + g(FromEq.33)$
$or\ 6m > 5$ (As maximum value of g could be 1)

$$or\ m > \frac{5}{6} \tag{38}$$

Also from eq.(18)
$g < 6m$ ($sin\,(\alpha_1)$ is less than 1)
Hence $6m > 1$ (As maximum value of g is 1)

$$\text{Or } m > \frac{1}{6} \tag{39}$$

Similarly other constraints can be found out. Eq (38) and (39) put constraint on the values of g corresponding to m.

Eq. (35)-(37) are for the modulation index defined in the brackets as levels in output voltage reduces to 11, 9, 7 the brackets as levels in output voltage reduces to 11, 9, 7 respectively. Fig. 1(e) represents the Pseudo code for obtaining the $f(g) = m$ with the constraints of eq. (38) and (39).

The proposed scheme can be generalized for '$\boldsymbol{n}$' levels, where $\boldsymbol{n}$ < 31. The set of equations for implementing the scheme are given as shown in eq. (40).

$$\left(\frac{n-1}{2}\right) msin\,(\alpha_i) = (i-1) + g \tag{40}$$

where,

$$i = 1, 2, \ldots . \left(\frac{n-1}{2}\right)$$

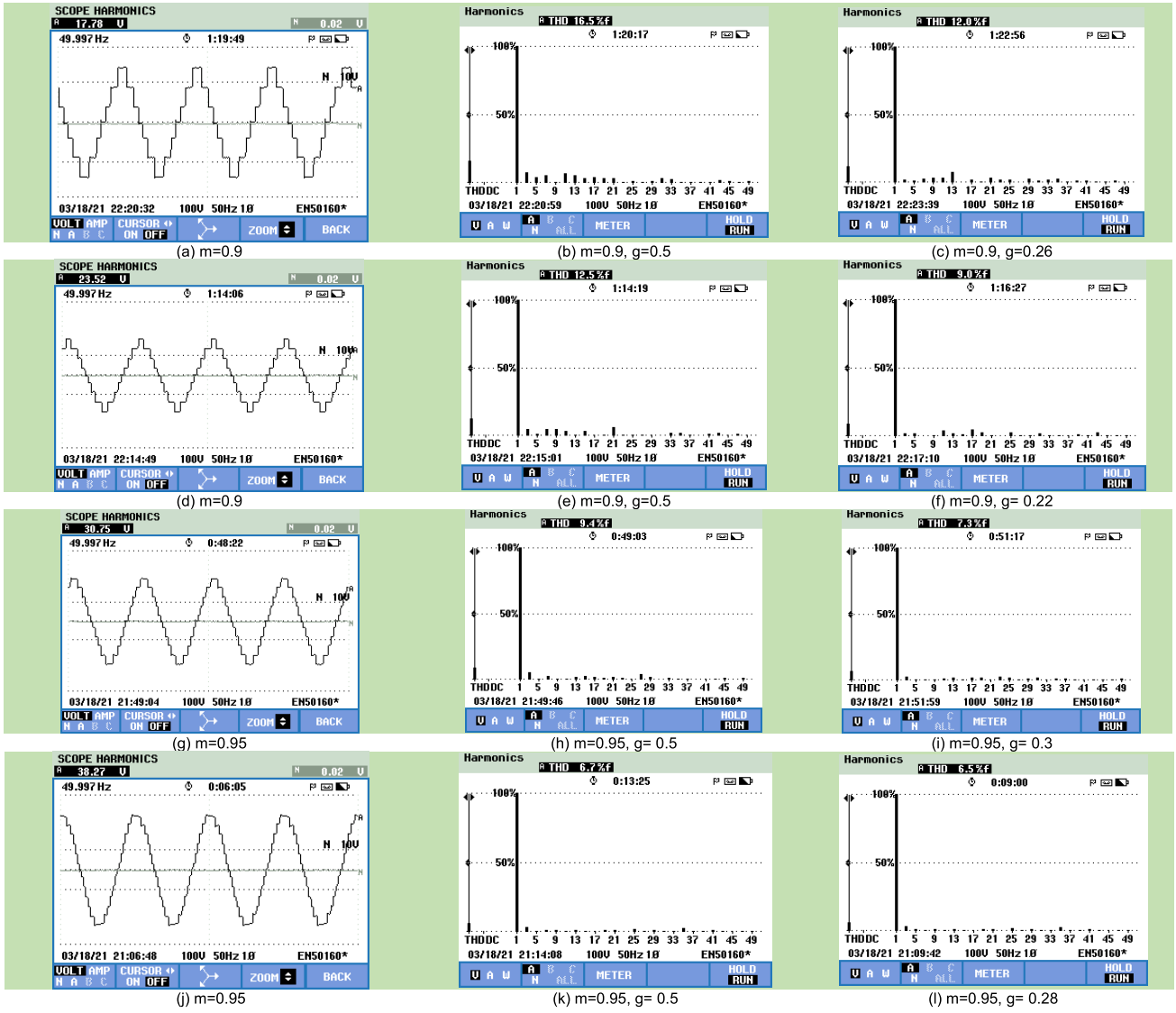


FIGURE 9. Experimental THD plots.

Moreover, the generalized relation between 'g' and 'm' is given by eq. (40)

$$g = am - b \quad \left(for \frac{n-3}{n-1} < m < 1\right) \tag{41}$$

where,

$$a = p_1 N^3 + p_2 N^2 + p_3 N + p_4 \begin{Bmatrix} p_1 = 0.001868 \\ p_2 = -0.07365 \\ p_3 = 1.007 \\ p_4 = -3.173 \end{Bmatrix}$$

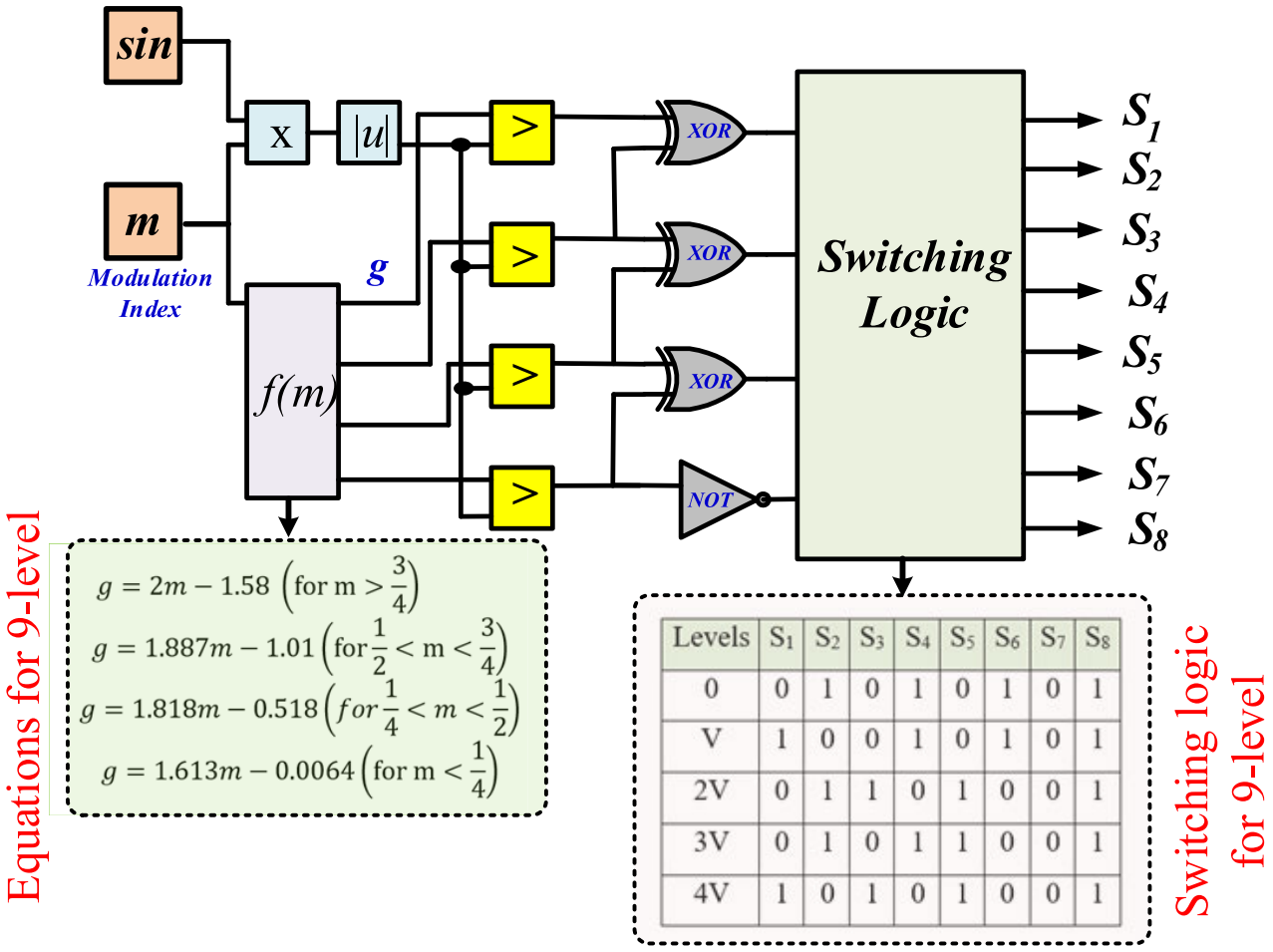
and,

$$b = q_1 N^3 + q_2 N^2 + q_3 N + q_4 \begin{Bmatrix} q_1 = 0.001778 \\ q_2 = -0.07037 \\ q_3 = 1.039 \\ q_4 = -3.439 \end{Bmatrix}$$

Fig. 5 shows the variation of parameters 'a' and 'b' with the number of levels (N).

IV. COMPARATIVE ANALYSIS

This section presents a comparative analysis of the proposed modulation strategy with NLC method. For comparison, the parameters taken are 3rd, 5th and 7th harmonic components. Along with these parameters, overall THD, which is obtained by simulation, is also compared. Based on the obtained data, the graphs have been plotted and shown in Fig. 6. Fig. 6(a) shows the comparison for 7-level CHB in which the 3rd, 5th and 7th harmonic components obtained with NLC modulation method are compared with the same harmonic components which are obtained with the proposed VSNLM modulation technique. Moreover, overall THD for both methods is also compared and shown in the same Fig. Similarly, for 9-level CHB, comparison is shown in Fig. 6(b) and for 11-levels and 13-level CHB inverters, the comparative analysis is presented in Fig.6(c) and 6(d) respectively. In all the results, it is clearly visible that the proposed modulation



Levels	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
0	0	1	0	1	0	1	0	1
V	1	0	0	1	0	1	0	1
2V	0	1	1	0	1	0	0	1
3V	0	1	0	1	1	0	0	1
4V	1	0	1	0	1	0	0	1

FIGURE 10. Control logic implemented in digital signal controller TMS320F28379D.

scheme in this paper is certainly an improvement over NLC method since there is a reduction in the obtained THD value.

The comparison of the proposed strategy with the selective harmonic elimination (SHE) technique has also been done and shown in Fig. 7. The switching angles for 7-level, 9-level, 11-level and 13-levels are depicted in fig. 7(a), 7(c), 7(e) and 7(g) respectively. Fig. 7(b) provides the THD comparison for 7-level in which it can be seen that the proposed VSNLM has lower value of THD than the SHEPWM for the entire range of modulation index. Similar information has been conveyed by fig. 7(d), fig. 7(f) and fig. 7(h) showing the THD comparison for 9-levels, 11-levels and 13-levels respectively which are showing that the proposed VSNLM technique is clearly performing better than SHE technique.

V. EXPERIMENTAL VERIFICATION

This section show the experimental implementation of the proposed modulation strategy on cascaded h-bridge inverter. Fig. 8(a), 8(b), 8(c) and 8(d) depicts the load voltage and current waveforms for 7-level, 9-level, 11-level and 13-level inverters respectively. The results are taken for resistive load. The values of load are Z = 20 Ω, Z = 22 Ω, Z = 40 Ω and Z = 35 Ω in Fig. 8(a), 8(b), 8(c) and 8(d) respectively. The results showing the comparison of THD with the conventional NLC and the proposed VSNLM strategy are presented in Fig. 9. The results show the experimental THD of the CHB inverter with the conventional NLC method and the proposed VSNLM strategy at the same value of modulation index (m). Whereas the carrier step size (g) in conventional NLC modulation method is 0.5, in the proposed VSNLM method, 'g' is obtained by using the relation between 'm' and 'g' which are already shown in the previous section. Fig. 9(a)-9(c) are results obtained for 7-level CHB inverter. In Fig. 9(b), for m = 0.9, the THD by using the conventional NLC, i.e. for g = 0.5, is 16.5%. However, for the same value of m, the value of g is 0.26 for the proposed VSNLM method. By using this value of g = 0.26, the THD, as shown in Fig.9(c), is 12% which is marked improvement over the conventional NLC strategy.

Similarly, the results for 9-level CHB inverter are displayed in Fig.9 (d)-9(f). For m = 0.9, Fig.9 (d) shows

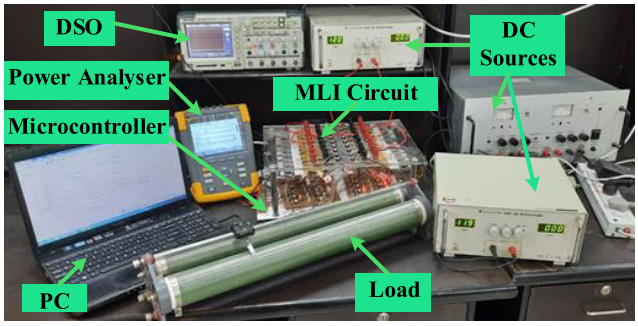


FIGURE 11. Experimental setup in the laboratory.

the load voltage waveform. Fig.9 (e) depicts the THD for g = 0.5 which is 12.5% whereas in Fig. 9(f), for g = 0.22, the THD is only 9%. For 11 levels the results are presented in Fig.9 (g) – 9 (i). For m = 95, g = 0.5, the THD is 9.5% as seen from fig. 9(h).

However, for same value of m and g = 0.22, the THD is coming only 7.4% which is shown in Fig. 9(i). Lastly, the results for 13-level CHB are also presented in Fig. 9(j)−9(l). For m = 0.95 and g = 0.5, the THD is shown in Fig. 9(k) which is 6.7%. By keeping the value of m same and g = 0.28, the THD gets reduced to 6.5% which is visible from Fig. 9(l). In all the results, the THD with the proposed VSNLM strategy is lesser than the conventional NLC method. This proves the superiority of the proposed modulation strategy over the conventional method. The control logic implemented in the digital signal controller to implement the proposed VSNLM strategy is shown in Fig. 10. Fig. 11 shows the experimental setup which is present in the laboratory and used for taking the results. IGBT FGA25N120 is used as a switch in the proposed circuit. The control signals are generated by using DSP board TMS320F28379D. For driving the IGBTs a driver circuit TLP 250H based is utilized. Different voltage and current waveforms are recorded using TPS2024 Tektronix digital oscilloscope. Fluke 435-II is used as the power quality analyzer for observing the harmonic waveforms.

VI. CONCLUSION

This paper proposes the idea of a novel modulation strategy for use in multilevel inverters. It is named as Variable Structure Nearest Level Modulation. In the paper, the strategy is implemented on 7-level, 9-level, 11-level and 13-level CHB inverters. The mathematical analysis behind the proposed modulation strategy is presented in the paper. The comparison of the proposed strategy with NLC modulation strategy is also shown in the paper. The comparison of THD shown by simulation is verified by the experimental implementation of the proposed strategy on CHB inverters. In simulation as well as experimental comparison, there is a significant improvement in THD by using VSNLM as compared to NLC. This shows the effectiveness of the proposed strategy in the paper.

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