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A Novel Single-Input-Multi-Output Converter for Flexible-Order Power-Distributive With MPPT Capability

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ABSTRACT This article proposes a novel single-input-multi-output (SIMO) converter for photovoltaic (PV) applications. The proposed structure produces multi-outputs with extended n stages. The voltage gain of the proposed topology for each output is enhanced by adding the number of the stage which in turn increases the power. The voltage across the switch is low, so it leads to using a lower RDS (ON) MOSFET. Besides, the peak voltage of the switch and diodes is reduced by enhancing the number of the stage. Thus, the proposed converter's power loss is reduced. This structure can operate in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) of operations. The proposed structure is capable to achieve maximum power point (MPP) using perturb and observe P&O) technique. To describe the foremost advantages of the proposed converter, comparison results between the recommended topology and other related structures in this field are presented. The dynamic analysis, and the principle of operation for n = 3, 4 stages are introduced. Finally, experimental results in CCM and DCM operations with 50 kHz switching frequency are provided.

INDEX TERMS Step-up converter, single-input-multi-output converter (SIMO), photovoltaic, high gain, CCM, DCM, PV application.

I. INTRODUCTION

Recently, multiport step-up converters are extensively used in power electronics. The main advantages of the multi-port converters consist of different output voltages [1], [2]. The outputs of this topology are used with different output voltages and controlled by the proper design of the control circuit, which reduces the input current ripple to a certain extent, which reduces the size of the passive elements used in the converter [3], [4]. The classical step-up converter is the ordinary topology for voltage lifting. Nevertheless, for output voltage higher than the input, the regulated duty cycle should be set nearing 1. Also, power losses will be enhanced by increasing duty-cycle which will lead to creating a low efficiency [5]–[7]. Therefore, need for one dc-dc converter interface among the production sources and consumption with high efficiency, high voltage gain and low current ripple [8]. In [9], an interleaved topology is proposed with a low input current. This topology has a high gain with a low peak voltage of switches using voltage multiplier cells (diode/capacitor, diode/capacitor/inductor). In addition, for low- and high-power usages, a multi-output step-up converter can distribute its output voltage between diverse series of the output stage. This type of DC-DC converters can be utilized alternatively for numerous single output structures. In [10], a multi-output converter is proposed which standby flyback converter is integrated with ZVS multi-output converter. A multi-output boost structure with a single inductor and series regulated output voltages is presented in [11]. Also, an uncomplicated control approach has been

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introduced to control its output voltages. This structure and its control method are easily extended for multiple outputs. Consequently, a boost dc-dc topology is employed between the production source and consumption, forming a two-stage conversion structure. For low-power usages, the input voltage of the renewable applications is regularly a few dozen volts, so need a high duty-cycle value. Therefore, the ESR of the inductors and capacitors increases significantly. So, the losses of the topology are increased and efficiency decreased by increasing inductors and capacitors ESR and increasing ON-state resistance of power MOSFET [12]. These suggested topologies can work in ZVS in on-state, and ZCS is the off-state switch. [13] proposes a high gain multi-input transformer-less bidirectional structure. However, the peak voltage across power diodes and power switches are high. In [14], low voltage stress and low switching loss buck-boost structure is suggested for renewable energy purposes. However, the appearance of the power switch on the input side leads to a high current ripple. In [15], [16], some new switched/capacitor (SC) and coupled/inductor (CL) based structures are suggested. In SC structures, the voltage is enhanced by the charging and discharging of the SCs. Also, the voltage gain is enhanced by using the coupling inductor and proper selection of the turn's ratio value. Generally, an extra snubber circuit is expected to receive the leakage energy. In addition, the number of power components has large, which will enhance the volume and the cost. Furthermore, these topologies have an influential disadvantage in that high voltage stress might be happening at the power switch due to the existence of a leakage of the coupling inductor. The leakage of the coupling inductor leads to a large spike at the power switch. So, the lossless passive snubber is presented in [17] to anticipate efficiency, decline by adding a snubber circuit. This structure has no power loss generated by adding a snubber circuit. Also, it is capable to achieve ZVS in MOSFETs with a decreased spike voltage stress. However, it needs an extra switch and also the control circuit of this structure is very complex due to the high components count. Fig. 1 shows the PV/grid-tied/EV battery system configuration.

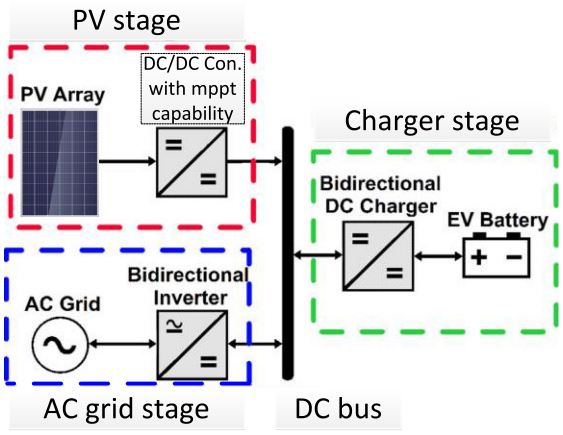

FIGURE 1. Overall PV system structure for grid-tied and electric vehicle (EV) charging applications.

In this article, a SIMO boost converter is suggested with multi-output for the PV usages. The voltage gain of this structure is higher than the classical step-up topologies. This structure is widespread to n stages by adding the number of VMCs. The presented converter uses a voltage multiplier unit which is consists of a capacitor-inductor-diode (C-L-D) to increase the output. The efficiency will be enhanced when the number of stages multiplier units will be increased by decreasing the voltage stress across semiconductors. Thus, the power loss of the power switch is decreased using low resistance ON-state. The suggested topology and operation modes are analyzed in section 2. Finally, to verify the analysis and the operation of the suggested converter, the laboratory prototypes and the simulation results are.

II. SUGGESTED TOPOLOGY AND PRINCIPLE OF OPERATION

Fig. 2(a) depicts the configuration of the recommended topology. This topology is a multi-output converter with an input dc supply, one power switch, and voltage multiplier units include two capacitors, diode, and inductor. To simplify the mathematical investigation, the following suppositions are taken:

- V_{in} is invariable,
- Semiconductor devices are ideal,
- The capacitance of the used capacitors is large; thus, their voltages are invariable

Fig. 2(d) exhibits the structure of the applied VMC to enhance the voltage in each stage. The VMC consists of a diode/capacitor/inductor which lifting the voltage in each stage. The stored energy in the previous stage is added to the next stage as a ladder. There are 2 operation modes in one switching period (T_s). In the first mode (DT_s), the power switch is turned on and in the second mode ($(1 - D)\ Ts$), the switch is turned off.

A. CCM OPERATION

The analysis of the suggested topology in CCM is described in this section. Figs. 2 (c) and (d) show the equivalent configurations in mode 1 and 2, respectively. According to Fig. 2(c), the proposed converter has two modes which are described as:

B. MODE 1 [$0 \le t \le DT_s$]

At $t = 0$, the switch is turned on and all semiconductor components omitting D_b are turned off. Inductors are magnetized by the input voltage (V_i), so their currents ($L_1, L_2, L_3, \ldots, L_n$) are linearly increased. The stored energy capacitor C_b will be transferred to capacitors C_a, and $C_1, C_2, \ldots, C_{n-1}, C_{o1}, C_{o2}, \ldots, C_{o(n-1)}$ will be discharged in this mode:

$$V_{L1} = V_i \tag{1}$$

$$\begin{cases} V_{Lk} = V_i + \sum_{j=1}^{k-1} V_{Cj} + V_{Co1} - V_{Cok} \\ j = 2, \ldots, (n-1)\ \&\ k = 2, 3, \ldots, n \end{cases} \tag{2}$$

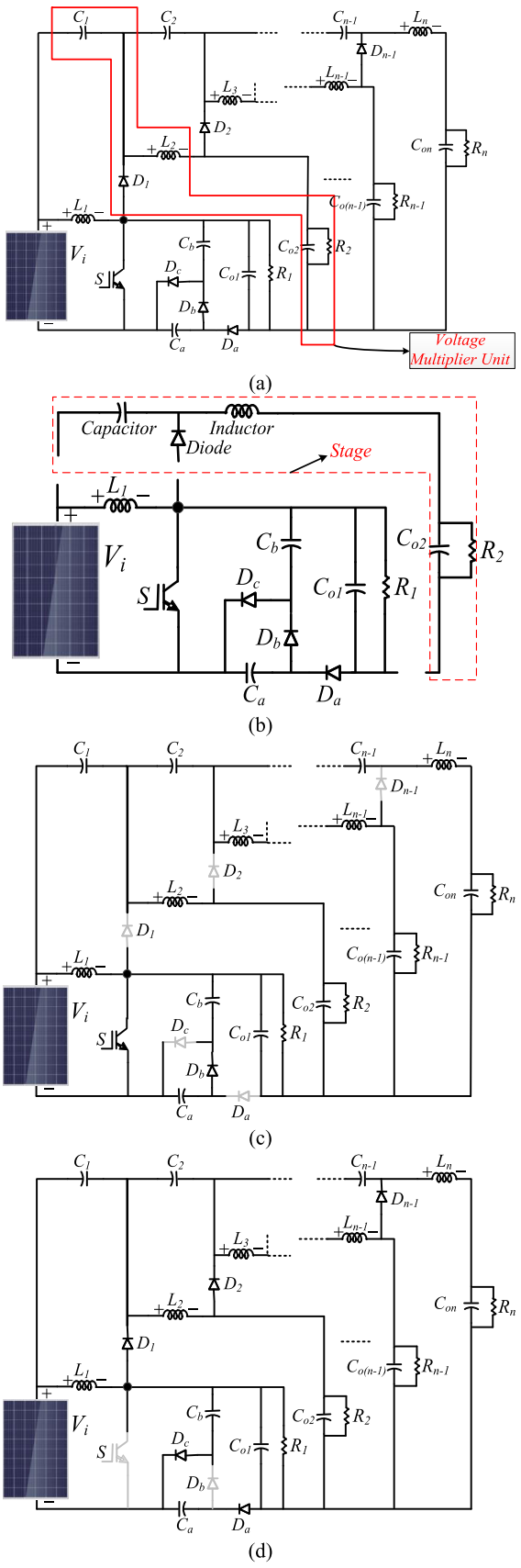

FIGURE 2. Suggested converter, (a) The circuit of the recommended topology, (b) Voltage multiplier unit in each stage, (c) Mode 1, (d) Mode 2.

$$V_{Ca} = V_{Cb} \tag{3}$$
$$V_{D1} = -V_{C1} - V_i \tag{4}$$
$$V_{Dj} = V_{Coj} - V_{Co1} - \sum_{k=1}^{j} V_{Ck} - V_i, \quad j = 2, 3, \ldots, n-1 \tag{5}$$
$$V_{Dc} = -V_{Ca} \tag{6}$$
$$V_{Da} = V_{Cb} - V_{Co1} \tag{7}$$

The current flow of $C_1, C_2, \ldots, C_{n-1}$ can be attained as:

$$I_{C(j-1)\text{on}} = I_{oj}, \quad j = 2, 3, \ldots, n \tag{8}$$

The currents of C_1 and C_2 are terminated as:

$$\begin{cases} I_{\text{C1(on)}} = I_{o1} \\ I_{\text{C2(on)}} = I_{o2} \end{cases} \tag{9}$$
$$I_{\text{Ca(on)}} = -I_{\text{Cb(on)}} \tag{10}$$

C. MODE 2 [$DT_s \le t \le T_s$]

Based on Fig. 2(d), the switch is turned off and all diodes omitting the diode D_b are forward biased. All inductors are discharged, so their currents ($L_1, L_2, L_3, \ldots, L_n$) are linearly decreased. The stored energy of capacitor C_a transfer to capacitors C_b and C_{o1}, also the capacitors $C_1, C_2, \ldots, C_{n-1}$, $C_{o1}, C_{o2}, \ldots, C_{o(n-1)}$ will be charged in this mode.

$$V_{L1} = V_i - V_{Cb} \tag{11}$$
$$V_{Lk} = -V_{Ck}, \quad k = 1, 2, \ldots, n-1 \tag{12}$$
$$V_{Lk} = V_{Co(k-1)} - V_{Cok}, \quad k = 2, 3, \ldots, n \tag{13}$$
$$V_{Co1} = V_{Ca} + V_{Cb} \tag{14}$$
$$V_{Db} = -V_{Ca} \tag{15}$$
$$V_S = -V_{Cb} \tag{16}$$

Using the volt-second balancing law on inductors $L_1, L_2, L_3, \ldots, L_n$ and employing (1), (2), (9) and (10), the voltage of capacitors is calculated as:

$$V_{Cj} = \frac{DV_i}{1-D}, \quad j = 1, 2, \ldots, n-1 \tag{17}$$
$$V_{Ca} = V_{Cb} = \frac{V_i}{1-D} \tag{18}$$
$$V_{Co1} = \frac{2V_i}{1-D} \tag{19}$$
$$V_{Coj} = \frac{2 + (\text{j} - 1)D}{1-D} V_i, \quad j = 2, 3, \ldots, n \tag{20}$$

Using (17), the voltage gain for all outputs in CCM operation (M_{CCM}) is achieved as:

$$M_{CCM(j)} = \frac{V_{Coj}}{V_i} = \frac{2 + (j-1)D}{1-D}, \quad j = 1, 2, \ldots, n \tag{21}$$

Using the current-second balancing on C_1, C_2, C_3, $\ldots$, C_{n-1} and using Figs. 1(a) and (c), equations (22)– (28) are achieved:

$$I_{Da} = I_{Dc} = \frac{1}{1-D} \sum_{j=1}^{n} I_{oj} \tag{22}$$

$$I_{Db} = \frac{1}{D}\sum_{j=1}^{n} I_{oj} \tag{23}$$

$$I_{Dj} = \frac{1}{1-D}\sum_{k=j+1}^{n} I_{ok}, \quad j = 1, 2, \ldots, n-1 \tag{24}$$

$$I_{\mathrm{Ca(off)}} = -I_{\mathrm{Cb(off)}} \tag{25}$$

$$I_{o(i)} = \frac{1-D}{(i-1)D+2} I_i, \quad i = 1, 2, \ldots, n \tag{26}$$

$$\begin{cases} I_{\mathrm{Ln}} = I_{on} \\ I_{\mathrm{L(n-1)}} = I_{o(n-1)} + I_{on} \\ \vdots \\ I_{\mathrm{L2}} = I_{o2} + I_{o3} + \ldots + I_{on} \\ \quad = \dfrac{-D+1}{2} I_i \left(\dfrac{1}{1+\frac{D}{2}} + \dfrac{1}{1+\frac{2D}{2}} \right. \\ \quad \left. + \ldots + \dfrac{1}{1+\frac{Dn}{2}}\right) \end{cases} \tag{27}$$

$$I_{L1} = I_{L2} + I_{C1(\mathrm{off})} - I_{C2(off)} + I_{o1} + I_{Cb(off)} \tag{28}$$

The RMS current of the switch is achieved as:

$$\begin{aligned} &I_{S(rms)} \\ &= \sqrt{\frac{1}{T_S}\int_0^{DT_S} (I_{L1} - I_{Cb(\mathrm{on})} - I_{Co1(\mathrm{on})} - I_{o1})^2 dt} \\ &= (1-D)\left(\frac{1}{D+2} + \frac{1}{2D+2} + \ldots + \frac{1}{Dn+2}\right) I_i - \frac{3D+1}{2} I_i \end{aligned} \tag{29}$$

The peak current ripple of $L_1, L_2, \ldots, L_n$ can be terminated as:

$$\begin{cases} \Delta I_{L1} = \dfrac{DV_i}{f_S L_1} \\ \Delta I_{L2} = \dfrac{D(V_i + V_{C1} - V_{Co2})}{f_S L_2} \\ \vdots \\ \Delta I_{Ln} = \dfrac{DV_i + (\sum_{k=1}^{n-1} V_{Ck}) - \mathrm{V}_o}{f_S L_n} \end{cases} \tag{30}$$

The peak currents flow of the inductors (the current at the end of mode 1) $L_1, L_2, \ldots, L_n$ are calculated:

$$\begin{cases} I_{L1} = I_{L1(\mathrm{av})} + \dfrac{\Delta I_{L1}}{2} = I_{L1(\mathrm{av})} + \dfrac{DV_i}{2f_S L_1} \\ I_{L2} = I_{L2(\mathrm{av})} + \dfrac{\Delta I_{L2}}{2} = I_{L2(\mathrm{av})} \\ \quad + \dfrac{D(V_i + V_{C1} - V_{Co2})}{2f_S L_2} \\ \vdots \\ I_{Ln} = I_{Ln(\mathrm{av})} + \dfrac{\Delta I_{Ln}}{2} = I_{Ln(\mathrm{av})} \\ \quad + \dfrac{DV_i + (\sum_{k=1}^{n-1} V_{Ck}) - V_o}{2f_S L_n} \end{cases} \tag{31}$$

where, the inductors average current is calculated as:

$$\begin{cases} I_{L1(\mathrm{av})} = I_i \\ I_{L2(\mathrm{av})} = \dfrac{1+D}{2} I_i \\ \vdots \\ I_{Ln(\mathrm{av})} = \left(\dfrac{2+D(n-1)}{1-D}\right) I_i \end{cases} \tag{32}$$

Voltage ripple of the output capacitors is achieved as:

$$\begin{cases} \Delta V_{o1} = \dfrac{\Delta Q_1}{2} = \dfrac{1}{2} \times \dfrac{T_S}{2} \times \dfrac{1}{C_{o1}} \times \dfrac{\Delta I_{L1}}{2} \\ \quad = \dfrac{DV_i T_S}{8 f_S L_1 C_{o1}} \\ \Delta V_{o2} = \dfrac{\Delta Q_2}{2} = \dfrac{1}{2} \times \dfrac{T_S}{2} \times \dfrac{1}{C_{o2}} \times \dfrac{\Delta I_{L2}}{2} \\ \quad = \dfrac{D(V_i + V_{C1} - V_{Co2}) T_S}{8 f_S L_2 C_{o2}} \\ \vdots \\ \Delta V_{on} = \dfrac{\Delta Q_n}{2} = \dfrac{1}{2} \times \dfrac{T_S}{2} \times \dfrac{1}{C_{on}} \times \dfrac{\Delta I_{Ln}}{2} \\ \quad = \dfrac{[DV_i + (\sum_{k=1}^{n-1} V_{Ck}) - V_o] T_S}{8 f_S L_n C_{on}} \end{cases} \tag{33}$$

In equation (33), the minimum value of the capacitors will be achieved by the selection of D_{min}.

D. VOLTAGE STRESS

Based on Fig. 2(d) and (18), the peak voltage of the switch (S) is as follows:

$$V_S = V_{Cb} = \frac{V_i}{1-D} \tag{34}$$

By combining (21) and (34), the peak voltage of the switch (S) versus difference outputs is calculated as (35) (n is the number of outputs):

$$M_{Switch} = \frac{V_{Switch}}{V_{o_n}} = \frac{n+M-1}{(n+1)M} \tag{35}$$

By combining (4)-(7), (15) and (17)-(21), the normalized peak voltage of power diodes ($D_a, D_b, D_c, D_1, D_2, \ldots, D_{n-1}$) versus difference outputs can be obtained as:

$$M_{Diodes} = \frac{V_{Diodes}}{V_{o_n}} = \frac{n+M-1}{(n+1)M} \tag{36}$$

The voltage and current of the suggested topology in CCM operation are shown in Fig. 3.

E. DCM OPERATION

DCM analysis is described in this section. This operation of the suggested topology has 3 modes. Since modes 1 and 2 in CCM are comparable to modes 1 and 2 in DCM. So, these figures are not shown. In mode 3 of DCM operation, the semiconductor devices are a turn-off.

The current of inductors is a constant value and the current of all diodes is zero. Fig. 4 (a) and (b) show waveforms

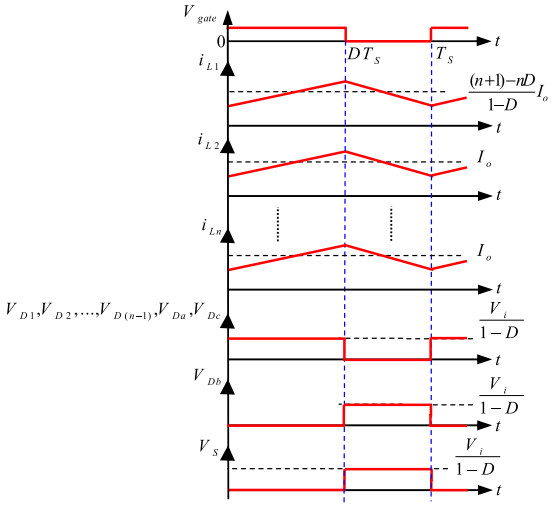

FIGURE 3. The waveforms at CCM operation.

in DCM operation and the equivalent circuit of mode 3, respectively. Based on Fig. 2(a) and (22)-(25), the average currents of inductor and diodes are as follows:

$$I_{D1}+I_{D2}+\ldots+I_{D(n-1)}+I_{Da}+I_{Dc}=I_{L1}+I_{L2}+\ldots+I_{Ln} \tag{37}$$

$$\begin{cases} I_{D1}=I_{L2}=I_{o2}+I_{D2} \\ I_{\mathrm{L1}}=I_s+I_{D1}+I_{o1} \\ I_{D2}=I_{\mathrm{L3}}=I_{D3}+I_{o3} \\ \vdots \\ I_{D(n-2)}=I_{\mathrm{L(n-1)}}=I_{D(n-1)}+I_{o(n-1)} \\ I_{D(n-1)}=I_{\mathrm{Ln}}=I_{on} \\ I_{Da}=I_{Db}=I_{Dc}=I_{o1}+I_{o2}+\ldots+I_{on} \end{cases} \tag{38}$$

Using (26) and (38), the following equations are obtained:

$$\begin{cases} \frac{3(1-D)}{4+2D}I_i+(1-D)(\frac{1}{2D+2}+\ldots+\frac{1}{nD+2})I_i \\ \quad +\ldots+\frac{(1-D)4+(2n-3)D}{2+Dn}I_i \\ \quad +\frac{1-D}{2+(n-1)D}I_i=\frac{1}{2}D'I_{D-PK} \end{cases} \tag{39}$$

$$\begin{cases} I_{\mathrm{L1}}=I_i, \quad I_{D1}=I_{\mathrm{L2}}=(1-D) \\ \quad \times(\frac{1}{2+D}+\frac{1}{2+2D}+\ldots+\frac{1}{2+nD})I_i \\ I_{D2}=I_{\mathrm{L3}}=I_{D3}+I_{o3}=(1-D) \\ \quad \times(\frac{1}{2+2D}+\ldots+\frac{1}{2+nD})I_i \\ \vdots \\ I_{D(n-2)}=I_{\mathrm{L(n-1)}}=\frac{(1-D)4+(2n-3)(1-D)D}{D+2}I_i \\ I_{D(n-1)}=I_{\mathrm{Ln}}=\frac{1}{2+Dn}I_i \\ I_{Da}=I_{Db}=I_{Dc}=(1-D)(\frac{1}{2}+\frac{1}{2+D}+\frac{1}{2+2D} \\ \quad +\ldots+\frac{1}{2+(n-1)D})I_i \end{cases} \tag{40}$$

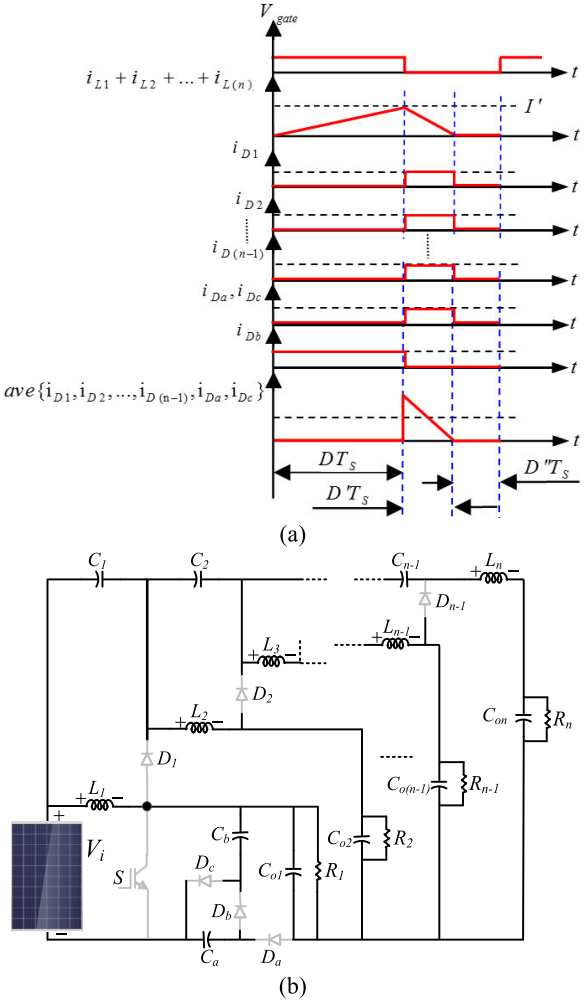

FIGURE 4. DCM operation, (a) The waveforms, (b) Mode 3.

The total inductors peak current is calculated as:

$$\begin{cases} I_{D-PK}=I_{L1}+I_{L2}+I_{L3}+\ldots+I_{Ln}=\frac{V_iDT_S}{L} \\ \frac{1}{L}=\frac{1}{L_1}+\frac{1}{L_2}+\frac{1}{L_3}+\ldots+\frac{1}{L_n} \end{cases} \tag{41}$$

$$\begin{cases} \frac{3(1-D)}{4+2D}I_i+4(1-D)(\frac{1}{2+2D}+\ldots+\frac{1}{2+nD})I_i \\ \quad +\ldots+\frac{(2n-3)D}{2+Dn}I_i+\frac{1-D}{(n-1)D+2}I_i \\ \quad =(\frac{V_iDD'T_S}{2L}) \end{cases} \tag{42}$$

Using the volt-second law on inductors, D' is obtained:

$$\begin{cases} D'=\frac{2LI_i}{V_iDT_S}[\frac{3(1-D)}{4+2D}+4(1-D) \\ \quad \times(\frac{1}{2D+2}+\ldots+\frac{1}{nD+2}) \\ \quad +\ldots+\frac{(1-D)+(2n-3)D}{2+Dn}+\frac{1-D}{2+(n-1)D}] \end{cases} \tag{43}$$

Using (42) and (43), the voltage gain in DCM operation is obtained by (44):

$$\begin{cases} M_{DCM} = \dfrac{D}{\xi} \\ \xi = \dfrac{2LI_i}{V_i T_S}[\dfrac{3(1-D)}{4+2D} + 4(1-D) \\ \quad \times (\dfrac{1}{2+2D} + \ldots + \dfrac{1}{2+nD}) \\ \quad + \ldots + \dfrac{(1-D)+(2n-3)D}{2+Dn}] \end{cases} \tag{44}$$

F. INDUCTOR DESIGN

The inductor peak-to-peak current ripple ΔI_L can be achieved from Figs. 2 and 3. Assuming in Figs. 2 and 3 that $\Delta I_L = ri\%I_L$, for inductor design is obtained as the following equation:

$$\begin{cases} L_1 = \dfrac{TDV_i^2}{r_1\%P_i} \\ L_2 = \dfrac{TR(1-D)DV_i^2}{r_2\%I_{L_2}[P_i(1-D)R - 2V_i^2]} \\ \vdots \\ L_n = \dfrac{TD[2+(j-1)D] \times V_i^2}{r_n\%P_i(1-D)} \end{cases} \tag{45}$$

III. DYNAMIC MODEL AND CONTROL

To dynamic response analysis, the state-space averaging model is applied in each operation mode by considering the equations of modes and following assumptions:

- Semiconductors are ideal
- V_{in} is steady
- Inductors have the same value: $L_1 = L_2 = \ldots = L_{n-1} = L_n = L$
- Capacitors are equal.

With the abovementioned descriptions for the fourth stage $n = 4$, there are thirteen state variables (for inductors and capacitors). Where, $u = V_i$.

The state variables vector x is defined as:

$$x = [\, V_{C1}\ V_{C2}\ V_{C3}\ V_{Ca}\ V_{Cb}\ V_{Co1}\ V_{Co2}\ V_{Co3}\ V_{Co4}\ i_{L1}\ i_{L2}\ i_{L3}\ i_{L4}\,]^T \tag{46}$$

According to Fig. 2(c), the output equations can be expressed by (47)-(50), as shown at the bottom of the next page. Also, the related matrixes are as (51)-(53), as shown at the bottom of the next page.

$$x' = A_1 x + B_1 u \tag{47}$$

IV. MPPT AND CHARACTERISTICS OF PV PANEL

Generally, PV panel's technology is advanced with higher efficiency and lower cost which leads to a huge enhance in demand. Therefore, maximum power tracking (MPPT) of the solar PV panel is an important issue in the discussion of power management, attained through controlling the duty ratio of the interface converter. Electric model of PV array

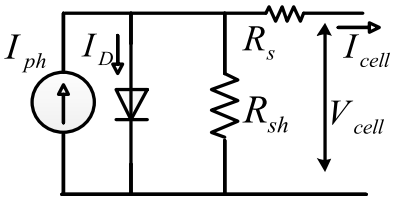

FIGURE 5. PV model of PV array.

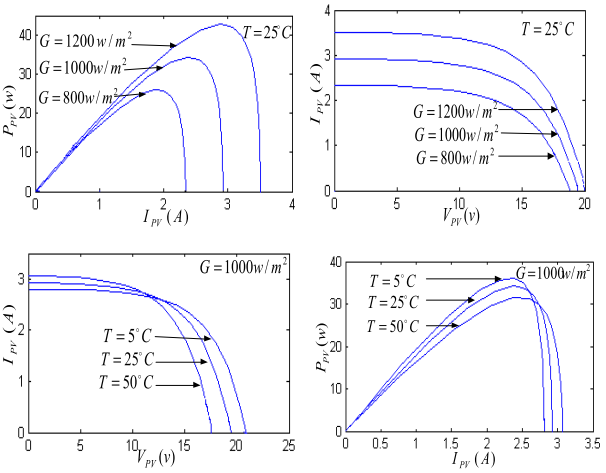

FIGURE 6. P-I, I-V characteristics of the PV array under different environmental conditions.

and P-I, I-V characteristics of the PV array for different environmental conditions are shown in Fig. 6. where, I_{sc} cell short circuit current, I_0 diode saturation current, R_s cell series resistance, T_c environment temperature, G power density, α_{sc} short circuit current's thermal coefficient, and β_{oc} open-circuit voltage's thermal coefficient.

The P&O MPPT algorithm is used to track the maximum power from the solar PV panel via controlling the duty ratio of the proposed DC/DC converter topology in this paper. Finally, the required power load by comparing the output voltage and the reference voltage (Vo,ref) will be transferred to the load. The PI has two coefficients: 1) gain and 2) time constants.

V. COMPARISON STUDY

A comparison of the recommended topology and other topologies is shown in Table 1 versus voltage gain, voltage stress of semiconductors, total devices number, number of switches and efficiency. Considering Table 1, it is obvious that the voltage gain of the suggested topology is enhanced by adding the VMCs (by enhancing n). The voltage stress across semiconductors will be reduced by enhancing the number of VMCs. In fact, can be said that the efficiency of the presented structure will be high by decreasing the nominal power of devices. The components count of the suggested topology is $4n + 7$, where n is the VMC number. So, the presented topology has lower losses and costs.

Using a small-signal model, the dynamic response of the suggested topology is investigated. For uniformity, inductors

and capacitors are considered $500\mu H$ and $330\mu F$, respectively. Bode diagram of the suggested multi-port converter with $n = 3, 4$ is depicted in Fig. 7. Regarding Fig. 7(b), the closed-loop transfer function of V_o to D, $G_{Vod}(s)$ is applied which it is clear that the suggested structure have a stable state in the desired range. Fig. 7(c) shows the P&O algorithm.

A. VOLTAGE GAIN

Figure 8(a) depicts the converters voltage gain versus D. The voltage gain of the suggested topology is higher than other topologies. The voltage gain and output voltage of the presented topology (for all outputs) will be enhanced by n. Finally, the power will be enhanced, so it can be useful for different power levels. The proposed topology can be achieved different power levels with lower duty-cycle values.

B. SWITCH NORMALIZED VOLTAGE STRESS

Figure 8(b) depicts the peak voltage on switch versus D. The peak voltage of switch of the suggested topology for $n \geq 3$ is lower than other structures except for converter in [27]. In addition, the suggested converter's normalized peak voltage on the power switch is decreased by a rising of n.

C. DIODE NORMALIZED VOLTAGE STRESS

Regarding to Fig. 8(c) and Table 1, the peak voltage of the diodes will be decreased by enhancing the number of VMCs. In addition, it leads to an increase in the number of output ports and the power level of the recommended topology. Based on Table 1, the peak voltage of diodes is limited to $1/(n+1)$ when the voltage gain value is enhanced. Generally, the losses of the recommended topology will be reduced by decreasing the diode's rated power. The overall cost of the suggested topology depends on these values (stress of power devices) which finally will be low.

VI. EFFICIENCY ANALYSIS

The power losses of the presented converter include power switch (conduction and switching losses), diodes conduction and forward voltage loss, capacitors ESR loss, and magnetic components loss (conduction and core losses). The efficiency of the presented converter can be calculated as (54):

$$\eta = \frac{P_o}{P_{in_1} + P_{in_2}} \times 100\% = \frac{P_o}{P_o + P_{Loss\_tot}} \times 100\% \quad (54)$$

Considering abovementioned components losses, total power loss can be expressed as follows:

$$P_{Loss\_tot} = P_{Loss}^{Switch} + P_{Loss}^{Diodes} + P_{Loss}^{CL} + P_{Loss}^{Capacitors} \quad (55)$$

$$A_1 = \begin{bmatrix}
-\frac{r_L}{L} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & -\frac{r_L}{L} & \frac{r_C}{L} & \frac{r_C}{LC} & 0 & -\frac{1}{L} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & -\frac{r_L}{L} & \frac{r_C}{LC} & 0 & 0 & 0 & (\frac{r_C}{L}) & 0 & 0 & 0 & \frac{1}{L} & 0 \\
0 & 0 & \frac{1}{L} & -(\frac{r_L+r_C}{L}) & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{L} & -\frac{1}{L} \\
\frac{1}{C} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\frac{1}{C} & \frac{1}{C} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\frac{1}{C} & \frac{1}{C} & \frac{1}{C} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{2r_C C} & \frac{1}{2r_C C} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{2r_C C} & -\frac{1}{2r_C C} & 0 & 0 & 0 & 0 \\
0 & -\frac{1}{C} & -\frac{1}{C} & -\frac{1}{C} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & \frac{1}{C} & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{2r_C C} & 0 & 0 & 0 & 0 \\
0 & 0 & \frac{1}{C} & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{2r_C C} & 0 & 0 & 0 \\
0 & 0 & 0 & \frac{1}{C} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix} \quad (48)$$

$$B_1 = [\,\tfrac{1}{L}\ \tfrac{1}{2L}\ \tfrac{1}{2L}\ \tfrac{1}{2L}\ 0\ 0\ 0\ 0\ 0\ \tfrac{1}{2r_C C}\ \tfrac{1}{2r_C C}\ \tfrac{1}{2r_C}\ \tfrac{1}{2r_C}\,]^T \quad (49)$$

$$C_1 = [\,0\ 0\ 0\ 0\ \tfrac{R}{r_C+R}\ \tfrac{R}{r_C+R}\ \tfrac{R}{r_C+R}\ 0\ 0\ \tfrac{R}{r_C+R}\ 0\ \tfrac{R}{r_C+R}\ 0\,] \quad (50)$$

$$A_2 = \begin{bmatrix}
-\frac{r_C RC}{L(Cr_c-CR)} & \frac{r_C(r_C C-2RC)}{L(Cr_c-CR)} & -\frac{(r_C C-2RC)}{L(Cr_c-CR)} & -\frac{(1+2r_L)(r_C C-RC)}{L(Cr_c-CR)} & 0 & 0 & 0 & \frac{1}{L} & \frac{1}{L} & \frac{1}{L} & \frac{RC}{2L(Cr_c-CR)} \\
\frac{r_C RC}{L(r_C C-RC)} & -\frac{(r_L+2r_C)(r_C C-RC)}{L(r_C C-RC)} & -\frac{r_C(r_C C-2RC)}{L(r_C C-RC)} & \frac{r_C RC}{L(r_C C-RC)} & 0 & -\frac{1}{L} & 0 & 0 & 0 & -\frac{1}{L} & -\frac{1}{L} & -\frac{1}{L} & -\frac{RC}{2L(Cr_c-CR)} \\
\frac{r_C RC}{L(r_C C-RC)} & -\frac{r_C(r_C C-2RC)}{L(r_C C-RC)} & -\frac{r_C C-RC}{L(r_C C-RC)} & \frac{(r_C+2r_L)(r_C C-RC)+r_C(2RC-r_C C)}{L(r_C C-RC)} & 0 & 0 & \frac{1}{L} & \frac{1}{L} & 0 & \frac{1}{L} & \frac{1}{L} & \frac{1}{L} & -\frac{RC}{2L(Cr_c-CR)} \\
\frac{2r_C(r_C C-RC)}{L(Cr_c-RC)} & \frac{r_C RC}{L(Cr_c-CR)} & \frac{r_C RC}{L(Cr_c-CR)} & \frac{r_C RC}{L(Cr_c-CR)} & 0 & 0 & 0 & 0 & -\frac{1}{L} & 0 & -\frac{1}{L} & -\frac{1}{L} & -\frac{RC}{2L(Cr_c-CR)} \\
0 & \frac{1}{C} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & -\frac{1}{C} & 0 & 0 & 0 & \frac{1}{r_C C-RC} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & \frac{1}{C} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & -\frac{1}{C} & 0 & 0 & 0 & \frac{1}{r_C C-RC} & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & \frac{1}{C} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
-\frac{1}{C} & \frac{1}{C} & \frac{1}{C} & 0 & 0 & 0 & 0 & 0 & \frac{1}{r_C C-RC} & 0 & 0 & 0 & 0 \\
-\frac{1}{C} & 0 & \frac{1}{C} & -\frac{1}{C} & 0 & 0 & 0 & 0 & 0 & -\frac{1}{r_C C-RC} & 0 & 0 & 0 \\
\frac{1}{C} & -\frac{1}{C} & \frac{1}{C} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{r_C C-RC} & 0 & 0 \\
-\frac{R}{r_C C-RC} & \frac{R}{r_C C-RC} & -\frac{R}{r_C C-RC} & \frac{R}{r_C C-RC} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{r_C C-RC}
\end{bmatrix} \quad (51)$$

$$B_1 = [\,\tfrac{1}{L}\ \tfrac{1}{2L}\ \tfrac{1}{L}\ \tfrac{1}{2L}\ 0\ 0\ 0\ 0\ 0\ \tfrac{1}{r_C C}\ \tfrac{1}{r_C C}\ \tfrac{1}{r_C}\ \tfrac{1}{r_C}\,]^T \quad (52)$$

$$C_1 = [\,0\ 0\ 0\ 0\ \tfrac{R}{r_C+R}\ -\tfrac{R}{r_C+R}\ \tfrac{R}{r_C+R}\ \tfrac{R}{r_C+R}\ 0\ \tfrac{R}{r_C+R}\ 0\ -\tfrac{R}{r_C+R}\ 0\,] \quad (53)$$

TABLE 1. The comparison between the recommended SIMO topology and other structures.

structures	$M_{Converter}$	M_{Switch}	M_{Diodes}	No. of switches	No. of diodes	No. of capacitors	No. of inductors	No. of coupled inductors	Power [W] / Eff. [%]	Capability of MPPT
Conventional	$\frac{1}{1-D}$	1	1	1	1	1	1	0	- / -	-
[18]	$\frac{-2D+2}{1-2D}$	$\frac{m-2}{2m}$	$\frac{m-2}{2m}$	2	7	3	2	0	90 / 91	Yes
[19]	$\frac{n+1}{1-D}$	0.25	0.5	2	2+n	2+n	2	0	170 / 93	Yes
[20]	$\frac{n+1}{1-D}$	0.278	0.722	1	3	4	1	1	70/ 92.2	Yes
[21]	$\frac{3D}{1-D}$	$\frac{3+m}{3m}$	$\frac{3+m}{3m}$	1	3	5	3	0	300 / 95.2	No
[22]	$\frac{1+(n+1)D}{1-D}$	$\frac{1+n+m}{m(n+2)}$	$\frac{1+m}{m}$	$n+2$	$2n$	1	$n+2$	0	200 / 96.35	No
[23]	$\frac{1+(2n+1)D}{1-D}$	$\frac{(2n+1)(2n+1+M)}{2M(n+1)}$	$\frac{2n+1+m}{m(n+1)}$	2	2	2	0	2	200 / 95.2	Yes
[24]	$\frac{2-2D}{1-2D}$	$\frac{M-1}{M}$	$\frac{M-1}{M}$	1	2	3	2	0	72 / 94	No
[25]	$\frac{1+n(1+D)}{1-2D}$	$\frac{m-n-1}{2m+n}$	$\frac{m-n-1}{2m+n}$	1	$3n+1$	$3n+1$	0	n	200 / 95.1	No
[26]	$\frac{2+n}{1-D}$	$\frac{1}{2+n}$	$\frac{1+n}{2+n}$	1	3	4	1	1	290 / 95.5	Yes
[27]	$\frac{2(1+n)}{1-D}$	$\frac{1}{2(1+n)}$	$\frac{1+2n}{2(1+n)}$	2	6	5	0	2	340 / 95.6	Yes
[28]	$\frac{3-D}{1-D}$	$\frac{m+1}{m+3}$	$\frac{m+1}{m+3}$	2	5	4	3	0	300 / 94	No
[29]	$\frac{2-d_1}{2-d_1-d_2}$	$\frac{V_i}{2(2-d_1-d_2)}$	$\frac{V_i}{2(2-d_1-d_2)}$	4	2	3	2	0	300 / 95.9	Yes
[30]	$\frac{m}{1-D_{n+1}}$	$\frac{1}{m}$	$\frac{1}{m}$	n	$m+n+2$	$2m$-1	1	0	72 / 96.9	No
[31]	$V_{o1}=\frac{1}{1-D_1}$, $\begin{cases} V_{on}=\frac{D_n}{1-D_{n-1}} \\ n=2,3,\ldots \end{cases}$	1	-	$n+1$	0	n	1	0	200 / 95.2	Yes
[32]	$\frac{2(N+1)}{1-D}$	$\frac{1}{2(N+1)}$	$\frac{N}{N+1}$	2	4	4	2	2	280 /.94.4	No
Proposed	$\frac{(n-1)D+2}{1-D}$	$\frac{n+m-1}{(n+1)m}$	$\frac{n+m-1}{(n+1)m}$	1	$4n+7$	$n+2$	n	0	550 / 94.5	Yes

The power loss in power switches is obtained by (56):

$$P_{Loss}^{Switch} = P_{Loss}^{Switching} + P_{Loss}^{Conduction} \tag{56}$$

where $P_{Loss}^{Switching}$ and $P_{Loss}^{Conduction}$ are related to switching and conduction losses of power switch and achieved as (57) and (58), respectively:

$$P_{Loss}^{Switching} = \frac{1}{2} V_S I_S^{avg} f_s \left(t_S^{ON} + t_S^{OFF} \right) \tag{57}$$

$$P_{Loss}^{Conduction} = r_S \left(I_S^{rms} \right)^2 \tag{58}$$

The power losses of the diodes can be expressed as follows:

$$P_{Loss}^{Diodes} = P_{Loss}^{Forward\ Voltage} + P_{Loss}^{Conduction\_Diodes} \tag{59}$$

In (59), $P_{Loss}^{Forward\ Voltage}$ is forward voltage loss and calculated as (60). Also, $P_{Loss}^{Conduction\_Diodes}$ is the total conduction

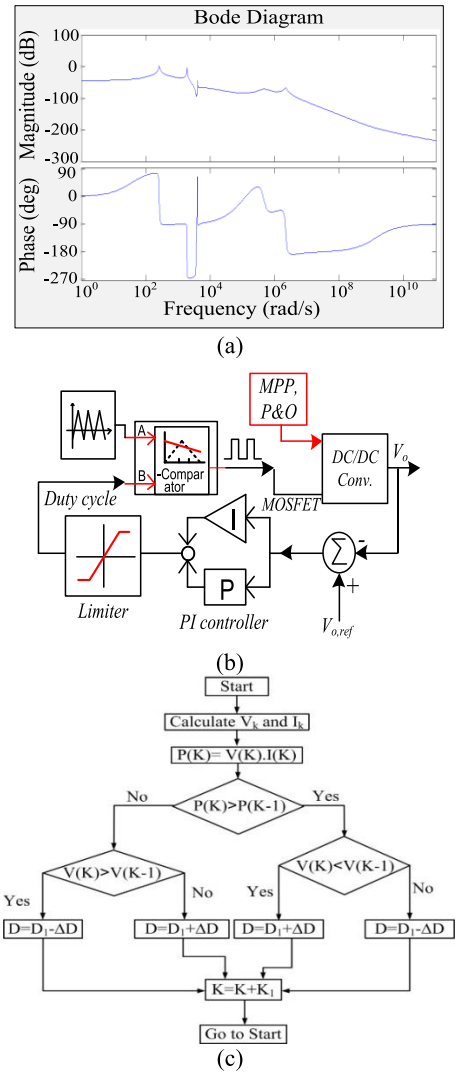

FIGURE 7. Dynamic of the proposed topology, (a) Bode plot, (b) Closed-loop control structure, (c) P&O flowchart.

TABLE 2. Characteristics of the suggested topology's elements.

V_{in}	12V
f_s	50 kHz
Inductor L_1	1mH
Inductors L_2, L_3,…, L_n	500 μH
Capacitors $C_{o(n-1)}$	330 μF
Capacitor C_{on}	470 μF
Power switch	2*SK*3131
Diodes	*MUR*1560

loss of diodes and obtained as (61).

$$P_{Loss}^{Forward\ Voltage} = \sum_{j=1}^{Number\ of\ Diodes} V_{D_j} I_{D_j}^{avg} \tag{60}$$

$$P_{Loss}^{Conduction\_Diodes} = \sum_{j=1}^{Number\ of\ Diodes} r_{d\_D_j} \left(I_{D_j}^{rms}\right)^2 \tag{61}$$

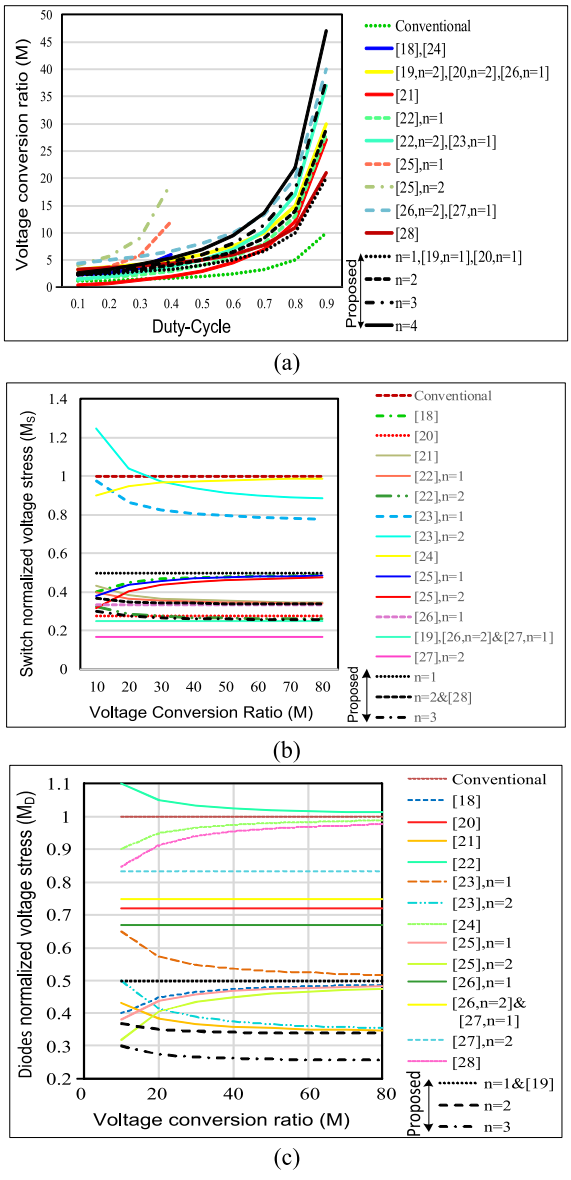

FIGURE 8. Comparison results, (a) M_{CCM}, (b) V_S/V_o, (c) V_D/V_o.

The magnetic components loss can be expresses as:

$$P_{Loss}^{L} = P_{Loss}^{Cores} + P_{Loss}^{Conduction\_L} \tag{62}$$

where P_{Loss}^{Cores} and $P_{Loss}^{Conduction\_L}$ are calculated as (63) and (64), respectively:

$$P_{Loss}^{Cores} = \sum_{j=1}^{Number\ of\ L} P_{L_j}^{Cores} \tag{63}$$

$$P_{Loss}^{Conduction\_L} = \sum_{j=1}^{Number\ of\ L} r_L \left(I_{L_j}^{rms}\right)^2 \tag{64}$$

Finally, the capacitors total conduction loss can be written as follows:

$$P_{Loss}^{Capacitors} = \sum_{j=1}^{Number\ of\ Capacitors} r_{C_j} \left(I_{C_j}^{rms}\right)^2 \tag{65}$$

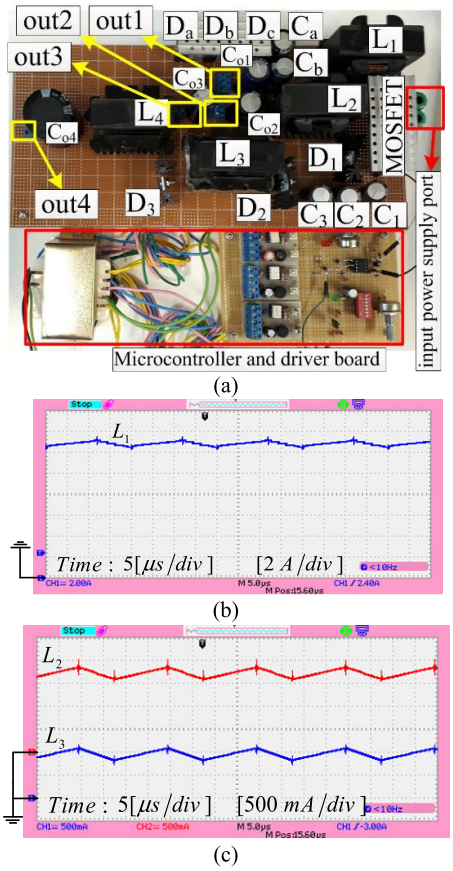

FIGURE 9. The laboratory prototype (with n = 3,4), the current waveforms of the inductor with n = 3 and the average input current, (a) The laboratory prototype, (b) L_1, (c) L_2 and L_3.

TABLE 3. Experimental results and simulation results of the proposed converter with $n = 3,4$.

Components	n=3		n=4	
	Sim.	Exp.	Sim.	Exp.
Max. voltage across switch S [V]	30.08	30.03	69.50	69.41
Ave. current switch S [A]	13.06	13.08	22.48	22.53
RMS current switch S [A]	17.43	17.47	29.78	29.88
Max. voltage across diode D_1 [V]	30.07	30.01	30.02	29.95
Ave. current diode D_1 [A]	1.75	1.79	2.88	2.92
RMS current diode D_1 [A]	3.04	3.09	5.15	5.18

VII. EXPERIMENTAL RESULTS

To confirm the mathematical analysis, the experimental prototypes (with $n = 3$ and $n = 4$) are built. The characteristics of each element are given in Table 2. In this section, Figs. 9-12 illustrate the experimental results of the presented converter of Fig. 2(a) for $n = 3, 4$ at CCM operation. Fig. 9(a) shows the laboratory prototype of the suggested topology for $n = 3, 4$.

Figs. 9 and 10 related to case $n = 3$ at CCM operation. Fig. 9(b) illustrates the current waveform of L_1. By observing Fig. 9(b), the current of L_1 is almost 15.5A. The ripple of L_1 is 0.9% that is confirmed (32). Fig. 9(c) shows the current waveforms of L_2 and L_3. By observing Fig. 9(c), the current of L_2 is 1.71A. The ripple of L_2 is 15.8% that is confirmed (32). The current of L_3 is 0.94A. Also, the ripple current of L_3 is about 28.7% which confirms (32). Fig. 10(a) exhibits the voltage of C_{o2} and C_{o3} which are about 78V and 96V. The obtained value for output voltages of the capacitor C_{o2} and C_{o3} confirm (21).

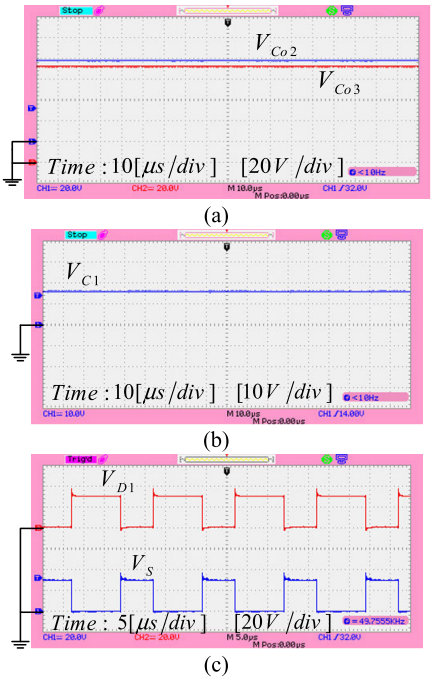

FIGURE 10. The maximum voltage waveforms, (a) capacitors C_{o2} and C_{o3}, (b) capacitor C_1, (c) switch S and diode D_1.

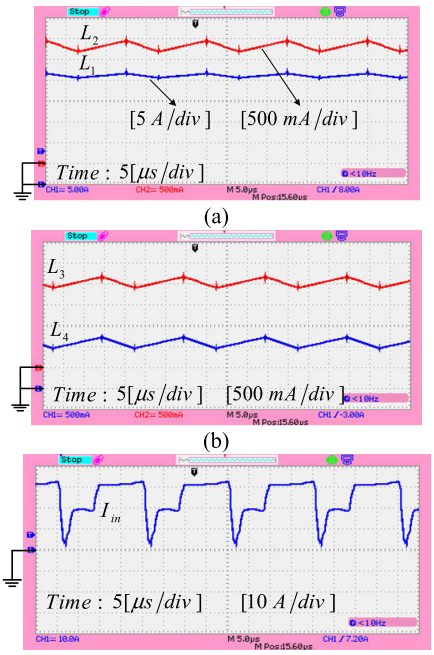

FIGURE 11. The current waveforms of the inductor with n = 4 and the average input current, (a) L_1, (b) L_2 and L_3, (c) The input current.

Fig. 10(b) depicts the voltage of C_1 which is 16V. The measured value for V_{C1} confirms (17). Fig. 10(c) depicts the maximum voltage of S and D_1 which are about 30V and 30V, respectively. This value verifies the equation (4). Figs. 11 and 12 related to case $n = 4$ at CCM operation.

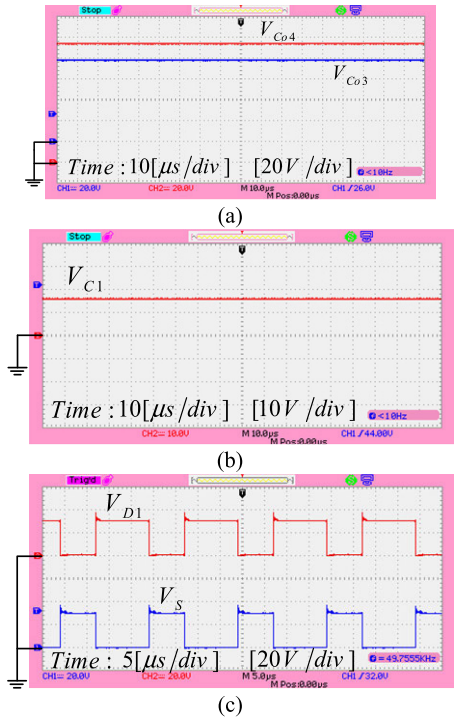

FIGURE 12. The maximum voltage waveforms, (a) capacitors C_{o3} and C_{o4}, (b) capacitor C_1, (c) switch S and diode D_1.

Fig. 11(a) shows the current of L_1 and L_2. According to Fig. 11(a), the current of L_1 is 26.1A. The ripple current of L_1 is 0.75% that is confirmed (32). Also, the current of L_2 is 2.83A. Ripple current of L_2 is 8.7% that is confirmed (32). Fig. 11(b) shows the current of L_3 and L_4. With regarding this figure, the average current of L_3 and L_4 are almost 2.07A and 1.12A, respectively. Also, the ripple current of the inductors L_3 and L_4 is about 13% and 24%, respectively. The input current with $n = 4$ is shown in Fig. 11(c). Fig. 12(a) depicts the voltage of the capacitors C_{o3} and C_{o4} which are about 96V and 114V. The obtained voltages of the capacitor C_{o3} and C_{o4} confirm (21). Fig. 12(b) exhibits the voltage of C_1 which is about 16V. The achieved value for V_{C1} confirms (17). Fig. 12(c) exhibits the maximum voltage of S and the maximum voltage of D_1 which are about 30V and 30V, respectively. By comparing Fig. 10(c) and Fig. 12(c), the obtained maximum voltage value of the power switch S is equal for $n = 3$ and $n = 4$. Therefore, the peak voltage of the switch is reduced by enhancing the VMCS.

By inspecting Fig. 10(c) and Fig. 12(c), the peak voltage of the diodes is reduced when the number of n is increased. The waveforms of D_2, D_3, D_a, and D_c are not depicted because the maximum voltage stress value across these power diodes is similar to diode D_1. The peak voltage value of D_b is equal to D_1, but the complement forwards each other. The experimental and simulation results are compared in Table 3 which match each other.

Fig. 13 illustrates the experimental efficiency for $D = 0.6$. Regarding Fig. 13(a), the maximum efficiency (96.71%) is obtained with about 283W power level when $n = 3$. The

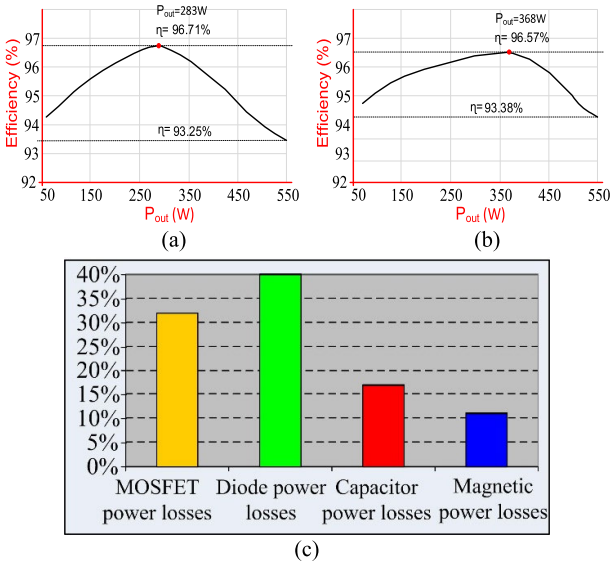

FIGURE 13. The efficiency for diverse power levels and total losses, (a) The efficiency with n = 3, (b) The efficiency with n = 4, (c) Total losses of each element.

efficiency of the suggested topology is 95.86% at 368W. The minimum efficiency is equal to 93.25 % with $n = 3$ for all power levels. Therefore, by noticing Fig. 13(a), the tolerances efficiency limits to 3.21% for 550W power level. Fig. 13(b) illustrates the efficiency versus different powers, when $n = 4$. By observing this figure, the maximum efficiency is 96.57% for 368W. Therefore, can be said that the maximum efficiency is obtained in higher powers when the VMCs are increased. Finally, the current and the voltage of the suggested topology are enhanced by adding the VMCs. Thus, the power will be enhanced. Power losses of each element are pictured in Fig. 13(c). As can be seen in this figure, the major losses are related to semiconductors.

Figure 14 shows the dynamic response for 50% changes at the load's current. Based on this figure, the output voltage of the capacitor C_4 is about 114 V and the output current of this port is approximately 1.20 A. Then, with a sudden change (50% changes) in load, the converter power enhances to 1.80A in the output port of capacitor C_4. The output voltage of the converter, reaches 112.8 V after transient changes of 400 m-seconds. Due to the high output power, the output voltage is 1.2 V lower than the reference voltage which is about 114 V. Therefore, the closed-loop system is stable and the output voltage can be fixed in reference value.

The MPPT algorithm performance is verified with Simulink. For this work, the proposed converter is simulated with a $P_{mpp} = 300$ W (for irradiance = 1000 W/m^2) PV panel. Figure 15, shows the result of Simulink. As can be seen in this figure, at $0 < t < 5$ sec, the irradiance of the PV panel is equal to 600 W/m^2. For this value of irradiance, the available power of the PV panel is 167 W and the MPPT algorithm tracks the power at 160 W with 95.8 % efficiency. At $5 < t < 10$ sec, the irradiance is changed to 800 W/m^2. For this value of irradiance, the available power of the PV panel is 260 W and the MPPT algorithm tracks the power at

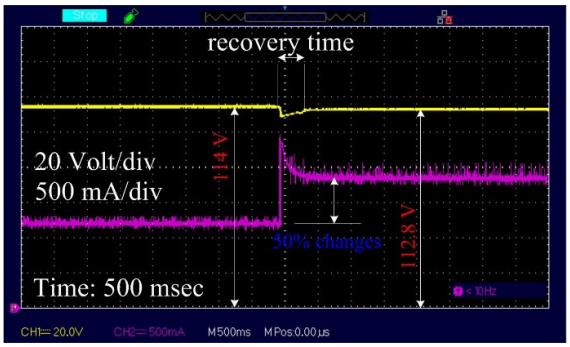

FIGURE 14. Dynamic response for 50% changes at the load's current.

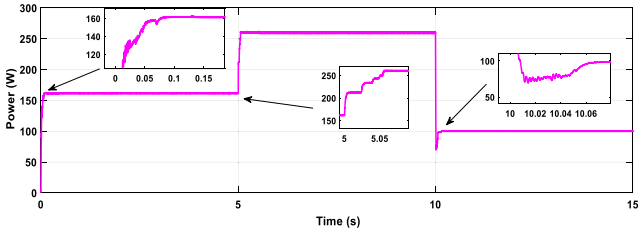

FIGURE 15. Simulink result to verify the performance of the MPPT algorithm.

250.8 W with 96.5 % efficiency. Finally, at $10 < t < 15$ sec, the irradiance is changed to 400 W/m^2. For this value of irradiance, the available power of the PV panel is 110 W and the MPPT algorithm tracks the power at 99.89 W with efficiency of 90.8 %.

VIII. CONCLUSION

A new high-efficiency SIMO converter is presented. The suggested topology has a single power switch, so it has a simplified control method. Based on the obtained results, can be said that the power losses of the suggested structure are reduced by enhancing the VMCs. Thus, by lower $R_{DS(ON)}$ of the switch, the efficiency of the recommended topology is higher than 93 % and finally the overall cost is decreased. The efficiency is almost 93.25 % at rated power (550 W) for $n = 3$ and 94.5 % for $n = 4$. Also, the output power can be controlled by duty-cycle value, hence can be said that each output can have a suitable power level for independent applications. To achieve a high voltage level for each output, this topology could be widespread to n stages of VMCs. Hence, each output power level will increase. The experimental and mathematical results indicate that the proposed converter is obtained low voltage stress and high overall efficiency at all power levels. Therefore, the proposed converter could be a good candidate for renewable usages.

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