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A 3rd/5th Order Active RC Chebyshev Analog Baseband Low-Pass Filter With Reconfigurable Bandwidth and Gain

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ABSTRACT The design of 3rd/5th order active RC Chebyshev low-pass filter (LPF) with reconfigurable bandwidth and gain is based on 55 nm CMOS technology. The filter is integrated into draft IEEE 802.11ax concurrent dual band four antenna transceiver analog baseband circuit. Programmable capacitor bank of the filter is used to adjust bandwidth. The typical bandwidth of receiving filter is 10/20/40 MHz, and that of transmitting filter is 12/24/50 MHz. Adjust the gain ranging from −10 to 18 dB in passband by programmable resistor bank. The current consumption of typical bandwidth of receiving filter is 2.08 mA at a 1.5 V supply and has properties of 10 MHz bandwidth (BW), 36 dB gain, −62 dBm input signal, −39 dB third intermodulation distortion (IMD3), 17.1 nV/$\sqrt{}$Hz equivalent input noise (EIN). As for transmitting filter, the current consumption of typical bandwidth is 1.25 mA at a 1.5 V supply and has the properties of 10 MHz BW, −6 dB gain, 0 dBm input signal, −38 dB IMD3, 75 nV/$\sqrt{}$Hz EIN. Area of the whole filter is 0.08 mm^2.

INDEX TERMS Active RC, analog baseband, low-pass filter.

I. INTRODUCTION

Wireless local area networks (WLAN) is the product of computer network and wireless communication technology. IEEE 802.11 protocol has been experienced a/b/g/n/ac/ax version and the rate of data throughput is getting higher and higher [1], [2]. The bandwidth of IEEE 802.11a/b/g system is 20 MHz whereas it can reach to 40 MHz in IEEE 802.11n by using high throughout and bandwidth can be 80 MHz or even 160 MHz in IEEE 802.11ac. The maximum bandwidth is 160 MHz in IEEE 802.11ax [3], and reconfigurable low-pass filter (LPF) has great importance in design of the direct-conversion or zero intermediate frequency (IF) receiver structures, with a cutoff frequency of 10/20/40/80 MHz required. The devices of 802.11ax are designed to operate in existing 2.4- and 5-GHz spectrums, requiring a dual-band transceiver. In the literatures and commercial products, two separate radio frequency (RF) transceiver channels are used different operating frequencies and integrated together to enable 2.4-/5-GHz dual band operation [4]–[9]. There are two major issues when the wideband LPF is designed. One is the selection of filter prototype, that is, Butterworth or Chebyshev. The other is selection Gm-C or active-RC.

As for selection of LPF prototype, filter rejection response and group delay response must be considered. Owing to the stringent adjacent channel rejection of IEEE 802.11 and rectangular spectra of orthogonal frequency division multiplexing (OFDM), the filters of Chebyshev are more suitable and require less orders than Butterworth. Since OFDM systems can tolerate a non-uniform group delay response, making Chebyshev filters more suitable [10].

Regarding the selection of Gm-C or active-RC, amplifier of Gm-C filter is open loop making it possible to obtain higher frequency easily and less power consumption, however the linearity performance is severely degraded. In the active-RC filter, amplifier is employed in closed-loop state, with good linearity, however capacitor and resistor element are vulnerable to influence of process, voltage and temperature, leading to the direct changes of frequency. IEEE 802.11ax requires high linearity to receiver, the active-RC filter has wide dynamic ranges and is suitable for WLAN since OFDM with 1024 quadrature amplitude modulation (QAM) [11]–[13] requires a high linearity.

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Filter is one of the core module of transceiver with a Zero-IF, main function of transmitting IF filter is to filter out noise at sampling frequency of digital to analog converter (DAC) which is at least 2 times of the useful signal frequency. Therefore, transition band of transmitting IF can be slow, whereas filter of receiving IF needs to have strong frequency selectivity and transition band can be relative steep. So the order of transmitting filter is lower than that of receiving filter. Filter is designed in the way of configurable order, and high-order filter is used when receiving link is working whereas the low-order filter is employed when transmitting link is working, which can reduce power consumption, noise, and linearity of transmitting. In this way, receiving IF filter is multiplexed with transmitting IF filter, and the appropriate gain and low-pass cut-off frequency are configured according to signal size and bandwidth requirements, which can be great flexibility and cut down area of transmitting IF filter.

In 2006, Broadcom designed a transceiver architecture based on low-pass filter multiplexing by using Gm-OTA-C integrator. The receiving filter and transmitting filter are both fourth-order Chebyshev's leapfrog architecture, with an adjustable range of 2-15 MHz or 10-25 MHz [14]. In 2009, Samsung designed a transceiver structure based on IF low-pass filter multiplexing by using a 5th order Chebyshev Gm-C filter. The corresponding RX mode (SW1 and SW2 are on) and TX mode (SW3 and SW4 are on) can be adjusted by using different switches [15]. The first two are characterized by the same order of LPF, and linearity will be deteriorated by using Gm-C integrator. In 2014, M. He, *et al.* designed a transceiver structure based on IF low-pass filter multiplexing. The 5th order Chebyshev active RC biquad architecture is applied to RX/TX mode, supporting all IEEE 802.11a/b/g/n/ac and public safety standards [4]. It is characterized by the same filter order. In our design, Chebyshev active RC leapfrog architecture with different orders is adopted so that the order can be reconstructed and have good linearity when meeting design specifications.

In this paper, the design of 3rd/5th order active RC Chebyshev LPF is based on 55 nm CMOS technology. The designed filter consists of fully differential operational amplifier, programmable capacitor bank and programmable resistor bank. The bandwidth and gain can be reconfigurable and adjustable independently. The mode can be reconfigurable, that is, transceiver multiplexing, reducing the power consumption, noise, linearity, and area of transmitting filter itself. With Cadence software and Spectre simulator, post layout simulation results verify performance of the design.

II. ARCHITECTURE

A. RX/TX

Filter is one of the core module of transceiver with a Zero-If. The block diagram of RX/TX is shown in Fig. 1. In receiver with zero IF architecture, input signal of analog-to-digital converter during normal operation is 0 dBm, and dynamic range from antenna to baseband is 0-74 dB. Most of gain is provided by IF circuit. In this design, low noise amplifier

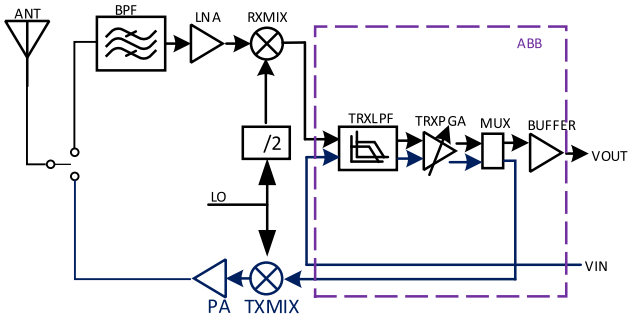

FIGURE 1. The block diagram of RX/TX.

provides a gain dynamic range of 0-24 dB, while gain dynamic range of receiving mixer is 0-14 dB. In addition, receiving IF and transmitting filter provide a gain dynamic range of 0-36 dB and 0-18 dB, respectively. Due to output signal power of digital to analog converter is relatively large, which is about 0 dBm. IF transmitter provides a gain dynamic range from −9 to 3.5 dB, while the gain dynamic range of transmitting filter is from −10 to 2 dB.

B. LPF

The RLC ladder filter synthesis method is adopted in this design. For example, the 5th order low pass filter is obtained from RLC ladder prototype, as shown in Fig. 2. In a 55 nm CMOS process, the error of ploy resistance and metal capacitance with change of temperature and process is about ±20%. Compared with cascade filter, the ladder filter synthesis method is less sensitive to component mismatch and more suitable for high-precision filter.

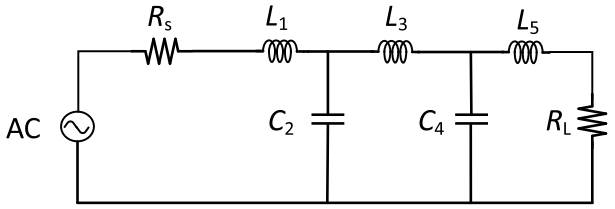

FIGURE 2. The 5th order low pass filter RLC ladder prototype.

The RLC ladder filter synthesis method is to transform node voltage current relationship of passive filter into leapfrog structure, and then to active filter by integrator and adder. The filter of this architecture is easy to implement, and frequency characteristic is relatively fixed even when element value is changed.

III. CIRCUIT DESIGN

A. OPERATIONAL AMPLIFIER

The two-stage fully differential operational amplifier and Miller compensation capacitor technology are used for filter which is shown in Fig. 3. In order to reduce interference of substrate to input small signal, PMOS is used as input different pair transistor. To improving phase margin and stability

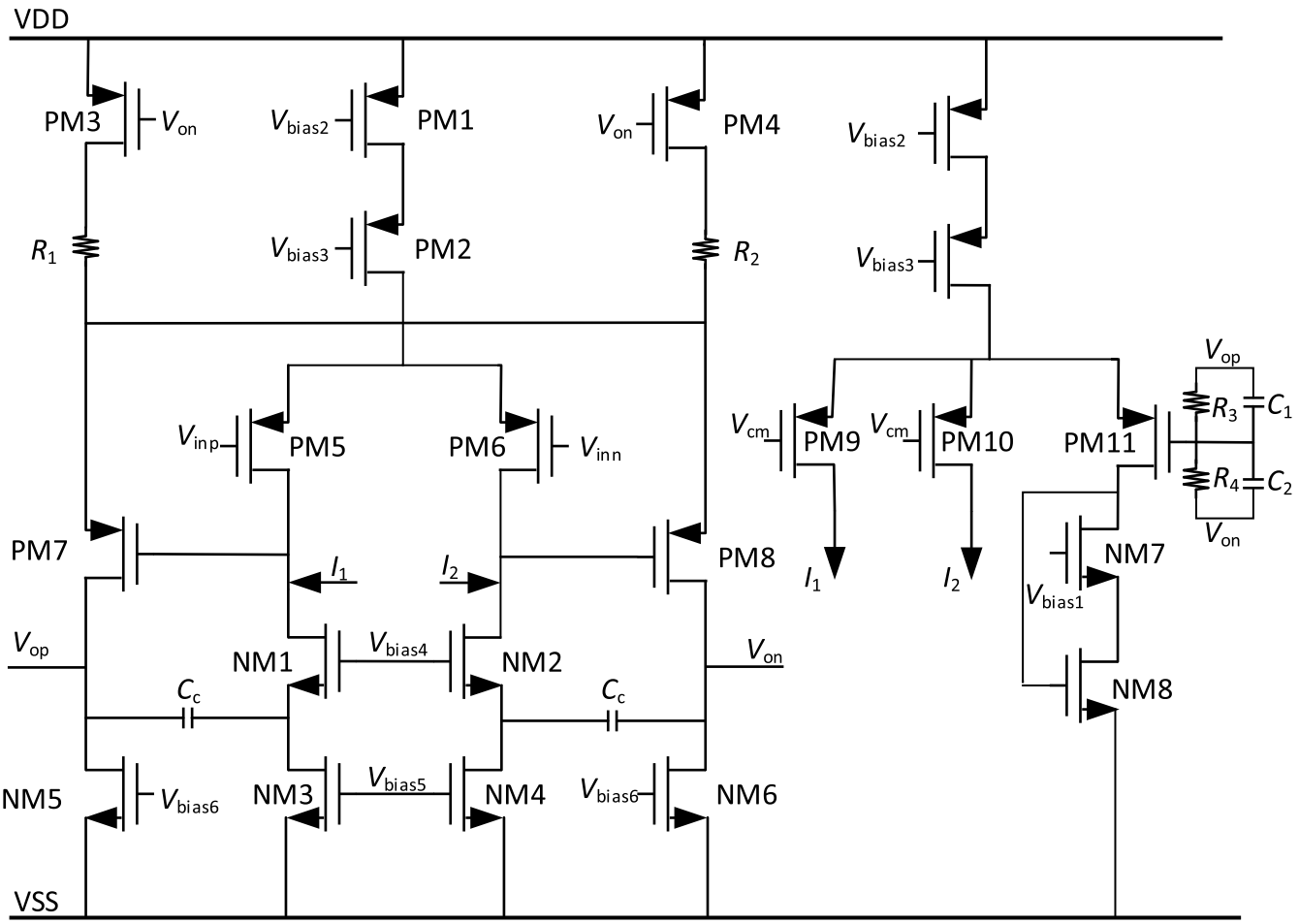

FIGURE 3. The 2-stage Miller operational amplifier.

of two-stage operational amplifier, Miller compensation technology is used to move dominant poles to lower frequency and non-dominant poles to higher frequency to achieve pole splitting. However, right-half-plan zero is introduced to produce a -90° phase shift when Miller capacitors are used. Therefore, the compensation capacitor must be directional in order to eliminate positive zero, that is, transistors are connected in series (as shown in NM1 and NM2) to cut off feedforward path. The fully differential architecture can be used to suppress noise, signal of common-mode, the second and even higher-order harmonics. In this paper, open-loop DC gain and unity-gain frequency are 66.57 dB and 1.11 GHz, respectively. Operation amplifier dissipates 0.437 mA.

B. MODE RECONFIGURATION

Filter is designed in the way of order configurable. First, order number of receiving/transmitting filter is determined. For example, order number of receiving filter is determined according to the out of band attenuation index. $f_1 = 19.7\text{MHz}$, $f_s = 40\text{MHz}$, $A_{\max} = 3\text{dB}$, $A_{\min} = 50\text{dB}$, then $x = \sqrt{\frac{10^{0.1A_{\min}}-1}{10^{0.1A_{\max}}-1}} \approx 316.98$, $y = \frac{f_s}{f_1} = \frac{40}{19.7}$, $n = \frac{\ln(x+\sqrt{x^2-1})}{\ln(y+\sqrt{y^2-1})} \approx 3.94$, the filter order should $f_1 = 19.7\text{MHz}$ be 4 at least. Considering R and C change with temperature and process, the 5th order filter can meet design requirements. Similarly, the design of transmitting filter order is the same. $f_1 = 40\text{MHz}$, $f_s = 80\text{MHz}$, $A_{\max} = 12\text{dB}$, $A_{\min} = 30\text{dB}$, then $x = \sqrt{\frac{10^{0.1A_{\min}}-1}{10^{0.1A_{\max}}-1}} \approx 8.2$, $y = \frac{f_s}{f_1} = \frac{80}{40}$, $n = \frac{\ln(x+\sqrt{x^2-1})}{\ln(y+\sqrt{y^2-1})} \approx 2.12$, the filter order should be 3 at least. Therefore, high order filter is used when receiving link is working, and low order filter is used when transmitting link is working. The order determination of filter is summarized from Table 1.

Next, taking the structure design of 5th order filter as an example, leapfrog structure is carried out. The passive circuit model of filter is shown in Fig. 2. The normalized parameters are obtained by looking up the table: $Rs = 1$, $L1 = 1.14681$, $C_2 = 1.37121$, $L3 = 1.975$, $C4 = 1.37121$, $L5 = 1.14681$, $RL = 1$.

The circuit model transforms passive circuit into active circuit, and relationship between voltage and current is shown in Fig. 4.

TABLE 1. The order determination of filter.

Parameter	Receiving filter	Transmitting filter
Passband frequency f_l (MHz)	19.7	40
Stopband frequency f_s (MHz)	40	80
Maximum passband ripple A_{max} (dB)	3	12
Minimum stopband rejection A_{min} (dB)	50	30
Calculated order	3.94	2.12
Actual order	5	3

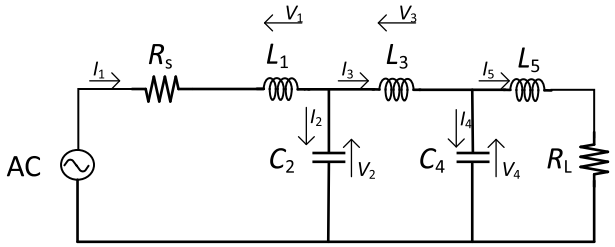

FIGURE 4. The relationship between voltage and current.

The following formula can be got by using Kirchhoff's law,

$$V_1 = V_0 - V_2, V_3 = V_2 - V_4, I_2 = I_1 - I_3, I_4 = I_3 - I_5, \tag{1}$$

so

$$I_1 = \frac{V_1}{sL_1 + R_s}, I_3 = \frac{V_3}{sL_3}, I_5 = \frac{V_4}{sL_5 + R_L},$$
$$V_2 = \frac{I_2}{sC_2}, V_4 = \frac{I_4}{sC_4}, \tag{2}$$

then

$$I_1 = Y_1(V_0 - V_2), I_3 = Y_3(V_2 - V_4), I_5 = Y_5V_4,$$
$$V_2 = Z_2(I_1 - I_3), V_4 = Z_4(I_3 - I_5). \tag{3}$$

The following formula can be got by converting relationship of voltage and current into voltage and voltage,

$$R_pI_1 = R_pY_1(V_0 - V_2) \text{ or } v_{I1} = t_{Y1}(v_0 - v_2),$$
$$V_2 = \frac{Z_2}{R_p}(R_pI_1 - R_pI_3) \text{ or } v_2 = t_{Z2}(v_{I1} - v_{I3}),$$
$$R_pI_3 = R_pY_3(V_2 - V_4) \text{ or } v_{I3} = t_{Y3}(v_2 - v_4),$$
$$V_4 = \frac{Z_4}{R_p}(R_pI_3 - R_pI_5) \text{ or } v_4 = t_{Z4}(v_{I3} - v_{I5}),$$
$$R_pI_5 = R_pY_5V_4 \text{ or } v_{I5} = t_{Y5}v_4, \tag{4}$$

With

$$Y_1 = \frac{1}{sL_1 + R_s}, Z_2 = \frac{1}{sC_2}, Y_3 = \frac{1}{sL_3},$$
$$Z_4 = \frac{1}{sC_4}, Y_5 = \frac{1}{sL_5 + R_L}. \tag{5}$$

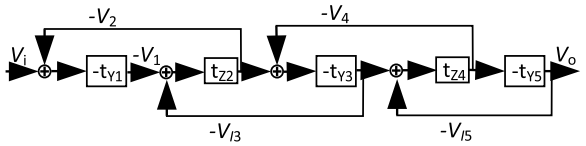

FIGURE 5. The equivalent structure of leapfrog.

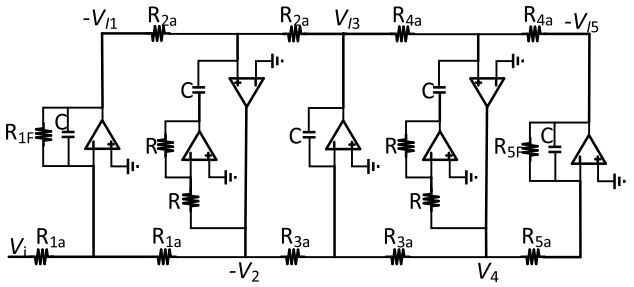

FIGURE 6. The structure diagram of signal ended circuit.

The following formula can be got by transforming relation of difference into sum,

$$-v_{I1} = -t_{Y1}[v_0 + (-v_2)], -v_2 = t_{Z2}[(-v_{I1}) + v_{I3}],$$
$$v_{I3} = -t_{Y3}[(-v_2) + v_4], v_4 = t_{Z4}[v_{I3} + (-v_{I5})],$$
$$-v_{I5} = -t_{Y5}v_4. \tag{6}$$

It is transformed into a structure by using (6), as shown in Fig. 5, with

$$t_{Y1} = R_pY_1 = \frac{1}{\frac{sL_1}{R_p} + \frac{R_s}{R_p}} = \frac{1}{s\tau_1 + q_s}$$
$$t_{Z2} = \frac{Z_2}{R_p} = \frac{1}{sC_2R_p} = \frac{1}{s\tau_2}$$
$$t_{Y3} = R_pY_3 = \frac{R_p}{sL_3} = \frac{1}{s\tau_3}$$
$$t_{Z4} = \frac{Z_4}{R_p} = \frac{1}{sC_4R_p} = \frac{1}{s\tau_4}$$
$$t_{Y5} = R_pY_5 = \frac{R_p}{sL_5 + R_L} = \frac{1}{s\tau_5 + q_L}, \tag{7}$$

Two lossy integrators and three lossless integrators are required by using (7), so

$$-v_{I1} = -t_{Y1}[v_0 + (-v_2)] = -\frac{1}{\frac{sL_1}{R_p} + \frac{R_s}{R_p}}[v_0 + (-v_2)]$$
$$= -\frac{v_0 + (-v_2)}{s\tau_1 + q_s}$$
$$-v_2 = t_{Z2}[(-v_{I1}) + v_{I3}] = -\frac{1}{sC_2R_p}[v_{I1} + (-v_{I3})]$$
$$= -\frac{v_{I1} + (-v_{I3})}{s\tau_2}$$
$$v_{I3} = -t_{Y3}[(-v_2) + v_4] = -\frac{R_p}{sL_3}[(-v_2) + v_4]$$
$$= -\frac{1}{s\tau_3}[(-v_2) + v_4]$$

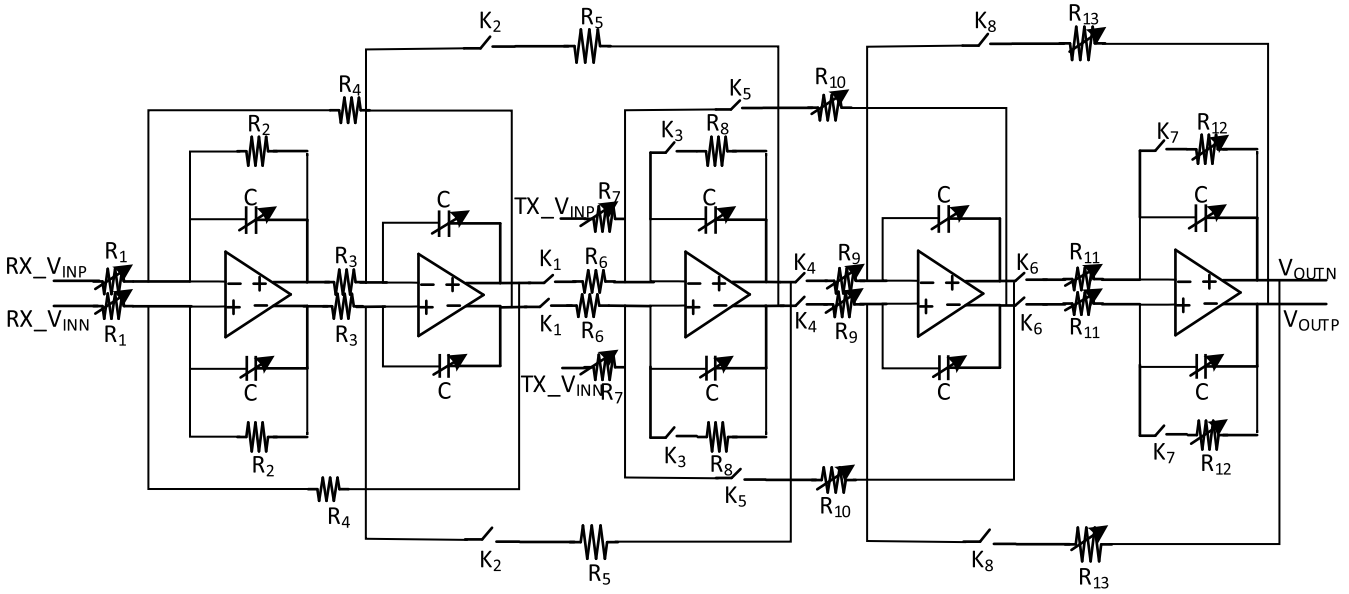

FIGURE 7. The fully differential structure of final 3rd/5th order configurable filter.

$$v_4 = t_{Z4}[v_{I3} + (-v_{I5})] = \frac{1}{sC_4R_p}[v_{I3} + (-v_{I5})]$$
$$= \frac{1}{s\tau_4}[v_{I3} + (-v_{I5})]$$
$$-v_{I5} = -t_{Y5}v_4 = -\frac{R_p}{sL_5 + R_L}v_4 = -\frac{1}{s\tau_5 + q_L}v_4. \quad (8)$$

According to (8), the functional structure diagram of Fig. 5 is transformed into Single-ended circuit structure diagram, as shown in Fig. 6.

According The following formula can be got by substituting normalized parameters into (7),

$$t_{Y1} = \frac{1}{\frac{sL_1}{R_p} + \frac{R_s}{R_p}} = \frac{1}{\frac{s1.14681}{R_p} + \frac{1}{R_p}}$$
$$t_{Z2} = \frac{1}{sC_2R_p} = \frac{1}{s1.37121R_p}$$
$$t_{Y3} = \frac{R_p}{sL_3} = \frac{R_p}{s1.975}$$
$$t_{Z4} = \frac{1}{sC_4R_p} = \frac{1}{s1.37121R_p}$$
$$t_{Y5} = \frac{R_p}{sL_5} = \frac{R_p}{s1.14681 + 1}. \quad (9)$$

Design of resistance and capacitance parameters is as shown below, the first integrator coefficient is defined by comparing the coefficients of integrators, $-v_{I1} = -[v_0 + (-v_2)]/(\frac{s1.14681}{R_p} + \frac{1}{R_p})$, $V_o = -\frac{1}{sCR_{1a}+G_{1F}R_{1a}}(\frac{R_{1a}}{R_{11}}V_1 + \frac{R_{1a}}{R_{12}}V_2)$, so $CR_{1a} = \frac{1.14681}{R_p}\frac{R_s}{\omega_c}$, $\frac{R_s}{R_p} = \frac{R_{1a}}{R_{1F}}$, $R_{1a} = R_{11} = R_{12}$, then $R_{1F}C = \frac{1.14681}{\omega_c}$. Among the value is set for $C = 1.2$pF, $\omega_c = 2\pi * 8.9$MHz, $R_s = 4$ Kohms, then $R_{1a}R_p = 68.36\text{Mohms}^2$. In the same way, $R_{2a} = 5.108R_p$, $R_{3a}R_p = 117.727\text{Mohms}^2$, $R_{4a} = 5.108R_p$, $R_{5a}R_p = 68.36\text{Mohms}^2$. Among the value is set for $R_p = 4$ Kohms, then

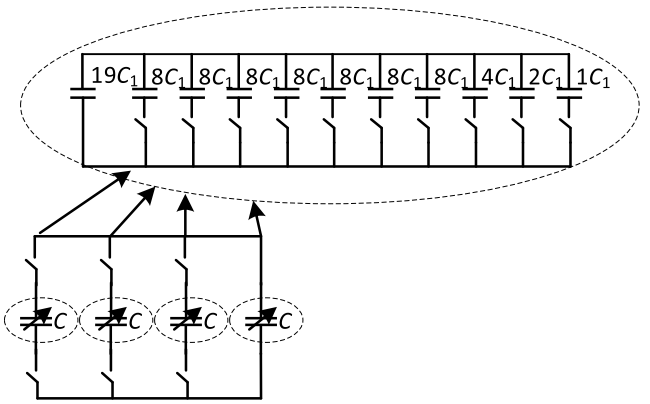

FIGURE 8. The capacitor bank used for bandwidth reconfiguration.

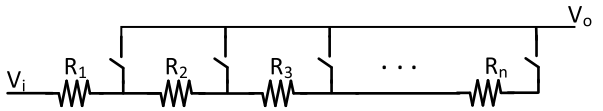

FIGURE 9. The resistor bank used for gain reconfiguration.

$R_{1a} = 17.09$ Kohms, $R_{2a} = 20.432$ Kohms, $R_{3a} = 29.432$ Kohms, $R_{4a} = 20.432$ Kohms, $R_{5a} = 17.09$ Kohms.

Similarly, after circuit design of leapfrog structure, resistance and capacitance parameters of the third-order passive filter are designed as follows, $R_p = 4$ Kohms, then $R_{1a} = 17.09$ Kohms, $R_{2a} = 19.008$ Kohms, $R_{3a} = 17.09$ Kohms.

Finally, the third and the fifth order filters are multiplexed. In order to make filter switch between them and further reduce the complexity of circuit implementation, this design is used $R_s = R_L = R_P = 4$ Kohms, and feedback resistance of filter is adopted the same value $R_F = 17.09$ Kohms.

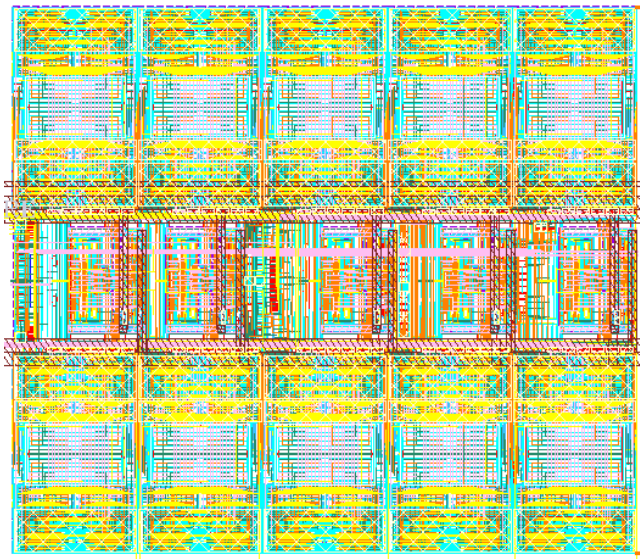

FIGURE 10. The filter layout.

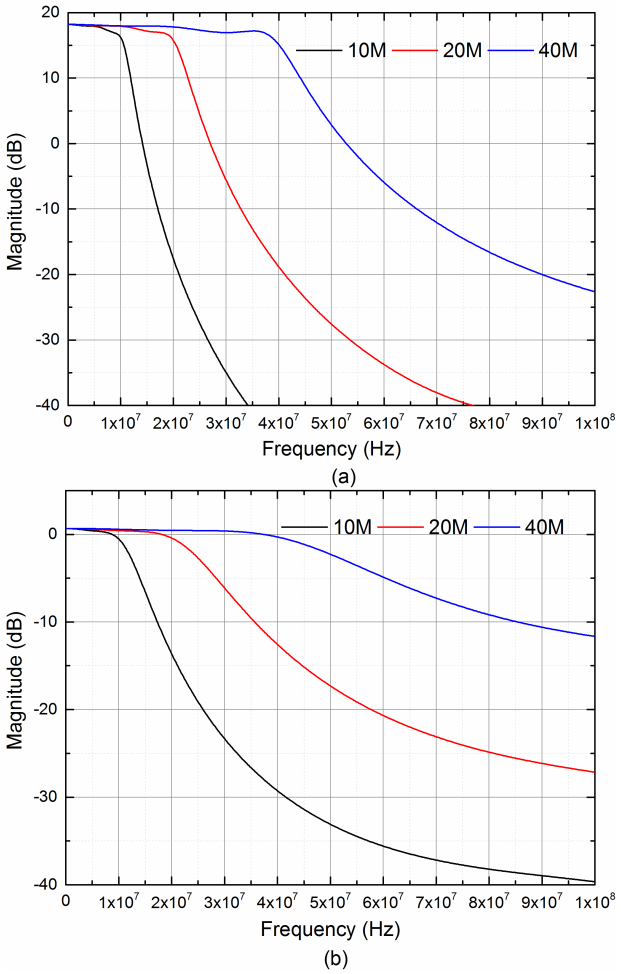

FIGURE 11. Simulated frequency response: a) receiving filter b) transmitting filter.

The fully differential structure of final 3rd/5th order configurable filter is shown in Fig. 7.

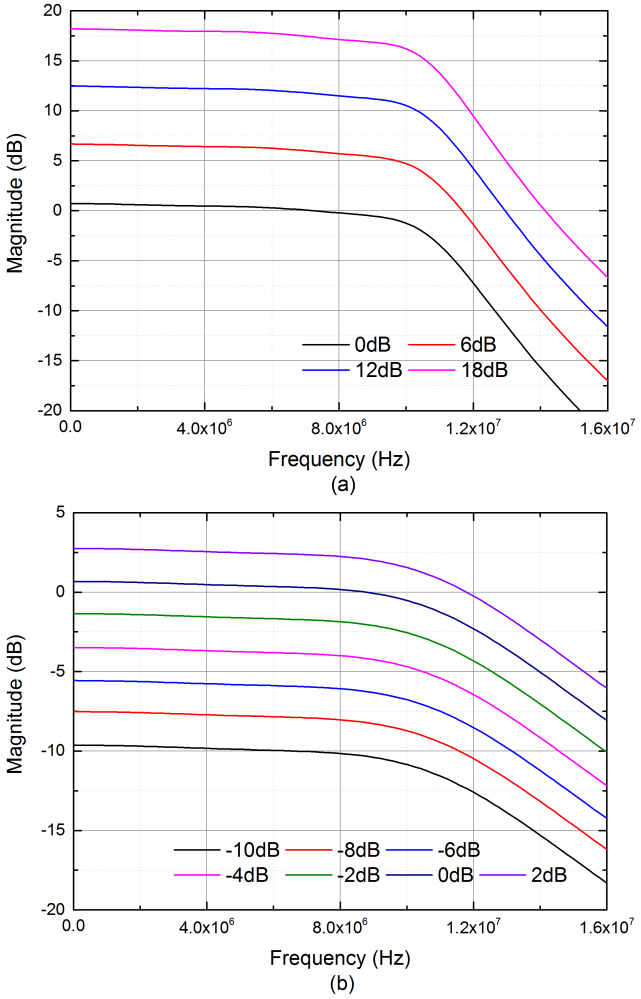

FIGURE 12. Simulated gain characteristics: a) receiving filter b) transmitting filter.

C. BANDWIDTH RECONFIGURATION

In derivation of 5th filter mentioned above, capacitance value remains constant, whereas resistance value varies according to the same adder or reverse adder. Therefore, the cut-off frequency of filter is inversely proportional to capacitance, that is $f_o \propto \frac{1}{C}$, then cut-off frequency of filter can be changed only by controlling whether capacitance is doubled or not, without modifying value of resistance.

The capacitor bank used for bandwidth reconfiguration is shown in Fig. 8. The number of C in connection circuit is used to select filter BW whereas C is shown in circle.

The decoding method of thermometer code and binary code is adopted in capacitor bank. The characteristic of thermometer code is that capacitance values need to be reused as much as possible during continuous adjustment, reducing burr in capacitance calibration process. The characteristic of binary code is that value of capacitance is equal to weight of corresponding control code, which is convenient to adjust capacitance value flexibly. Considering advantages of

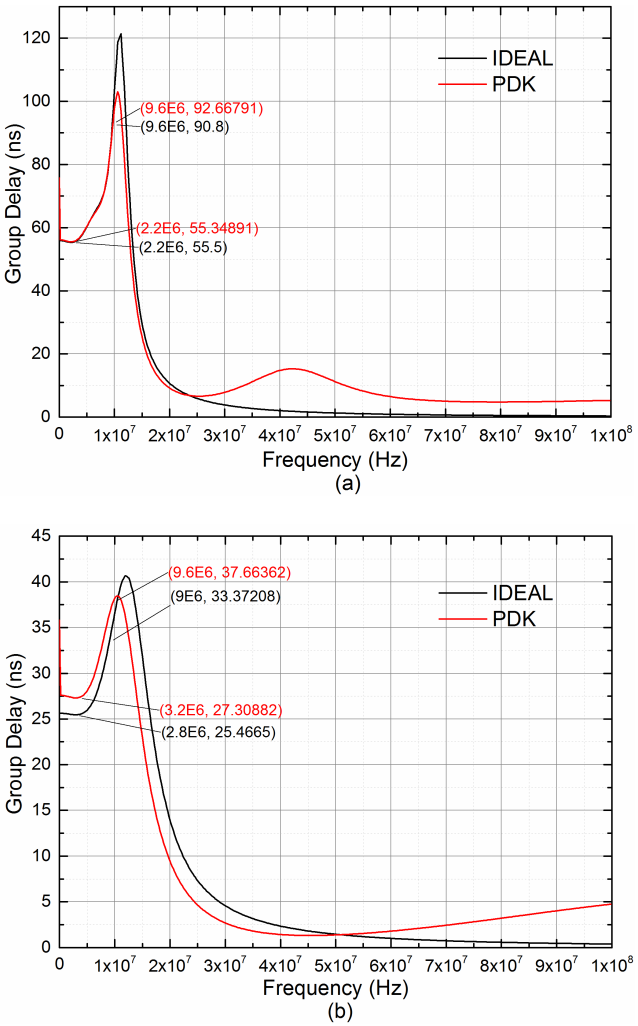

FIGURE 13. Simulated group delay characteristics: a) receiving filter b) transmitting filter.

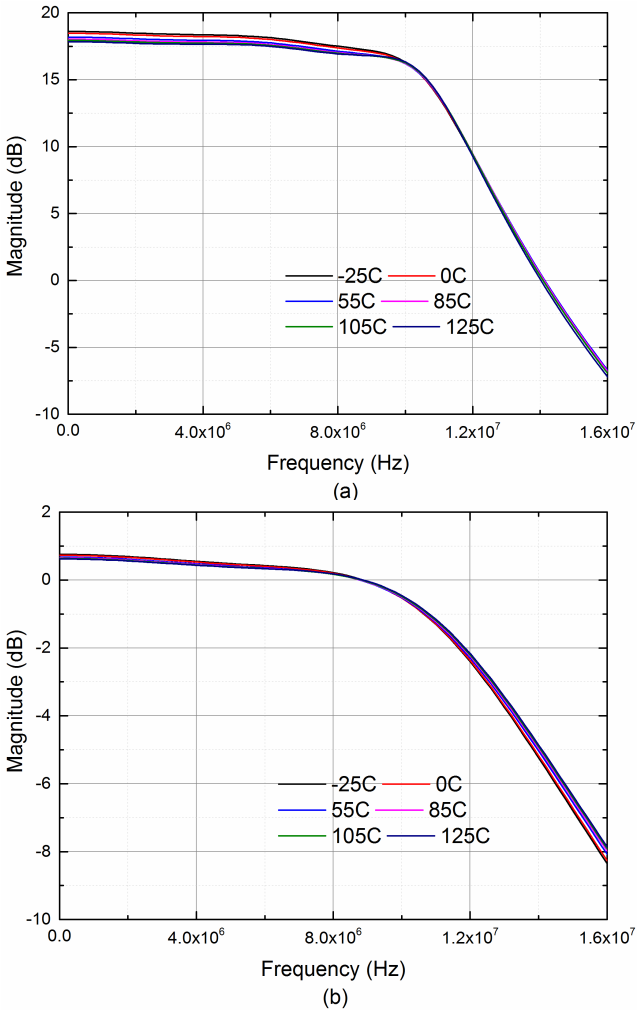

FIGURE 14. Frequency characteristic for different values of tempera-ture: a) receiving filter b) transmitting filter.

each coding method, high bit thermometer coding and low bit binary coding of control code are adopted. The typical cut-off frequency of receiving filter controlled by capacitor bank is 10/20/40 MHz, and that of transmitting filter is 12/24/50 MHz.

D. GAIN RECONFIGURATION

In order to control bandwidth and gain independently, the values of input resistor bank (R1 and R7) are adjusted to achieve corresponding gain. The gain of receiving filter is 0-18 dB, and each step is 6 dB. The gain of transmitting filter is −10 to 2 dB, and each step is 2 dB. Both receiving filter and transmitting filter adopt the same resistor bank design method. The resistor bank used for gain reconfiguration as shown in Fig. 9.

The switch is composed of transmission gate, which gate size is large enough to make parasitic resistance negligible. The output of one-hot resistor bank is connected to virtual ground terminal of active filter. Then half of parasitic capacitance on transmission gate switch is grounded, which reduces parasitic capacitance effect and optimizes frequency response.

TABLE 2. The key specifications of receiving filter.

Parameter	This work
Technology	55 nm CMOS
Filter Type	Active RC Chebyshev
Filter Order	5
Supply Voltage (V)	1.5
Current @1.5V (mA)	2.08
Typical receiving filter BW (MHz)	10/20/40
Pass-band gain (dB)	0.7-18.18
Pass-band ripple (dB)	< 0.5
Stop band rejection @20/40/80 MHz offset for 10/20/40 MHz the receiving filter (dB)	17.3/18.4/16
Rx_IMD3 (dB) @Gain: 36 dB, Vin: -62 dBm, BW: 10 MHz	-39
Area (mm^2)	0.08
Settling Time (ns)	< 200

TABLE 3. The key specifications of transmitting filter.

Parameter	This work
Technology	55 nm CMOS
Filter Type	Active RC Chebyshev
Filter Order	3
Supply Voltage (V)	1.5
Current @1.5V (mA)	1.25
Typical receiving filter BW (MHz)	12/24/50
Pass-band gain (dB)	-9.7 to 2.73
Pass-band ripple (dB)	< 0.5
Stop band rejection @20/40/80 MHz offset for 10/20/40 MHz the transmitting filter (dB)	19.8/18.6/14.8
Tx_IMD3 (dB) @Gain: -6 dB, Vin: 0 dBm, BW: 10 MHz	-38
Area (mm^2)	0.048
Settling Time (ns)	< 200

Considering resistance value, linearity, temperature coefficient, area and parasitic capacitance effect, the un-doped and non-silicified polysilicon resistance is superior to the other kinds of resistance. In order to accurately control proportional relationship between resistances, all resistances are composed of standard unit resistance in series or in parallel.

IV. SIMULATION RESULTS

The design of our filter is implemented in a 55 nm CMOS process, and the filter layout is shown in Fig. 10. The receiving filter is fifth order. Five operational amplifiers, upper and lower capacitors for all, and corresponding resistance bank are used. While the transmitting filter is third order, last three operational amplifiers, corresponding upper and lower capacitors are multiplexed. The area of receiving filter is 302 μm∗263 μm, which is about 0.08 mm^2. The area of transmitting filter is 181 μm∗263 μm, which is about

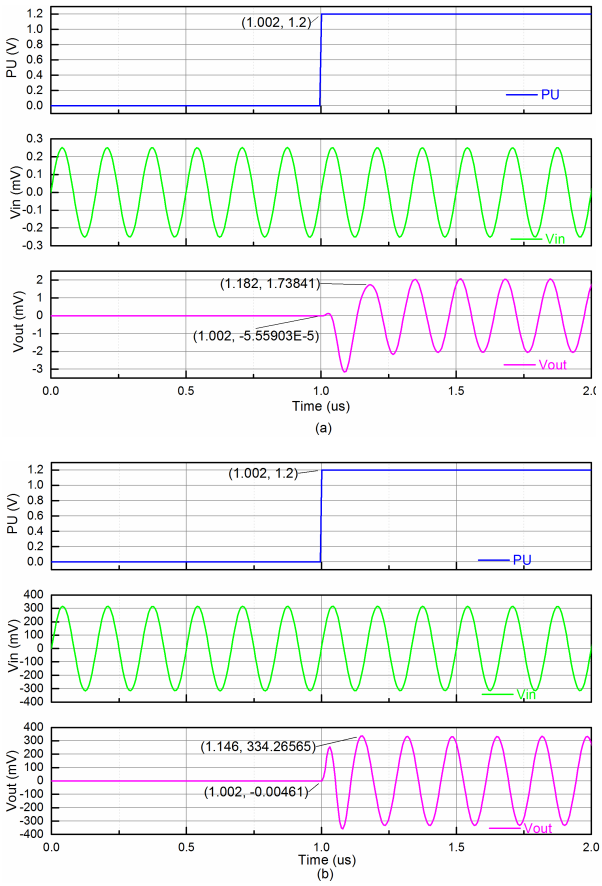

FIGURE 15. Simulated time domain response: a) receiving filter b) transmitting filter.

TABLE 4. Comparison with similar receiving filters.

Parameter	[16] 2008	[17] 2009	[18] 2014	[19] 2019	[20] 2020	This work*
Technology	0.13 um	0.13 um	0.18 um	0.18 um	0.13 um	55 nm
Architecture	Active RC	Active RC	SC	Active RC	Active RC	Active RC
Order	5	1/3/5	5	5	4	5
Type	Butterworth /Chebyshev /Elliptic	Chebyshev /Inverse Chebyshev	Elliptic	Chebychev	Butterworth	Chebyshev
-3 dB BW (MHz)	10/20/40	1-20	10.2	5/10/20/40	20/40/80/160	6-67
Pass-band gain (dB)	-6/0/6	0	0	12	66.56/66.90/66.33/65.72	0.7-18.18
Supply (V)	1.2	1	1.8	1.8	0.6	1.5
Current (mA)	11	0.6-1.5	10	3.8/4/5/5.2/6.04	9.27/17.7/26.07/39.62	2.08
Power (mW)	13.2	0.6-1.5	18	6.84/7.2/9/9.36/10.872	5.56/10.6/15.64/23.77	3.12
Pass-band ripple (dB)	/	/	< 0.5	< 1	/	< 0.5
SFDR (dB)	/	71.4	47	105.4	66.55/60.7/61.83/50.7	48
EIN (nV/ √ Hz)	/	85/52	/	18	54.34/44.59/40.14/41.11	17.1
Area (mm^2)	0.6	1.53	0.412**	0.4921	0.236	0.08

*represents post simulation results.

** includes measured pads.

0.048 mm^2. After multiplexing of transmitting filter, overall layout area is reduced by about 37.5% compared with conventional circuit layout without multiplexing.

The result of post layout simulated frequency response is depicted in Fig. 11. Typical bandwidth of receiving filter is 10/20/40 MHz, and transmitting filter is 12/24/50 MHz. The simulated gain characteristics is shown in Fig. 12. The gain of receiving filter is 0.7-18.18 dB, and step is about 6 dB. The gain of transmitting filter is −9.7 to 2.73 dB, and step is about 2 dB. The simulated group delay characteristics that ideal filter has been compared with actual filter built with PDK is proven in Fig. 13. When cut-off frequency is 10 MHz and gain is 0 dB, the group delay fluctuation of receiving filter is 30.7 ns, and that of transmitting filter is 9.5 ns with PDK. Within useful signal frequency, group delay fluctuation produced by ideal filter and actual filter is not obvious, but there is a significant difference outside band. The frequency response under different temperature corners that is −25 °C, 0 °C, 55 °C, 85 °C, 105 °C and 125 °C, is shown in Fig. 14 and this result proves satisfactory low sensitivity to temperature variations. The simulated output voltage sinusoidal signal in time-domain for filter is depicted in Fig. 15. In this simulation, sine waves input voltage of receiving filter with −62 dBm, frequency is 6 MHz, gain is 18 dB, and transmitting filter is 0 dBm, frequency is 6 MHz, gain is 0 dB. The setting time of both is less than 200 ns, to ensure stable gain required after gain switching.

The key specifications of receiving filter and transmitting filter are summarized as shown Table 2 and Table 3, respectively.

V. COMPARISON TABLE

Comparing some key specifications of designed receiving filter with published state of art similar designs, results are shown in Table 4. By comparison, it is found that the proposed receiving filter has low power consumption (3.12 mW), small area (0.08 mm^2), relatively wide cut-off frequency (6-67 MHz), and certain advantages equivalent input noise (17.1 nV/$\sqrt{}$Hz).

VI. CONCLUSION

In this work, the design of 3rd/5th order active RC Chebyshev LPF is presented. Also, bandwidth and gain can be reconfigurable and adjustable independently by programmable capacitor bank and programmable resistor bank. Moreover, by compared with the characteristics of some previous filters, it is found that proposed receiving filter has some advantages, such as low power consumption, small area, and relatively wide cut-off frequency. The filter is integrated into draft IEEE 802.11ax concurrent dual band four antenna transceiver analog baseband circuit.

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