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Dynamic Power Splitting Simultaneous Wireless Information and Power Transfer Split Receiver for Wireless Sensor Networks

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ABSTRACT Simultaneous wireless information and power transfer (SWIPT) presents a genuine opportunity toward achieving sustainable low-energy wireless devices. This paper introduces a receiver design for an energy harvesting sensor node (SN). The receiver is equipped with multiple radio frequency (RF) inputs. Furthermore, the receiver contains separate circuitries for information decoding (ID) and energy harvesting (EH) with dynamic power splitting (PS). The ID and EH circuits are connected to a power splitter that first combines all the RF inputs and then splits the power between the circuitries. Moreover, dynamic PS allows regulating the power split ratio between EH and ID circuitries. Consequently, the output of the EH circuit can be monitored and increased by adjusting the PS ratio. The proposed receiver design increases the harvestable energy by moving the ID into a separate circuitry. A voltage multiplier arranged in a Dickson scheme is used to level up the received voltage. At the transmitter side, the energy signal (ES) is sent through high power unmodulated continuous wave centered at the carrier frequency, while the information signal (IS) is sent via low power subcarriers around the carrier frequency. Such power allocation increases the harvestable power while reducing interference to external wireless networks. Moreover, different system measurements, including harvested energy from the received signal and data rates, are presented, where the split receiver scheme showed a significant improvement compared to the combined scheme in terms of harvestable power.

INDEX TERMS Simultaneous wireless information and power transfer, power splitting, dynamic power allocation, time switching, power transfer, wireless energy harvesting.

I. INTRODUCTION

The exponential growth in the Internet-of-Things (IoT) field and the related applications led to the introduction of low-energy wireless sensor networks (WSN) [1], where small sensing nodes collect various types of data from the environment [2], ranging from temperature to radiation levels at the nuclear plants. The most significant predicament against any efficient implementation of such WSN is energy sourcing, as these sensors can accommodate a limited size battery. Once that battery is depleted, the battery replacing cost for thousands of such nodes is even more expensive than the cost of the node itself. Not to mention the environmental cost of producing and discarding millions if not billions of batteries and Sensor Nodes (SNs) [3].

One solution to the energy constraint is powering SNs wirelessly [4], [5]. A radio frequency (RF) signal carrying both power and information can be sent to an SN to harvest energy and decode information from the received signal. Therefore, simultaneous wireless information and power transfer (SWIPT) is one of the most discussed topics in the field of low energy sensor networks.

One of the main merits of SWIPT, as the name indicates, is the ability to provide energy and information concurrently. Such merit represents a sustainable solution for battery-limited SNs. There exist two primary SWIPT schemes in the literature, time switching (TS) and power splitting (PS) [6], [7]. PS splits the received signal between the energy harvester and the information decoder. It assigns

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$\rho(t)$ to the energy harvester and $1-\rho(t)$ to the information decoder as shown in Fig. 1, where ADC stands for analog to digital converter and $0 \leq \rho(t) \leq 1$. The energy to rate ratio (E-R) of the received power in PS according to [8] is expressed as:

$$C_{(E-R)} = \left\{ E \leq \eta\rho hP, R \leq \log_2\left(1 + \frac{(1-\rho)\,hP}{(1-\rho)\,\sigma_a^2 + \sigma_d^2}\right)\right\} \tag{1}$$

where h is the propagation channel matrix, P is the average received power, σ_a^2 and σ_d^2 are the antenna noise and conversion noise, respectively, and η is the efficiency of the harvester circuit. In [9], the optimal E-R region for a power splitting system is studied, where the received power is assumed to be linearly proportional to the harvested power. In other words, the energy conversion efficiency η is considered to be independent of the input power. However, such a linear model could lead to resource allocation mismatches [10]–[14]. In [14], a practical nonlinear model based on logistic function is presented, where the proposed model achieved a near-optimal similarity with the measured data. Moreover, the system capacity and resource allocation of PS systems in an orthogonal frequency division multiple access (OFDM) environment are studied in [15], where the authors presented a resource allocation algorithm that approaches the optimal system solution within a small number of iterations.

PS divides the received energy between energy harvesting (EH) and information decoding (ID) circuitries without considering the different power requirements of the EH and ID circuitries [16]. Furthermore, PS in the literature unnecessarily modulates the energy signal (ES), resulting in a high peak to average power ratio (PAPR) thus, incurring an unnecessary burden on the high-power amplifier (HPA). Likewise, the high-power modulated signal can also cause severe interference to external wireless networks.

On the other hand, in TS, the total transmission time is divided between EH and ID [17], which means, at any specific point of time, the receiver can only receive ES or information signal (IS), not both at the same time [18] as shown in Fig. 2, where w is the IS physical bandwidth. Moreover, in time switching, the receiver is harvesting energy for a duration of $(1-\delta)$ and decoding information for δ. Where $\delta = 1$, is the total transmission time. Furthermore, TS in the literature have similar flaws to PS as it modulates the ES at the transmitter. The E-R ratio of TS is expressed as [6]:

$$\mathcal{C}_{E-R} = \left\{ E \leq (1-\delta)\eta hP, R \leq \delta\log_2\left(1 + \frac{hP}{\sigma^2}\right)\right\} \tag{2}$$

In [19], the SWIPT scheme is extended to multiple input multiple output systems (MIMO), where the authors studied and derived the optimal E-R region for MIMO SWIPT. Moreover, a TS MIMO system where each antenna can independently switch between ID and EH is studied in [10]. In [11], [20], the PAPR is used to improve the RF to direct

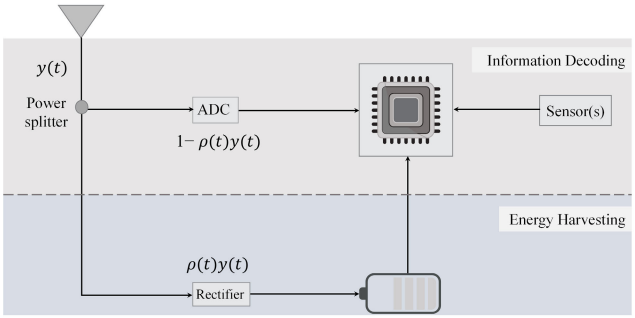

FIGURE 1. Power splitting receiver architecture recreated from [22].

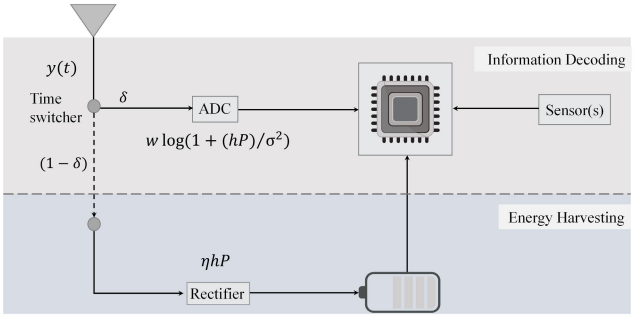

FIGURE 2. Time switching receiver architecture recreated from [23].

current (DC) conversion of the rectifying circuit. In fact, the implementation of multitone waveforms to wireless power transmission (WPT) improves power conversion efficiency significantly due to the pulse-like shape of the multi sine signal [11], [21].

The pulse peak can reach the threshold of the rectifying circuit without increasing the average power. However, this creates a high PAPR, incurring a substantial penalty on the HPA. As a solution to the high PAPR, a novel multitone SWIPT scheme is presented in [24], where the power signal is sent through an unmodulated high-power continuous wave (CW) signal centered at the carrier frequency. While the IS is sent on low power subcarriers around the carrier frequency; thus, the interference to outer devices is minimized since the high-power signal is confined to a very narrow spectrum. However, this work uses one combined circuitry for both ID and EH. Hence, reducing the level of the harvestable power significantly as the distance between transmitter and receiver increases.

A. MOTIVATIONAL EXAMPLE

In wireless communication, when receiving an IS, the signal is required to be just above the noise threshold of the receiving node, around -120 *dBm* [25]. Whereas a state-of-the-art low-power microcontroller, e.g., Texas Instruments MSP430F247, requires at least a power level of 0 dBm to operate [26]. Thus, neglecting the different power requirements of ID and running an SN is not an option. Therefore, any effort to increase the input power level of the EH circuitry is a step toward achieving fully autonomous WSNs.

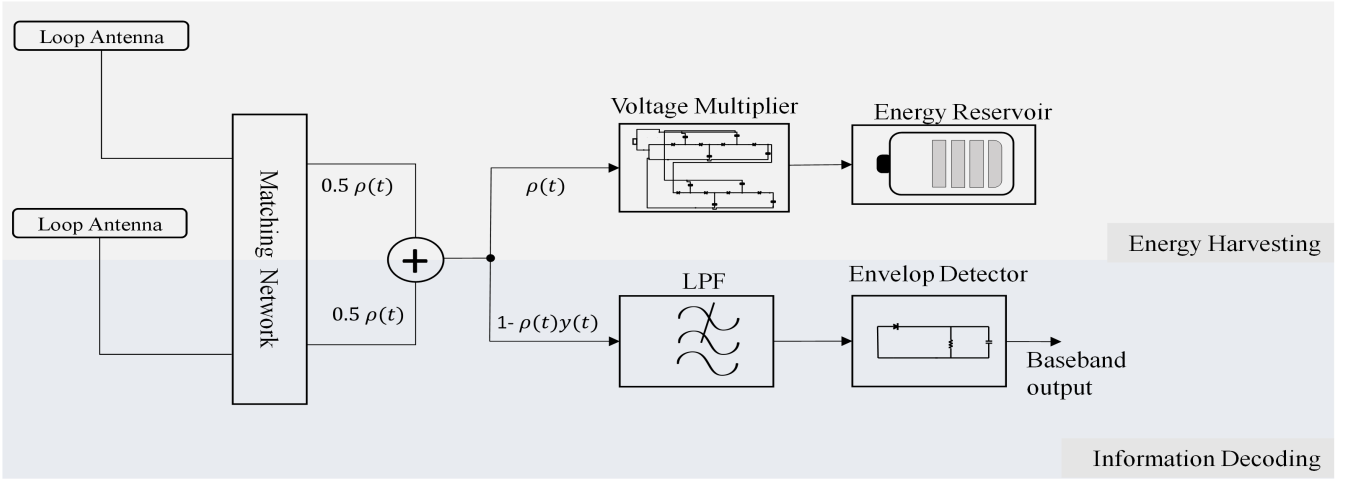

FIGURE 3. Receiver design.

Accordingly, this paper aims to increase the Energy harvester's low input power by allowing more power to flow to the EH circuit by separating the receiver's ID and EH circuitries. And also by adopting a DC-biased high power CW at the transmitter. Hence, providing higher energy levels to the SN without necessarily increasing the interference to outer networks. Ultimately, energy-neutral SNs are essential in many applications, such as manufacturing plants, where a large number of SNs have to be maintained.

The contribution of this paper is the design of a dynamic PS split receiver for WSN with an adjustable PS ratio with the following features. The split design is made to increase the available harvestable power at the EH circuit output (Fig. 13) by moving the ID load to a separate circuit. Moreover, the receiver design combines the input power from multiple RF sources and splits it according to the PS ratio between the EH and ID circuitries. Furthermore, the design fills the gap in PS and TS systems, where the different power requirements of EH and ID are neglected by adopting a dynamic power allocation (DPA), which applies a DC-biased CW to the transmitted signal.

In addition, the adoption of DPA reduces PAPR due to the presence of unmodulated CW high power DC component in the transmitted signal, leading to a more linear behavior. Furthermore, compared to PS and TS, it reduces the interference to external networks, as the high-power CW is confined to a very narrow spectrum at the carrier frequency. Accordingly, the design in this paper is an extension of the work done in [24] to a PS split receiver with an adjustable PS ratio. The PS split receiver scheme provides higher input power to the energy reservoir as there is no ID load sharing the rectified power with the energy reservoir. In short, this article presents an RF energy harvesting system with DPA and an adjustable PS split receiver.

The rest of the article is arranged as follows: section two presents the system model, section three demonstrates results, and finally, section four concludes the paper.

II. SYSTEM MODEL

This section presents the system model. Section A presents the receiver design, section B describes the channel model, section C presents the ID part of the receiver circuit, and section D presents the DC-biased OFDM. The DC bias is considered as the ES. Furthermore, section E presents the diode modeling, and section F presents a voltage multiplier consisting of diodes arranged in Dickson's design. Sections E and F form the EH part of the circuit.

A. RECEIVER CIRCUIT

The receiver circuit consists of antennas, impedance matching network, power splitter, charge multiplier or rectifier, low pass filter, energy reservoir, and an envelope detector, as shown in Fig. 3. The antenna consists of a voltage source and impedance, which are the equivalent Thevenin of a receiver antenna. The normalized power wave at the antenna output is defined as [27]:

$$P_A(t) = V_A(t)/(2\sqrt{Z_a}) \tag{3}$$

The normalized power wave $P_A(t) = \sqrt{\mathrm{W}}$, where W stands for power unit watt. $V_A(t) = V_a(t) + I_a Z_a$ where $V_a(t)$ is the voltage at the antenna connector input, I_a is the antenna connector input current and Z_a is the antenna port reference impedance [27]. Furthermore, $Z_a \in \mathrm{Re}$ and $V_A \in \mathrm{Re}$, where Re is the real part of a complex expression. V_A comprises only RF signal, such that $V_A(t) = \mathrm{Re}[V(t)\, e^{(j2\pi f_c t)}]$, where f_c is the carrier frequency, which is set to 1.5GHz in this paper, as there are numerous rectenna design works in the literature at this frequency, [28]–[32]. The active power of the power wave is equal to the maximum power when the characteristics impedance is real-valued [33].

B. CHANNEL MODEL

The studied system is a point-to-point link between a transmitter and receiver with SWIPT support. The transmitted signal $x(t) = A(t)e^{j\theta(t)}$ is a complex signal, where $A(t)$

stands for amplitude and $\theta(t)$ is the phase shift of the signal $x(t)$. The bandwidth of $x(t)$ is denoted by B. Furthermore, the transmitted RF signal can be given as $s(t) = \sqrt{2P}\mathrm{Re}\left\{x(t)\, e^{j2\pi f_c t}\right\} = \sqrt{2P}\cos(2\pi f_c(t) + \theta(t))$ where P is the average transmitted power, moreover, the bandwidth B of $s(t)$ is considered significantly smaller than f_c. The noise in the system is considered to be a narrow-band Gaussian noise such that $n_{A(t)} = \sqrt{2}\mathrm{Re}\{\bar{n}_A(t)\, e^{j2\pi f_c t}\}$. $n_A(t)$ is the antenna noise, where $\bar{n}_A$ is the equivalent complex noise. $\bar{n}_A$ can be further expanded to quadratic $n_Q(t)$ and in-phase $n_I(t)$ noise components, $\bar{n}_A = n_Q(t) + n_I(t)$. Both $n_Q(t)$ and $n_I(t)$ are assumed to be random Gaussian distributed variables with zero mean and $\sigma_A^2/2$ variance $\sigma_A^2 = N_0 B$, N_0 is the noise power of the one-sided spectrum. $\bar{n}_A(t) \sim \mathcal{CN}(0, \sigma_A^2)$. Furthermore, $\bar{n}_A(t)$ can be considered as a circularly symmetric Gaussian random variable. Moreover, the power combiner and splitter are considered to be passive splitting units. For instance, they do not consume any power, and they do not introduce any noise. Furthermore, the received complex signal with antenna noise is expressed as:

$$y_R(t) = S_R(t) + P_R(t) + \bar{n}_A(t) \tag{4}$$

where $S_R(t)$ and $P_R(t)$ are the IS and ES, respectively. The ES represents the DC-biased CW. Furthermore, due to the conversion losses, the harvestable energy is always smaller than $P_R(t)$.

The received ES at the SN is expressed as follows:

$$P_R(t) = \sum_{n=0}^{N_E} P_n \times e^{j2\pi f_n t} \tag{5}$$

where P_n is the instantaneous received power from the subcarrier f_n. In addition, $(n, \ldots .N_E)$ are the subcarriers used for energy transfer at each instant of time t. Furthermore, for the SN to achieve power independence, the following inequality must be satisfied:

$$E_H \geq E_D \tag{6}$$

$$P_R(t) \geq P_H(t) \tag{7}$$

$$\frac{P_H(t)}{P_R(t)} \leq 1 \tag{8}$$

E_H is the harvested energy, E_D is the dissipated energy by the SN circuitry and $P_H(t)$ is the harvested power. According to (6), the harvested energy should be higher or equal to the consumed energy for the SN to be energy neutral. In addition, (7) ensures that the aggregated received power from subcarriers $(n, \ldots .N_E)$ at time (t) is larger than or equal to the harvested power P_H at time (t). Furthermore, the efficiency of the energy harvester in (8) is the ratio between the power available at the rectifier output and the received ES.

For the IS, an amplitude shift keying (ASK) is implemented as a modulation technique, which is expressed as follows:

$$S(t) = A\cos(2\pi f(t) + \theta(t)) \tag{9}$$

where θ is the phase reference and $A \in \{\beta, 2\beta \ldots, M\beta\}$ is the amplitude, M characterizes the available amplitude levels. The amplitude unit β can be obtained by calculating the average signal power at the receiver and decoding it to the nearest amplitude codeword. The receiver implements an envelope detection [34]; therefore, certain active components can be omitted from the information decoder, such as low noise amplifier (LNA) and local oscillator (LO). Such features consume high power, making it very difficult to design self-sustaining SNs. Accordingly, the power consumption of envelope detection is much lower than it is counterpart IQ-based detection. As proven in [35], the power consumption of envelope detection is 0.016 mW, while for the IQ detection, the power consumption is almost 2 mW, which translates to 125 times more power than envelope detection; this is a direct consequence of the use of active components. The received IS at the sensor node when implementing envelope detection is expressed as follows:

$$S_R(t) = \sum_{m=0}^{M} \sum_{n=1}^{N_R} A_m \cos(2\pi f_n t + \theta) \tag{10}$$

The received IS is a combination of all the carriers used for information transfer $(n, \ldots .N_R)$. For each subcarrier f_n there exist different levels of A_m used to modulate information on the subcarrier. Moreover, the receiver implements non-coherent detection due to the absence of a phase-locked LO with the transmitter carrier. The absence of a synchronized LO increases the error probability, reducing the data rate. However, the non-coherent detection using an envelope detector is less complex and energy-efficient compared to IQ-based detection [35].

C. INFORMATION DECODER

The receiver implements envelope detection [34] to extract information. Envelope detector (ED) is considered one of the earliest and simplest signal detection devices. The ED can be built using a few passive components. A basic envelope detector consists of a diode, capacitor, and resistor that acts as the information decoder's output load. In low data analog applications, such as AM radio, the capacitor can act as a low pass filter that retains the envelope and suppresses most of the carrier signal.

Furthermore, in digital communication applications where the data rate is high, an LC filter is implemented for more effective carrier suppression. The capacitor value of an envelope detector should be large enough to detect the beak of the modulating signal. Nonetheless, it is important to note that choosing larger capacitor values than required could lead to the attenuation of the information content because of the capacitor's inability to discharge fast enough to keep up with the signal. The relation between capacitive reactance and frequency is calculated using the following expression [36]:

$$A_C = \frac{1}{2\pi f_c C} \tag{11}$$

where C is the capacitance in farads, the ED output is equivalent to half of the original envelope, leaving only the positive

half cycle. OFDM is selected as a modulation technique due to it is robustness to frequency selective channels. Furthermore, for the sake of completeness Vienna 5G link Level simulator [37] is implemented to simulate the data rates at the ED output, where f_n is assumed to be a multiple of 12 for the validity of the central limit theorem. Moreover, different power levels of 100 mW and 10 W are allotted for IS and ES carriers, respectively. The rest of the simulation parameters are listed in Table 1.

TABLE 1. Simulation parameter.

Simulation parameters	Value
Carrier frequency	1.5 GHz
Number of simulated frames	10000
Number of symbols per frame	15
Information signal bandwidth	$(15 \times 10^3 \times 60)$ KHz
Energy signal bandwidth	$(15 \times 10^3 \times 12)$ KHz
Modulation type	ASK
Information signal Tx power	20 dBm
Energy signal Tx power	40 dBm
Number of SN antennas	2
Channel coding	LDPC
Decoding algorithm	Sum-Product
Decoding iterations	5

D. BIASED OFDM

As a modification to suit this paper specific application, DC-biased OFDM is adopted. In this type of OFDM, only half of the subcarriers are used to transmit the information, as the frequency domain signal is restricted to have self-adjoint symmetry in order to get a time-domain signal with real values [38]. Thus, when the transmitter performs inverse fast Fourier transform (IFFT), the resulting signal is real. Accordingly, the transmitter adds a cyclic prefix to the signal and then converts it to an analog waveform. The transmitted ISs at any given symbol with a period of t is presented as:

$$S(t) = \sum_{n=1}^{N_R} P(t)_n \, |d(n)| \cos(2\pi f_n t + \theta) \tag{12}$$

where $P(t)_n$ is the transmission power dissipated by subcarrier f_n at time instant t and $d(n)$ is the real-valued IS. In DC biased OFDM, a relatively high DC bias is added to the IS signal $S(t)$ [39]. Furthermore, in RF EH communications, the DC bias can be utilized as the ES. Hence, the transmitted signal can be presented as follows, Where S_{DC} is the DC component.

$$x(t) = S(t) + S_{DC} \tag{13}$$

Furthermore, considering the HPA performance is one of the most critical metrics in any wireless communication system, DPA-SWIPT introduces a continuous high DC bias to the transmitted signal. The dominating DC signal reduces the PAPR, enhancing the end-to-end power efficiency of the system. While in PS SWIPT, the ES is modulated, causing the HPA to consume more power due to the high PAPR. The high PAPR is not just inefficient in terms of power, but it can also degrade the data rate [40].

Moreover, the signal may encounter nonlinear distortion due to clipping [41], especially when the transient signal power surpasses the HPA threshold. Nonlinear distortion sustains a severe penalty on wireless communication systems [42], particularly in multicarrier communications like OFDM, where it can cause intercarrier interference. In DPA-SWIPT, the data-carrying signal is less prone to nonlinear distortion as it is centered by a high-power static wave, thus leading to a more linear behavior.

E. DIODE MODELING

This section evaluates the receiver rectifier circuit. Furthermore, as the diode presents the main component of any rectifier, an analytical model for a diode with nonlinear behavior is used. The diode model utilizes the Shockley diode law, which consists of series resistance R_d and a parallel capacitor C_d. The voltage across the diode is denoted as $V_d(t)$ and the current as $I_d(t)$. Furthermore, due to the low input power of the RF signal, the diode voltage V_d is very small to reach the breakdown point. Hence, a Shockley diode model can be used to model the diode's forward current. Every k diode in the Dickson charge multiplier cascade has a direct RF current input $\mathrm{Re}\left\{I_{d_{rf}}(t)\, e^{(j2\pi f_c t)}\right\}$ and a baseband input from the previous diode $k-1$, $I_{d_b}(t)$. Furthermore, assuming there is no harmonic voltage and current components in the signal, $V_d(t)$ and $I_d(t)$ are expressed as follows:

$$I_d(t) = I_{d_b}(t) + I_{d_{rf}}(t)\, e^{(j2\pi f_c t)} \tag{14}$$

$$V_d(t) = V_{d_b}(t) + V_{d_{rf}}(t) e^{(j2\pi f_c t)} \tag{15}$$

where $V_{d_b}(t)$ and $V_{d_{rf}}(t)$ are the baseband and RF voltages, respectively.

The Shockley diode model is given as [43]:

$$I_d(t) = I_s\left(e^{\frac{V_D}{nV_T}} - 1\right) \tag{16}$$

where I_s is the saturation current, and n is the ideality factor usually ranges between 1 and 2, and it depends on the semiconductor material used and the fabrication process, V_T stands for thermal voltage. Furthermore, the Shockley model can be expanded for the RF signal as follows [24]:

$$I_{d(t)} = I_S\left(e^{\frac{V_{d_b}(t)}{nV_T}} \mathrm{Re}\left[e^{\frac{V_{d_{rf}}(t) e^{j2\pi f_c t}}{nV_T}}\right] - 1\right) \tag{17}$$

$$I_{d(t)} = I_S e^{\frac{V_{d_b}(t)}{nV_T}} \delta_0 \frac{V_{d_{rf}(t)}}{nV_T} - I_S + 2\mathrm{Re}\left[I_S e^{\frac{V_{d_b(t)}}{nV_T}} \delta_1 \frac{V_{d_{rf}(t)}}{nV_T} e^{j2\pi f_c} e^{j\theta \frac{V_{d_{rf}(t)}}{nV_T}} \right] \quad (18)$$

where δ_{f_n} is the modified Bessel function of the first kind [44], k is the kth diode and θ is the phase angle of $V_{d_{rf}(t)}$.

$$\delta_{f_n}(V_d) = \sum_{k=0}^{\infty} \frac{(V_d)^{2!+f_n}}{k!\,(k+f_n)!(2^{2!+f_n})} \quad (19)$$

Due to the rapid damping behavior of the Bessel function, the harmonic components in (18) decrease and decimates rapidly. Thus, the harmonics can be neglected. Furthermore, equation (18) can be decomposed into baseband and RF currents:

$$I_{d_b}(t) = I_S e^{\frac{V_{d_b}(t)}{nV_T}} \delta_0 \frac{V_{d_{rf}(t)}}{nV_T} - I_S \quad (20)$$

$$I_{d_{rf}}(t) = 2I_S e^{\frac{V_{d_b(t)}}{nV_T}} \delta_1 \frac{V_{d_{rf}(t)}}{nV_T} e^{j\theta \frac{V_{d_{rf}(t)}}{nV_T}} \quad (21)$$

F. DICKSON VOLTAGE MULTIPLIER

The RF to DC conversion output is very low due to the well-established inverse square law [45]. Hence, a DC-to-DC voltage multiplier is required to level up the input voltage into practical levels that can be used to power an integrated circuit. Different voltage lifting schemes exist in the literature, including the Cockcroft-Walton charge multiplier, inductor-based potential lifters, and Dickson charge multiplier [46]. Inductor-based charge boosters are large and expensive [47], making them infeasible in board-level applications. Thus, only two practical multiplier schemes can be used for board-level applications: Cockcroft-Walton and Dickson.

Cockcroft-Walton multiplier consists of a cascade of half-wave voltage multipliers where the coupling capacitors and diodes are connected in series. Furthermore, as the number of stages increases, the output voltage drops quickly because of the aggregated output impedance [48], shown in Fig. 4. On the other hand, in the Dickson charge multiplier, coupling capacitors are connected in parallel to the RF source. For example, there is only one capacitor between the RF source and any diode in the Dickson cascade. Hence, reducing the voltage drop across the voltage multiplier. A detailed comparison of various rectification techniques is presented in [49], which showed a conversion efficiency of 92.3% for the Dickson topology. Furthermore, when designing a Dickson charge multiplier, one must consider the last capacitor's voltage tolerance, as the potential difference between its plates is the elevated output of the charge multiplier. A solution tackling this specific problem was recently proposed in [50], which is basically a combination of Dickson and Cockcroft-Walton charge multipliers.

As shown in Fig. 5, the DC voltage across the rectifier is analyzed by following the charge in the Dickson charge multiplier. During the negative half cycle of the RF signal,

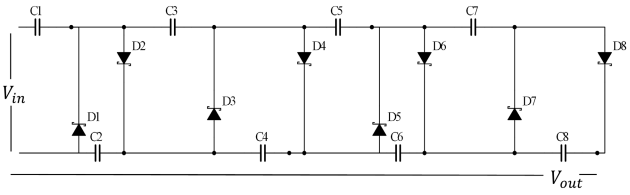

FIGURE 4. 4 stage Cockcroft-Walton multiplier recreated from [50].

the even-numbered capacitors are charged, and consequently, the forward current is drawn through odd-numbered diodes. Likewise, when the incident RF voltage is positive, the odd-numbered capacitors are charged, and the forward current follows in even-numbered diodes. In other words, When the forward current is following through odd-numbered diodes, the even-numbered diodes are reverse biased and vice versa [51]. The input voltage and current of the rectifier are real-valued signals such that $V_{inRF}(t) = V_d(t)\, e^{2\pi f_c(t)}$ and $I_{inRF}(t) = I_d(t)\, e^{2\pi f_c(t)}$. The output voltage and current for an eight stage Dickson multiplier are:

$$V_{Dout}(t) = V_{d8} \quad (22)$$

$$I_{Dout}(t) = I_d \quad (23)$$

where V_{d8} is the output voltage of diode 8, output DC is the same for all diodes in the cascade. Furthermore, the output voltage of the rectifier is as follows:

$$V_{Rout}(t) = \sum_{i=1}^{k} (V_{di}(t) - R_d I_{di}(t)) \quad (24)$$

The incident RF voltage on odd and even diodes at time instant (t) have a phase difference of π, and the same magnitude. Similarly, the RF current for the even and odd diodes has a phase difference of π. In this paper, we simulated a Dickson multiplier using the simulation model of Skyworks SMS7621, a commercial low-power Schottky diode with a breakdown voltage of 2 V and high-frequency support of up 24 GHz, making it an ideal platform to test with different frequencies. For this simulation, 8 diodes and 8 capacitors are implemented. The capacitance of the capacitors is rated at 22 pF, and the carrier signal frequency is set to 1.5 GHz. Furthermore, the findings of this study can be extended to wireless local area network (WLAN) frequencies.

The proposed scheme can be implemented physically, using antennas followed by an RF combiner to combine the different power received by the antenna elements. Furthermore, an RF splitter splits the signal between the information decoder and the energy harvester. The information decoder consists of an envelope detector followed by an analog to digital converter ADC and then followed by a digital signal processor. While on the energy harvester side, the signal goes through a rectification process using low-power Schottky diodes arranged in a Dickson scheme. Then the rectified signal is collected in an energy storage unit, for example, a supercapacitor.

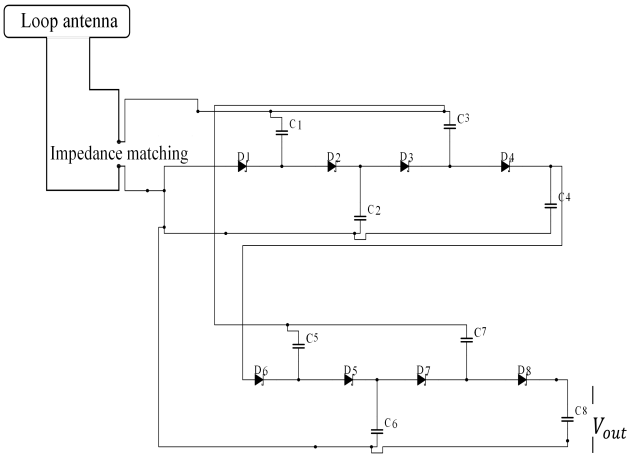

FIGURE 5. 8 stage Dickson multiplier.

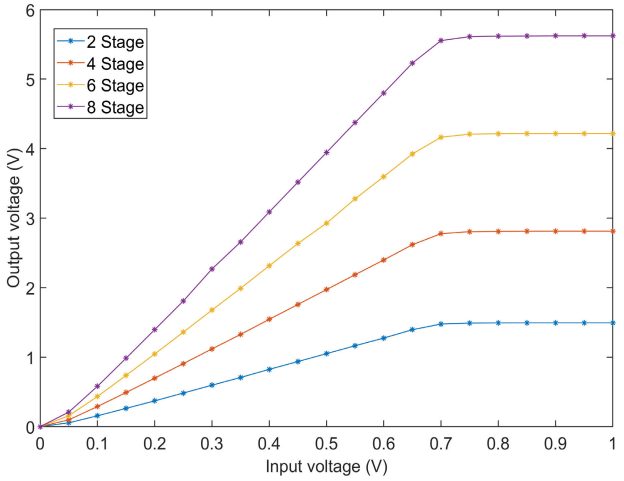

FIGURE 6. Dickson rectifier output voltage throughout 2, 4, 6, and 8 rectifying stages at 0.5 ρ.

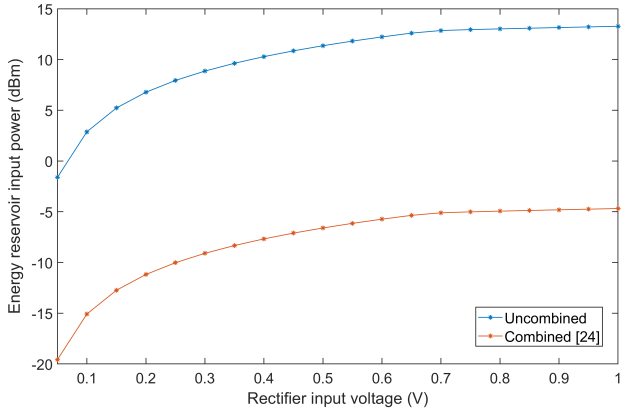

FIGURE 7. Rectifier input voltage VS the energy storage input power at 0.5 ρ.

III. RESULTS DISCUSSION

In this section, the simulation results are presented and discussed to evaluate the presented design. Starting with the most crucial charge multiplier parameter, the output voltage level, Fig. 6 demonstrates the DC output of the energy harvester's Dickson voltage multiplier at 2, 4, 6, and 8 rectifying stages. The multiplier output rises rapidly as the input voltage grows from 0.05 V to 0.65 V. From 0.7 V, the voltage gain starts to become flat due to the rise in the reverse saturation current caused by the high input current, thus, reducing voltage gain. Fig. 7 describes the relationship between the rectifier input voltage and the energy reservoir input power. For the combined and uncombined receiver schemes. Fig. 7 shows that the uncombined receiver design delivers higher input power to the energy storage unit due to the absence of the ID load. Furthermore, it is important to note that the minimum input power to the circuit is equal to the minimum input power of the diode used, SMS762, which is around -5 dBm.

In addition, the rectifier input voltage according to the receiver circuit load over different transmitter-receiver separations is shown in Fig. 8, assuming perfect matching and free space path loss. The input voltage positively increases with the receiver load. This is because higher loads decrease current follow, thus decreasing the power dissipated by the circuit. Moreover, Fig. 9 demonstrates the Dickson charge multiplier's efficiency through 2, 4, 6, and 8 rectifying stages, showing that the charge multiplier efficiency tends to reduce as the input voltage approaches 1 V. When the input voltage approaches 1 V, the input current approaches the maximum forward current of the SMS762 diode, 50 mA. Hence, the forward DC current drops due to the reverse saturation current. The rectifier efficiency in this context is the ratio between the actual rectifier output and the ideal Dickson rectifier output, e.g.,

$$Ideal\ rectifier = input\ voltage * (number\ of\ stages + 1).$$

On the other hand, on the ID side, the bit error rate (BER) of the receiver across different signal-to-noise ratio (SNR) values, implementing the simulation parameters stated in table 1, at 1.5 GHz carrier frequency is depicted in Fig. 10 with and without channel coding. 1000 frames are used in the simulation. Furthermore, the confidence intervals are plotted together with the BER values to demonstrate their statistical reliability. Likewise, the achievable throughput of the ID, also with confidence intervals, is illustrated in Fig. 11, showing relatively adequate data rates when considering the intermittent and low data rate nature of WSNs.

The power spectrum density (PSD) of the DPA-SWIPT transmitter vs. conventional PS and TS transmitter is shown in Fig. 12, indicating that in order to transfer the same power carried by the DPA-SWIPT, all the subcarriers transmission power has to be increased in TS and PS SWIPT, which leads to a higher PAPR. Furthermore, transmitting at high power using large bandwidth may lead to severe interference to outer networks. In DPA-SWIPT, the high power signal is confined in the subcarriers at the carrier frequency surrounded by low power subcarriers carrying the information signal, thus, reducing interference to external networks. Fig. 13 compares the harvestable power between combined and uncombined

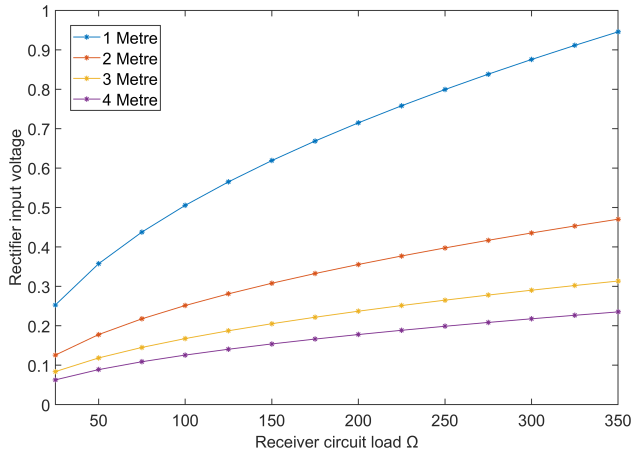

FIGURE 8. Receiver load VS rectifier input voltage at 0.5 ρ.

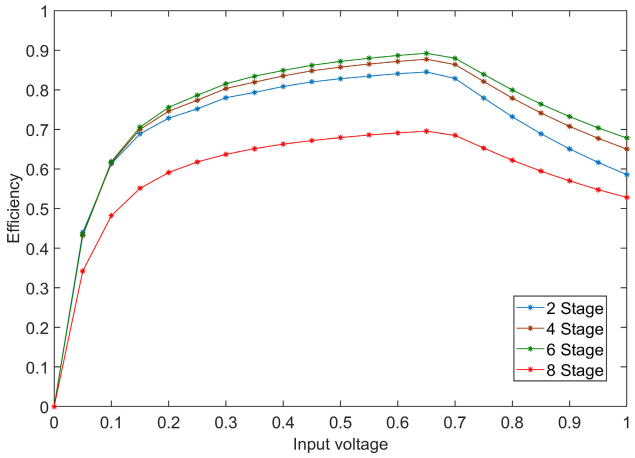

FIGURE 9. Rectifier efficiency over 2, 4, 6, and 8 rectifying stages.

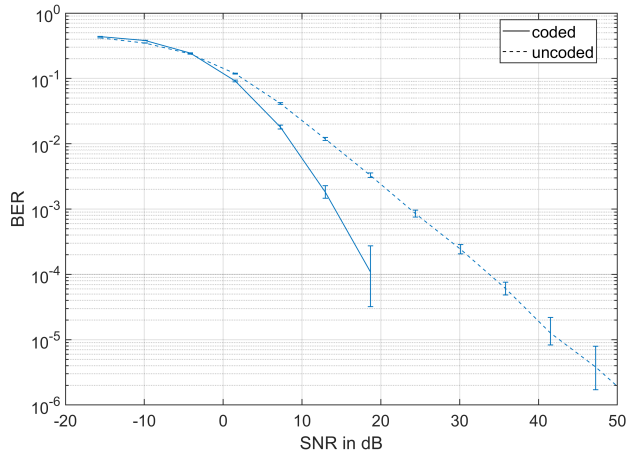

FIGURE 10. BER of the information decoder.

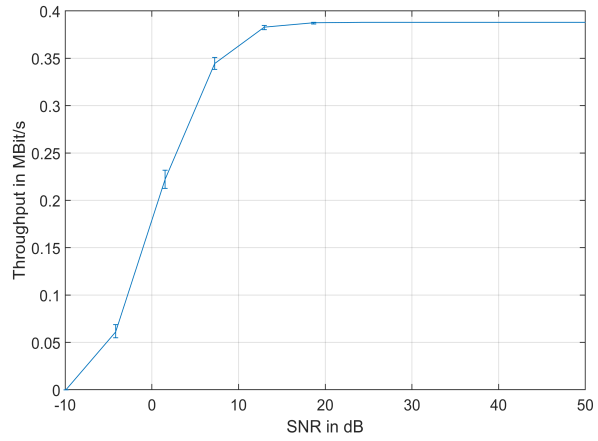

FIGURE 11. Throughput of the information decoder.

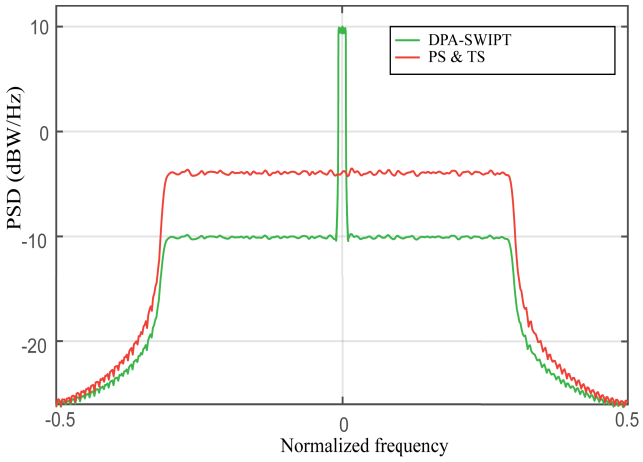

FIGURE 12. PSD of the IS and ES signal.

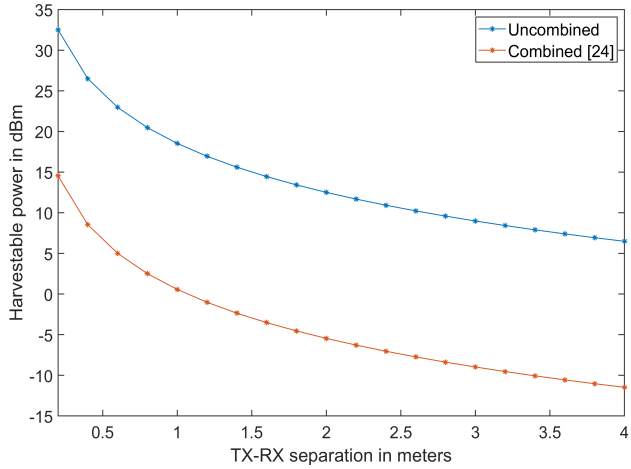

FIGURE 13. The harvestable power for combined and uncombined EH and ID circuitries at 0.5 ρ.

energy harvester and information decoder receiver schemes, with a 0.5 ρ power allocation for the EH circuit, showing that the uncombined scheme has higher available power as there is no ID load sharing the rectified power with the energy harvester reservoir. Although a power split ratio of 0.5 ρ is adopted in this paper, the uncombined scheme allows steering most of the input signal to the EH circuit depending on the channel gain and the intended application by adjusting the PS ratio ρ.

IV. CONCLUSION

RF energy harvesting presents a new approach toward powering low-power WSN networks, especially when a large number of SNs are required to be monitored. The contribution of this article is the introduction of an RF energy harvesting split-receiver design with an adjustable PS ratio. The presented receiver design combines the input signal from multiple RF sources, then splits it between the EH and ID circuitries. The split design increases the harvestable power at the energy harvester by shifting the ID load into a separate circuitry. Moreover, the receiver implements dynamic PS to regulate the power split ratio between EH and ID circuitries. Consequently, the output of the EH circuit can be monitored and increased by adjusting the PS ratio. Furthermore, DPA-SWIPT is implemented at the transmitter, where the ES is sent via unmodulated high-power CW, centered at the carrier frequency, and the IS is sent on a low power signal around the carrier frequency. In conventional TS and PS, the ES is carried on a modulated wave, resulting in higher interference to external networks. While, in DPA-SWIPT, the high-power ES is confined to a narrow spectrum at the carrier frequency, resulting in a lower interference to outer networks. Different system characteristics, including the EH circuit voltage multiplier output, and ID data rates, were presented. Accordingly, the split receiver design showed a significant improvement in harvestable power level compared to the combined receiver.

Finally, in their future work, the authors will extend the proposed system to higher frequencies; furthermore, they will also study the thermal design power (TDP) of the SN processor to increase the power efficiency of the SN.

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