

Received August 5, 2021, accepted September 7, 2021, date of publication September 15, 2021, date of current version September 27, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3113033

Cross-Talk Issues in Time Measurements

NICOLA LUSARDI¹, (Member, IEEE), NICOLA CORNA¹, (Member, IEEE),
FABIO GARZETTI¹, (Member, IEEE), SIMONE SALGARÒ,
AND ANGELO GERACI¹, (Senior Member, IEEE)

Politecnico di Milano, 20133 Milano, Italy

Corresponding author: Nicola Lusardi (nicola.lusardi@polimi.it)

ABSTRACT The enormous diffusion of Time-Mode circuits, in particular Time-to-Digital Converter (TDC) time measurement circuits, and at the same time the dizzying increase in parallel channels required by the most recent applications, for example in the automotive and digital imaging fields, brings the problem of electromagnetic interference between channels ever more to the fore. This phenomenon, generally known as Cross-Talk (XT), is particularly critical given the increase in the operating frequency and density of systems components, and its effect on the timing parameters in TDC measurements is investigated. Considering the time measurements, XT creates temporal shift on the physical events from which the timestamps are extracted; in this manner, an error in the measurements is generated. In order to detect the XT phenomena, a methodical analysis based on Code-Density Test (CDT) is performed; in this terms, two different typologies of XTs are investigated, which are correlated and uncorrelated XT. Furthermore, a TDC board is used as case study and all the XT sources are detected and classified. Thus, a classification of the importance of the different sources of XT is achieved and a solution to minimize the different causes is proposed.

INDEX TERMS Cross-Talk (XT), time measurement, Time-to-Digital Converter (TDC), Code-Density Test (CDT), linearity.

I. INTRODUCTION

For several decades, advances in technology have led to a pressing increase in the density of components in electronic systems, to the point of real congestion in time and space. In fact, nowadays, integrated and discrete electronic circuits are overloaded, from the point of view of both components per unit of area (space) and of operating frequency (time). One of the most negative consequences of this is the surge in the Cross-Talk (XT) phenomenon [1]. In Time-Mode (TM) circuits [2], and in experiments based on time measurements in general, where the information is represented as the time position of events, the coupling of electromagnetic energy by the XT induces time shifts of the events degrading the information they carry (Figure 1). As is known, the operating principle behind TM circuits is based on measuring the position of events over time in relation to an absolute reference or as measuring of the duration of time intervals [2]. This is accomplished by means of analog (Time-to-Amplitude Converter, TAC) or digital (Time-to-Digital Converter, TDC) circuits. Of the two methodologies, considering the consolidated trend towards multi-channel architectures, the digital

one is certainly applied the most today as it offers the best performance in terms of noise immunity in an electromagnetic dirty environment such as a complex compact system [3], [4]. Moreover, the implementation of TDCs within configurable devices based on Programmable Logic (PL), such as Field Programmable Gate Arrays (FPGAs) [5] and System-on-Chips (SoCs) [6], has achieved the state-of-the-art in terms of performance, greatly improving system versatility [7]. This has led to a very intense research in recent years into TDC architectures designed for FPGA devices [8]–[10] and this is the reason why we refer in this discussion to this type of TDC as a case study.

In a great number of modern Time-of-Flight (TOF) applications, the need to measure multiple timestamps is increasingly frequent and this leads to the development of TDC architectures with an ever greater number of channels [11], [12]. Using the TOF approach physical events are converted into time intervals and measured by TDCs. In time-resolved spectroscopy [13], [14], e.g. Time Correlated Single Photon Counting [15], the measurement of the decay time of particles is used to properly identify materials. Instead, in TOF imaging [16], such as LIDAR [17] and Time-of-Flight Positron Emission Tomography (TOF-PET) [18], distances and volumes are measured as the duration of the round trip of

The associate editor coordinating the review of this manuscript and approving it for publication was Pedro Miguel Cabral¹.

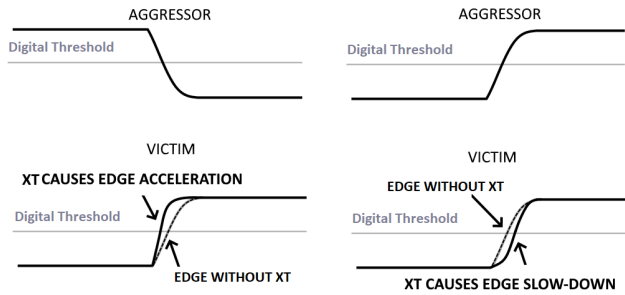


FIGURE 1. Energy coupling due to the XT translates into a temporal shift in time of digital signal edges. This phenomenon is remarkable and cannot be overlooked at all. Remember in this regard the designers' rule of thumb that an XT amplitude equal to $\pm X$ percent of the signal's swing induces a jitter equal to $\pm X$ percent of the signal's rise or fall time.

particles. To increase the performance in terms of resolution and acquisition time, more and more timestamps are digitized in parallel, in increasingly shorter conversion times, through even larger number of channels and higher speed TDCs [19], [20]. Since an increase in the size of the circuits proportional to the number of channels implemented and compatible with the electromagnetic interference produced by the signals is obviously not feasible, it goes without saying that the density of the TDC circuits and therefore the XT phenomena inside them increase more and more. This makes signal integrity a vital issue in TM designing in general and TDC circuits in particular [21], where depth measurement alterations in LIDAR systems [5] or halos and graphical artifacts in Time-of-Flight Positron Emission Tomography (TOF-PET) systems [22] or in TOF based imaging in general, consequent to the XT, can be devastating for application purposes.

The linearity of many electronic circuits can be evaluated by means of the Code-Density Test (CDT) [23]. This is the case for ADCs [24] and also TDCs. For the latter, which convert a time interval defined by the occurrence of a START and a STOP edge into a number, two random digital signals, START and STOP, with randomly distributed 0-1-0 transitions are used for measuring in the input channels. The digital codes generated at the output are the time distance between corresponding START and STOP edges. These values can be collected in a histogram which, if the distribution of the START and STOP edges is uniform, is flat. Over a statistically significant number of measurements, any deviation from the uniform distribution of the measured values indicates non-linearity of the system. As is known, for TDCs non-linearity is quantified in the two parameters called Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) [7], [25].

Non-linearity may depend on the circuit layout but may also be the effect of the presence of XT between the TDC's channels. In implementations where it is possible to exclude appreciable non-linearity due to the layout, it is clear how strong the effect of XT can be on the non-linearity (Figure 2).

XT is the electromagnetic interaction between parts of the circuit due to mutual spatial proximity. Therefore it is an intrinsic and unavoidable phenomenon in modern

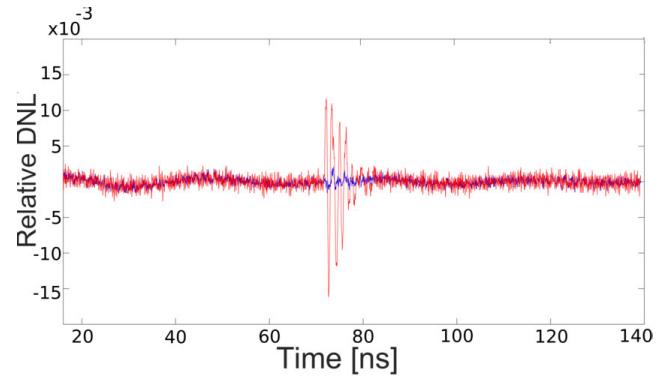


FIGURE 2. Histogram of uniformly distributed nominal value measurements in the presence (red) and absence (blue) of XT. The measurement was performed on a TDC in FPGA [7] with no appreciable non-linearity due to the layout. The LSB is equal to 5 ps.

miniaturized circuits, which can only be countered in order to guarantee the integrity of information. In order to characterize a circuit in terms of XT and to counteract the effects as much as needed, it is necessary first of all to start from the physical genesis of the phenomenon.

For this reason Section II presents an overview of the physical phenomenon and then the consequent implementation issues are investigated in Section III. This is to get to characterizing the effects that XT has on performance in time measurements in the rest of the discussion, and the consequent necessary design rules or circuits, in particular referring to TDCs.

II. OVERVIEW OF CROSS-TALK

In principle, XT in electronic systems is due to the coupling of a variable electromagnetic field between a circuit that emits energy (aggressor) and a circuit that receives the emitted energy (victim) [26]. Without taking away the generality of the discussion, the two circuits can be simply two lines [27]. It is known that the impedance of the transmission medium of an electromagnetic signal, which carries the information in an electronic circuit, determines the distribution of the signal's energy between the magnetic component and the electrical component. In low impedance circuits, such as modern digital circuits where the reference impedance varies from 50 to 100 Ohm, the signal's energy is mainly magnetic and so is the field associated with the propagation of the signal and which interacts with what is around it [28]. Conversely, in high impedance circuits, such as the first circuits of the valve era, the energy is mainly contained in the electrical component of the field. Depending on the two conditions, if the aggressor's interaction with the victim is magnetic, it is called inductive, or if it is electrical, it is called capacitive. Correspondingly, the coupling phenomenon is called inductive XT or capacitive XT. Therefore, in digital XT problems, when a low-impedance circuit is exposed to the air through a package pin, connector, or component body, first look for inductive XT. Higher impedance circuits involving larger dv/dt and smaller di/dt experience more capacitive XT.

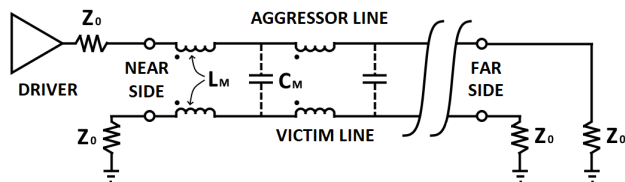


FIGURE 3. Model of two transmission line in spatial proximity for the analysis of XT effects. The subscript M of the reactive components of the model stands for “Mutual”.

Whether due to the electric or the magnetic field, the XT causes an energy transfer that generates perturbations in the victim circuit.

Consider two 50-Ohm transmission lines, i.e. characteristic impedance equal to Z_0 , correctly terminated and laid out in parallel. As for the XT phenomenon, the lines are modelled as a cascade of LC cells in which the L_M components recreate the coupling mechanism of the magnetic field while the C_M components that of the electric field (Figure 3). One line (the aggressor) is driven by a digital signal, the other one (the victim) is at rest.

Now consider a single edge of the digital signal propagating on the driven (aggressor) line. Figure 4 freezes the edge in space and time and shows the corresponding XT signals induced in the victim line. Both magnetic and electric field coupling induce two pulses propagating in opposite directions. In particular, the electric field, whose coupling is modelled by C_M , generates two positive pulses since the aggressor edge is supposed to be rising (according to the capacitor’s constitutive equation). The magnetic field, whose coupling is modelled by L_M , produces a negative pulse in the victim that propagates in the same direction as the aggressor edge, referred as the far-end side, and a positive pulse propagating in the opposite direction, referred as the near-end side (according to the inductor’s constitutive equation) [26]–[28].

In the case of modern digital circuits at high currents and low voltages, i.e. at low impedance, magnetic coupling is dominant by roughly one order of magnitude [29]. Therefore, for these circuits we generally talk of far-end XT or near-end XT depending on which end of the victim line we look at the XT effects from.

With reference to Figure 4, a negative impulse propagates towards the far-end side and consists of the sum of the negative pulses induced by the aggressor edge which, step by step, propagates in the same direction. Therefore the far-end XT is a large negative pulse of width equal to the rise time of the aggressor edge. On the other hand, towards the near-end side positive pulses are propagated induced by the aggressor edge but propagate in the opposite direction to the former. Therefore these pulses are queued as if they were the wagons of a train, propagating towards the near-end side. The last of these pulses is generated when the aggressor edge reaches the far-end, taking a time equal to the propagation time to reach the near-end terminal and where it completes the XT signal. Therefore, the near-end XT is a positive pulse of width equal

to double the propagation time of the edge on the aggressor line. The amplitudes of both far- and near-end XT signals depend on the technological and geometric parameters of the layout which are summarized in the values of C_M and L_M .

It would seem correct to conclude that in TDC applications the XT signals induced in a victim line could generate false events and therefore wrong measurements of time intervals. In reality this does not happen. The XT signals are generally too small in amplitude to generate false events. Instead what can occur, as will be seen in going on, is a distortion of the edges of real signals eventually present on the victim line, which leads to errors in the timestamping of the events.

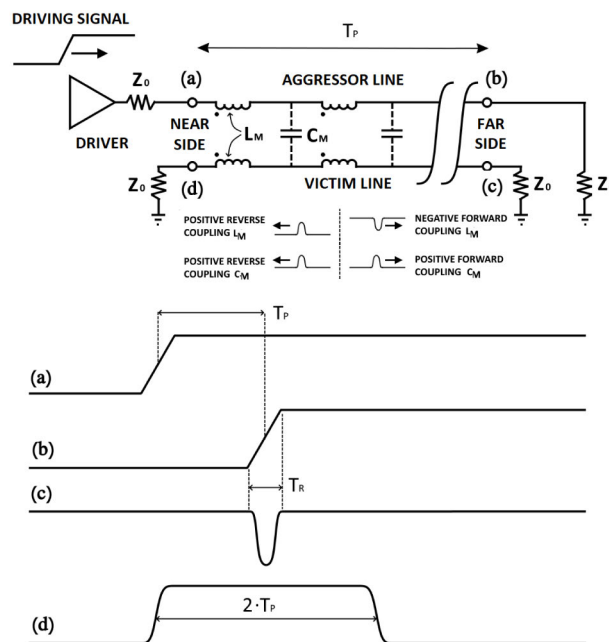


FIGURE 4. Pulses induced by XT in the victim line due to the effect of the rising edge propagating on the aggressor line. Neglecting the contributions of the electric field coupling, the picture shows (a) the aggressor edge at the driver with rise time equal to T_R (near-end side); (b) the edge at the end of the aggressor line after the propagation time T_P (far-end side); (c) the XT pulse of width T_R at the far-end side, and (d) the XT pulse lasting $2 \cdot T_P$, i.e. the complete round-trip of the signal generated by the digital driver at near-end side.

Theoretically it has been possible to frame the XT by referring to the simple layout of two parallel lines. Now let’s briefly focus on the topology of the real circuit contexts in which the phenomenon develops.

Starting from the theoretical model of the two parallel lines, two real transmission lines (a.k.a. microstrips and striplines) are the corresponding circuit case. A transmission line consists of a trace, or two in the case of differential signalling, laid out on a reference plane that constitutes the return path of the current along the line. It is known that this return current on the plane, in modern high speed digital systems due to the minimisation of inductance, is concentrated below the outgoing line. Therefore, the magnetic field generated by the propagation of a digital signal along that line (aggressor) generates lines of force that concatenate the

nearby transmission line (victim). Given that the magnetic field is much smaller, and therefore the XT, the closer the aggressor is to the reference plane, the greater the effect of the XT, while the less the XT the greater the distance between the aggressor and the victim [27].

The first design rule to minimize XT in transmission line is therefore to keep the lines at the maximum possible distance from each other and minimum possible distance from the reference plane.

Regarding the reference plane, if this is interrupted by slots that force the return current to divert from the path with minimum inductance, it is obvious that the magnetic field increases and consequently also the effects of the XT being equal the other topological parameters.

From this the second fundamental design rule follows, that is to preserve the integrity of the reference plane or, if this is not typically feasible due to space requirements, to provide an adequate number of stitching capacitors that offer a return path as close as possible to the one with minimum inductance despite the presence of the slots [30].

It is surely that, among others things, differential signalling involves a great advantage in terms of reduction of XT. Indeed, even if the distance between the aggressors and victims is slightly different and consequently each victim line experiences slightly different XT effects that cannot be rejected by the differential receiver, the global XT is reduced by orders of magnitude compared to the single-ended case [27]. Even in the case of a cut reference plane, compared to a single-ended line, the adjacent line driven with opposite polarity provides a relatively low-impedance path for the return current [27]. In other words, between the pair of conductors of the differential lines, a so-called virtual-plane is created, which helps a lot to preserve signal integrity [27].

Therefore, the third fundamental design rule for definitely minimising XT in transmission lines is to use differential lines.

As is known, connectors are extremely critical elements for signal integrity, also from the point of view of XT. Always more often, due to dimensional constraints, designers are forced to use high density connectors of small size. Given the extreme proximity of the pins, the causes and effects of XT described with reference to the transmission lines multiply, not least those connected with the obvious interruption of the reference plane. From the point of view of the XT, it is therefore good practice to limit the use of connectors, especially at high density and if necessary to resort to multiple connectors with a shielded lines layout.

III. CROSS-TALK IMPACT IN TIME MEASUREMENTS

The causes of XT have been examined so far. From here on, It will be investigated the impact of XT effects on time measurement particularly in TDC systems.

The mechanism by which the effects of XT can induce errors in the measurement of time can be summarized in the distortion of the edges of the digital signals associated with

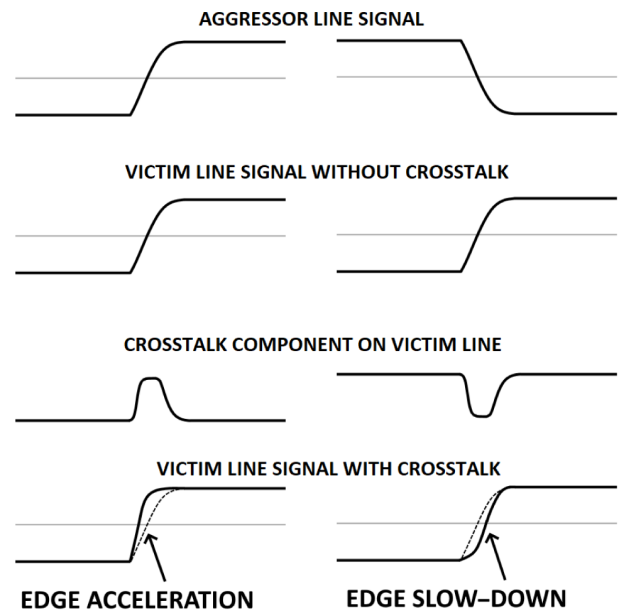


FIGURE 5. Effect of XT on victim line signal. Edges distortion due to crosstalk.

the time events. As already pointed out above, the XT signals are generally too small in amplitude to generate false events.

Figure 5 schematically shows the effect of an aggressor signal on a victim signal due to XT coupling. Assuming detection of the signal through a threshold crossing, an operation at the base of every digital system, due to the distortion of the victim signal edge, there is a time shift of the threshold crossing point.

Usually from an electronic point of view, as you can see in Figure 6, the duration T_{MEAS} of the time interval under measure is obtained as the difference between the timestamps of the rising edges of START and STOP events. These events correspond to physical input events, coming for instance from detectors such as Cross Delay-Line (CDL) [14], Silicon Photomultiplier (SiPM) [31], Single Photon Avalanche Detector (SPAD) [17], Superconducting Nanowire Single-Photon Detector (SNSPD) [32], Photon Multiplier Tube (PMT) [33], which are converted into digital pulses by means of constant fraction discriminators or programmable threshold comparators. If an electromagnetic coupling occurs, i.e. XT, the shape of the reference edges can be altered, causing a time shift that is converted by the TDC in a measurement error. In these terms, we face two different cases. Firstly, a third signal, not belonging to the measurement process (i.e. uncorrelated to the START and the STOP events), acts as aggressor. Secondly, the other edges of the START and STOP pulses, that do not define the time interval T_{MEAS} (e.g. the falling edges in Figure 6), operate as aggressors on the other ones (e.g. the rising edges in Figure 6). In the last case, the XT is due to the interaction between START and/or STOP signals only, thus resulting correlated to T_{MEAS} .

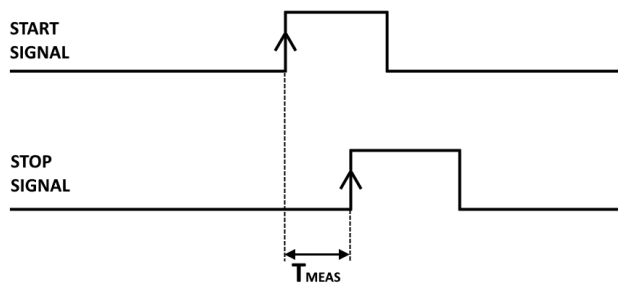


FIGURE 6. The duration T_{MEAS} of the time interval being measured is obtained as the difference between the timestamps of the rising edges of START and STOP events. These events correspond to physical input events, coming for instance from detectors, which are converted into digital pulses by means of constant fraction discriminators or programmable threshold comparators.

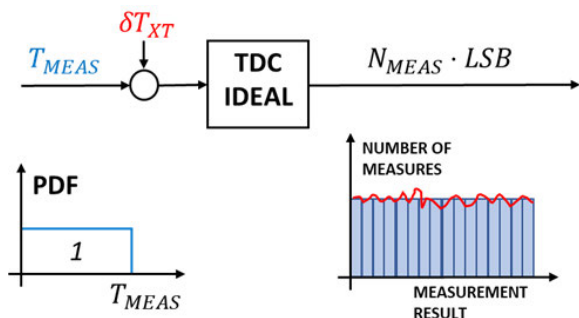


FIGURE 7. Relationship between XT and linearity in the time measurement process.

A. HOW TO DETECT CROSS-TALK EVENTS

The TDC is a digital electronic device that converts the time interval T_{MEAS} provided as input in a digital code (N_{MEAS}) related to T_{MEAS} by means of the so called Last Significant Bit (LSB) value, i.e. $T_{MEAS} = N_{MEAS} \cdot LSB$. In addition, a perfectly linear TDC is characterized by both DNL and INL equal to zero. In these ideal conditions, if we provide multiple inputs (T_{MEAS}) characterized by a specific Probability Density Function (PDF), the histogram of the measured time intervals at output ($N_{MEAS} \cdot LSB$) maintains the same shape. In the case of CDT, the PDF of T_{MEAS} is a uniform distribution over the Full-Scale Range (FSR) of the TDC, and, consequently, the histogram of $N_{MEAS} \cdot LSB$ will be completely flat. As can be seen in Figure 7, the XTs couplings move the edges of the START/STOP signals, distorting T_{MEAS} before the TDC with a value δT_{XT} that is characterized with a PDF different from that of T_{MEAS} . In this way, a modification in the histogram of the measured time intervals at output ($N_{MEAS} \cdot LSB$) occurs, which also reflects in change of values of DNL and INL respectively.

The sources of δT_{XT} are characterized by different PDFs, depending on the physical mechanisms of XT generation. As focused in this Section, two main types of mechanisms are at stake, correlated and uncorrelated XT.

B. CORRELATED CROSS-TALK

Correlated XT is present when the aggressor signal is locked in phase (correlated) to the START or STOP signals that

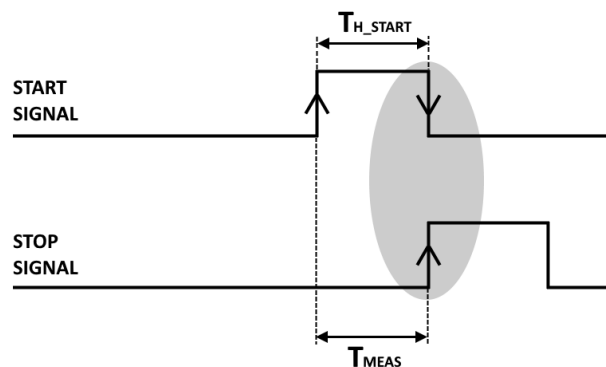


FIGURE 8. Correlated XT effect between START and STOP signal pulses. The falling edge of the START (aggressor) induces a disturb over the rising edge of the STOP (victim) modifying T_{MEAS} .

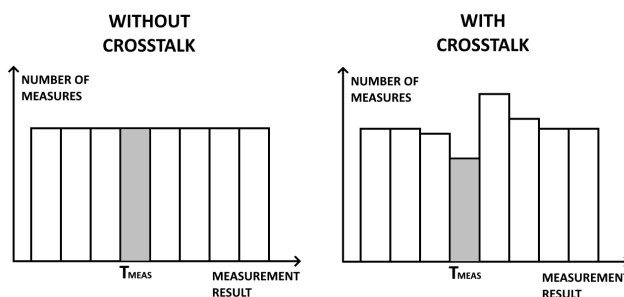


FIGURE 9. Histograms of repeated measurements of time intervals of different width with and without correlated XT. The dark bin corresponds to the time interval of width equal to the START event's duration. The presence of correlated XT, due for instance to bad layout of input channels, causes a significant local redistribution of measurements. This increases DNL and INL.

define the time interval under measure. With reference to Figure 8, it may happen that the interval to be measured lasts exactly as long as the digital START event. In this way, the falling edge of the START event and the rising edge of the STOP event are concomitant. If the layout of the two channels of the instrument implies XT, the STOP signal is distorted by the end of the high-level of the START signal (T_{H_START} in Figure 8) and the measurement (T_{MEAS} in Figure 8) is incorrect. Imagining repeating the measurement of intervals of different time duration, a statistically significant number of times for each one, the resulting histogram is shown in Figure 9. There is a very accentuated local perturbation corresponding to the measurement interval of the critical duration (e.g. $T_{MEAS} = T_{H_STAT}$), with consequent degradation of linearity.

In this case the XT can have a fatal impact on the linearity of the measurement system. It can obviously be compensated for by an accurate layout or by adapting the system's operating modes, by excluding for instance the measurement of intervals with durations that fall within the critical condition.

C. UNCORRELATED CROSS-TALK

Uncorrelated XT occurs when the disturbance comes from an aggressor signal that has no time relation with the START and STOP events, for instance a clock signal or a nearby

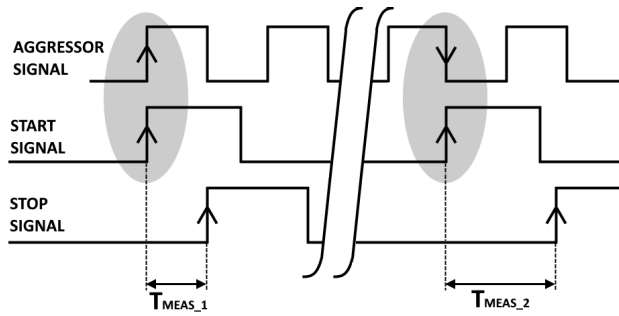


FIGURE 10. Uncorrelated XT effect on START and STOP signal pulses. The third signal is the aggressor of the START: both rising and falling edges of the aggressor inject disturbs on the rising edge of the START that defines the time under measure.

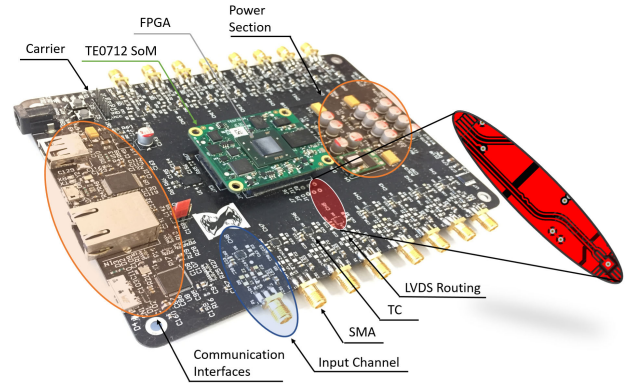


FIGURE 12. Instrument presented in [7], where different sections are put in evidence.

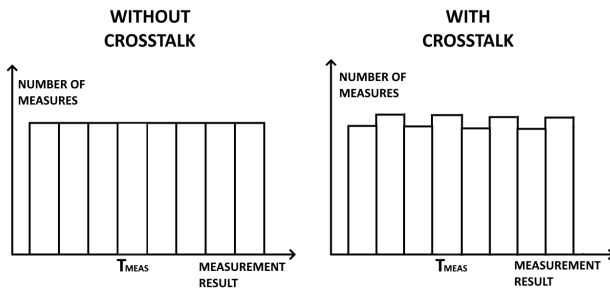


FIGURE 11. Histograms of repeated measurements of time intervals of different widths, with and without uncorrelated XT. Compared with the corrupted one in Figure 9, the histogram in the presence of uncorrelated XT appears uniformly but less intensely perturbed. In this case XT reduces the precision of measures.

switching signal in a power stage (Figure 10). In this case, whether the victim is the START or STOP front or both, the distortion induced by the XT compromises the result of the measurement whatever the duration of the interval, with a statistically uniform probability of error, as there is no temporal correlation between the aggressor and victim. Similarly to what was done for the correlated XT case, this results in a histogram of measurements that presents a perturbation uniformly distributed among all the measurements. In this case the XT has an impact on the precision of the measurement system, that is much less important than the effect of the correlated XT on linearity but, unlike the former, very often in practice it cannot be removed.

IV. CASE STUDY

In order to contextualize the XT issue in the experimental reality, let’s examine the effects of XT in an instrument for time measurements based on TDC.

A. REFERENCE INSTRUMENT

The instrument (Figure 12) is a multi-channel Tapped Delay-Line based TDC (TDL-TDC) implemented in FPGA [7]. The FPGA device is a Xilinx 28-nm 7-Series Artix-7 200T that it soldered on a TE0712 System-on-Module (SoM) provided by Trenz Electronics [34], connected to a carrier board by means of high density board-to-board connectors.

TABLE 1. TDC reference instrument main features.

Feature	Value
Number of channels	16
TDC frequency	416.7 MHz
Channel resolution	5 ps
Channel precision	12 ps r.m.s.
Temperature drift	286 fs/°C

This configuration provides the instrument in addition the natural firmware and hardware re-configurability, allowing the FPGA device to be modified in a simple way by the user by replacing the TE0712 with other SoMs of the same TE07xx category [34]. The instrument can operate in multi-channel mode up to 16 parallel channels at high-performance. As you can see in Figure 12, each input can accept an analog signal in a range from 0 V to 3.3 V; a programmable Threshold Comparator (TC) converts it in a LVDS digital pulse. By means of 100 Ω differential traces, it goes to the connector and then to the FPGA, where the TDC is holed. Obviously, the power section and the communication interfaces are hosted on the carrier board.

Table 1 summarizes the main features of the instrument used in this paper. In particular, we would underline that the resolution is set to 5 ps instead of the 2 ps reported in [7] .

As represented in Figure 13, the timestamps collected by the TDC are conveyed to the PC using an USB 3.0 interface and processed by a proper software. In this way, it is possible to obtain raw timestamps and to generate histograms in real-time of the time interval between two user-selected channels.

B. HOW TO MEASURE CROSS-TALK

The characterization of the instrument in terms of XT was obtained directly by quantifying the corresponding measurement errors. The basis of this method is the Code-Density Test (CDT) [23]. Two random digital signals, START and STOP, with uniform distribution time distance are put out for measurement at input channels. The digital codes generated at the output are the time distance as between corresponding START and STOP edges. These values can be collected in a

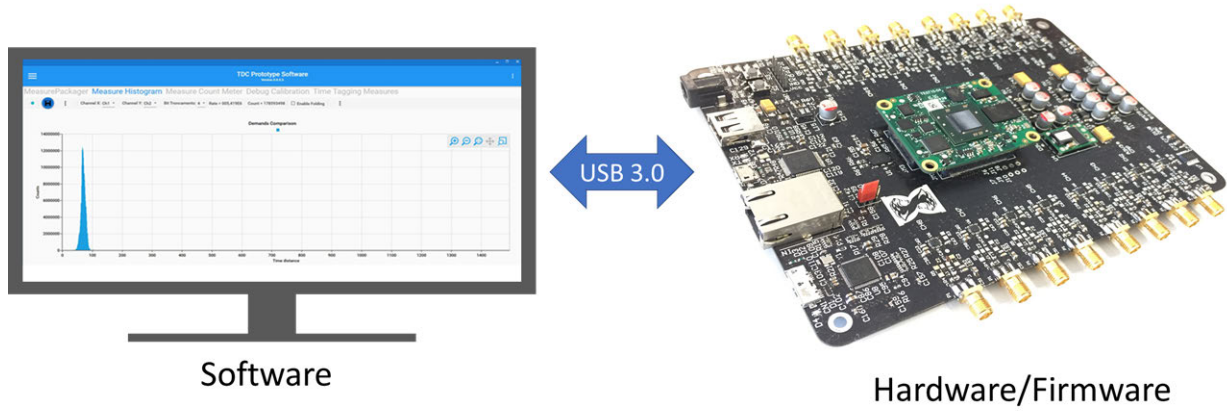


FIGURE 13. Connection between START/STOP input signals, the TDC hardware instrument and PC.

histogram which, if the distribution of the START and STOP edges is uniform, is flat. We suppose that each bin of the histogram is LSB-wide and that a statistically significant number of measures covers the range of interest, possibly up to the instrument’s Full-Scale Range (FSR).

1) LINEARITY ESTIMATION FROM CODE-DENSITY TEST

Let’s briefly summarize the information on the linearity of the system given by the CDT.

Consider a histogram of N LSB-wide bins and T_{MAX} the maximum measurable time interval width

$$N = \frac{T_{MAX}}{LSB} \tag{1}$$

The bins are $h_{CD}[n]$ high with $n \in [0; N - 1]$. Considering to perform overall N_{SAMPLE} measures,

$$N_{SAMPLE} = \sum_{n=0}^{n=N-1} h_{CD}[n] \tag{2}$$

The average height N_{CD} of the bins, that is the average number of sample of sufficient statistical significance that fall in each bin, is

$$N_{CD} = \frac{1}{N} \cdot \sum_{n=0}^{n=N-1} h_{CD}[n] = \frac{N_{SAMPLE}}{N} \tag{3}$$

If $h_{CD}[n]$ refers to a uniform distribution of measurements, it is immediate to deduce the expression of the relative differential non-linearity (DNL) error associated with each bin ($dnl_{Rel}[n]$).

$$dnl_{Rel}[n] = \frac{h_{CD}[n] - N_{CD}}{N_{CD}} \tag{4}$$

Consequentially, we can simply deduce the absolute DNL value associated with each bin ($dnl_{Abs}[n]$) by multiplying Equation (4) by the LSB in Equation (1),

$$dnl_{Abs}[n] = dnl_{Rel}[n] \cdot LSB \tag{5}$$

i.e.,

$$dnl_{Abs}[n] = \frac{h_{CD}[n] - N_{CD}}{N_{SAMPLE}} \cdot T_{MAX} \tag{6}$$

Of course, for uniform distribution of measure corresponding to a flat histogram, the DNL error is equal to zero.

The relative and absolute bin-by-bin integral non-linearity (INL) error curves ($inl_{Rel}[n], inl_{Abs}[n]$) can also be derived as integral of the DNL ones,

$$inl_{Rel}[n] = \sum_{i=0}^{i=n} dnl_{Rel}[i] \tag{7}$$

$$inl_{Abs}[n] = \sum_{i=0}^{i=n} dnl_{Abs}[i] \tag{8}$$

Obviously,

$$inl_{Abs}[n] = inl_{Rel}[n] \cdot LSB \tag{9}$$

2) HOW TO GENERATE A UNIFORM DISTRIBUTION OF INTERVALS

In order to generate a uniform distribution of intervals that ideally gives uniformly distributed measurements $h_{CD}[n]$ performing a CDT, there are several techniques based on a physical source of random events. In particular, a Single Photon Avalanche Detector (SPAD) diode placed in dark space generates the random START pulses and a square wave signal generator produces the periodic STOP pulses. The SPAD diode in dark space generates events at variable time intervals according to the Poisson distribution. Therefore, START pulses occur at an average rate equal to R_{DARK} .

We have set the conditions of generating random time interval widths to cover a range of interest T_{MAX} equal to 100 ns , using the reference TDC with LSB set to 5 ps and producing average value of $N_{CD} = 10^5$ measurements for each bin.

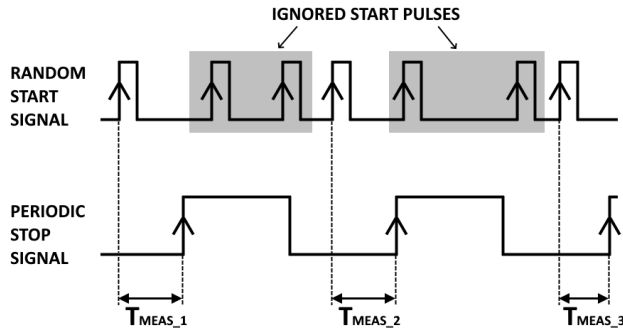


FIGURE 14. START and STOP digital signals in case of violation of Equation (12). The selection of short intervals being measured (T_{MEAS-i}) is evident.

The T_{MAX} of interested gives the frequency of the STOP signal,

$$f_{STOP} = \frac{1}{T_{STOP}} = \frac{1}{T_{MAX}} \quad (10)$$

that for the set operating conditions is equal to 10 MHz.

On average, the total number of measurements will be equal to

$$N_{SAMPLE} \approx N_{CD} \cdot \frac{T_{MAX}}{LSB} \quad (11)$$

that is $N_{SAMPLE} \approx 10^9$.

In order to approximate the Poissonian distribution of uniform SPAD, we must guarantee one STOP for each START generated by the SPAD, that is

$$R_{DARK} \ll f_{STOP} \quad (12)$$

In this way, between two consecutive STOP events there is at most one START event. If this were not the case, the generation of short measurements would be greatly favoured, since the interval is defined by a START event followed by a STOP one (Figure 14) illustrates the situation in which R_{DARK} is excessively high.

The sustainable engineering choice was to fix

$$R_{DARK} = \frac{1}{100} \cdot f_{STOP} \quad (13)$$

that is a SPAD with $R_{DARK} = 100$ kHz.

The time required for generating the overall set of samples is

$$t_{TEST} = N_{SAMPLE} \cdot \frac{1}{R_{DARK}} \quad (14)$$

that is $t_{TEST} = 2.7$ h in the considered conditions. Moreover, this time has to be further multiplied for all the combinations of channels for which the DNL/INL must be characterized. From here it is evident that the hard drawback of this method is the time required for the test, mostly dedicated to the generation of the samples to be measured.

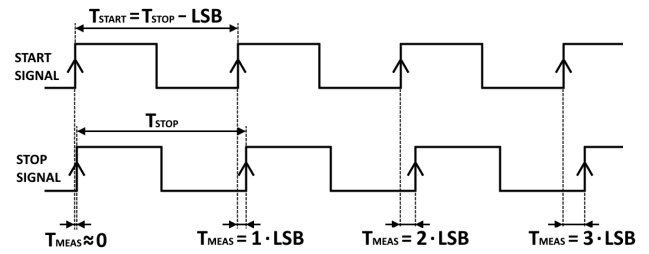


FIGURE 15. Generated time intervals setting $q=1$.

TABLE 2. Specifications of the START and STOP signals for correlated XT evaluation. In particular, $q = 7$ and $LSB = 5$ ps.

Signal	Frequency (MHz)	Period (ns)	Duty-Cycle (%)
START	7.143	$140 - LSB$	50
STOP	1.02	980	50

3) HOW TO SPEED UP THE UNIFORM DISTRIBUTION GENERATION

A simple generation technique consists of using two generators of periodic signals at different frequencies, one for the START and one for the STOP signal, for instance

$$T_{STOP} = T_{MAX} \quad (15)$$

$$T_{START} \leq T_{MAX}/q - LSB \quad (16)$$

where $q \in \mathbb{Q} \setminus \{0\}$.

Let's consider $q = 1$, so $T_{START} = T_{MAX} - LSB$. In this way, increasingly greater time intervals, spaced by one LSB from each other, would be generated as shown in Figure 15.

Maintaining the conditions in the previous paragraph, $f_{START} \approx 10.0005$ MHz and $f_{STOP} = 10$ MHz.

The rate of generation and consequently of measurement is f_{STOP} , taking the time for performing the test equal to

$$t_{TEST} = N_{SAMPLE} \cdot T_{STOP} \quad (17)$$

that is $t_{TEST} = 100$ s, two orders of magnitude shorter than the use of the physical source.

To be precise, this shortcut does not generate a set of intervals of random width, but a pseudo-random sequence [35] throughout the range of interest T_{MAX} . Moreover, the unavoidable jitter error and the accuracy of the signal generators cause the distribution to deviate from the ideal uniform shape, but without a practical impact on the significance of the test. Therefore this method was chosen for the generation process in the linearity test.

4) CORRELATED CROSS-TALK EVALUATION

Two square wave signals (Figure 16), START and STOP, characterized by low/high voltage levels of 0.1 V and 2.7 V with rise/fall time of 8 ns at frequencies compatible with the onset of the correlated XT (Table 2), have been put as inputs of two channels of the reference instrument.

The range of interest, i.e. the dynamic-range of the time difference among START and STOP (T_{MEAS}), is the smaller

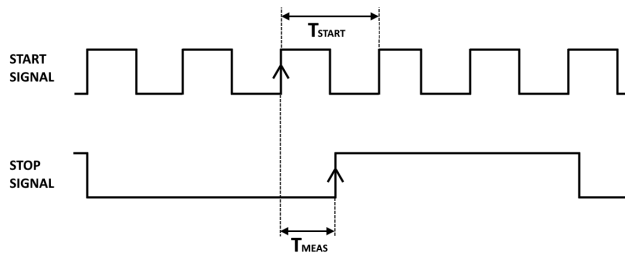
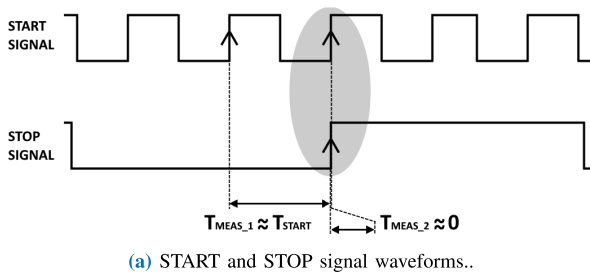
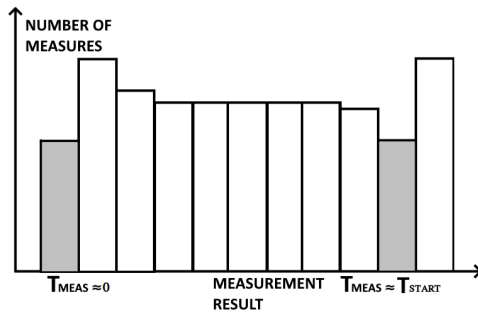


FIGURE 16. Waveforms of the START and STOP signals for correlated XT evaluation.



(a) START and STOP signal waveforms..



(b) Histogram, XT located in $T_{MEAS} = 0$ and $T_{MEAS} = T_{START}$.

FIGURE 17. XT interaction between rising edges of both START and STOP signals.

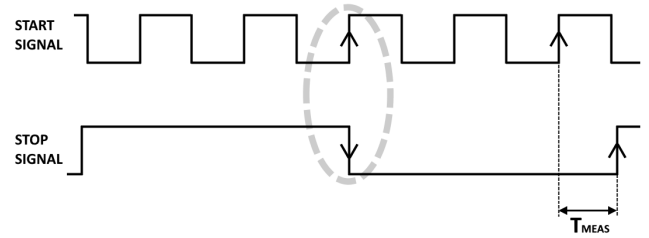
period between those of the two signals, in this case T_{START} . In particular, the test has been carried out arbitrarily setting $f_{START} > f_{STOP}$ and duty-cycle of 50% for both waveforms.

Four types of XT interactions of interest can occur.

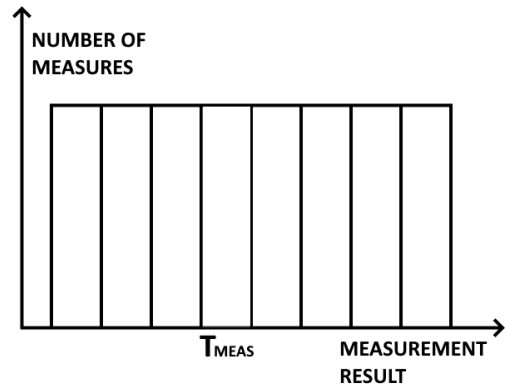
First, Figure 17 shows simultaneous rising edges of START and STOP. In this case, there are two possible measurement results, $T_{MEAS-1} \approx T_{START}$ or $T_{MEAS-2} \approx 0$, depending on whether the STOP edge is detected by the system before or after the START one respectively. In both cases, the possible measurements are at the edges of the region of interest (i.e. $T_{MEAS} = 0$ and $T_{MEAS} = T_{START}$).

Secondly, with reference to Figure 18, it may happen that a rising edge of START is simultaneous with a falling edge of STOP. In this case no measurement error occurs as the edge of the START signal affected by the XT is not involved in the measurement.

Thirdly, in Figure 19 a rising edge of STOP is simultaneous with a falling edge of START. In this case, a measurement error occurs due to the distortion of the STOP signal edge.

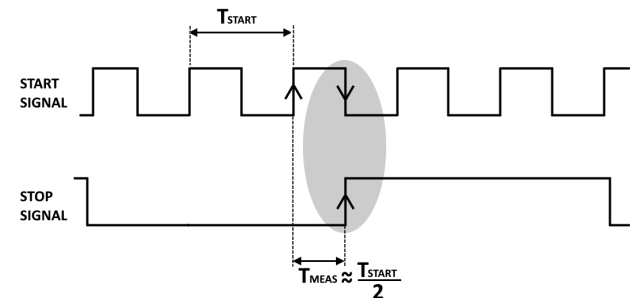


(a) START and STOP signal waveforms.

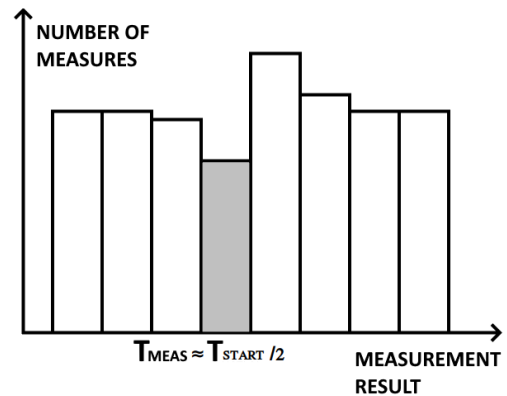


(b) Histogram, no XT is observed.

FIGURE 18. XT interaction between the rising edge of the START and falling edge of the STOP signal.



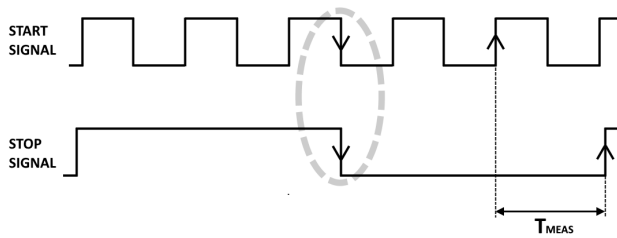
(a) START and STOP signal waveforms.



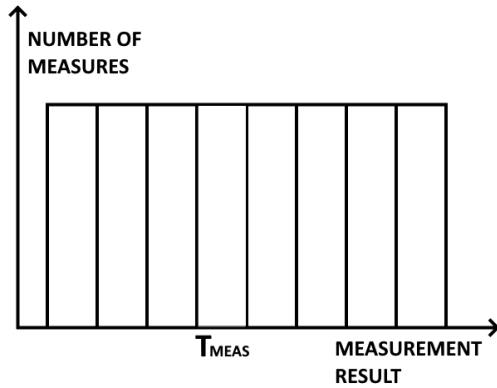
(b) Histogram, XT located in $T_{MEAS} = T_{START}/2$.

FIGURE 19. XT interaction between the falling edge of the START and rising edge of the STOP signal.

The resulting measurement is $T_{MEAS} \approx \frac{T_{START}}{2}$, i.e. halfway through the measurement region of interest.



(a) START and STOP signal waveforms.



(b) Histogram, no XT is observed.

FIGURE 20. XT interaction between the falling edge of the START and falling edge of the STOP signal.

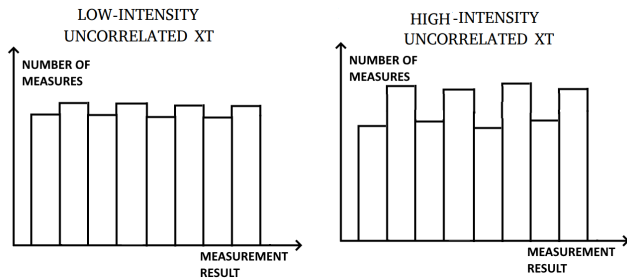


FIGURE 21. CDT comparison between low-intensity (left) and high-intensity (right) uncorrelated XT.

Fourthly, the case of simultaneous falling edges of START and STOP (Figure 20). In this case no error occurs as the falling edges are not involved in the measurement process.

5) UNCORRELATED CROSS-TALK EVALUATION

As already pointed out at the end of Section III, uncorrelated XT limits the instrument’s precision. Its evaluation is more difficult to perform because the error is distributed homogeneously over the overall region of interest. Obviously, a higher level of uncorrelated XT is detectable as a reduction of the flatness of the CDT (Figure 21)

However, the measurement of uncorrelated XT also gives an indication of the magnitude of the uncorrelated one, both being energetic couplings of common origin.

V. EXPERIMENTAL RESULTS

Purpose of this Section is to show which type of XT, correlated and uncorrelated, and which sources of XT, layout issues, are more dangerous in time measurements. To do this,

in Paragraph V-A, we have considered a XT free experiment taken as reference; in Paragraph V-B most significant sources of XT (layout issues) are classified in base of the magnitude of the generated disturb; in Paragraph V-C, we demonstrate that, at same intensity, the correlated XT is more dangerous than the uncorrelated one.

All the measurements have been performed for several combinations of different channels and firmwares using the CDT approach. Considering that DNL, INL and histogram are mathematically related (see Subparagraph IV-B1), we have chosen as figure of comparison the relative DNL curve (Equation (4)) using its peak-to-peak value as index of the magnitude of the XT.

The setup is shown in Figure 22 and we assume that the T_{MEAS} is delimited by the rising edges of the START and STOP signals (Paragraph III-A) that are provided at input of two of the sixteen channels of the TDC presented in Paragraph IV-A. In order to obtain the uniform distribution over T_{MEAS} in a short time, as exposed in Subparagraph IV-B3, START and STOP are 2 V wide TTL square waves generated by two independent function generators as reported in Table 2. All the timestamps and the histograms used to compute the DNL curves are referred to $LSB = 5 ps$.

As shown in Subparagraph IV-B4, the correlated XT is investigated considering only the START ($T_{START} \simeq 140 ns$) and STOP ($T_{STOP} \simeq 980.4 ns$) signals and observing the increasing on the peak-to-peak DNL curve amplitude in correspondence of $T_{MEAS} = 0$ (Figure 17), $T_{MEAS} = T_{START}$ (Figure 17), and $T_{MEAS} = T_{START}/2$ (Figure 19). Unfortunately, due to limitations of the acquisition system, only the value of T_{MEAS} in a range of 15% ÷ 85% of T_{START} (i.e. 20 ÷ 120 ns) can be properly taken into account, making the correlated XT p detectable only in proximity of $T_{START}/2 \simeq 70 ns$, as Figure 19 shows.

Instead, the uncorrelated XT is obtained turning on a third function generator connected to a third channel of the TDC (3rd SIGNAL) between the START and STOP and detected. The disturbance manifests itself as a global increasing of the peak-to-peak DNL curve amplitude over the entire FSR.

A. NO CROSS-TALK CASE

First of all, to have a reference for evaluating the effects of XT, several measurements were carried out using channels of the reference instrument among which there is no risk of correlated and uncorrelated XT at all. From a theoretical point of view, it is impossible to identify a couple of channels, among the sixteen available, completely free by XT coupling and linearity errors (Paragraph III-A). As a consequence, we have selected the couple of channels that returned the flattest histogram with a CDT test.

As you can find in Section II, the magnitude of the XT is proportional to the distance of the components and traces, in the sense that the greater is the distance the lower is the XT intensity. This means that START and STOP signals were put into channels chosen to maximize the distance of the

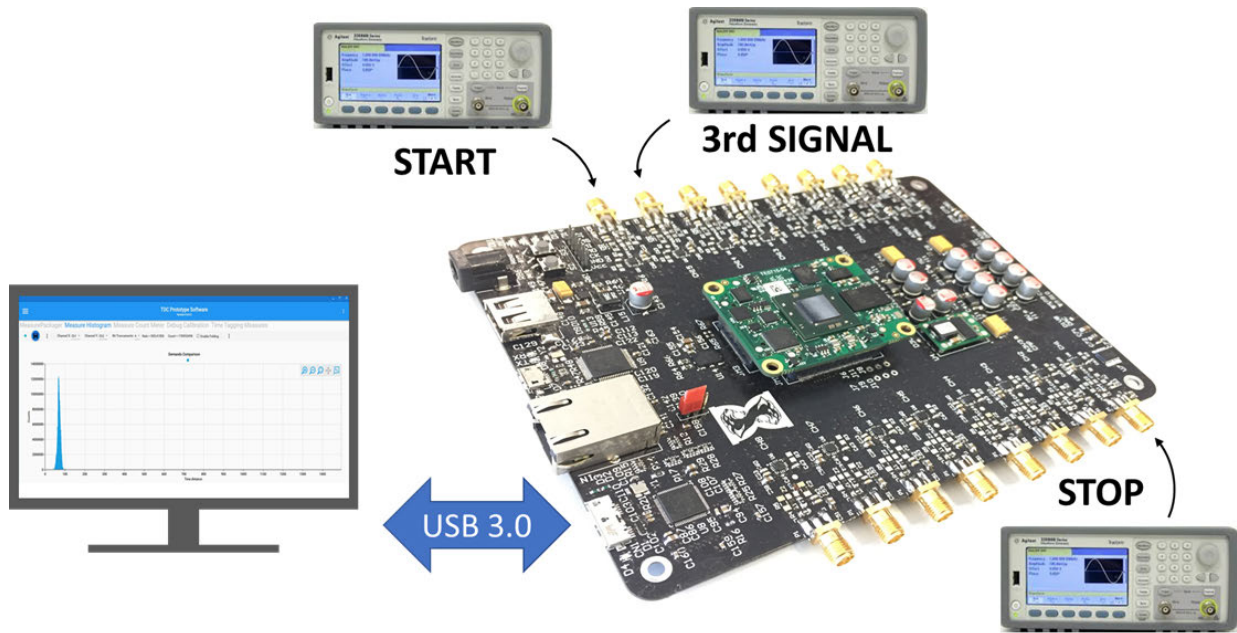


FIGURE 22. Schematic diagram of the measurement setup.

routing on the PCB carrier (Figure 23b), the board-to-board connector (Figure 23c), and the position of the FPGA input pads (Figure 23d) at the same time. Furthermore, the internal routing in the FPGA was automatically optimized by the FPGA compiler, i.e. Vivado, for making the TDC as scattered possible (channels distant enough) to rule out the possibility of XT. Figure 23a shows the measured DNL curve with a peak-to-peak value lower than $3.7 \cdot 10^{-3}$. Since this is the lowest detectable value, we have assumed this condition as reference XT free.

To be precise, in proximity of $T_{START}/2 \simeq 70\text{ ns}$ we observe an aberration, not present elsewhere in the plot, due to correlated XT. No uncorrelated XT events are detectable, and the observed oscillations depend on the characteristics of the used real TDC.

B. IDENTIFICATION OF INTENSITY OF CROSS-TALK CASE

Aim of this Paragraph is the discrimination of contributions to XT coming from the FPGA internal routing (Subparagraph V-B1), the FPGA input pads' proximity (Subparagraph V-B2), and the PCB layout (Subparagraph V-B3).

1) FPGA INTERNAL LAYOUT

Using the same experimental setup of Paragraph V-A, we forced the compiler, by means of proper spatial constraints, to crowd the FPGA internal routing minimizing the distance between the TDC circuitual components (Figure 24b), thus favoring the electromagnetic coupling between the parts to the maximum. Figure 24a shows the relative DNL error curve showing the presence of a modest correlated

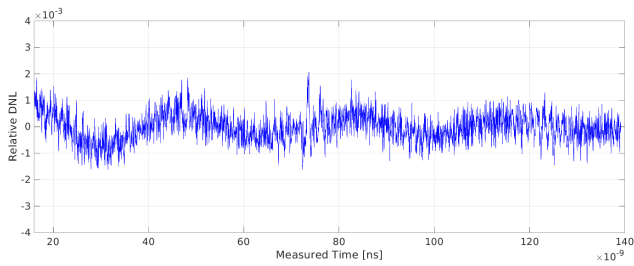
XT detected at $T_{START}/2 \simeq 70\text{ ns}$ with a peak-to-peak amplitude of $5.1 \cdot 10^{-3}$, only 1.4 times greater than the reference ($3.7 \cdot 10^{-3}$) in Figure 23a. As can be seen by comparing the DNL curves, the observed XT is minimal, of the same order of the fluctuations of the reference curve. This allows to conclude that the architecture routing into the device does not present any particular criticality with regards to XT between channels, also considering that in the real design the nets and the logical cells of the FPGA are placed at proper distance to keep electromagnetic coupling as low as possible. Moreover, the compiler automatically works for keeping the layout as much scattered as possible.

2) FPGA INPUT PADS' PROXIMITY

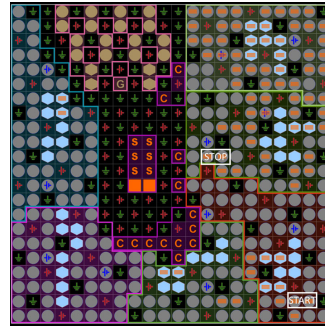
To perform this test, we have chosen a couple of channels of the TDC that have adequate distance in the PCB layout and board-to-board connector (similar to Figures 23b and 23c respectively) but present two adjacent pins of the device for the START and STOP, as shown in Figure 25b. We used the firmware described in Paragraph V-A. Obviously, we have changed the nets of the ports of START and STOP.

Figure 25a shows the relative DNL error curve with negligible correlated XT detected at $T_{START}/2 \simeq 70\text{ ns}$ with a peak-to-peak amplitude of $5.4 \cdot 10^{-3}$, only 1.5 times bigger than the reference case ($3.7 \cdot 10^{-3}$) presented in Figure 23a. Also in this case, the observed XT is comparable with the fluctuations of the reference curve presented in Figure 23a, which allows us to conclude that the pin arrangement of the device is not particularly critical as regards XT.

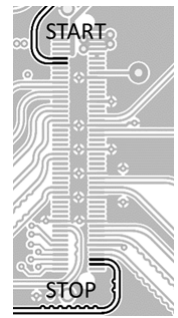
This confirms that the FPGA is designed to minimize the electromagnetic coupling between adjacent pins.



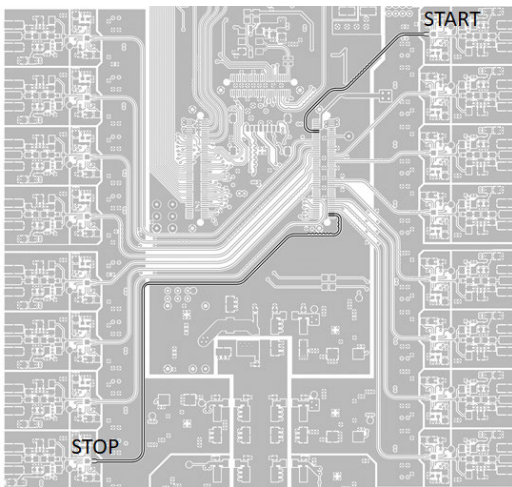
(a) Relative DNL curve measured with no XT presence ($LSB = 5 ps$).



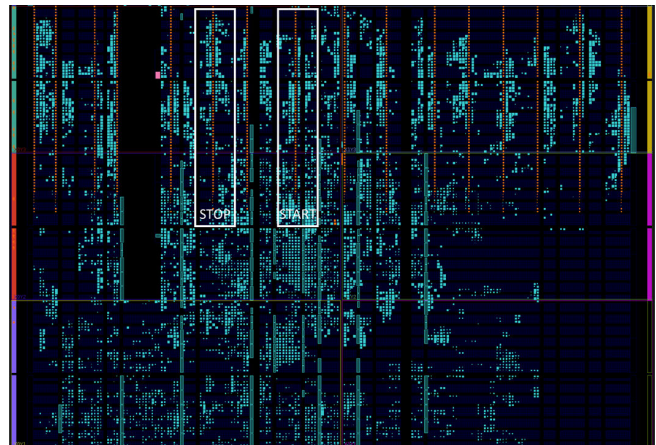
(b) Corresponding layout that maximizes the distance between START and STOP on the PCB.



(c) Corresponding layout that maximizes the distance between START and STOP on the board-to-board connector.



(d) Corresponding layout that maximizes the distance between START and STOP input pads.



(e) Corresponding layout that maximizes the distance of FPGA internal routing.

FIGURE 23. Corresponding layout that maximizes the distance and, consequently, reducing XT.

3) PCB LAYOUT

In this Paragraph, we observe and characterize the behavior of XT considering only PCB layout issues over the START and STOP signals; i.e. high density connector and differential routing proximity, and cutoff in the reference plane.

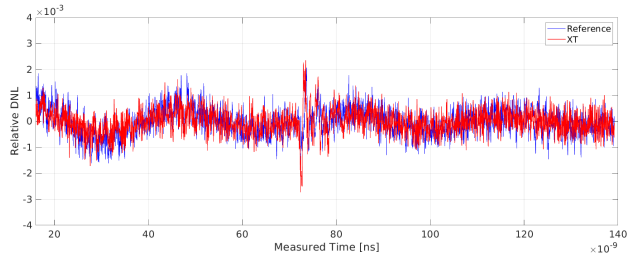
Figures 26a, 27a, 28a and 29a show a significant effect of correlated XT with an improvement of the DNL peak-to-peak amplitude up to $32.9 \cdot 10^{-3}$ at $T_{START}/2 \simeq 70 ns$. This is attributable to the critical routing conditions shown in Figures 26b, 27b, 28b and 29b. These correspond to critical layout conditions for the XT at the level of the high density board-to-board connectors between the carrier board and the module hosting the FPGA, and of the PCB carrier itself.

In particular, Figures 26a and 26b refer to XT that depends only on the proximity of the pads and internal conductors of the high density board-to-board connector. Figures 27a and 27b also add the contribution of parallel transmission lines on the PCB carrier, arriving at connectors pins. Figures 28a and 28b show XT dependent perturbation on the DNL curve due to an internal interruption

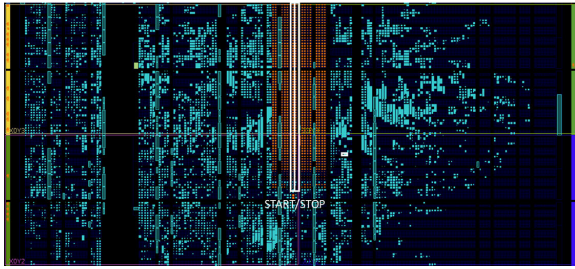
of the ground plane with no stitching capacitors. Finally, in Figures 29a and 29b the DNL curve is corrupted by the XT effect only on the internal conductors of the board-to-board connector. The comparison with conditions referring to Figure 26a highlights that the greatest XT contribution is due to the internal conductors of the connector and not to the proximity to the pads on the PCB. This contribution can be eliminated only if the connector is removed, making the connector one of the main and most critical sources of XT.

4) FINAL CONSIDERATIONS

Table 3 summarizes the effect of XT measured as relative DNL peak-to-peak variation for the different sources of disturbance considered in the previews Paragraphs, i.e. internal FPGA routing, adjacent pins, and PCB layout. It is evident that connectors and PCB layout, i.e. line proximity and cutoff in the reference plane, are by far the predominant sources of XT and this can be considered to be a conclusion of general significance.

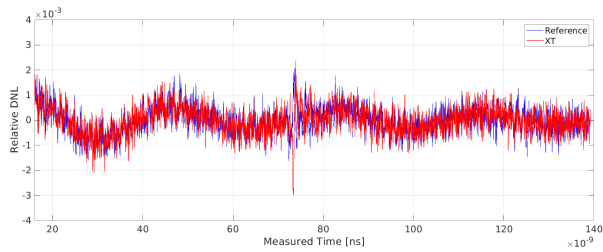


(a) Relative DNL curve ($LSB = 5 ps$) the correlated XT disturbance ($5.1 \cdot 10^{-3}$) is comparable (only 1.4 times bigger) with the reference curve's fluctuation ($3.7 \cdot 10^{-3}$).

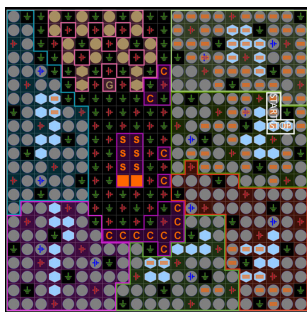


(b) FPGA internal routing changing.

FIGURE 24. Internal FPGA routing changing in the case of minimal distance between FPGA internal routing.



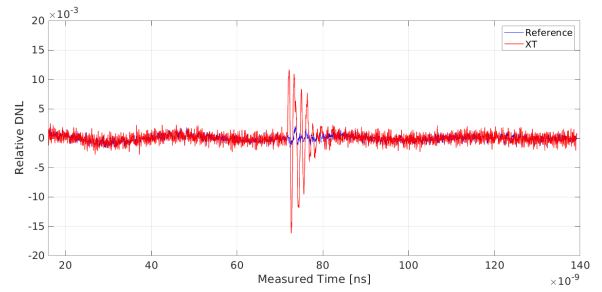
(a) Relative DNL curve ($LSB = 5 ps$) the correlated XT disturbance ($5.4 \cdot 10^{-3}$) is comparable (only 1.5 times bigger) with the reference curve's fluctuation ($3.7 \cdot 10^{-3}$).



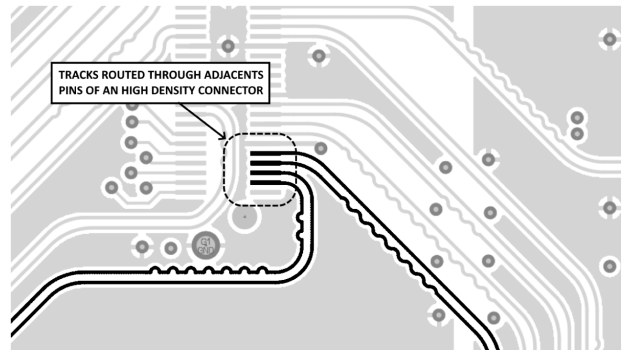
(b) FPGA input pads' proximity.

FIGURE 25. Case of FPGA input pads' proximity.

With experimental evidence, we can assert that 28-nm 7-Series Xilinx FPGAs are designed also for minimizing XT issues due to internal placing and input pads proximity. Consequently, at first order approximation, we have observed no limit in area occupancy, and for this reason the maximum number of channels instantiable is limited only by the

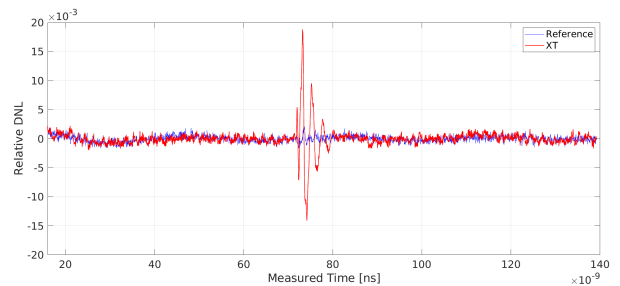


(a) Relative DNL curve ($LSB = 5 ps$) in presence of correlated XT disturbance ($28.7 \cdot 10^{-3}$), that is 7.8 times greater than the reference curve's fluctuation ($3.7 \cdot 10^{-3}$).

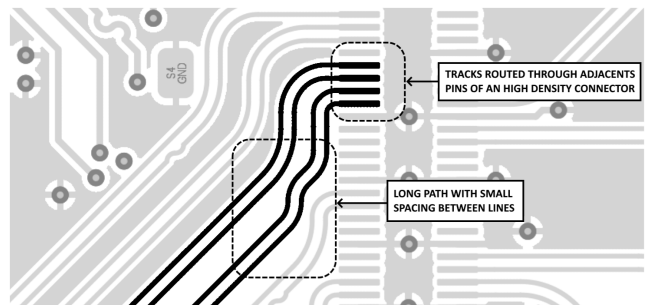


(b) Corresponding layout.

FIGURE 26. Corresponding critical layout in the board-to-board high density connectors; i.e coupling between both pads and internal conductors.



(a) Relative DNL curve ($LSB = 5 ps$) in presence of correlated XT disturbance ($28.7 \cdot 10^{-3}$), that is 7.8 times greater than the reference curve's fluctuation ($3.7 \cdot 10^{-3}$).



(b) Corresponding layout.

FIGURE 27. Corresponding critical layout in the board-to-board high density connectors and in the transmission lines on the carrier PCB.

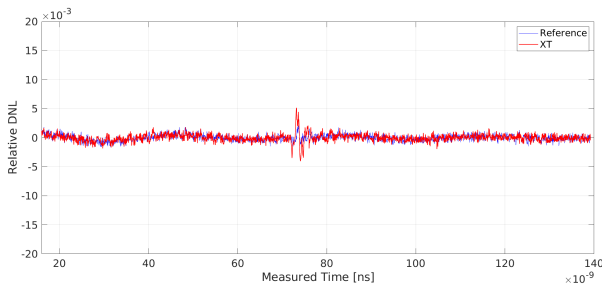
availability of hardware resources, i.e. logic elements, nets and pins.

TABLE 3. Effect on relative DNL ($LSB = 5 ps$) for different XT sources.

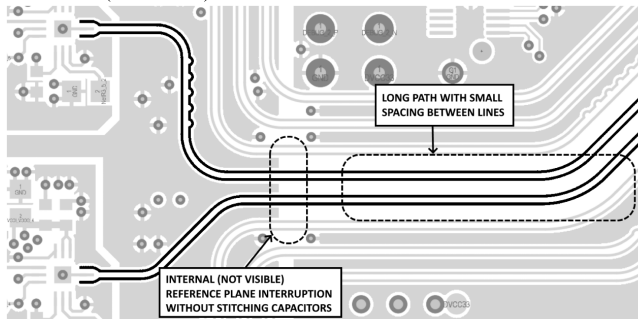
XT Sources	relative DNL error (peak-to-peak)	DNL error relative to the reference case	Type of XT	Figure
Reference DNL	$3.7 \cdot 10^{-3}$	1	Correlated	23a
FPGA internal placing	$5.1 \cdot 10^{-3}$	1.4	Correlated	24a
FPGA input pads	$5.4 \cdot 10^{-3}$	1.5	Correlated	25a
High density connector	$27.7 \cdot 10^{-3}$	7.5	Correlated	26a
Connector and lines	$28.7 \cdot 10^{-3}$	7.8	Correlated	27a
Cutoff in the reference plane	$9.6 \cdot 10^{-3}$	2.6	Correlated	28a
High density connectors	$32.9 \cdot 10^{-3}$	8.9	Correlated	29a

TABLE 4. Effect on relative DNL ($LSB = 5 ps$) with and without uncorrelated XT.

Criticality category	relative DNL error (peak-to-peak)	DNL error relative to the reference case	Figure 30
Without XT (Reference DNL)	$3.7 \cdot 10^{-3}$	1	Blue
With XT	$5.2 \cdot 10^{-3}$	1.4	Red



(a) Relative DNL curve ($LSB = 5 ps$) in presence of correlated XT disturbance ($9.6 \cdot 10^{-3}$), that is 2.6 times greater than the reference curve's fluctuation ($3.7 \cdot 10^{-3}$).



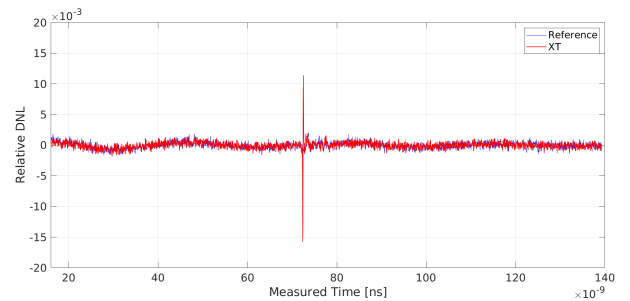
(b) Corresponding layout.

FIGURE 28. Corresponding layout critical in the presence of a cutoff in the reference plane of the carrier PCB.

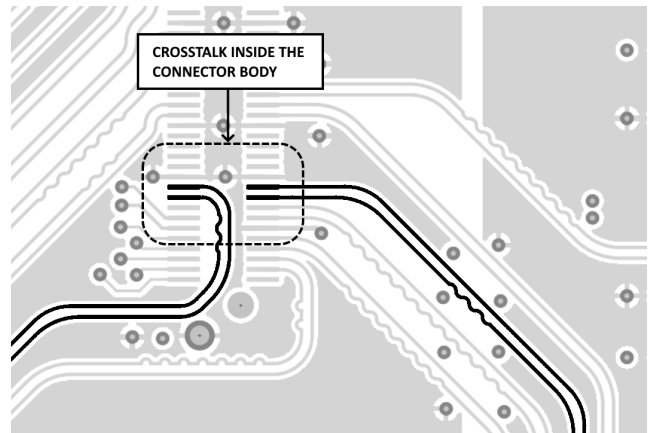
C. UNCORRELATED CROSS-TALK EVALUATION

In this Paragraph, we verify that the effect of uncorrelated XT is negligible with respect to the correlated one at same magnitude, also discussing why no uncorrelated XT issues were observed in Paragraph V-B. For this reason, according to Figure 22, we have turn on the 3rd SIGNAL with a 10 MHz square wave 2 V wide that is coupled with the START into the differential routing and board-to-board connector.

Figure 30 shows the effects of uncorrelated XT. Here, we can see how the DNL in the presence of the uncorrelated XT, red line, is quite a lot greater ($5.2 \cdot 10^{-3}$) than the ideal case, blue line, ($3.7 \cdot 10^{-3}$).



(a) Relative DNL curve ($LSB = 5 ps$) in presence of correlated XT disturbance ($32.9 \cdot 10^{-3}$), that is 8.9 times greater than reference curve's fluctuation ($3.7 \cdot 10^{-3}$).



(b) Corresponding layout.

FIGURE 29. Corresponding critical layout in the internal conductors of the board-to-board high density connectors. Input pads are far apart.

Table 4 summarizes the effect of uncorrelated XT measured as the relative DNL peak-to-peak variation for the different sources of disturbance considered. It is evident that uncorrelated XT is negligible respect to connectors and PCB layout.

Moreover, we can observe that the uncorrelated XT perturbation on the DNL is distributed on the whole FSR, unlike

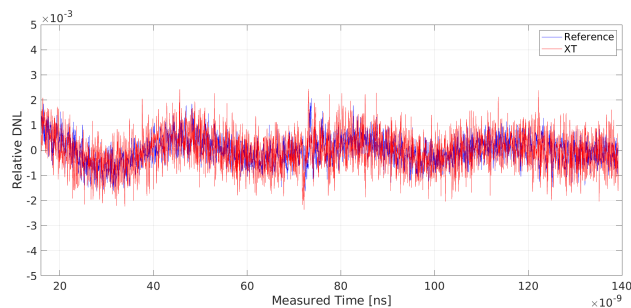


FIGURE 30. Comparison between relative DNL curve measured with (red, $5.2 \cdot 10^{-3}$) and without (blue, $3.7 \cdot 10^{-3}$) uncorrelated XT presence (LSB = 5 ps).

the correlated one, which is distributed in a single region. Therefore, the uncorrelated XT has a much lower impact than the correlated one.

VI. CONCLUSION

The effects of XT on time measurements are investigated and a reliable and effective method for characterizing XT interference, based on the Code-Density Test (CDT), is presented.

The experimental characterization of the phenomenon was performed from a real instrument for time measurements, that is a 16-channels TDC implemented in a Xilinx 7-Series 28-nm FPGA device. Different sources of XT have been taken into account, i.e. internal FPGA firmware layout, input pads' proximity, PCB layout issues. For each of them, the effects have been assessed qualitatively and quantitatively. It has been highlighted that the XT due to internal FPGA routing and pins position can be neglected with respect to the XT due to PCB layout, that is represented by board-to-board high density connectors, coupling between transmission lines, and cut-off in the reference plane. Moreover, we have experimentally verified that the XT due to connectors with high pin density is the most critical for time measurement.

Each XT effect has been classified as correlated or uncorrelated. In this manner, it has been observed that uncorrelated XT is negligible with respect to the correlated one at the same intensity; in fact, uncorrelated XT injects disturbs randomly distributed in a defined measurement range, whereas correlated XT concentrates all the disturb power on a precise measure value.

The analysis also made it possible to deduce design principles required to minimize the effects of XT by identifying the most critical sources that need to be kept under control. In this sense, experiments pointed out that the internal FPGA routing and pins position can be neglected with respect to the XT effect due to PCB layout in terms of board-to-board high density connectors, coupling between transmission lines, and cut-off in the reference plane. Moreover, it was also demonstrated that high density connectors issues have the biggest impact.

In this sense, we have pointed out that 28-nm 7-Series Xilinx FPGA is designed also for making negligible the electromagnetic coupling into the internal layout and also among the pads. Consequently, at first order, we have

observed no limit in area occupancy, and for this reason the maximum number of instantiable channels is only limited by the availability of the necessary hardware resources.

ACKNOWLEDGMENT

The authors would like to thank Dr. Christophe Galland for the precious collaboration in the experimental evaluation of the effects of the phenomenon.

REFERENCES

- [1] H. Wang, J. Song, F. Liu, H. Xiang, W. Gao, and L. Wan, "Crosstalk analysis and optimization of high-speed interconnections," in *Proc. 12th Int. Conf. Electron. Packag. Technol. High Density Packag.*, Aug. 2011, pp. 1–4.
- [2] F. Yuan, *CMOS Time-Mode Circuits and Systems*, B. Raton, Ed. Boca Raton, FL, USA: CRC Press, 2016.
- [3] J. Solomon, "Analog versus digital design," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 26, Feb. 1983, pp. 216–217.
- [4] B. J. Hosticka, "Performance comparison of analog and digital circuits," *Proc. IEEE*, vol. 73, no. 1, pp. 25–29, Jan. 1985.
- [5] D. Li, M. Liu, R. Ma, and Z. Zhu, "An 8-ch LIDAR receiver based on TDC with multi-interval detection and real-time *in situ* calibration," *IEEE Trans. Instrum. Meas.*, vol. 69, no. 7, pp. 5081–5090, Jul. 2020.
- [6] M. Adamić and A. Trost, "A fast high-resolution time-to-digital converter implemented in a Zynq 7010 SoC," in *Proc. Austrochip Workshop Microelectron. (Austrochip)*, Oct. 2019, pp. 29–34.
- [7] N. Lusardi, F. Garzetti, and A. Geraci, "Digital instrument with configurable hardware and firmware for multi-channel time measures," *Rev. Sci. Instrum.*, vol. 90, no. 5, May 2019, Art. no. 055113, doi: 10.1063/1.5028131.
- [8] J. Y. Won and J. S. Lee, "Time-to-digital converter using a tuned-delay line evaluated in 28-, 40-, and 45-nm FPGAs," *IEEE Trans. Instrum. Meas.*, vol. 65, no. 7, pp. 1678–1689, Jul. 2016.
- [9] R. Machado, J. Cabral, and F. S. Alves, "Recent developments and challenges in FPGA-based time-to-digital converters," *IEEE Trans. Instrum. Meas.*, vol. 68, no. 11, pp. 4205–4221, Nov. 2019.
- [10] S. Tancock, E. Arabul, and N. Dahmoun, "A review of new time-to-digital conversion techniques," *IEEE Trans. Instrum. Meas.*, vol. 68, no. 10, pp. 3406–3417, Oct. 2019.
- [11] M. Gersbach, Y. Maruyama, E. Labonne, J. Richardson, R. Walker, L. Grant, R. Henderson, F. Borghetti, D. Stoppa, and E. Charbon, "A parallel 32×32 time-to-digital converter array fabricated in a 130 nm imaging CMOS technology," in *Proc. ESSCIRC*, Sep. 2009, pp. 196–199.
- [12] C. Uğur, G. Korcyl, J. Michel, M. Penschuk, and M. Traxler, "264 channel TDC platform applying 65 channel high precision (7.2 psRMS) FPGA based TDCs," in *Proc. IEEE Nordic-Medit. Workshop Time-to-Digit. Converters (NoMe TDC)*, Oct. 2013, pp. 1–5.
- [13] P. O'Keefe, P. Bolognesi, M. Coreno, A. Moise, R. Richter, G. Cautero, L. Stebel, R. Sergo, L. Pravica, Y. Ovcharenko, and L. Avaldi, "A photoelectron velocity map imaging spectrometer for experiments combining synchrotron and laser radiations," *Rev. Sci. Instrum.*, vol. 82, no. 3, Mar. 2011, Art. no. 033109, doi: 10.1063/1.3563723.
- [14] L. Stebel, M. Malvestuto, V. Capogrosso, P. Sigalotti, B. Ressel, F. Bondino, E. Magnano, G. Cautero, and F. Parmigiani, "Time-resolved soft X-ray absorption setup using multi-bunch operation modes at synchrotrons," *Rev. Sci. Instrum.*, vol. 82, no. 12, Dec. 2011, Art. no. 123109, doi: 10.1063/1.3669787.
- [15] W. Becker, *Advanced Time-Correlated Single Photon Counting Techniques*. Berlin, Germany: Springer, 2005.
- [16] E. Charbon, "Introduction to time-of-flight imaging," in *Proc. IEEE SENSORS*, Nov. 2014, pp. 610–613.
- [17] R. Lussana, F. Villa, A. D. Mora, D. Contini, A. Tosi, and F. Zappa, "Enhanced single-photon time-of-flight 3D ranging," *Opt. Exp.*, vol. 23, no. 19, pp. 24962–24973, Sep. 2015. [Online]. Available: <http://www.opticsexpress.org/abstract.cfm?URI=oe-23-19-24962>
- [18] D. R. Schaart, "Physics and technology of time-of-flight PET detectors," *Phys. Med. Biol.*, vol. 66, no. 9, Apr. 2021, Art. no. 09TR01, doi: 10.1088/1361-6560/abee56.
- [19] J. Kuang, Y. Wang, and C. Liu, "A 128-channel high performance time-to-digital converter implemented in an UltraScale FPGA," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Oct. 2017, pp. 1–4.

- [20] C. Niclass, C. Favi, T. Kluter, M. Gersbach, and E. Charbon, "A 128 × 128 single-photon imager with on-chip column-level 10b time-to-digital converter array capable of 97ps resolution," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2008, pp. 544–594.
- [21] D. Bucur, "Crosstalk—An overview for high speed design," in *Proc. 21st Telecommun. Forum Telfor (TELFOR)*, Nov. 2013, pp. 701–704.
- [22] B. J. Lee, P. D. Olcott, K. Jo Hong, A. M. Grant, C.-M. Chang, and C. S. Levin, "Studies of electromagnetic interference of PET detector insert for simultaneous PET/MRI," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Nov. 2013, pp. 1–3.
- [23] R. Pelka, J. Kalisz, and R. Szplet, "Nonlinearity correction of the integrated time-to-digital converter with direct coding," *IEEE Trans. Instrum. Meas.*, vol. 46, no. 2, pp. 449–453, Apr. 1997.
- [24] J. Blair, "Histogram measurement of ADC nonlinearities using sine waves," *IEEE Trans. Instrum. Meas.*, vol. 43, no. 3, pp. 373–383, Jun. 1994.
- [25] S. Salgaro, N. Corna, F. Garzetti, N. Lusardi, and A. Geraci, "Time-mode analysis of crosstalk interference in a FPGA-based TDC implementation," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Oct. 2019, pp. 1–3.
- [26] H. W. Johnson and M. Graham, *High Speed Signal Propagation: Advanced Black Magic*. Upper Saddle River, NJ, USA: Prentice-Hall, 2003.
- [27] S. H. Hall and H. L. Heck, *Advanced Signal Integrity for High-Speed Digital Designs*. Hoboken, NJ, USA: Wiley, 2009.
- [28] H. W. Johnson and M. Graham, *High-Speed Digital Design: A Handbook of Black Magic*. Upper Saddle River, NJ, USA: Prentice-Hall, 1993.
- [29] H. Johnson and M. Graham, *High Speed Signal Propagation: Advanced Black Magic*. Upper Saddle River, NJ, USA: Prentice-Hall, 2003, p. 321.
- [30] J. H. Lee, P.-S. Lee, T.-H. Lee, C. Kim, I.-C. Song, and J.-K. Wee, "Effect of split power/ground planes using stitching capacitors on radiated emission," in *Proc. 11th Electron. Packag. Technol. Conf.*, 2009, pp. 541–545.
- [31] E. Conca, V. Sesta, M. Buttavava, F. Villa, L. D. Sieno, A. D. Mora, D. Contini, P. Taroni, A. Torricelli, A. Pifferi, F. Zappa, and A. Tosi, "Large-area, fast-gated digital SiPM with integrated TDC for portable and wearable time-domain NIRS," *IEEE J. Solid-State Circuits*, vol. 55, no. 11, pp. 3097–3111, Nov. 2020.
- [32] I. E. Zadeh, J. W. N. Los, R. B. M. Gourgues, V. Steinmetz, G. Bulgarini, S. M. Dobrovolskiy, V. Zwiller, and S. N. Dorenbos, "Single-photon detectors combining high efficiency, high detection rates, and ultra-high timing resolution," *APL Photon.*, vol. 2, no. 11, Nov. 2017, Art. no. 111301, doi: 10.1063/1.5000001.
- [33] J. Bortfeldt et al., "Timing performance of a micro-channel-plate photomultiplier tube," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 960, Apr. 2020, Art. no. 163592. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S0168900220301613>
- [34] Trezz Electronic. Accessed: 2021. [Online]. Available: <http://www.trenz-electronic.de>
- [35] M. Benssalah, M. Djeddou, and K. Drouiche, "Pseudo-random sequence generator based on random selection of an elliptic curve," in *Proc. Int. Conf. Comput., Inf. Telecommun. Syst. (CITS)*, Jul. 2015, pp. 1–5.



NICOLA LUSARDI (Member, IEEE) was born in Piacenza, Italy, in November 1990. He received the Ph.D. degree, in 2018.

He developed his thesis work at the Digital Electronics Laboratory, DEIB, on a topic regarding high-resolution time-to-digital converters (TDCs) in field programmable gate arrays (FPGA). He is currently a temporary Researcher with the Digital Electronics Laboratory, DEIB; a Professor of electronics with the Politecnico di Milano; and an

Associate Member of Italian National Institute for Nuclear Physics (INFN). He is also the Co-Founder of TEDIEL S.r.l., an Italian start-up and spin-off of the Politecnico di Milano. His research line and knowledge as a digital designer have been acknowledged by public and private research centers. Since 2014, he has been collaborating with CERN in the LHCb Experiment; CAEN S.p.A., Viareggio, Lucca, Italy; CAEN ELS S.R.L., Basovizza, Trieste, Italy; Elettra Sincrotrone Trieste S.C.p.A., Basovizza; Single Quantum B.V., Delft, The Netherlands; the Technology University of Delft; École Polytechnique Fédérale de Lausanne; and Rete Ferroviaria Italiana.



NICOLA CORNA (Member, IEEE) was born in 1992. He received the bachelor's and master's degrees in electronics engineering from the Politecnico di Milano, in 2015 and 2018, respectively, where he is currently pursuing the Ph.D. degree with DEIB, with a focus on development of systems on FPGA and SoC reconfigurable devices, particularly time-domain devices. He has always been interested in free software. He is the author and a developer of various open-source projects.



FABIO GARZETTI (Member, IEEE) received the bachelor's and master's degrees in electronic engineering from the Politecnico di Milano. He developed his thesis work at the Digital Electronics Laboratory, DEIB, on a topic regarding innovative solutions for calibration and triggering of asynchronous signals for time-to-digital converters (TDCs) in field programmable gate arrays (FPGA), where he applied for the award of a temporary research fellowship within the framework of the "Design of modules for readout and processing of sampled data based on FPGA architectures" research program, supported by CAEN ELS S.R.L.



SIMONE SALGARO received the bachelor's and master's degrees in electronic engineering from the Politecnico di Milano. He developed his thesis work at the Digital Electronics Laboratory, DEIB, on a topic regarding high-performance communication interfaces for programmable logic and Linux-based SoC platforms.



ANGELO GERACI (Senior Member, IEEE) received the M.Sc. degree (*cum laude*) in electrical engineering from the Politecnico di Milano, in 1993, and the Ph.D. degree (*cum laude*) in electronics and communication engineering from the Politecnico di Milano, in 1996. Since 2004, he has been an Associate Professor with the Department of Electronics, Information and Bioengineering (DEIB), Politecnico di Milano, where his research activity is mainly focused on digital electronics

based on microcontrollers, and DSP and FPGA devices, specifically in the areas of radiation detection, medical imaging, energy storage for automotive electric systems, and HPC applications. He is currently a Lecturer for the "sistemi elettronici digitali" and "digital electronic systems design" courses with the School of Industrial and Information Engineering, Politecnico di Milano, and holds courses for the Ph.D. program in information technology. He has been scientific collaborator of Italian National Institute for Nuclear Physics (INFN), since 1995. He is a member of the Management Board and the Deputy Coordinator of the Ph.D. School of Information Engineering, Politecnico di Milano. He is an Auditor of projects on behalf of the Italian MIUR. In 2003, he was elevated to the grade of a Senior Member of the IEEE Nuclear and Plasma Society. As a Referee for several international journals, including IEEE TRANSACTIONS ON NUCLEAR SCIENCE and *Review of Scientific Instruments*, he is the author or coauthor of more than 320 publications on refereed international congress proceedings and journals (the IEEE TRANSACTIONS Prize Paper Award by the IEEE Power Electronic Society, in 2004). He has been the advocate and the manager of several sponsored joint research projects between the Politecnico di Milano and private/public companies.

...