IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received July 1, 2021, accepted September 10, 2021, date of publication September 14, 2021, date of current version September 21, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3112531

Development of a Modular Educational Kit for Research and Teaching on Power Electronics and Multilevel Converters

WILSON C. SANT'ANA[1], (Member, IEEE), BRUNO R. GAMA[2], GERMANO LAMBERT-TORRES[1], (Fellow, IEEE), ERIK L. BONALDI[1], LEVY E. L. OLIVEIRA[1], FREDERICO O. ASSUNCAO[2], DANIEL A. ARANTES[2], ISAC A. S. AREIAS[2], LUIZ E. BORGES-DA-SILVA[2], (Life Senior Member, IEEE), AND FABIO M. STEINER[3]

[1]Instituto Gnarus, Itajuba 37500-052, Brazil
[2]Instituto de Engenharia de Sistemas e Tecnologias da Informacao (IESTI), Universidade Federal de Itajuba, Itajuba 37500-903, Brazil
[3]EDF Norte Fluminense, Macae 27910-970, Brazil

Corresponding author: Wilson C. Sant'Ana (wilson_santana@ieee.org)

ABSTRACT This paper presents the detailed project of a modular educational kit to be used in research and teaching activities in the area of power electronics - with emphasis on applications in medium voltage multilevel converters. The half bridge topology has been chosen for the submodules, as they can be arranged together in a multitude of other topologies. A system composed by a mother board and daughter cards is presented. A DSP control card and a FPGA System-On-Module are inserted in the mother board in order to control the half bridge submodules. The targets of this project are applications in medium voltage - hence, the communication between the submodules and the FPGA/DSP is performed through optical fibers. Also a self power system is presented for the submodules, in order for them to operate at floating potentials. Experimental results have been presented for the most usual topologies of converters, including a Modular Multilevel Converter operating at 2000V.

INDEX TERMS Education, modular multilevel converters, power electronics.

I. INTRODUCTION

Converters based on power electronics have had an unquestionable role in the electric power system in the last decades. Recent surveys/reviews point to trending topics for research where these converters are an essential part: Xu *et al.* [1] present a review of sensorless control methods for motor drives; Kong and Karagiannidis [2] present a survey on the state of the art of battery charging schemes for plug-in electric vehicles; Sarkar *et al.* [3] present a review on aspects related to reactive power control on the modern grids (with high penetration of renewable generation); Nejabatkhah *et al.* [4] present an overview of methods for compensation of power quality issues (harmonics and unbalance) in micro grids; Elsanabary *et al.* [5] present a review of interface schemes between photovoltaic systems and medium voltage grids, using multilevel converters; Watson and Watson [6] present an overview of HVDC systems, with emphasis on voltage source type multilevel converters.

The Gnarus Institute (located in the city of Itajuba, Brazil) have had partnerships with several utility companies in Brazil on research projects. An ongoing trend in these projects is being the increase of voltage levels of the converters, aiming medium voltage distribution grids. An early prototype of a series active power filter for distribution systems in 13.8kV has been developed by their researchers in [7] - however a step-up transformer (with 220:13800 ratio) had been used and this had resulted in elevated currents at the low voltage side. Recently, the Institute has also partnered in the project of a peak-shaving equipment with energy storage on batteries, also for distribution systems in 13.8kV [8] - still using a coupling transformer - however, using a multilevel topology (Cascaded H Bridge) on the converter, which resulted in a smaller transformer ratio (2400:13800) and decreased the current rating on the semiconductors. The limitation to increase even further the number of cascaded bridges (hence,

The associate editor coordinating the review of this manuscript and approving it for publication was N. Prabaharan.

reducing even further the transformer ratio) had been the number of PWM channels available at the DSP (Digital Signal Processor) boards. Henceforth, it had become evident the necessity to use a FPGA (Field-Programmable Gate Array) to perform the PWM operations - since these devices have a multitude of programmable digital pins available. Also, the Institute has an educational role with a recently started professional multidisciplinary master's degree covering areas such as power systems, power electronics and electrical engineering.

In the work of Gamboa *et al.* [9], it is reported a progressive lack of interest of new students in power engineering courses and the measures taken by that research group in order to improve the student enrollment, which included the introduction of industrial material in laboratory work. Their approach included the development of didactic kits in order to provide a configurable framework and the appropriate physical interface for easy and safe operation in laboratory work. Also, a very usual educational tool (and, most often, less expensive than hardware experiments) in engineering is simulation. Although a simulation is a risk free environment for the students (specially, in power systems) and for the material resources exposed to damage, a simulation only provides a numerical result and it is important that the student develop more feeling about the experiment [10]. It is also common sense that laboratory and hardware experiments are mandatory for a proper education [11] and should be an integral component of a power electronics curriculum [12].

Hence, considering the necessity of the researchers of the Institute for more PWM channels (in order to control more sophisticated converters) and the educational need for the students, a modular educational kit has been developed and is presented in this article.

The literature presents quite a few developments of educational kits in power electronics - however, most of them are focused on specific subjects to be taught in a laboratory class (for example, DC-DC converters, inverters and drives) and do not offer the flexibility that researchers or graduate students would require in order to perform their investigations. In the work of Stepanov *et al.* [13], it is presented a versatile kit, based on half bridge submodules, that can be configured in several topologies - however, that work does not contemplate the control devices (either a micro controller or a DSP or a FPGA). In the work of Viola *et al.* [14], it is presented a system integrating a DSP and a FPGA, in order to control H-bridge (also known as full bridges) submodules. The H-bridge submodule, however, is not as versatile as the half bridge - as the former can be obtained from the latter, but not the opposite. Also, both [13] and [14] provided an exhibition of the functionalities of the designs but no details were provided in order for the readers to develop their own designs based on the aforementioned papers.

The contribution of this current paper is to provide a detailed project of a whole system of boards with application in both teaching and research. It is composed of a mother board and daughter boards (which includes a DSP control card and a FPGA System-On-Module, besides analog and digital cards with fiber optics communication, that may be inserted at the mother board, according with the student/researcher necessity). Also submodule boards in half-bridge topology (which can be arranged in a multitude of other topologies) have been developed and are also presented. The idea of the development of these boards is that they can be available to all students in the research group - which, in turn, would increase the students understanding about a given subject taught in class and also increase their creativity and motivation to develop their own applications. Initially, these boards are expected to be used more specifically by the Power Electronics research group - although, in the future, they may also be considered to be employed in other courses, such as Electric Machinery and Drives, Mechatronics, Power Quality, Smart Grids and etc.

Section II presents the conceptual idea of the modular kit and its applicability. Section III presents a detailed project of the gate driver circuit used in the submodule boards. Section III presents a detailed project of the optical fiber circuit used in some of the boards of this kit. Section V presents the detail project of all boards of the kit. Section VI presents the experimental results, obtained with the submodules arranged in the most usual topologies of converters, including a Modular Multilevel Converter operating with a DC link of 2000V.

II. CONCEPTUAL PROJECT OF THE MODULAR KIT

The goal of this project is to offer the students/researchers a complete modular platform, where they can implement their projects according to their requirements. Hence a complete modular setup has been idealized, composed by a mother board with daughter cards - which simplifies connections, minimizing the chance of connection errors or electromagnetic noise on the signals. As the algorithms are, usually, implemented in a DSP, the mother board has a slot for a Texas Instruments TMS320F28379D control card [15]. In small projects, without requirements for a large number of PWM channels, the internal PWM modules of the TMS320F28379D can be used. This gives the student/researcher the possibility to use until 12 PWM channels. However, in case of multilevel converters, a higher number of PWM channels would be required. Considering this case, the mother board has also a slot for a KRTKL snickerdoodle System-On-Module (SOM) [16] with a Xilinx Zynq 7020 FPGA [17], which provides an extra number of 36 PWM channels. The DSP and the FPGA communicates via SPI through the mother board. Figure 1 presents the conceptual mother board, with indication of location of its daughter cards (discussed next).

The building block chosen for the power electronics converter is the half bridge topology. Using a half bridge as the basic building block, several other topologies can be achieved with a simple repetition of blocks and the respective connections. Figure 2 presents the half bridge building block and some of the most common topologies that can be made

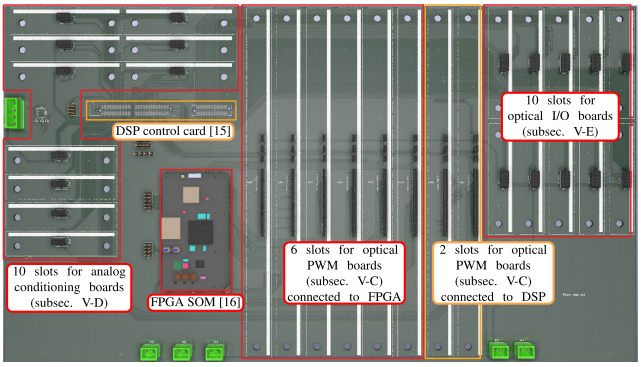

FIGURE 1. Conceptual mother board with indication of location of its daughter cards.

with it. The half bridge SM (a) is formed by two IGBTs (with their anti-parallel diodes) and a DC capacitor. In each SM there are three connection poles, identified in this figure as Superior (in red color), Central (in Orange color) and Inferior (in black color). With the use of three or two half bridges (connected together from their superior and inferior poles), the two most basic topologies for DC-AC converters - namely, the three phase bridge (b) and the single phase H bridge (c), respectively, can be obtained. Also, stacking a number of H bridges in series, the multilevel cascaded H bridge (d) can be obtained. Another popular multilevel topology is the MMC (e), where the half bridge SMs are connected between the inferior and central poles - forming two arms per phase, with an arm inductance between the arms of each phase.

On the control side, the SM boards must communicate with a micro-controller (uC), DSP, FPGA or any other circuit capable of generate PWM signals based on an algorithm that take decisions based on the values of certain analog signals (either voltages, currents, torque, temperature, etc.). As a matter of simplicity, from now on, only the acronym uC will be generically used in this text, unless otherwise specified.

Usually, the IGBTs need a current at their gate terminal higher than the capability of a regular uC, hence a gate-driver circuit or device is needed. Section III will discuss more specifically about the gate driver - nonetheless, it desired that gate driver could send a signal to the uC, in order to inform if some failure is detected. Also, in case of a failure, the gate driver should turn off its IGBT and wait for a reset signal from the uC.

In order to provide isolation between the uC and the power circuit, an opto-coupler or an interface circuit with optic fibers is required. When the SMs operate at elevated voltages (as, usually, the case for multilevel converters), the isolation provided by a regular opto-coupler may not be enough - as the physical isolation barrier inside the chip of the opto-coupler is thin. Hence, if optical fibers are used as the insulation barrier, the isolated voltage is increased to virtually infinity. Section IV will discuss more specifically about the optical fiber circuits.

On the control side, each SM board must have two inputs for the gate signals of the IGBTs, an error output (in order to

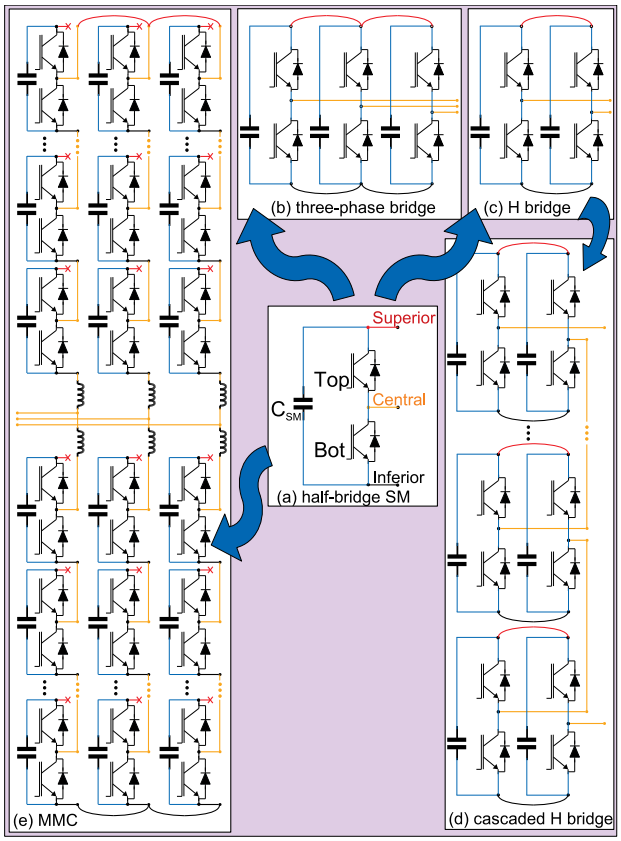

FIGURE 2. Half bridge building block (a) and some usual topologies made from it.

inform the uC if some failure is detected) and a reset input (in order to be able to turn on the gate driver again after a detected failure). In case of a multilevel converter using several SMs, the number of I/O pins on the uC is a limiting issue - hence, any savings on these pins are welcomed. As the uC does not necessarily needs to reset a SM individually, only one reset output could be used on the uC and each SM could redistribute the reset signal to the next SM. This implies on an extra output on each SM - however it saves pins on the uC, when the number of SMs is high. Figure 3 illustrates the use of only one reset output from the uC distributed to several SM boards. This figure presents a conceptual example application of an MMC converter (with 3 SMs per arm - only one phase shown). The red, orange and black rectangular prisms represent the Superior, Central and Inferior poles of the SM (as presented in Figure 2-(a)). The blue prisms represent the optical fiber receivers (Rx), whereas the gray prisms represent the optical fiber transmitters (Tx). Each SM board has its own Top and Bot input fiber and its own Error output fiber - which are not shown in the figure in order to keep the drawing clean. The reset fibers are represented in green: one SM board receives it from the previous SM (or from the uC) at its *RST in* Rx and transmits it to another SM board from its *RST out* Tx. The power connections are the same as shown in Figure 2-(e).

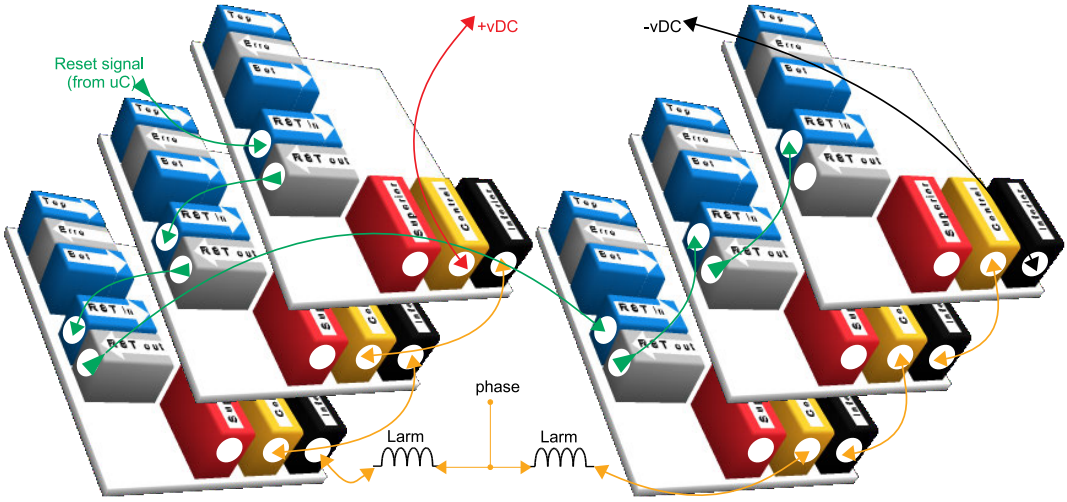

FIGURE 3. Conceptual application of the SM boards as MMC converter with 3 SMs per arm - only one phase shown.

A detailed project of the half bridge SM boards is presented in subsection V-A. These boards are composed of low power IGBTs (1200V, 15A) as this project is focused on laboratory applications - although small modifications can be performed in order to use IGBTs with higher ratings. The control signals for the IGBTs are received trough optical fibers from optical interface boards, whose detailed project is presented in subsection V-C. Each of these optical interface boards can control 6 SMs (allowing the control of 3 independent H bridges or 2 independent three-phase bridges or some multilevel topologies). According with Figure 1, 2 of these optical interface boards can be inserted on the slots connected to the DSP on the mother board (in order to control until 12 SMs) and more 6 of these boards can be inserted on the slots connected to the FPGA (in order to control more 36 SMs).

The TMS320F28379D DSP has 4 independent analog-to-digital converters (ADC), with a total 24 single-ended or 12 differential multiplexed analog inputs. The voltage input range of these ADCs, however, is from 0V to 3V - which is lower than the voltage output of some of the sensors commonly used in power electronics applications. Hence, slots for 10 signal conditioning boards (with operational amplifiers with gains selected via resistors) have been included in the mother board. Each of these 10 slots have access to a pair of single ended inputs (or one differential) of the DSP. Subsection V-D presents the detailed project of a 2 single-ended channel board to be inserted in one the 10 analog slots. At these same analog slots, boards with differential amplifiers are also planned - although not yet designed at this time.

In power electronics projects, the students/researchers usually need to switch loads and to energize a circuit. Hence an interface circuit between the DSP and relays/breakers is often required. When considering medium voltage applications, it is important that the relays/breakers be physically isolated from the low voltage electronics - thus a system with optical fibers has been idealized. The mother board is designed with 10 slots for digital I/Os. Each slot has access to four GPIO (General Purpose Input Output) pins of the DSP. The selection between Input or Output is performed during the initialization of the DSP software. Subsection V-E presents the detailed project of a board to be inserted in one the 10 digital I/O slots capable of sending (through optical fibers) signals to two remote devices (e.g., relays) and receiving (also through optical fibers) signals from other two remote devices (e.g., buttons or auxiliary contacts). At these same digital I/O slots, boards with other combination of input or output (e.g., 4 outputs or 4 inputs) can be used - although not yet designed at this time. Also, subsection V-F presents the detailed project of a relay board that is connected to optical fiber to one of the optical outputs of the optical I/O board (subsection V-E). This board has a relay with contacts that support 10A, that can drive the coils of high power circuit breakers.

III. GATE DRIVER CIRCUIT

The gate driver circuit has the function to supply the gate current necessary to switch the IGBT. In this project, it has been chosen the integrated gate driver HCPL-316J [18], which has also a feature of failure detection. Figure 4 presents a functional diagram of the HCPL-316J. The HCPL-316J isolates the power side from the low voltage side by two optical couplings: one to transmit the switching command from the low voltage to the power side (diodes represented in red in the figure) and another to signal the detected failure (diodes represented in blue).

When a difference of potential of $V_{cc1} = 5V$ is applied between the input pins V_{IN+} (pin 1) and V_{IN-} (pin 2), the LED1 (represented in red in Figure 4) will be activated. In this condition, an output with voltage given by V_{cc2} will charge the gate of the IGBT, making it to saturate between collector and emitter. For an IGBT on its saturation state, its voltage between collector and emitter (V_{ce}) should be

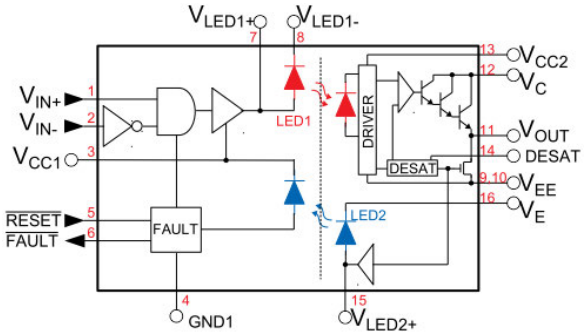

FIGURE 4. Functional diagram of the HCPL-316J gate driver [18].

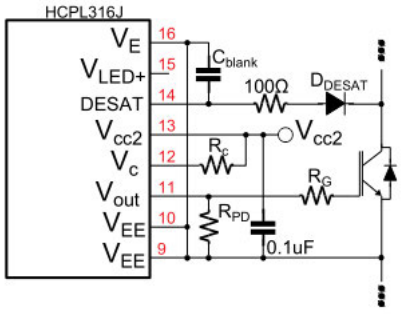

FIGURE 6. Connection of the power side of the HCPL-316J to the IGBT.

minimal. However, if an external circuit is incorrectly driving the collector voltage to an elevated potential, an elevated fault current may destroy the IGBT. Hence, the HCPL-316J has a built in circuit to monitor V_{ce}: if the IGBT is saturated and, at the same time, its V_{ce} is higher than 7V, then its output voltage is reduced and an error signal is sent (through LED2 - represented in blue in Figure 4) to its pin 6 ($\overline{FAULT}$). Under normal operation, pin 6 stays in high logic level. During a fault condition, pin 6 stays in low logic level, until a ($\overline{RESET}$) signal is applied on its pin 5.

The pin 6 ($\overline{FAULT}$) of the HCPL-316J has an open collector. This allows that the pin 6 of several HCPLs be connected together (with a common external pull-up resistor), forming a wired AND logic. Figure 5 presents an example of this connection. Under normal operation, the pull-up resistor keeps the voltage at the input $\overline{FAULT}$ of the microcontroller/DSP/FPGA (represented in the figure as uC) at a logic level high. When the pin 6 of (at least) one of the HCPLs drops to logic level low (indicating fault), the uC will receive the low level indication (even if the pin 6 of the other HCPL is at high level - as its pin 6 has an open collector). According with the datasheet of the HCPL-316J [18], a pull-up resistor of value 3.3kΩ is recommended - as well as a pull-down capacitor of value 330pF, as presented in the figure.

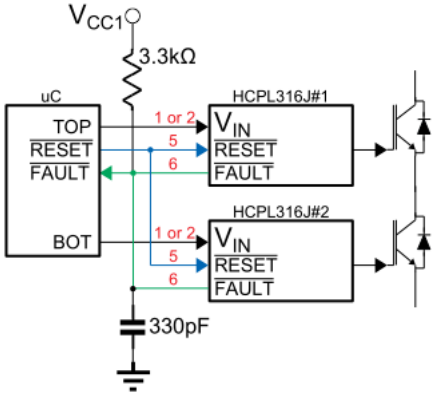

FIGURE 5. Wired AND connection of RESET and FAULT pins of multiple HCPL-316J.

Figure 6 presents the recommended circuit by the datasheet of the HCPL-316J [18] for its power side and the connection with the IGBT. The pull-down resistor R_{PD} at pin 11 must be calculated according with equation (1) in order to drain a current of 650μA and to keep the output voltage stabilized when the gate of the IGBT is already charged (as the gate current after its capacitance is already charged is null).

$$R_{PD} = \frac{V_{cc2} - 3 \cdot V_{be} - V_{EE}}{650\mu A} = \frac{15V - 3 \cdot 0.7V - 0V}{650\mu A} = 19.8k\Omega, \quad (1)$$

where $3 \cdot V_{be}$ is the voltage drop between base and emitter of the triple Darlington transistor of Figure 4 and V_{EE} is the voltage of a negative power supply connected to the emitter of the IGBT (on this project $V_{EE} = 0V$).

The value of the capacitor C_{blank} must be determined in order to tolerate a certain time for the V_{ce} to drop below 7V at the transition from OFF to ON. The datasheet of the HCPL-316J [18] recommends a minimum $C_{blank} = 100pF$ for a blank time of 2.8μs.

The diode D_{DESAT} must be of type *fast recovery*. The datasheet of the HCPL-316J [18] lists some recommended models for this diode. Among them, it has been chosen for this project the MUR1100E. The datasheet also recommends a 100Ω in series with this diode (as seen in Figure 6), in order to limit its current.

An IGBT can be seen as a combination of a bipolar transistor (at its output stage) with a MOSFET input stage. Hence, its gate terminal behaves as a capacitance, that needs to be charged until a certain value, until the bipolar stage be able to saturate. As a capacitance, until its charge, there is a peak current. It is important that the gate driver be able to supply the maximum current it is able to, in order to have the fastest transitions possible at the bipolar stage (avoiding, thus, losses at its linear region). It is important to notice that there is a peak in the gate current at its charge and another at its discharge. The resistor R_G (as seen in Figure 6) limits both peaks. However, it is desirable a higher discharge peak, in order to accelerate the turn off transition (as this transition is slower on the IGBTs). Hence, a low ohmic value resistor R_c can be inserted between pins 12 and 13. This resistor acts to increase the total resistance to the charge current only, as the paths for

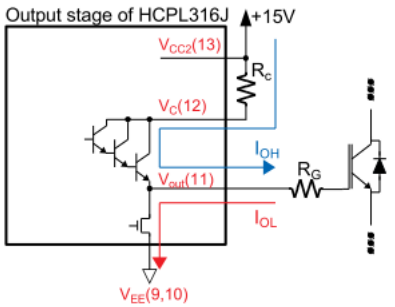

FIGURE 7. Charge and discharge paths for the gate current.

the charge and discharge currents inside the HCPL-316J are different, as presented in Figure 7.

The blue arrow in Figure 7 indicates the path of the gate current during the charge of gate capacitance. This path starts at the power supply at pin 13 (in this project, $V_{cc2} = 15V$) and flows through the resistor R_c, through the triple Darlington transistor and through the gate resistor R_G until it reaches the gate of the IGBT. The highest peak occurs when the gate capacitance is completely discharged (or when it is charged with a negative potential VEE). This results in the equation (2).

$$R_c + R_G = \frac{V_{cc2} - V_{OH} - (V_{EE})}{I_{OH}}, \tag{2}$$

where I_{OH} is the output current at high logic level and V_{OH} is the output voltage at high logic level. This values are obtained from the datasheet of the HCPL-316J [18] as $I_{OH} = 0.5A$ and $V_{OH} = V_{cc2} - 4V$. Hence, considering that this project does not use a negative power supply on V_{EE} (hence, $V_{EE} = 0V$), the sum of R_c and R_G can be calculated as (3).

$$R_c + R_G = \frac{4V - (0V)}{0.5A} = 8\Omega. \tag{3}$$

The red arrow in Figure 7 indicates the path of the gate current during the discharge of gate capacitance. This path starts at the gate of the IGBT and flows through the gate resistor R_G and through the DMOS transistor until it reaches V_{EE}. The highest peak occurs when the gate capacitance is completely charged with V_{OH}. This results in the equation (4).

$$R_G = \frac{V_{OH} - V_{OL} - (V_{EE})}{I_{OL}}, \tag{4}$$

where I_{OL} is the output current at low logic level and V_{OL} is the output voltage at low logic level.

The values of V_{OH} and V_{OL} are dependent on the output current. Considering that turn off transition occurs already at the steady state of V_{OH}, with the minimum current 650μA (drained by the pull-down resistor, according with 1), the datasheet of the HCPL-316J [18] shows that (at this condition) $V_{OH@650\mu A} = V_{cc2} - 1V$. On the other hand, the value of V_{OL} must be related with the discharge peak current. Considering a discharge peak current of 2A, the datasheet shows that (at this condition) $V_{OL@2A} = 1.5V$. Hence, considering in this project $V_{cc2} = 15V$ and $V_{EE} = 0V$, R_G can be calculated as (5)

$$R_G = \frac{15V - 1V - 1.5V - (0V)}{2A} = 6.25\Omega$$
$$\Rightarrow R_G = 6.8\Omega \ (comercial\ value). \tag{5}$$

Finally, substituting the value of R_G into (3), the value of R_c can be calculated as (6).

$$R_c = 8\Omega - 6.8\Omega = 1.2\Omega. \tag{6}$$

IV. OPTICAL FIBER CIRCUIT

The digital communication between the uC/DSP/FPGA with the gate drivers is performed through optical fibers, in order to increase safety (once the power circuit is completely isolated from the control circuit) and increase immunity to noise. As interface devices, this project utilizes the pair HFBR-1521 (transmitter - Tx) and HFBR-2521 (receiver - Rx) [19]. The wavelength of the laser on these devices is 660nm and they use plastic optical fiber with 1mm diameter.

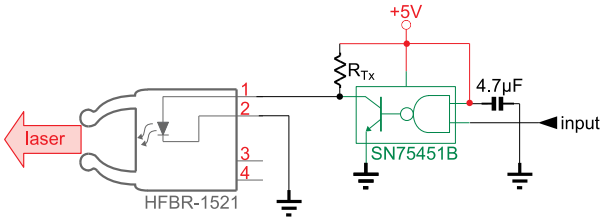

FIGURE 8. Circuit for optical transmission with the HFBR-1521.

Figure 8 presents the circuit for optical transmission with the HFBR-1521. As the led of the HFBR-1521 requires a relatively high current (in order to have enough power to transmit light to a given distance), an open collector circuit (with a pull-up resistor) is recommended to drive the led. The value of the pull-up resistor R_{Tx} is calculated in relation to the desired led current, as equation (7). According with the datasheet of the HFBR-1521 [19], in order to use an optic fiber of 5m in length, the current necessary in its led should be $I_F = 30mA$.

$$R_{Tx} = \frac{V_{cc} - V_F}{I_F} = \frac{5V - 1.67V}{30mA} = 111\Omega, \tag{7}$$

where V_{cc} is the potential to which the pull-up resistor is connected (in case of this project $V_{cc} = 5V$) and V_F is the voltage drop across the led (according with the datasheet [19], this value is typically $V_F = 1.67V$).

Figure 9 presents the circuit for optical reception with the HFBR-2521. The output stage of the HFBR-2521 has an open collector transistor with an internal (but not connected) 1kΩ pull-up resistor. For an output at 5V or 3.3V, the internal pull-up can be used, by the connection of pins 1 and 4 together.

It is important to notice that, when there is light at the optical fiber, the internal photo diode is activated and this saturate the output transistor, making its output to go to a low logic level. Conversely, when there is no light at the optical

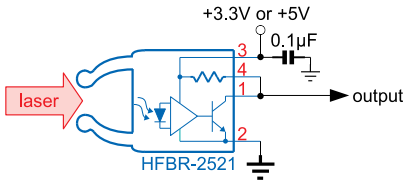

FIGURE 9. Circuit for optical reception with the HFBR-2521.

fiber, the output transistor is in its cut state and its output is a high logic level.

V. DEVELOPED BOARDS

A. HALF BRIDGE SMs

In order to ease the visualization, the schematics of the half bridge SM has been broken down into subcircuits. Figure 10 presents the subcircuit of isolated power supplies for the high side of the gate drivers. As each one of the two IGBTs of the half bridge will be at different potentials, it is necessary that the high side of each HCPL-316J be fed with an isolated power supply. Hence, two isolated DC-DC converters (Texas Instruments DCH01-0515-SN7 [20]) have been used in order to convert the 5V supply from the low side to two 15V isolated voltages: one to supply the high side of the gate driver (between pins 13-V_{ccT} and 16-V_{ET}) of the top IGBT on the bridge and another to supply the high side of the bottom gate driver (between pins 13-V_{ccB} and 16-V_{EB}). The 5V power supply may come from an external power supply or from the self power converter (to be discussed in subsection V-B).

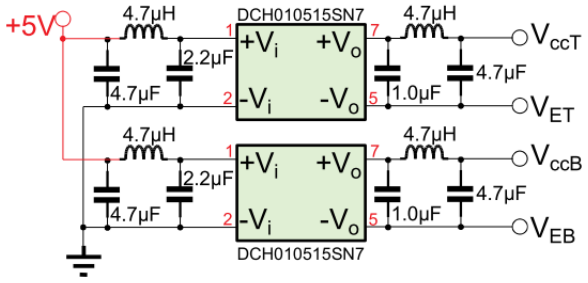

FIGURE 10. SM board: Subcircuit of isolated power supplies for the high side of the gate drivers.

Figure 11 presents the subcirctuit for optical communication of error and reset signals. This circuit has an optical Rx HFBR-2521 (as presented in section IV) in order to reset the gate drivers of this SM board (if necessary). This same reset signal is retransmitted to another SM board using an optical Tx HFBR-1521. Also, an error signal is transmitted to the DSP/FPGA in case of a fault detected by one of the gate drivers.

Under normal operation, the gate drivers have their $\overline{FAULT}$ signal (pin 6) at high logic level. When an error is detected, this signal changes to low logic level. This error signal is, then, transmitted to the optical interface board (to be discussed in subsection V-C) in order to be received at the

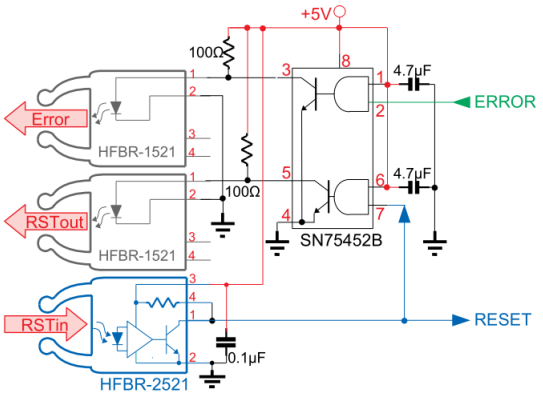

FIGURE 11. SM board: Subcircuit of optical communication of error and reset signals.

DSP/FPGA. In order to amplify the current of the led of the Tx, an open collector NAND (composed by an AND gate with an open collector inverter transistor inside the integrated circuit SN75452B [21]). Hence, when the gate driver indicates an error (low logic level at $\overline{FAULT}$), the Tx lights up the fiber. As the receivers have inverted logic (as discussed in section IV), the DSP/FPGA receives a low logic level signaling an error.

Concerning the reset, under normal operation, the DSP/FPGA sends low logic level at the respective pin. At this condition, the Tx of the optical interface board keep the fiber dark and the Rx of Figure 11 sends high logic level to the gate drivers (not resetting them). This high logic level is inverted by the NAND of Figure 11 - which, in turn, keeps the fiber RSTout dark. The next SM board receives a high logic level and the proccess is repeated to the subsequent SMs.

When a reset is necessary, the DSP/FPGA sends a high logic level at the respective pin. At this condition, the Tx of the optical interface board lights up the fiber and the Rx of Figure 11 sends low logic level to the gate drivers (resetting them). This low logic level is inverted by the NAND of Figure 11 - which, in turn, lights up the fiber RSTout. The next SM board receives a low logic level and the proccess is repeated to the subsequent SMs.

Figure 12 presents the subcircuit related to the control of the IGBTs. Two HCPL-316J are required: one for the top IGBT and another for the bottom IGBT. The low side of both HCPLs is fed by a common 5V power supply. The high side of each HCPL is fed by one of the isolated DC-DC converters of Figure 10. Both HCPLs receive the same reset signal (from Figure 11) and the $\overline{FAULT}$ signals are connected together (as the wired AND logic discussed in section IV) and sent to the DSP/FPGA.

The IGBTs in this board are the IKW15N120 [22] (from Infineon) - with a maximum v_{CE} of 1200V and rated for 15A (at a temperature of 100°C). According with [23], it is recommended a 60% (or less) ratio between the reference voltage of the SM and the IGBT voltage class - therefore, each of the SM boards on this project is intended to work until a maximum of 720V.

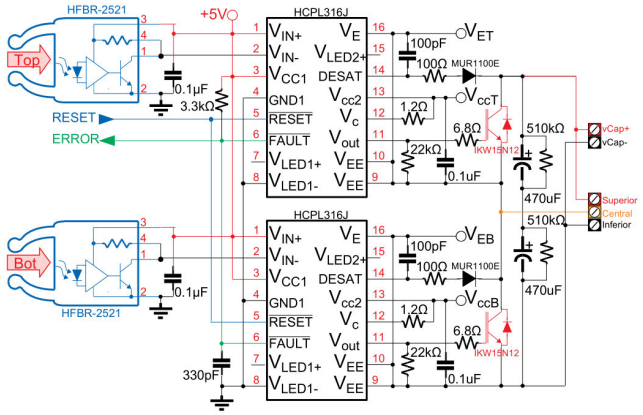

FIGURE 12. SM board: Subcircuit of control of the IGBTs.

The value of the capacitor of each SM is based on the energy to be stored on the converter. Equations specific for each topology and application have been presented in the literature. In order to reference to a few examples, in [24] a procedure is presented regarding a MMC converter - also, in [25] a procedure is presented regarding a H-bridge converter. As the SM boards developed in this project are intended to be used in laboratory experiments (hence, in low power setups), a series arrangement of two capacitors of 470μF/400V has been considered as enough, resulting in an equivalent capacitance of 235μF/800V. Also, if necessary, an external DC capacitance can be added, through the connectors *vCap+* and *vCap−*. The connectors *vCap+* and *vCap−* can also be used to extract energy from the capacitors in order to self power the board, using the additional board described in subsection V-B.

Figure 13 presents a photo of one of the SM boards with its components already soldered. This board has been intentionally manufactured on white solder mask, in order to ease the visual identification of an eventual burn mark.

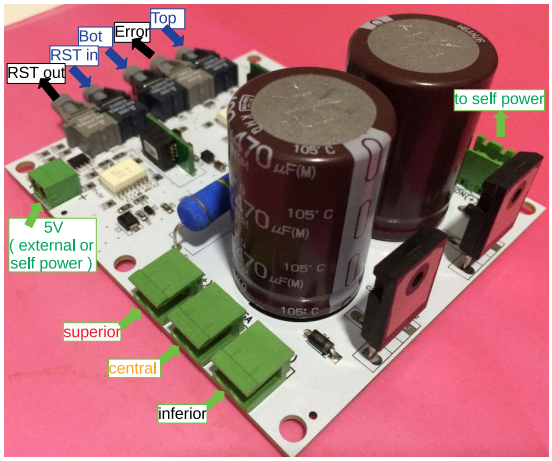

FIGURE 13. Half-bridge submodule board.

B. SELF POWER TO SMs

Considering operation in low voltage applications, the SM boards can be fed with a common external power supply of 5V. However, in case of medium/high voltage multilevel applications, the elevated difference of potential between IGBTs of different SM boards generally prohibit the use of a common ground-referenced power supply [26]. On such cases, each SM board must have a floating isolated power supply - generally a DC-DC converter, whose input is the DC capacitor voltage from the respective SM. The literature presents the development of medium voltage DC-DC converters to be used as a self power supplies when the SMs operate over thousands of volts - such as the 3kV series-connected MOSFET converter presented in [26] or the 10kV Silicon Carbide converter presented in [27]. On this particular project, the capacitors of the SMs developed in subsection V-A are limited to 800V - hence off-the-shelf DC-DC converters can be used.

As the capacitor voltage may oscillate within a certain range, the DC-DC converter must have a wide enough input range. For this project, it has been chosen the CUI's AE10-EW-S5, which allows an input from 100V to 1000V and has an isolated 5V output. The inconvenient of this converter, however, is its (relatively) large dimensions (48mm x 70mm x 23mm). On the other hand, as the DC capacitors at the SM boards have a (relatively) large height (45mm), a mezzanine structure has been proposed - where a board with the DC-DC converter can be stacked on top of the low height part of the SM board, according with Figure 14. Hence, the total height of the structure is kept the same.

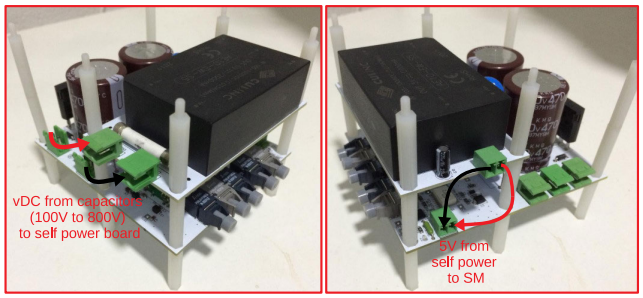

FIGURE 14. Self power boards mounted over SM boards in mezzanine structure.

Figure 15 presents the schematic circuit of the self power board, as suggested by the datasheet of the DC-DC converter AE10-EW-S5 [28]. In order to protect its inputs, a fuse, a thermistor (NTC) and a MOV are suggested. At its output stage, apart from filtering capacitors, a protection by TVS is also suggested.

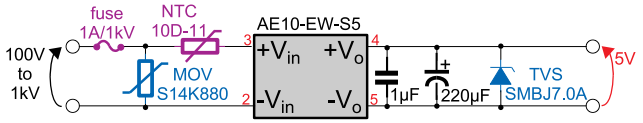

FIGURE 15. Schematic circuit of the self power board [28].

C. OPTICAL INTERFACE TO SMs

As presented in subsection V-A, the SM boards are controlled through optical fibers. Hence an optical interface is required

between those boards and the FPGA/DSP that controls the gate signals. In this project, it is proposed that these optical interface circuits be located in daugther cards, that can be modularly connected to the mother board (to be discussed in subsection V-G) according with the specific need of the student/researcher. In this project, each optical interface board can control 6 SMs (although the provided circuits can be used to customize a more specific project as needed).

In order to ease the visualization, the schematics of the optical interface board has been broken down into subcircuits - whose working principles have already been explained in section IV. Figure 16 presents the subcircuit of transmission of gate signals and reception of the error signal of the SM indicated by the x index, where $x = 1 \cdots 6$.

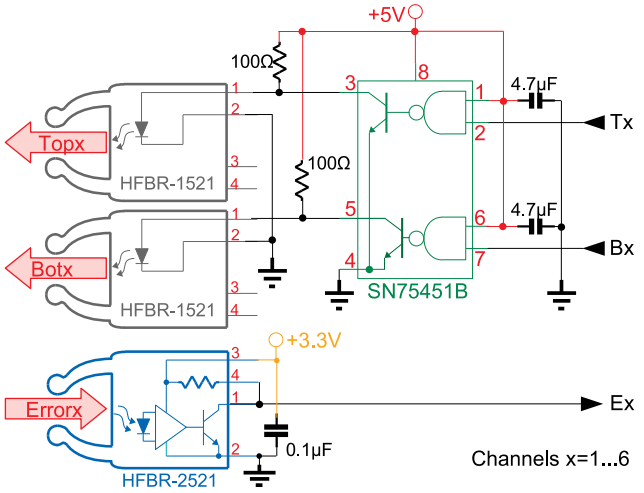

FIGURE 16. Optical interface board: Subcircuit of transmission of the gate signals and reception of the error signal (1 of 6 channels).

It is important to notice that the circuit of Figure 16 considers a uC/DSP/FPGA whose I/O pins are 3.3V TTL compatible (hence the +3.3V supply on the optical fiber receiver). On the other hand, the open collector driver SN75451 (although fed from a +5V supply) can receive as inputs both 5V or 3.3V TTL signals.

Figure 17 presents the subcircuit of transmission of the reset signal to the gate drivers. As discussed in section II, only one optical fiber is required to link the uC/DSP/FPGA with the SM boards. Then each SM board can redistribute the reset signal to the next SM board - saving I/O pins on the DSP/FPGA.

Figure 18 presents a photo of one of the optical interface boards with its components already soldered. The reset circuit of Figure 17 is required to be soldered on only one interface board (per converter) - at this particular board shown at the photo, this circuit is not soldered.

D. SINGLE-ENDED ANALOG CONDITIONING

The input pins of the ADCs of the TMS320F28379D DSP have a unipolar range from 0V to 3V. Hence some analog signal conditioning is required in order to interface these

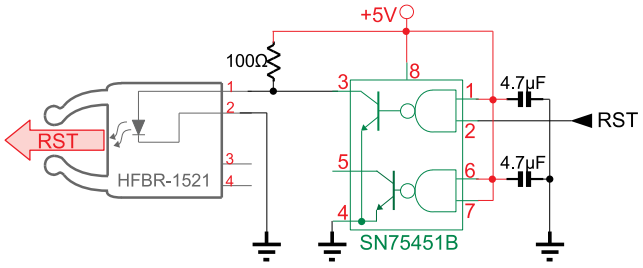

FIGURE 17. Optical interface board: Subcircuit of transmission of the reset signal.

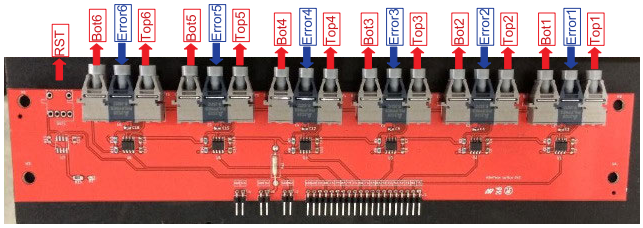

FIGURE 18. Optical interface to SMs board.

ADC pins with different sensors. Hence a circuit with three stages of operational amplifiers is presented in Figure 19 in order to:

- Perform a low pass anti-aliasing filtering;
- Provide a gain/attenuation to the sensor output, in order to match the ADC input voltage range;
- Provide an optional offset to the signal when sensor output is bipolar.

The circuit of this board has been initially proposed as an undergrad final project [29] from two students from the research group.

In order to ease the visualization, the schematics of the single-ended analog board has been broken down into subcircuits. Each of these boards has two identical channels. Figure 19 presents the subcircuit of signal conditioning of one of the two channels.

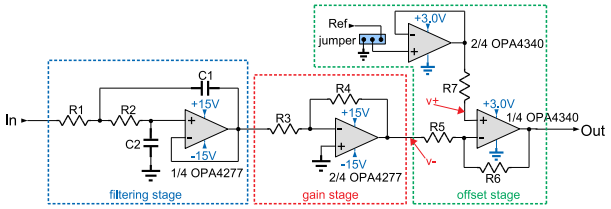

FIGURE 19. Single-ended analog board: Subcircuit of signal conditioning (1 of 2 channels).

The blue dashed region of Figure 19 presents the anti-alias low pass filtering stage. This circuit is the well-known unitary gain Sallen-Key second order low pass filter [30, pp. 807-810], whose cutoff frequency is given by (8). As an example, considering the relations $R_1 = R_2$ and $C_1 = 2 \cdot C_2$ (in order to achieve a Butterworth type of response), if a certain project requires a cutoff frequency of 5kHz, the components can be calculated as $R_1 = R_2 = 2.2k\Omega$,

$C_1 = 10nF$ and $C_2 = 5nF$.

$$f_c = \frac{1}{2 \cdot \pi \sqrt{R_1 \cdot R_2 \cdot C_1 \cdot C_2}}. \tag{8}$$

The red dashed region of Figure 19 presents the gain/attenuation stage. This circuit is the well-known inverting amplifier [30, p. 737], whose gain is given by (9). It is important to notice that the inversion in phase will be compensated in the offset stage. As an example, considering a sensor with $20V_{peak-to-peak}$ output (as most Hall effect sensors used to measure currents and voltages in power electronics circuits) and the ADC input with a range of $3V_{peak-to-peak}$, the required gain would be $A_v = 3/20 = 0.15$. Considering $R_3 = 10k\Omega$, the feedback resistor can be calculated as $R_4 = 1.5k\Omega$.

$$A_v = -\frac{R_4}{R_3}. \tag{9}$$

There are sensors that provide a bipolar output (from −v to +v) and others that provide an unipolar output (from 0 to +v). However, the input pins of ADCs of the TMS320F28379D are always unipolar (from 0 to +3V). Hence, in case of bipolar sensors, an offset of 1.5V must be added to the output of the gain stage. As both types of sensors are commonly used in power electronics applications, in order to be as general as possible, this board has the selection by jumper of the offset voltage (either 0V, in case of unipolar sensor - or 1.5V, in case of bipolar sensors).

The green dashed region of Figure 19 presents the offset stage. This circuit is the combination of the inverting amplifier [30, p. 737] (whose input v_- receives the output of the gain stage) with the non-inverting amplifier [30, p. 738] (whose input v_+ receives the offset voltage to be added). By the principle of superposition, its output is given by (10). If one choses $R_5 = R_6 = 10k\Omega$, then the signal from the gain stage (v_-) receives an unitary gain with inversion in phase (in order to compensate the inversion of the previous stage). On the other hand, the voltage to be added (v_+) will receive a gain of 2. This implies v_+ must be half of the desired offset at the output. Hence, when working with bipolar sensors, a reference voltage of 0.75V must be connected to the point *Ref*, in order to produce an offset of 1.5V at the output.

$$Out = \left(1 + \frac{R_6}{R_5}\right) \cdot v_+ - \frac{R_6}{R_5} \cdot v_i. \tag{10}$$

As proposed in the undergrad final project [29], the reference voltage of 0.75V is obtained from a resistive voltage divider from the DSP supply voltage itself. Hence, in case of variations at the DSP supply voltage, the offset is supposed to follow the variation.

Figure 20 presents the subcircuit of power supplies, which includes the 0.75V reference generation to the offset stage of the circuit of Figure 19 and the supplies to the operational amplifier at that circuit. The amplifiers of the filtering and gain stage must be fed with a symmetrical power supply. On the other hand, the amplifiers of the offset stage must be fed with a single 0 to 3V (in order to guarantee that the input voltage at the ADC pins is always limited to this range). Hence, an external symmetrical ±15V power supply is used to fed the amplifiers of the filtering and gain stages and to fed a voltage regulator LM317 [31], configured to generate a +3.0V.

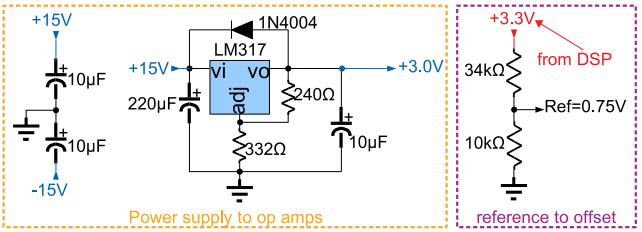

FIGURE 20. Single-ended analog board: Subcircuit of power supplies.

Figure 21 presents a photo of one of the single-ended analog conditioning boards with its components already soldered. The green connectors at the top receive the input from the sensors, while the connector at the bottom exchanges signals with the mother board (the symmetrical ±15V power supply, the DSP power supply and the outputs to the ADCs).

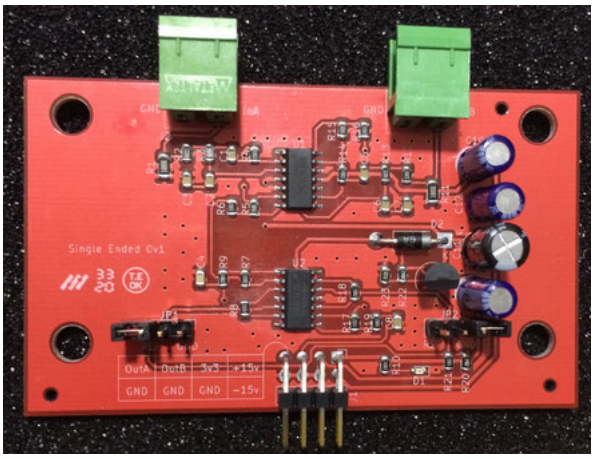

FIGURE 21. Single-ended analog conditioning board.

E. OPTICAL I/O

Frequently, in a power electronics project, the students/researchers are required to switch on and off loads, capacitor banks, circuit breakers, etc and also to accept user information from buttons or read auxiliary contacts. Also, considering medium to high voltage projects, it is important that the power circuit be completely isolated from the electronic circuit. Hence, an optical I/O board has been developed, in order to do all communication between the uC/DSP/FPGA and the relays, breakers, buttons, etc through optical fibers.

In order to be as generic as possible, each of these boards has two input channels and two output channels (although any other combination of inputs and outputs can be made in the future with very little modifications). The reception and transmission circuits are exactly the same as the ones presented for

the optical interface board to SMs (subsection V-C), with the only difference that, here, only two optical receptors and only two optical transmitters are used. Figure 22 presents a photo of one of the optical I/O boards with its components already soldered.

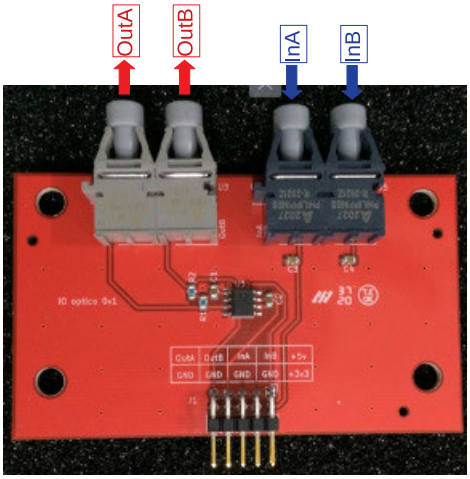

FIGURE 22. Optical I/O board.

F. RELAY BOARD (OPTICALLY CONTROLLED)

This subsection presents the development of a relay board that connects, through optical fibers, with the optical I/O board of the previous subsection. The relay at this board is a general purpose SPDT relay with a $24V_{DC}$ coil and contacts capable to switch a current of 10A at a voltage of $277V_{RMS}$ or $28V_{DC}$, which is enough to drive the coils of much larger circuit breakers.

Figure 23 presents the schematic circuit of the relay board. One important safety requirement is that the relay be active only when there is light on the fiber. Hence, in case of an accidentally broken fiber, the relay stays off. As discussed in section IV, the HFBR-2521 receiver will produce an active high output in the absence of light in the fiber. With a NPN transistor in common emitter configuration, that will turn on the relay when there is base is high, an one gate inverter IC (74AHCT1G04) had to be added to the circuit, in order to activate the base of the BC547 (hence, the relay) only in the presence of light on the fiber.

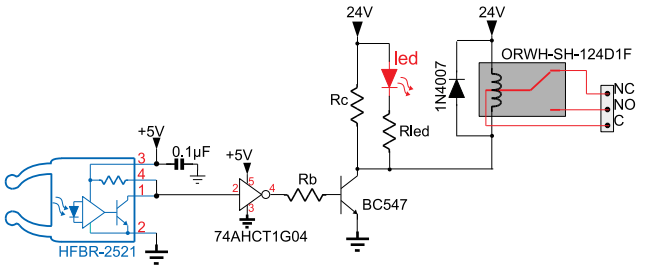

FIGURE 23. Schematic circuit of the relay board.

This particular relay (ORWH-SH-124D1F) needs 24V and 15mA on its coil in order to be active. The well-known common emitter circuit of a BC547 NPN transistor is used to drive the relay's coil. The BC547 must, also, drive a LED (which is important to give a visual information to the user about the operation of the circuit) and a bias resistor (R_c). In order to limit the LED current, in 24V, a resistor R_{LED} =4.7kΩ is used. Hence, the LED current can be calculated (considering a voltage drop at the LED as $v_{LED} = 1.9V$ and a voltage drop between collector and emitter of the BC247 as $v_{cesat} = 0.2V$) as (11).

$$i_{LED} = \frac{24V - v_{LED} - v_{cesat}}{R_{LED}} = \frac{24V - 1.9V - 0.2V}{4.7k\Omega} = 4.7mA. \quad (11)$$

The total collector current at the BC547 is the sum of the currents of the relay's coil ($i_{coil} = 15mA$), the LED ($i_{LED} = 4.7mA$) and the bias current at R_c (which is calculated to be 10% of $i_{coil} + i_{LED}$). Hence, the bias resistor R_c can be calculated as (12).

$$R_c = \frac{24V - v_{cesat}}{10\% \cdot (i_{coil} + i_{LED})} = \frac{24V - 0.2}{10\% \cdot (15mA + 4.7mA)} = 12k\Omega. \quad (12)$$

Considering that the current gain between base and collector is, at least, 20, the minimum base current to drive the BC547 is $i_b = (1.1 \cdot (i_{coil} + i_{LED}))/20 = 1.1mA$. Hence, the bias resistor R_c can be calculated as (13).

$$R_b = \frac{5V - v_{be}}{i_b} = \frac{5V - 0.7}{1.1mA} = 3.9k\Omega. \quad (13)$$

Figure 24 presents a photo of one of the relay boards with its components already soldered. Similar to the SM and self-power boards, this board has been intentionally manufactured on white solder mask, in order to ease the visual identification of an eventual burn mark. The green connector at top receives the 24V and 5V power supplies and the other green connector at right gives access to the relay contacts.

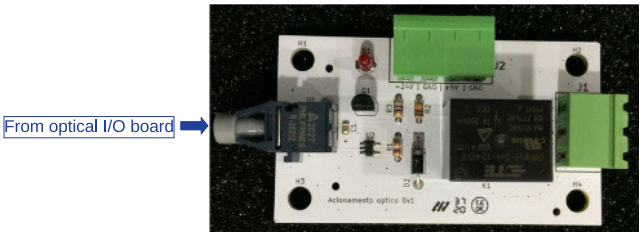

FIGURE 24. Optically controlled relay board.

G. MOTHER BOARD

The boards described in subsections V-C, V-D and V-E communicate either with the DSP control card TMS320F28379D [15] or with the System-On-Module FPGA snickerdoodle [16] through a mother board. Figure 25 presents a photo of the mother board, with some of its daughter cards inserted.

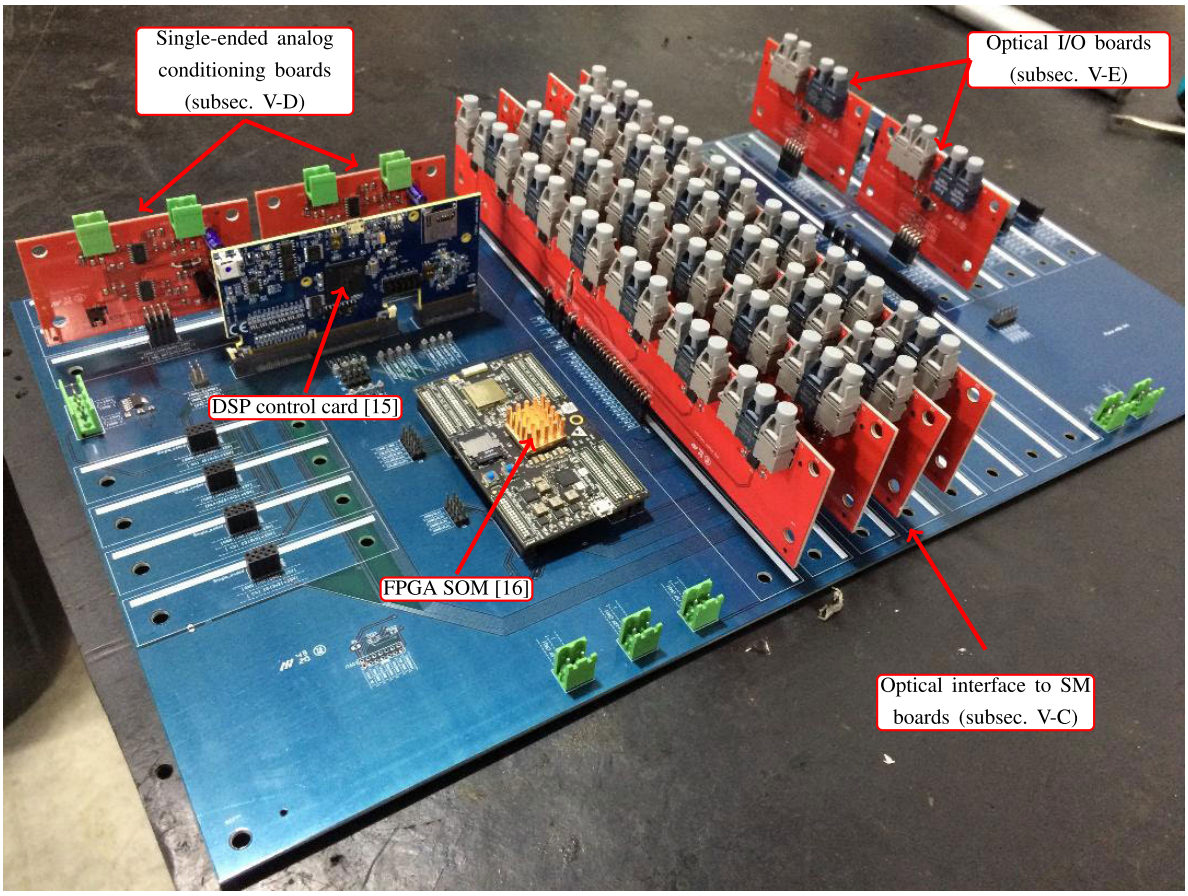

FIGURE 25. Mother board with inserted daughter cards.

The DSP TMS320F28379D has 12 PWM modules. Hence, the mother board has been designed with 2 slots in order to connect these modules to the optical interface to SM boards (described in subsection V-C, each of them controlling 6 SMs). In applications where a higher number of PWM channels are required, the FPGA can be used. Hence, the mother board has been designed with additional 6 slots for optical interface to SM boards in order to connect them to the FPGA - providing, thus, control to more 36 SMs. The mother board has two dedicated SPI links between the DSP control card and the FPGA.

From the 24 single-ended analog pins available at the DSP, the mother board is designed to use until 20 of them, with 10 slots to insert the single-ended boards (described in subsection V-D, each of them conditioning 2 analog signals). For future applications, at any of these 10 slots, instead of a 2 channel single-ended board, a 1 channel differential board can be inserted (although not yet developed at this time).

The mother board is also designed to give access to 40 GPIO pins of the DSP, divided in 10 slots for boards using 4 GPIOs (each board). At any of these 10 slots, the optical I/O boards (described in subsection V-E) can be inserted. For future applications, other types of boards (although not yet developed at this time) can also be inserted at any of these slots.

VI. EXPERIMENTAL RESULTS

In order to show the versatility of the half-bridge SM boards and their potential of use on a wide range of projects, some of the most usual topologies in power electronics have been tested. The topologies tested are: H bridge (subsection VI-A), three-phase bridge (subsection VI-B), cascaded H bridge (subsection VI-C) and MMC (subsections VI-D and VI-E). From subsection VI-A until VI-C, the tests have been performed in a low voltage setup, with a bench power supply as the DC link of the converters. The tests of subsections VI-D and VI-E have been performed with a medium voltage rectifier (although in subsection VI-D the DC voltage was still kept low). Subsection VI-E presents also the test of the self powered converter.

In all tests, the reference signal to the PWM modulators is a sinusoid stored in the memory of the DSP and the switching frequency is 5kHz. From subsection VI-A until VI-C, the PWM modulation is performed using the internal PWM modules of the DSP. A detailed procedure for programming the PWM modules of the C2000 family of DSPs

(emphasizing multilevel converters) is presented in [32]. As the TMS320F28379D have only 12 PWM modules, the tests of subsections VI-D and VI-E have been performed with a multilevel PWM modulator implemented in VHDL language in the FPGA, based on [33]. In this last case, the DSP sends the sinusoidal modulation indexes to the FPGA through one of the dedicated SPI buses available at the mother board. In either case, the basic building block of a PWM modulator is based on a comparison of the reference (also known as the modulating signal) with a triangular carrier, as presented in Figure 26. For a half-bridge submodule, the top and bottom IGBTs have complimentary states, i.e., $B_n = \overline{T_n}$ (for a particular SM#n). Whenever the modulating signal is greater or equals to the triangular carrier, the top IGBT T_n is activated (and the bottom IGBT B_n is deactivated) - conversely, whenever the modulating signal is less than the triangular carrier, the bottom IGBT B_n is activated (and the top IGBT T_n is deactivated), as illustrated in Figure 27. For each of the following topologies, this basic PWM scheme is repeated (for each of the SMs), with differences on the phase angles of the reference or on the phase angles of the carriers, as presented in the next subsections.

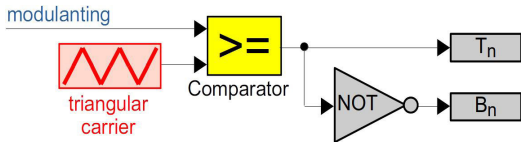

FIGURE 26. Basic PWM modulation.

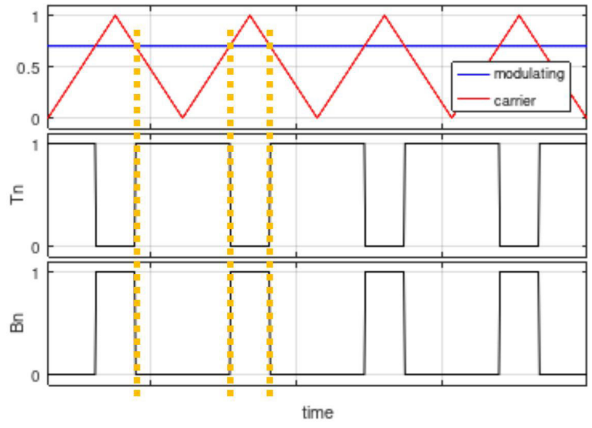

FIGURE 27. PWM pulse generation.

A. LOW VOLTAGE TEST OF SM BOARDS IN H BRIDGE CONFIGURATION

The H bridge (also known as full bridge) is a popular single-phase topology. It can be obtained using two half bridge SMs, as presented in Figure 28. Also, this figure informs the PWM parameters - which is based on the well-known Unipolar PWM technique [34, pp. 215-218]: two sinusoidal modulating references (with a phase difference of 180° between them - indicated by mod:0° for one SM and mod:180° for the other) are respectively compared against two triangular carriers with no phase difference between them (indicated by carrier:0° for both SMs).

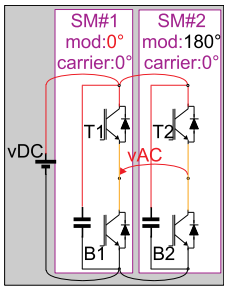

FIGURE 28. Schematics of 2 SMs connected in H bridge topology.

Figure 29 presents a photo of 2 of the SM boards of subsection V-A connected in the H bridge topology, whose connections are the ones of Figure 28.

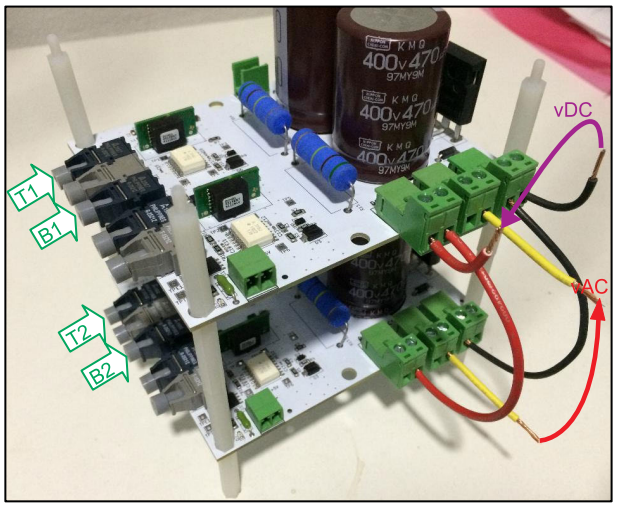

FIGURE 29. Photo of 2 SMs connected in H bridge topology.

Figure 30 presents the low voltage test of the H bridge converter, using a 10V power supply at the DC link. The plots in yellow and green are the DSP outputs of the PWM modules for the top IGBTs of the bridge. The red plot is the output of the converter: with a unipolar modulation, the voltage switches between $-v_{DC}$ and zero and between zero and $+v_{DC}$. The blue plot is the same measurement at the output of the converter, although with the digital low pass filtering function of the oscilloscope activated (hence, the phase delay) - in order to provide a more stable trigger signal.

B. LOW VOLTAGE TEST OF SM BOARDS IN THREE-PHASE BRIDGE CONFIGURATION

A very popular topology for electric machinery drives is the three-phase bridge. It can be obtained using three half bridge SMs, as presented in Figure 31. This figure also

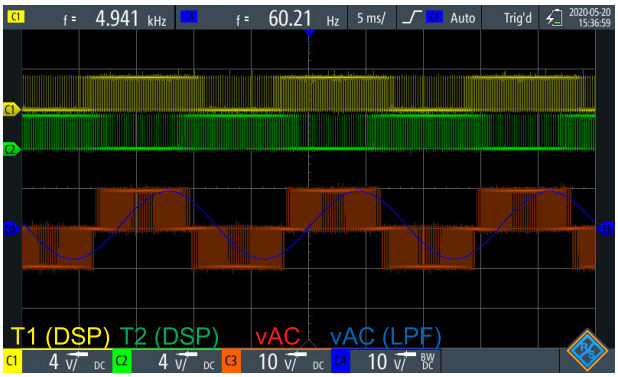

FIGURE 30. Waveforms of low voltage test of SMs connected in H bridge topology.

informs the PWM parameters - which is based on the well-known three-phase PWM technique [34, pp. 226-228]: three sinusoidal modulating references (with a phase difference of 120° between them) are respectively compared against three triangular carriers with no phase difference between them.

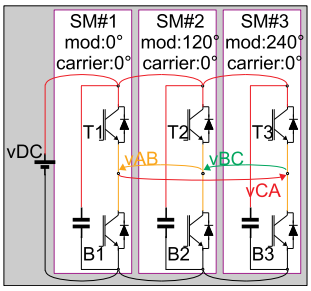

FIGURE 31. Schematics of 3 SMs connected in three phase topology.

Figure 32 presents a photo of 3 of the SM boards of subsection V-A connected in the three-phase topology, whose connections are the ones of Figure 31.

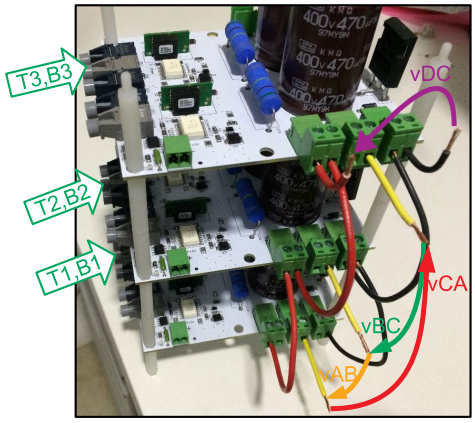

FIGURE 32. Photo of 3 SMs connected in three phase topology.

Figure 33 presents the low voltage test of the three-phase bridge, using a 10V power supply at the DC link. The plots in yellow, green and red are the phase-to-phase voltages. It can be noticed that these voltages are 120° out of phase from each other. The blue plot is the same measurement of v_{AB} (yellow), although with the digital low pass filtering function of the oscilloscope activated.

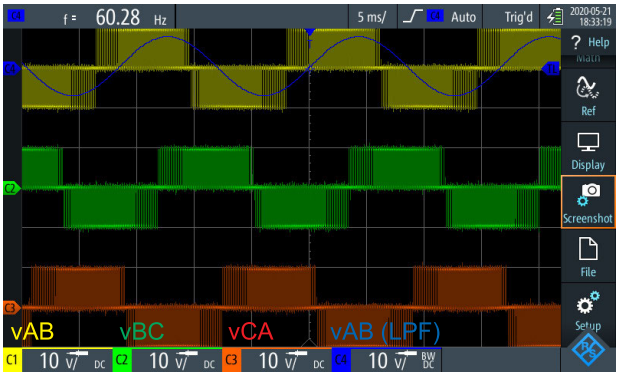

FIGURE 33. Waveforms of low voltage test of SMs connected in three phase topology.

C. LOW VOLTAGE TEST OF SM BOARDS IN CASCADED H BRIDGE CONFIGURATION

The Cascaded H Bridge is a very popular multilevel topology, used when the DC sources must operate isolated from each other - as in the case of energy storage through batteries. Figure 34 presents the schematics of four half bridge SMs connected in the Cascaded H Bridge topology. In this topology, the number of levels at the resulting output voltage is given by (14), according with [35, p. 124]. This figure also informs the PWM parameters used in this case. Each of the H bridges operates with the unipolar technique [34, pp. 215-218] - however, the triangular carriers have a phase-shift between each bridge. This phase-shift $\phi_{carrier}$ is calculated as (15), according with [35, p. 127]. Hence, in the case of two H bridges, the phase-shift between carriers (from one bridge to the other) must be 90°.

$$m = 2 \cdot H + 1, \tag{14}$$

where m is the number of voltage levels obtained for a H number of H bridges in cascade.

$$\phi_{carrier} = \frac{360°}{m-1} = \frac{180°}{H}. \tag{15}$$

Figure 35 presents a photo of the four of the SM boards of subsection V-A connected in the Cascaded H Bridge topology, whose connections are the ones of Figure 34.

Figure 36 presents the low voltage test of the Cascaded H Bridge converter, using two isolated 10V power supplies, one for each DC link. The plot in yellow is the DSP output of the PWM module for the T1 IGBT of one of the bridges. The green and red plots are the unipolar outputs of each H bridge (each of them switching between $-v_{DC}$ and zero and between zero and $+v_{DC}$). The blue plot is the resulting 5 level ($-2 \cdot v_{DC}$, $-v_{DC}$, 0, $+v_{DC}$ and $+2 \cdot v_{DC}$) output vT.

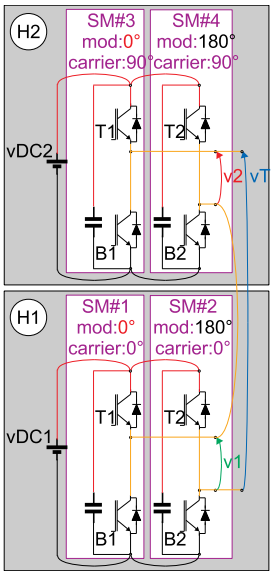

FIGURE 34. Schematics of 4 SMs connected in Cascaded H bridge multilevel topology ($H = 2$).

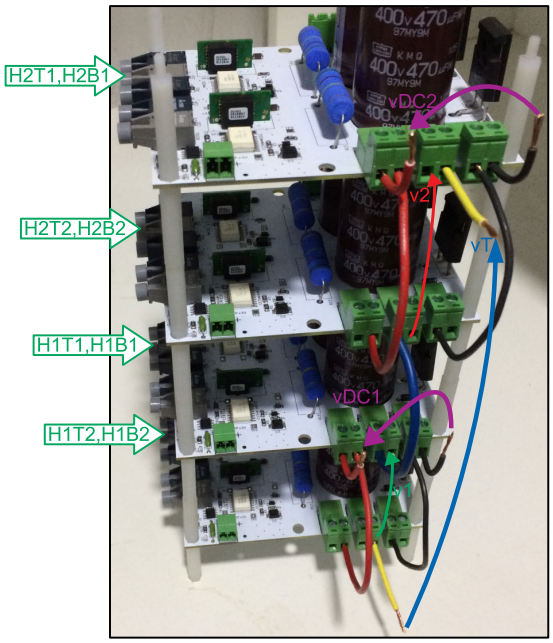

FIGURE 35. Photo of 4 SMs connected in Cascaded H bridge multilevel topology ($H = 2$).

D. LOW VOLTAGE TEST OF SM BOARDS IN MMC CONFIGURATION

In applications where a common DC source is required, such as in medium voltage drives or in voltage controlled HVDC, the Modular Multilevel Converter (MMC) is a popular topology. Figure 37 presents the schematics of the circuit of a bi-phase Modular Multilevel Converter, with N=6 SMs/arm. In case of the MMC, there are two arms per phase - hence, 4 arms in a bi-phase converter. Each phase of the converter has the modulating reference of its upper arm 180° in relation to its lower arm. In the case of a three-phase MMC

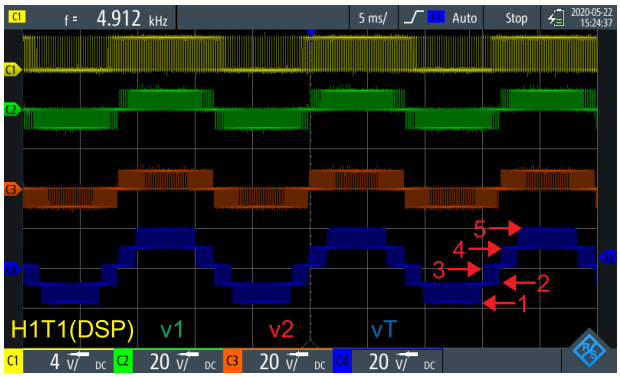

FIGURE 36. Waveforms of low voltage test of SMs connected in Cascaded H bridge multilevel topology ($H = 2 \Rightarrow 5$ levels).

(as the one depicted in Figure 2-e), the modulating references would also be 120° from one phase to another. In case of the bi-phase MMC of Figure 37, the modulating references are 180° from one phase to another. The phase shifts between the triangular carriers can be calculated as (16) and (17), according with [36].

$$\theta_{lower}(i) = \frac{360°}{N} \cdot (i-1), \tag{16}$$

where $\theta_{lower}(i)$ are the phase shifts for the i^{th} carrier of the lower arms (arm#1 and arm#3 in Figure 37) and N is the number of SMs per arm - hence $i = 1 \cdots N$.

$$\theta_{upper}(i) = \theta + \theta_{lower}(i), \tag{17}$$

where $\theta_{upper}(i)$ are the phase shifts for the i^{th} carrier of the upper arms (arm#2 and arm#4 in Figure 37). There is a constant phase difference θ between $\theta_{lower}(i)$ and $\theta_{upper}(i)$, which depends on some project criteria. When it is desired to minimize the harmonic distortion at the output voltage (resulting in $2 \cdot N + 1$ voltage levels), the constant angle θ can be calculated as (18), according with [36].

$$\theta = \begin{cases} 0°, & \text{when N is odd;} \\ 180°/N, & \text{when N is even.} \end{cases} \tag{18}$$

In the particular case of Figure 37, with $N = 6$ (even), the phase difference will be $\theta = 30°$ - hence the angles of the carriers will be given as $\theta_{lower} = [0°, 60°, 120°, 180°, 240°, 300°]$ and $\theta_{upper} = [30°, 90°, 150°, 210°, 270°, 330°]$.

At each arm of the converter, an inductance (L_{arm}) is placed in order to improve the harmonic characteristics of the circulating currents and to limit fault currents [23]. It is not on the scope of this paper to analyze the circulating currents nor the interactions between arm inductances with submodule capacitances (the reader may find such information in the literature, such as in [37]) - however, in general, suitable values for L_{arm} can be in the range of 0.1 p.u. [24].

Figure 38 presents a photo of 24 of the SM boards of subsection V-A connected in the bi-phase MMC topology, with N=6 SMs/arm. The cables used in all connections have

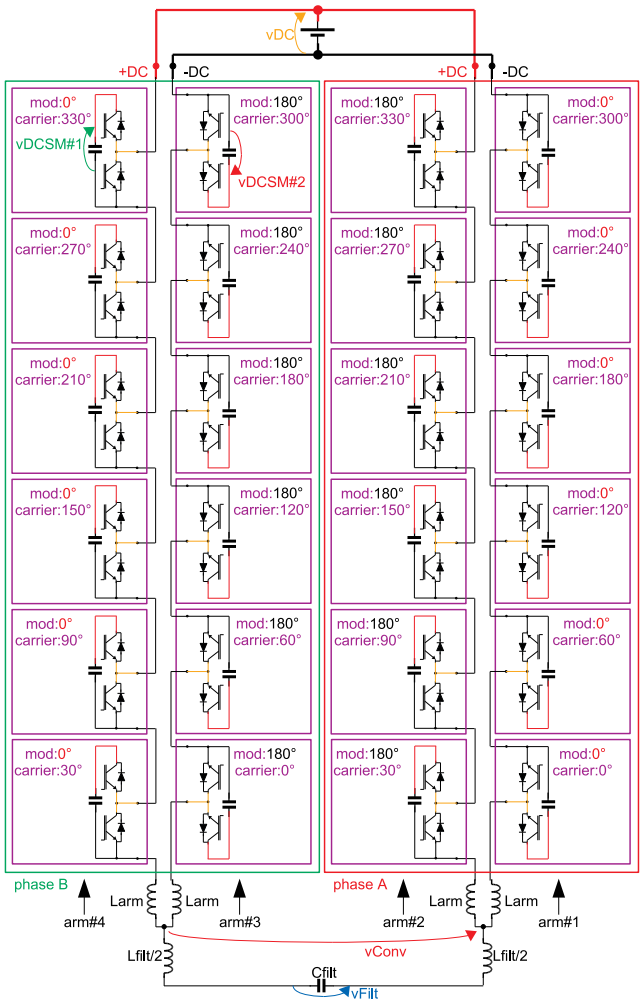

FIGURE 37. Schematics of 24 SMs connected in Modular Multilevel Converter (MMC) topology (bi-phase, 4 arms, $N = 6$ SMs/arm).

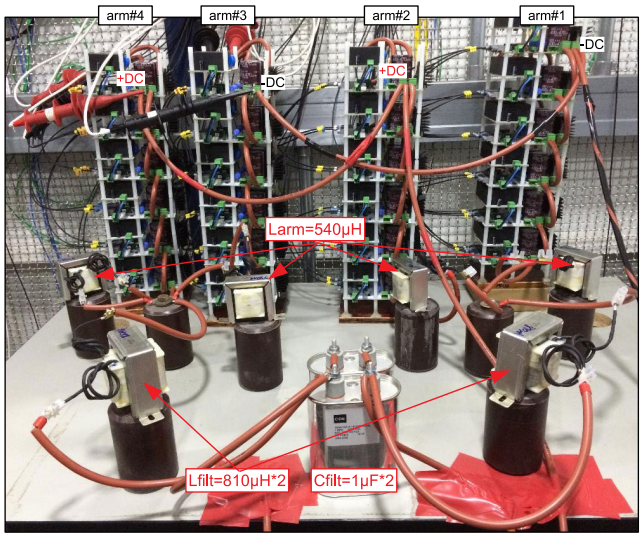

FIGURE 38. Photo of 24 SMs connected in Modular Multilevel Converter (MMC) topology (bi-phase, 4 arms, $N = 6$ SMs/arm).

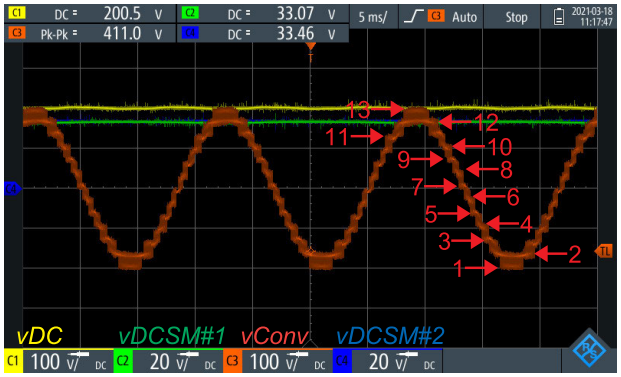

FIGURE 39. Waveforms of low voltage test of SMs connected in Modular Multilevel Converter (MMC) topology (bi-phase, 4 arms, $N = 6$ SMs/arm $\Rightarrow$13 levels).

insulation for 15kV and the AC filter capacitors have insulation for 5kV. The DC link is fed by a medium voltage rectifier with its AC input controlled by VARIAC. At this present subsection, the voltage of the VARIAC is still kept low. As the converter is operating in low voltage at this present subsection, the power source to the SM boards is an external power supply (common to all SM boards). It is important to notice, however, that at the presented photo, the SM boards are fed by their respective self-power board (which will be used in subsection VI-E).

Figure 39 presents the low voltage test of the MMC bi-phase converter, with the DC link voltage set (by VARIAC) to $v_{DC} = 200V$. During steady state operation, the total DC link voltage will be divided by the N SMs in an arm. The plot in yellow is the total DC voltage of the converter $v_{DC} = 200V$. The green and blue plots are the voltages at the DC capacitors of two of the SMs $v_{DCSM\#1} = v_{DCSM\#2} = v_{DC}/N = 200V/6 = 33V$. The red plot is the non-filtered output of the converter v_{Conv}. It can be noticed that this voltage has 13 levels, as expected for N=6 SMs/arm with modulation $2 \cdot N + 1$.

E. TEST OF SELF POWERED CONVERTER AND MEDIUM VOLTAGE TEST OF MMC CONFIGURATION

The SM boards of the previous subsection (operating in low voltage) had a common external power supply. When operating in multilevel topologies, the SM boards operate at different potentials from each other. If this difference of potential is superior to the isolation barrier of some components in the boards (namely the HCPL-316J gate driver of Figure 12 and the DCH010515 DC-DC converters of Figure 10 that supply the high side of the gate drivers), there might be some damage to these components. Hence, in subsection V-B it has been designed a system that enables the power supply of each SM to float in relation to each other - following the potential of its own DC capacitor.

The condition required by the self power system described in subsection V-B to supply the SM board is that its input voltage (the voltage at the board's DC capacitor) be higher than 100V. During steady state operation of an MMC converter, the voltages at each SM will be equals to the total

DC link voltage divided by the number of active SMs (which means N), hence $v_{DCSM}|_{steady-state} = v_{DC}/N$. However, at startup, with the IGBTs still off, the individual SM voltages will be equals to the total DC link voltage divided by the total number of SMs in a phase (which means $2 \cdot N$), $v_{DCSM}|_{startup} = v_{DC}/(2 \cdot N)$. This implies that the minimum total DC link voltage to startup the self-power converter of subsection V-B is $v_{DCmin}|_{startup} = 200 \cdot N$). In the particular case of the converter of Figure 37, with $N = 6$ SM/arm, the minimum DC voltage is $v_{DCmin}|_{startup@N=6} = 1200V$.

In order to obtain the results in medium voltage, the isolation of a regular isolated channel oscilloscope is not enough. Hence, in order to measure the signals indicated in Figure 37, high voltage differential probes (with attenuation of 2000x) have been utilized to measure v_{DC}, $v_{DCSM\#1}$, $v_{DCSM\#2}$ and v_{conv}. Also, in order to measure v_{filt}, a potential transformer with ratio $4160/\sqrt{3} : 115/\sqrt{3}$ has been used.

Figure 40 presents the medium voltage test of the MMC bi-phase converter, with the DC link voltage set (by VARIAC) to $v_{DC} = 2000V$. During steady state operation, the total DC link voltage will be divided by the $N = 6$ SMs in each arm. The plot in yellow is the total DC voltage of the converter $v_{DC} = 2000V$. The green plots is the voltage at the DC capacitor of one of the SMs $v_{DCSM\#1} = v_{DC}/N = 2000V/6 = 333V$. The red plot is the non-filtered output of the converter v_{Conv}. It can be noticed that this voltage has 13 levels, as expected for N=6 SMs/arm with modulation $2 \cdot N + 1$. The blue plot is the filtered output v_{filt} of the converter (with $L_{filt} = 2 \cdot 810\mu H$ and $C_{filt} = 2 \cdot 1\mu F$, as shown in Figure 38).

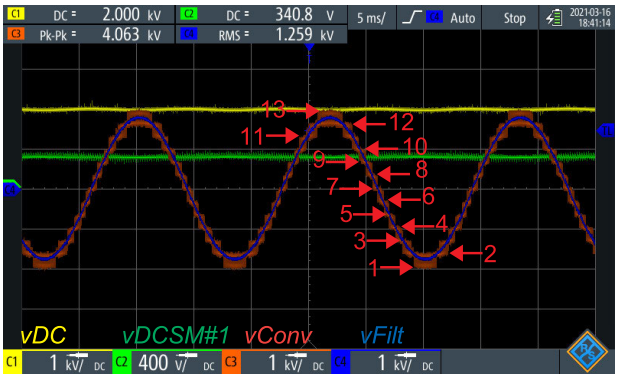

FIGURE 40. Waveform of medium voltage ($vDC = 2000V$) test of SMs connected in Modular Multilevel Converter (MMC) topology (bi-phase, 4 arms, $N = 6$ SMs/arm $\Rightarrow$13 levels).

Figure 41 presents the waveforms at the startup of the converter. The yellow plot is the total DC link voltage (v_{DC}). The green and red plots are the individual DC voltages at two SM boards (the voltages at the other SMs are supposed to be similar). The blue plot is the output of the converter (after the LC filter).

The total DC voltage v_{DC} is adjusted (through VARIAC and rectifier) to a value larger than the minimum of 1200V (required in order to have more than 100V at each self power converter). Figure 41 presents the instant of a step variation from zero to 2000V at v_{DC}. As the startup of the converter is not immediate, for about 3 time divisions of 50ms, the IGBTs are not switching - hence the total DC voltage is divided by $2 \cdot N$ SMs ($v_{DCSM\#1} = v_{DCSM\#2} = v_{DC}/N = 2000V/12 = 167V$). After the start of the self power converters, the individual DC voltages at each SM rise to the total DC voltage divided by N SMs ($v_{DCSM\#1} = v_{DCSM\#2} = v_{DC}/N = 2000V/12 = 333V$).

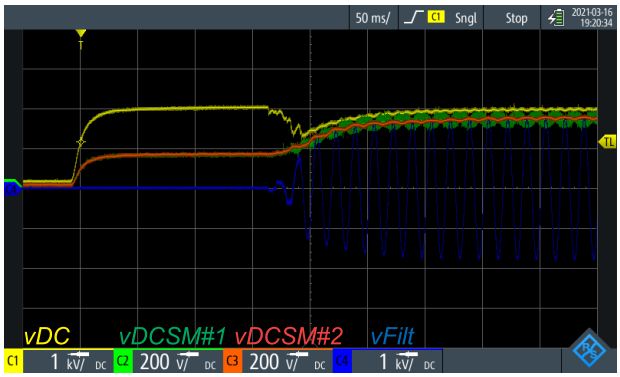

FIGURE 41. Waveforms at start-up of self-powered Modular Multilevel Converter (MMC) (bi-phase, 4 arms, $N = 6$ SMs/arm.

It is important to notice that, here, only the operation of the boards have been presented. In case of a real application, a control loop must ensure that the DC voltages at each self power modules are kept stable withing the operation range of these modules.

VII. CONCLUSION

This paper presented the project and the applicability of a modular educational kit to be used by research personnel and in laboratory classes in power electronics. The detailed project of all circuits have been presented. The kit is composed by a motherboard and daughter cards. This minimizes the chance of connection errors and also minimizes the contamination by electromagnetic noises on the signals.

The mother board has a connector where is inserted a TMS320F28379D DSP Control Card. This particular DSP model can control 12 half bridge submodules - which, depending on the application, might not be enough. Hence an FPGA System-On-Module can also be inserted in the mother board and additional 36 half bridge submodules can be controlled. The motherboard has been projected with two dedicated SPI buses between the DSP and the FPGA. The detailed project of the half bridge submodules is also presented, including a system for self-powered operation.

It is important to notice that the internal PWM modules of the DSP are implemented in hardware and not consume any computational resources. The same applies when the PWM is implemented externally in the FPGA (in VHDL, Verlilog or any hardware description language) and the student/researcher has the whole processing power of the DSP to implement his particular algorithm.

The motherboard also has been projected with 10 slots for analog signal condition cards and 10 slots for optical digital I/O cards (in order to control relays and read inputs from isolated peripherals). The paper has also presented the detailed project of these boards.

Experimental results have been presented with the sub-modules arranged in the most usual topologies (although many others can be implemented), in order to show the versatility and modularity of the boards and their potential to be used in a wide range of applications. Also, the use of optical fibers ensures safe operation (as the power circuit is completely isolated from the control circuit) and robustness against electromagnetic noise.

ACKNOWLEDGMENT

The authors would like to thank the following Brazilian Research Agencies CNPq, CAPES, FAPEMIG, and ANEEL Research and Development for the support of this project.

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WILSON C. SANT'ANA (Member, IEEE) received the B.S., M.Sc., and D.Sc. degrees in electrical engineering from Itajuba Federal University (UNIFEI), Itajuba, Brazil, in 2001, 2004, and 2016, respectively.

Since 2011, he has been a Researcher with the Gnarus Institute, Itajuba. He has experience with development of hardware and software for microcontrollers, DSPs, and FPGAs. His research interests include condition-based maintenance, frequency response analysis of electric machinery, power electronics, and control systems.

BRUNO R. GAMA received the B.S. degree in automation and control engineering and the M.Sc. degree in electrical engineering from Itajuba Federal University (UNIFEI), Itajuba, Brazil, in 2017 and 2019, respectively, where he is currently pursuing the D.Sc. degree in electrical engineering.

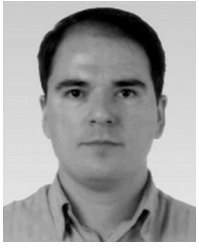
He has experience with development of systems based on SOC/FPGAs. His research interests include condition-based maintenance of electric machinery and digital signal processing.

GERMANO LAMBERT-TORRES (Fellow, IEEE) received the Ph.D. degree in electrical engineering from the Ecole Polytechnique de Montreal, Canada, in 1990.

From 1983 to 2012, he was with the Electrical Engineering Department, Itajuba Federal University (UNIFEI), Itajuba, Brazil, where he was also the Dean of the Research and Graduate Studies, from 2000 to 2004. From 1995 to 1996, he was a Visiting Professor with the University of Waterloo, Waterloo, ON, Canada. Since 2010, he has been the Director of Research and Development at PS Solucoes, Itajuba. He also serves as a Consultant for many utility companies in Brazil and South America, and he has taught numerous IEEE tutorials in the USA, Europe, and Asia. He is the author/editor or coauthor of ten books, more than 50 book chapters, and 100 transactions articles on intelligent systems and nonclassical logic.

ERIK L. BONALDI received the B.S., M.Sc., and Ph.D. degrees in electrical engineering from Itajuba Federal University, Itajuba, Brazil, in 1999, 2002, and 2006, respectively.

He is currently the CEO at PS Solutions and Research Associate and the Gnarus Institute, Itajuba. His research interests include industrial electronic automation, predictive maintenance, artificial intelligence methodologies, and rough sets classifier.



LEVY E. L. OLIVEIRA received the B.S., M.Sc., and Ph.D. degrees in electrical engineering from Itajuba Federal University, Itajuba, Brazil, in 1999, 2002, and 2006, respectively.

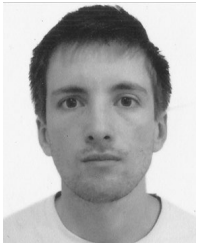
He is currently the CTO at PS Solutions and Research Associate and the Gnarus Institute. He has experience with development of electronic systems (hardware, firmware and software) for monitoring of electric machinery. His research interests include data acquisition systems, digital signal processing, and microcontrollers.

FREDERICO O. ASSUNCAO received the B.Sc. and M.Sc. degrees in electrical engineering from Itajuba Federal University (UNIFEI), Itajuba, Brazil, in 2003 and 2006, respectively, where he is currently pursuing the D.Sc. degree in electrical engineering.

From 2007 to 2008, he was a Substitute Lecturer with UNIFEI. He is currently an Entrepreneur acting on consulting in innovation, research and development. His research interests include industrial electronics, control systems, protection, and power quality.

DANIEL A. ARANTES received the B.S. degree in electronics engineering from Itajuba Federal University (UNIFEI), Itajuba, Brazil, in 2018, where he is currently pursuing the M.Sc. degree in electrical engineering.

He has experience with development of systems based on analog electronics and FPGAs/microcontrollers. His research interest includes analog and digital signal processing.



ISAC A. S. AREIAS received the B.S. and M.Sc. degrees in electrical engineering from Itajuba Federal University (UNIFEI), Itajuba, Brazil, in 2015 and 2019, respectively, where he is currently pursuing the D.Sc. degree in electrical engineering.

He has experience in power system protection and artificial intelligence. His research interests include condition-based maintenance of electric machinery, vibration analysis, and digital signal processing.

LUIZ E. BORGES-DA-SILVA (Life Senior Member, IEEE) received the B.S. and M.Sc. degrees in electrical engineering from Itajuba Federal University (UNIFEI), Itajuba, Brazil, in 1977 and 1982, respectively, and the Ph.D. degree from the Ecole Polytechnique de Montreal, Montreal, QC, Canada, in 1988.

He was a Visiting Professor with The University of Tennessee, Knoxville, TN, USA, in 1998. He is currently a Professor with the Department of Electronic Engineering, UNIFEI. His research interests include power electronics, electronic power systems, power converters, and applications of adaptive and intelligent control in industrial problems.

FABIO M. STEINER received the bachelor's degree in administration from the Candido Mendes University, Brazil, in 1991, and specializations in finance from IBMEC and in oil and gas business management from COPPE.

From 2003 to 2012, he was with the Brazilian National Electric System Operator (ONS—Operador Nacional do Sistema Eletrico). Since 2012, he has been with EDF Norte Fluminense, Brazil, as the Manager of Research and Development.