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Design and Analysis of a Multirate 5-bit High-Order 52 fs_{rms} $\Delta\sum$ Time-to-Digital Converter Implemented on 40 nm Altera Stratix IV FPGA

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ABSTRACT This paper describes FPGA implementation of a high-order continuous-time multi-stage noise-shaping (MASH) $\Delta\Sigma$ time-to-digital converter (TDC). The TDC is based on Gated Switched-Ring Oscillator (GSRO) and employs multirating technique to achieve improved performance over conventional $\Delta\Sigma$ TDCs. The proposed TDC has been implemented on an Altera Stratix IV FPGA development board. Dynamic and static tests were performed on the proposed design and experimental results demonstrate that it can perform its function without the need of calibration. The built-in clock circuitries of the FPGA board provides sampling clocks and operating frequencies of the GSROs. This work presents a 52 fs_{rms}, 89.7 dB dynamic range and 0.18 ps time-resolution at 200 MHz, 800 MHz, 1600 MHz sampling rate at the first, second and third stage, respectively, which demonstrate that the proposed third-order TDC can play an important role in applications such as ADPLLs and range finders in which accuracy and speed are vital.

INDEX TERMS Delta-sigma modulation, FPGA, gated switched-ring oscillator (GSRO), multirating technique, noise-shaping, time-to-digital converter (TDC).

I. INTRODUCTION

Measuring a time interval is a necessary step in various applications such as chemical sensors readout [1], biosensors [2], frequency synthesizers [3]–[6] and all-digital phase-locked loops (ADPLLs) [7] which is generally performed by time-to-digital converters (TDCs). Whether Nyquist rate or oversampling operation, TDCs critical performance parameters such as linearity, dynamic range and resolution are the main concern of designers to be improved [8]–[14]. Voltage-domain or time-domain $\Delta\sum$ TDCs benefiting from noise-shaping as an inherent property have become widely prevalent [15]–[19]. These structures not only unable to achieve a remarkable performance due to oversampling ratio (OSR) and noise-shaping order limitation, but also require calibration in most cases to compensate errors caused by disturbances such as frequency difference between stages which will consume higher power consumption and chip area on the system. Using Gated Switched-Ring Oscillator (GSRO) in a 1-1 MASH TDC eliminates the need of calibration and able to achieve finer time-resolution possible [20]. By increasing the order of noise-shaping we can decrease the power of in-band noise. Therefore, high-order $\Delta\sum$ TDC have been introduced by cascading of GSRO-TDCs and increasing the loop order using time-domain error-feedback filter [9], [21]. However, designing a high-order TDC requires stringent design considerations, higher complexity and increase power consumption. Hence, to enhance SNR a multirate FPGA-based second-order GSRO-TDC operating at higher sampling rates that achieves finer time-resolution has been proposed in [22].

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To reduce complexity and power consumption of the system a novel structure for 1-1 MASH Δ∑ TDC has been introduced in [23].

With the advent of high-performance FPGA chips and scaling of CMOS technology, fast and accurate FPGA-based and application specific integrated circuit (ASIC) TDCs have been introduced [24]–[30]. ASIC implementation has the advantages of design optimization, while the advantages of FPGA implementation is the flexibility which allows designer to provide a programmable design that can be tailored for a vast range of applications [31]. FPGA boards are very large. However, they are only used in the development phase. Once the design is confirmed, instead of the entire development board only the FPGA chip will be embedded in the system. Therefore, it can be said that the size of FPGA chip is almost the same as the ASIC IC while it is versatile to provide multiple operations and flexibility such as smart vehicles and drones.

This work presents a novel 5-bit third-order continuous-time ΔΣ TDC. Quantizers are based on GSRO and operates at high rates to achieve fine time-resolution. Multirating technique has been employed in this work to enhance the SNR which produce a high-performance Δ∑ TDC.

The remainder of this paper is organized as follows. Section II presents a background of multirate MASH Δ∑ GSRO-TDCs. The proposed third-order time-domain Δ∑ TDC is described in Section III. In Section IV implementation details are illustrated. Section V discusses the experimental results of the prototype TDC. Finally, conclusions are drawn in Section IV.

II. BACKGROUND

In a multirate 1-1 MASH TDC, *Start* and *Stop* pulses generate the input pulse using an edge-sensitive pulse generator (ESPG) to obtain a digital code from an input time interval. Supply and ground (SG) gates of the GSRO1 producing Y_1 are generally closed. The rising edges number of Y_1 is proportional to the input time interval. Inter-stage synchronizer (IntS Sync) unit controls SG gates of GSRO2 and synchronizes both GSROs operating frequency by producing the first stage quantization error pulse (Q_{EN}) and frequency sync pulse (Q_{IN}) in every cycle (Fig. 1). Quantization noise error of all stages are removed perfectly except the last stage. This process is carried out in digital cancellation filter (DCF) by shaping the overall quantization noise error by the noise transfer function (NTF) the order of which is the same as aggregate order of all stages. The overall digital output of the TDC (D_{OUT}) can be represented as:

$$D_{OUT} = z^{-1}Y_1 - \left(1 - z^{-1}\right)Y_2 = \frac{1}{2\pi}(\phi_{Q1}(z) - z\left(1 - z^{-1}\right)^2 \phi_{GSRO2}(z)) \quad (1)$$

By increasing the order of noise-shaping we can obtain higher SNR but at the expense of design complexity. In some cases, the improvement does not worth it. Moreover, stability of the system must be taken into consideration which can be problematic for the order of four and higher. Hence, based on targeted performance and available budget a suitable order is first defined by designers and followed by design improvement employing various techniques. Multirating technique has been introduced as an effective technique to enhance SNR in Δ∑ converters by increasing the OSR while not consuming too much power [32]. However, increasing the sampling frequency will increase the power consumption of the system. As the quantization noise error of the first stage is removed by DCF and has a negligible influence on the overall performance of the TDC, we maintain the same sampling frequency as conventional Δ∑ TDCs for the first stage to save power and increase the sampling frequency of higher stages to improve SNR. Employing this technique helps the designer to improve performance of converter by expanding the design space. Consequently, as our experimental results prove, operating at double sampling clocks costs only 7.44 % extra power consumption.

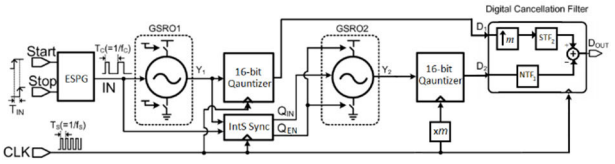

FIGURE 1. Employing multirating technique in a 1-1 MASH Δ∑ GSRO-TDC [22].

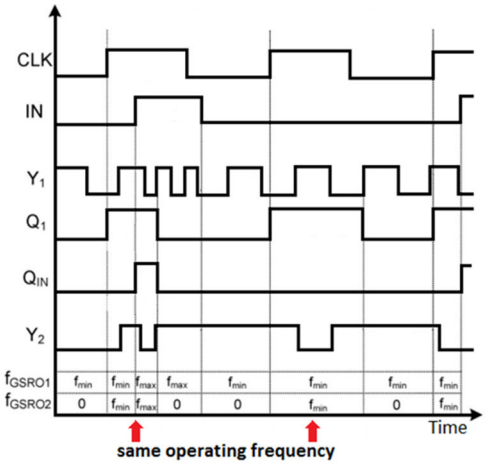

FIGURE 2. Timing diagram of multirate 1-1 MASH Δ∑ GSRO-TDC [22].

This technique in a 1-1 MASH Δ∑ TDC is shown in Fig. 1, and the timing diagram of the implementation is illustrated in Fig. 2. As shown, the sampling frequency of the second stage (f_{S2}) is higher than the sampling frequency of the first stage (f_{S1}) by the multirating coefficient (m) ($f_{S2} = m \times f_{S1}$). An N-stage MASH TDC which employs multirating technique has the overall NTF (NTF_{MR}) as given by:

$$NTF_{MR} = \prod_{1}^{N} (1 - z^{-\frac{OSR_1}{OSR_i}})^{n_i} \quad (2)$$

where n_i is the order of loop filter and OSR_i is the ith stage OSR. The NTF of a single-rate MASH TDC can be expressed as:

$$\mathrm{NTF_{SR}} = \prod_{1}^{N} (1 - z^{-1})^{n_i} \tag{3}$$

By comparing (2) with (3), it can be deduced that employing multirating technique results in the SQNR improvement compared with single-rate mode and can be estimated by:

$$\mathrm{SQNR_{MR-SR}} = \sum_{i=1}^{i=N-1} (2n_i 10log_{10}\left(\frac{OSR_i}{OSR_1}\right)) + (2n_N + 1)10log_{10}(\frac{OSR_N}{OSR_1}) \tag{4}$$

III. PROPOSED THIRD-ORDER GSRO-BASED $\Delta\sum$ TDC

This section proposes a new continuous-time third-order multirate $\Delta\sum$ GSRO-TDC architecture based on our previous design in [22] and [23]. We include a new static test on the proposed architecture on top of the dynamic test used in [26].

A. DESIGN PROCEDURE

Frequency differences between VCOs in a VCO-based MASH structure cause phase-domain quantization error leakage and hence the TDC cannot achieve desired order of noise shaping properly. To remedy this problem, we employ GSRO in all stages of our design. GSRO is basically a Switched-Ring Oscillator (SRO) with phase-holding gates at the supply and ground (Fig. 1). It emulates a SRO when the gates are closed and keeps its phase when they are open. Keeping phase in GSRO when SG gates are closed has a remarkable influence in avoiding leakage. Moreover, using Ints Sync unit for synchronizing GSROs operating frequency prevents any frequency difference between VCOs perfectly which results in precise operation of the proposed TDC without the need of any calibration while utilizing calibration unit to compensate the error is another possible solution which degrades the speed of the TDC and also imposes additional power consumption and chip area.

Generally, GSRO has three operating frequencies: f_{max}, f_{min} and 0. It is worth noting that as a residue pulse is required every cycle to accomplish second and higher-order of noise-shaping, designer must set frequency of the GSRO higher than sampling frequency (f_S) to guarantee existing minimum of one rising edge within a period of sampling. So, we can say that operating frequency of GSRO puts a limitation on OSR in GSRO-TDC. We set f_{max} and f_{min} of GSROs in this work at 4 GHz and 2 GHz, respectively. As a result, we can set f_{S1}, f_{S2}, and f_{S3} up to 2 GHz in this work that allows higher OSRs and achieving time-resolution below 0.5 ps.

On the one hand, using a high number of bits for quantization results in fine time-resolution. On the other hand, quantizers which have the most number of components are the most power hungry parts of the system. Hence, in order to avoid high power consumption we use a conventional small number of bits (5 bits) for quantizers in this work. Benefiting from all-digital structure and Multirating technique, this work can achieve high performance with this number of bits. Thus, it can be said that achieving a high performance TDC does not require a complex system.

The architecture of the proposed 1-1-1 MASH $\Delta\sum$ TDC is shown in Fig. 3. This work utilizes the same structure as the TDC in [22] and hence their operation principle are similar but an extra stage has been added to this work which increase the order of noise-shaping to third-order. Therefore, the accomplished steps for second-order noise-shaping is continued by producing Q_{EN} and Q_{IN} again by IntS Sync to control the GSRO3 and synchronize it with GSROs of the other stages. The third-order noise-shaping process is completed by filtering quantized output of three stages (D_1, D_2 and D_3) in digital cancellation filter.

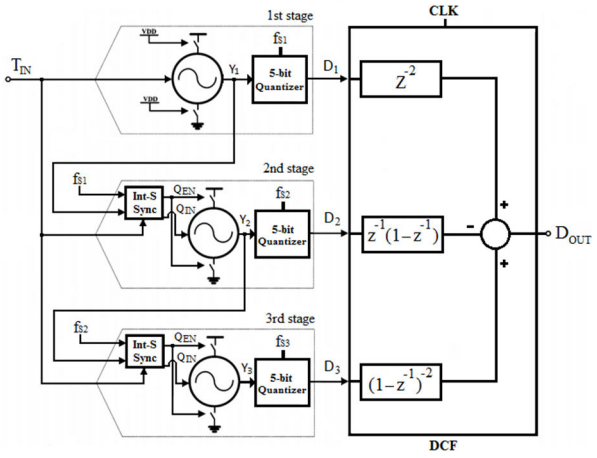

FIGURE 3. The proposed 1-1-1 MASH $\Delta\sum$ TDC architecture.

It should be mentioned that, since the sampling frequency of each stage is n times higher than the previous stage sampling frequency due to the multirating technique ($f_{S3} = n \times f_{S2}$ and $f_{S2} = n \times f_{S1}$), D_2 and $D_3$are up-sampled by multirating coefficient (n) in DCF. The overall output of the proposed 1-1-1 MASH TDC is given by:

$$\begin{aligned} D_{OUT} &= z^{-2}Y_1 - z^{-1}\left(1 - z^{-1}\right)Y_2 + \left(1 - z^{-1}\right)^2 Y_3 \\ &= \frac{1}{2\pi}(\phi_{Q1}(z) - z\left(1 - z^{-1}\right)^3 \phi_{GSRO3}(z)) \end{aligned} \tag{5}$$

Equation (5) shows that a third-order noise-shaping has been achieved by the proposed $\Delta\sum$ TDC.

B. DESIGN VERIFICATION

Detailed operation principle of the proposed design is illustrated in Fig. 4. First, the operation of the proposed TDC is evaluated with 1 ns and 4 ns input pulses at 100 MHz input frequency, 200 MHz f_{S1}, 400 MHz f_{S2} and 800 MHz f_{S3}. The result is shown in Fig. 4(a) and (b). It's evident that the control and synchronization of the GSROs are performed perfectly by IntS Sync unit in each sampling clock. As a result, we

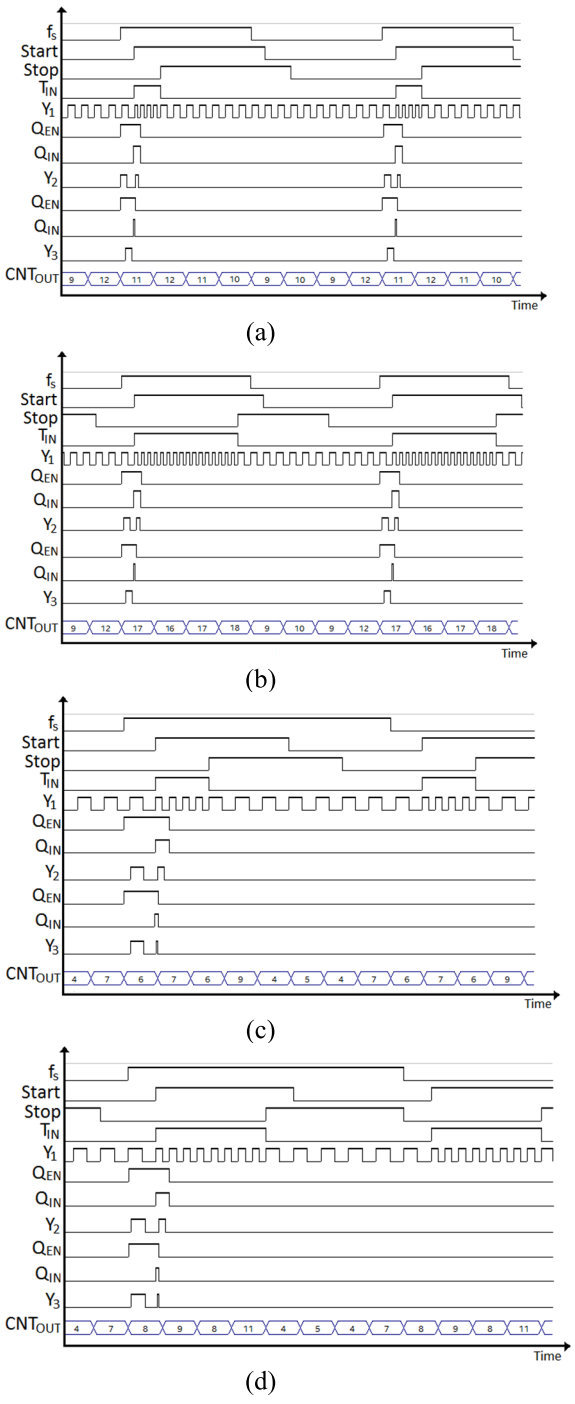

FIGURE 4. Operation principle of the proposed design in detail: (a) $f_S = 200$ MHz, $f_{S2} = 400$ MHz, $f_{S3} = 800$ MHz with $T_{IN} = 1$ ns, (b) $f_S = 200$ MHz, $f_{S2} = 400$ MHz, $f_{S3} = 800$ MHz with $T_{IN} = 4$ ns, (c) $f_{S1} = 200$ MHz, $f_{S2} = 800$ MHz, $f_{S3} = 1600$ MHz with $T_{IN} = 1$ ns, (d) $f_{S1} = 200$ MHz, $f_{S2} = 800$ MHz, $f_{S3} = 1600$ MHz with $T_{IN} = 2$ ns.

observe no quantization error leakage in this approach. Next, we evaluate the proposed TDC at 100 MHz input frequency, 200 MHz f_{S1}, 800 MHz f_{S2} and 1600 MHz f_{S3} for 1 ns and 2 ns input pulses to demonstrate the high frequency operation and the results are given in Fig. 4(c) and (d). Results shown in Fig. 4 demonstrate that the third-order Δ ∑ TDC performs its function and can be considered as a reliable choice to be incorporated in ADPLLs and Time-of-Flight systems for fast and precise applications.

IV. IMPLEMENTATION DETAILS

A. SAMPLING CLOCKS AND GSRO

The proposed architecture has been implemented on FPGA board utilizing the built-in oscillator and PLLs to establish the required clocks for TDC operation. We use the built-in 100 MHz crystal oscillator and PLLs of the FPGA board to extract different clocks (f_{S1}, f_{S2}, f_{S3}, f_{min} and f_{max}). The method of generating different clocks in the proposed TDC is shown in Fig. 5(a). As illustrated, f_{S1}, f_{min} and f_{max}, are obtained by multiplying 100 MHz input clock by 2, 20 and 40, respectively. f_{S2} and f_{S3} are obtained from the multiplication of f_{S1} by 4 and 8 as well. The GSROs is designed with a schematic shown in Fig. 5(b) such that if Q_{EN} is 0, for each state of Q_{IN} Y is 0. When Q_{EN} is 1 but Q_{IN} is 0 the output is f_{min}. If both Q_{EN} and Q_{IN} are 1 the unit passes f_{max} to the output. It is worth pointing out that this approach allows an easier measurement due to eliminating the need of any external source for providing sampling clocks.

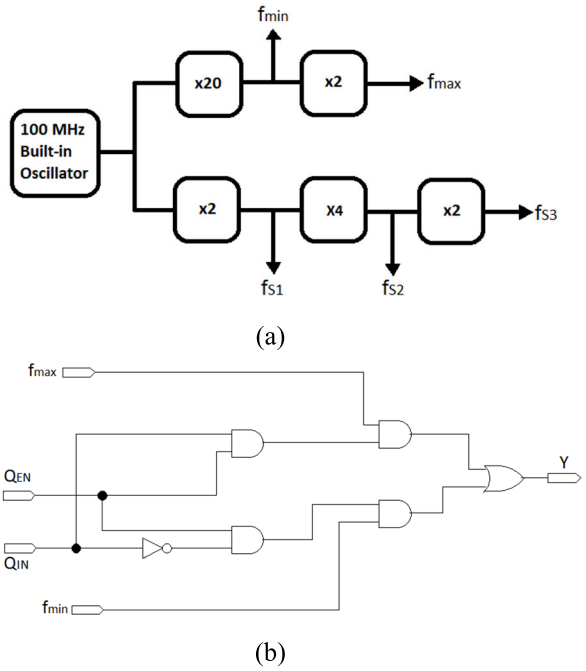

FIGURE 5. Generating different clocks in this work: (a) extracting all clocks from 100 MHz oscillator, (b) GSRO emulator unit.

B. INTER-STAGE SYNCRONIZER (INTS SYNC)

Accurate operation of MASH Δ ∑ GSRO-TDC demands a unit to synchronize operating frequency of two GSROs to prevent leakage. For this purpose, IntS Sync is exploited in the proposed TDC to produce Q_{EN} and Q_{IN} every cycle which performs synchronization as appropriated. Figs. 6(a) and (b) show the block diagram and timing diagram of this unit. As shown, this unit consists of an edge-sensitive pulse generator

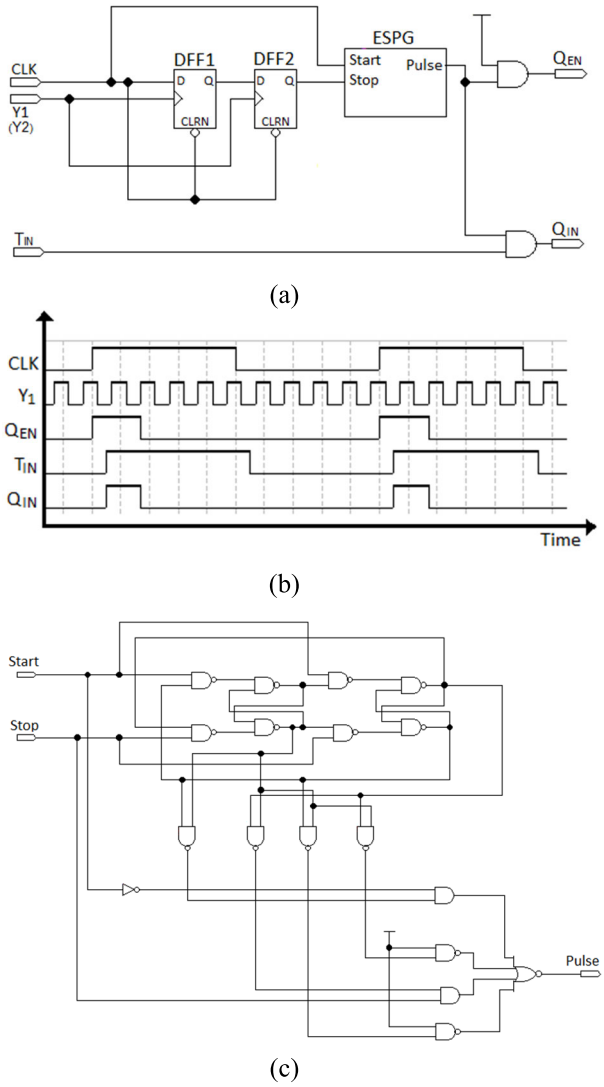

FIGURE 6. Inter-stage synchronizer (IntS Sync): (a) block diagram, (b) timing diagram, (c) implementation of the edge sensitive pulse generator (ESPG).

(ESPG), two DFFs and two AND gates. Fig. 6(c) depicts the schematic of ESPG. This block is used to produce a pulse with the width of interval between rising edges of *Start* and *Stop* pulses. The resulted Q_{EN} is fed to GSRO2 to enable it. It should be mentioned that if this pulse is narrower than rising time of the ESPG it would be ignored. Therefore, as switching time of GSRO gates is limited, a narrow Q_{EN} leads to a deadzone problem which declines the performance of the proposed TDC. However, the remedy of this problem is adding a static offset of 2π to Q_{EN} using *DFF2*. Digital cancellation filter removes this offset to prevent degradation of proficiency of the proposed 1-1-1 MASH $\Delta\sum$ TDC.

C. THE 5-BIT QUANTIZER

We use built-in counters and logic components of the FPGA board to build a 5-bit quantizer to quantize Y_1, Y_2 and Y_3 at every cycle. However, coinciding the reset time of the counter

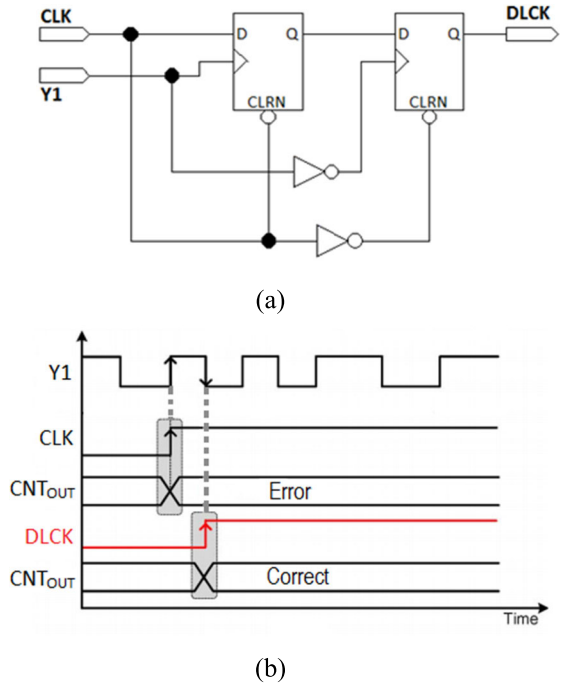

FIGURE 7. Avoiding error by delaying rising edge of *CLK*: (a) schematic, (b) timing diagram.

with rising edge of f_S is an error that must be avoided during operation of 5-bit quantizer. Nevertheless, we can prevent this error if rising edge of *CLK* is postponed until transition of counter output (CNT_{out}) has completed. For this purpose, a simple digital unit depicted in Fig. 7(a). Fig. 7(b) illustrates that the mentioned error can be suppressed properly by using this approach [20].

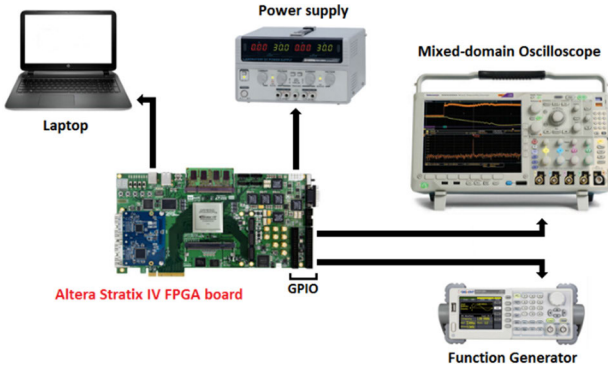

FIGURE 8. Dynamic test measurement setup.

V. EXPERIMENTAL RESULTS AND DISCUSSION

We implemented the prototype TDC on an Altera Stratix IV FPGA development board. Input pulses (T_{IN}) are applied to general purpose I/O (GPIO) port of FPGA board and digital output (D_{OUT}) is obtained from the same port. Regarding the I/O standard of Altera Stratix IV FPGA board, 3V 1MHz input pulses provided by a function generator (Siglent SDG 1050) are applied to the proposed TDC to attain the output spectrum. Then, a mixed-domain oscilloscope (Tektronix

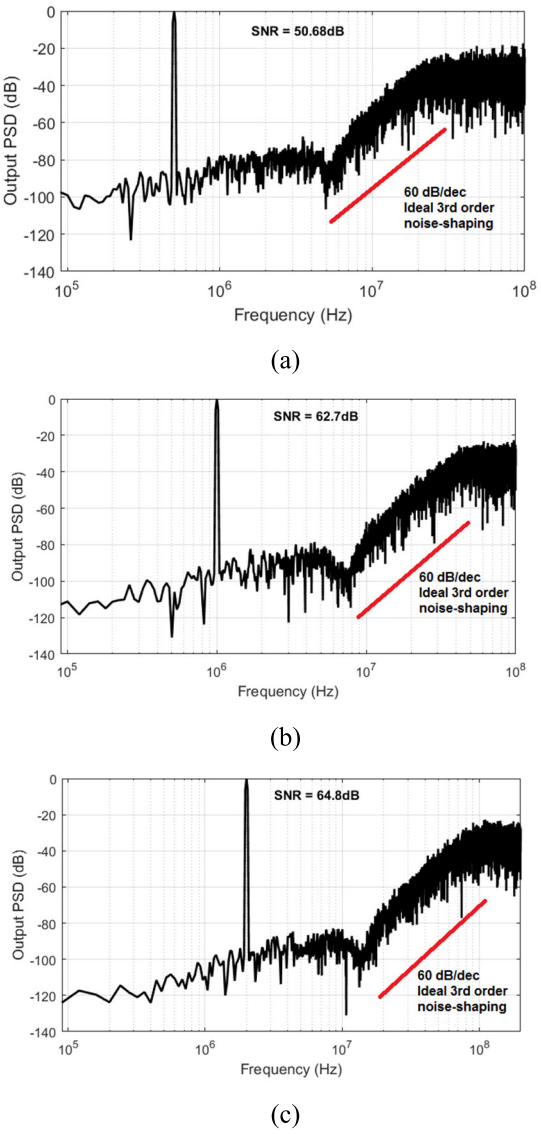

FIGURE 9. Output spectrum of the proposed TDC: (a) $f_{S1} = f_{S2} = f_{S3} = 200$ MHz, (b) $f_{S1} = 200$ MHz, $f_{S2} = 400$ MHz and $f_{S3} = 800$ MHz, (c) $f_{S1} = 200$ MHz, $f_{S2} = 800$ MHz and $f_{S3} = 1600$ MHz.

MDO 4104) with a Hann window captures 100-k samples. Finally, MATLAB is used for post-processing of the samples. Fig. 8 illustrates the measurement setup for the prototype TDC. The FPGA board control panel shows that the used resources in this work are 5 PLLs, 2 MB block memory bits and total of 311 registers.

We investigate two types of measurements to the proposed design for test and evaluation purposes. First, we perform dynamic test to verify the frequency-domain behavior of the proposed TDC and achieving the appropriated order of noise-shaping. The measured output spectrum of this work is shown in Fig. 9 for three cases. Fig. 9 (a) demonstrates third-order noise-shaping for single-rate mode at 200 MHz sampling rate for every stages and at 100 MHz input frequency (f_C). In this case the obtained SNR was 50.68 dB within 9.4 MHz

TABLE 1. Dynamic test results of the proposed architecture.

	Single-rate	Multirate1	Multirate2
T_{range} (ns)	4.5	4.5	4.5
f_{BW} (MHz)	9.4	9.6	9.9
	200	200	200
	-	-	-
f_S (MHz)	200	400	800
	-	-	-
	200	800	1600
DR (dB)	82.1	87.6	89.7
$T_{int,rms}$ ($f_{s,rms}$)[1]	125	66	52
SNR (dB)	50.68	62.7	64.8
Resolution (ps)[2]	0.43	0.23	0.18
Power[3] (mW)	8.2	8.6	9.24
FoM (dB)[4]	172.7	178	180

[1] Estimated integrated noise ($\sqrt{Resolution^2/12}$).

[2] Estimated resolution ($\sqrt{T_{int,rms}{}^2 . 12}$).

[3] FPGA core power consumption.

[4] FoM = DR + 10 $\log_{10}$ (Bandwidth / Power) [dB], where $DR = 20\ log_{10}(T_{range,rms}/T_{int,rms})$.

bandwidth. After making sure the proper operation of the proposed design, the advantage of employing multirating technique was verified by multiplying the second and third stages sampling rates. In this regard, we multiplied f_{S2} and f_{S3} by 2 and 4, respectively. The output spectrum of this case is depicted in Fig. 9 (b). As expected, we observe 12.02 dB enhancement in SNR and 200 KHz in bandwidth over single-rate mode.

Equation (4) shows that the benefits captured from multirating technique can be enhanced by increasing oversampling ratio. Thus, we applied higher sampling frequencies by doubling f_{S2} and f_{S3} compared to previous values ($f_{S1} = 200$ MHz, $f_{S2} = 800$ MHz and $f_{S3} = 1600$ MHz). Fig. 9 (c) shows the measured output spectrum for this case in which we can observe enhancement in SNR and bandwidth by 2.1 dB and 300 KHz, respectively. This enhancement costs only 0.64 mW more power consumption owing to extra switching of GSROs while improves the Figure-of-Merit (FoM) by 2 dB. This inconsiderable amount of increase in power consumption shows that it is quantizers which consume the most power in the proposed TDC due to the most number of constituent parts (counters, registers, subtractors and other logic gates) while even double switching of the GSROs and sampling rate have a slight impact on the overall power consumption. It should be noted that as the whole system was implemented on-chip on the FPGA, the core power consumption mentioned in the Tables comprises all constituent units of the proposed structure including clock circuitries such as oscillators and PLLs. Additionally, this work demonstrates 0.18 ps time-resolution and 10.47 effective number of bits (ENOB). These results are summarized and compared in Table 1 to highlight enhancement resulted from the multirating technique and increasing the oversampling ratio.

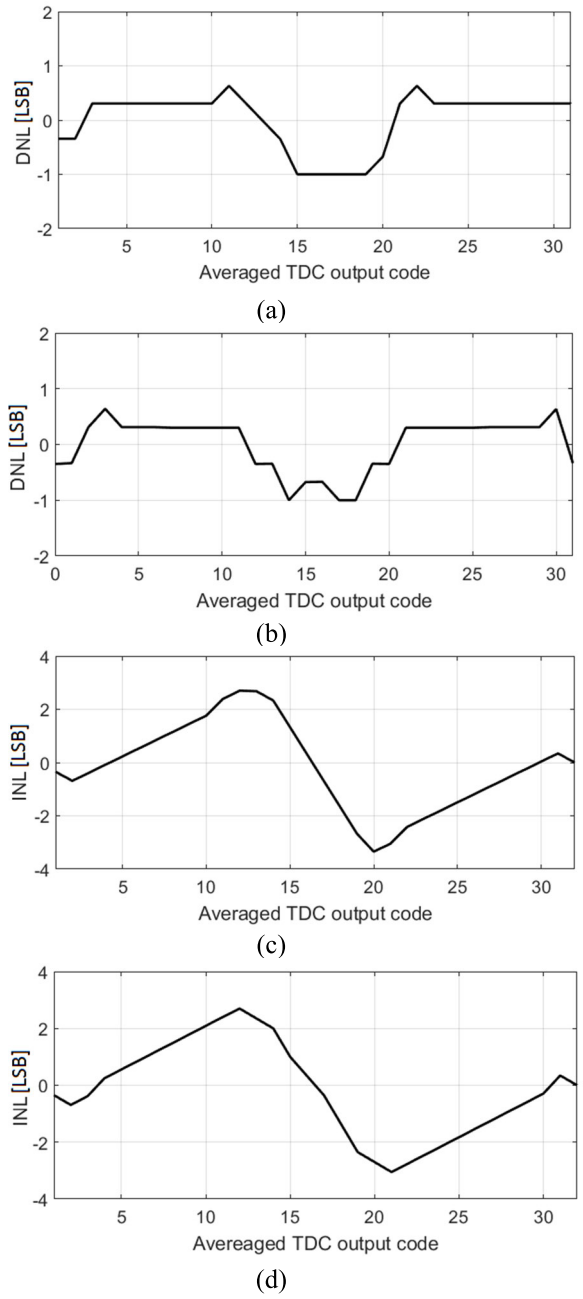

FIGURE 10. Static test results: (a) DNL of the 1-1 MASH structure (b) DNL of the 1-1-1 MASH structure (c) INL of the 1-1 MASH structure (d) INL of the 1-1-1 MASH structure.

Dynamic test cannot be used to measure linearity of a TDC since it's difficult to generate a high linearity phase modulated input [20]. Thus, in order to investigate the linearity of this work, we perform a static test to the proposed design where a ramp input are applied to the TDC. We generate the ramp input by applying 99.999 MHz and 100 MHz signals to the *Start* and *Stop* input of the proposed TDC, respectively. Differential non-linearity (DNL) and integral non-linearity (INL) of the proposed design for 1-1 and 1-1-1 MASH structure are shown in Fig. 10. As can be seen, the maximum INL of the second-order TDC is 3.2 LSB while the third-order TDC shows maximum INL of 3 LSB. By comparing Fig. 10 (c) with Fig. 10 (d), it can be seen that increasing the order of noise-shaping and employing multirating do not affect the linearity while their influence on improving the frequency-domain operation of a $\Delta\sum$ TDC is significant.

TABLE 2. Performance summary and comparison with other state-of-the art $\Delta\sum$ TDCs.

	[24]	[34]	[33]	[20]	[22]	This work	
Process (nm)	65	40	65	65	40 FPGA	**40 FPGA**	
Shaping order	2	3	3	2	2	**2**	
T_{range} (ns)	4.5	0.32	2	4	4.5	**4.5**	
f_{BW} (MHz)	2.5	2.5	1	4	9.6	**9.6**	**9.9**
f_S (MHz)	205	50	250	400	400 - 1600	**200 - 400 - 800**	**200 - 800 - 1600**
DR (dB)	52.55	66.76	80.8	79.6	86.2	**87.6**	**89.7**
$T_{int,rms}$ ($f_{s,rms}$)[1]	3753	147	182	148	78	**66**	**52**
SNR (dB)	56	N/A	N/A	N/A	61.02	**62.7**	**64.8**
Resolution (ps)[2]	13	0.51	0.63	0.51	0.27	**0.23**	**.018**
Power (mW)	0.63	1.32	8.4	6.72	7.84[3]	**8.6[3]**	**9.24[3]**
FoM (dB)[4]	148.5	159.5	161.6	167	177	**178**	**180**

[1] Estimated integrated noise ($\sqrt{Resolution^2/12}$).

[2] Estimated resolution ($\sqrt{T_{int,rms}{}^2 . 12}$).

[3] FPGA core power consumption.

[4] FoM = DR + 10 $\log_{10}$ (Bandwidth / Power) [dB], where $DR = 20\ log_{10}(T_{range,rms}/T_{int,rms})$.

Table 2 presents the experimental results of this work and a comparison with the recent state-of-the-art $\Delta\sum$ TDCs. As expected, this work reveals higher SNR in comparison with the 1-1 MASH TDC in [22] at the expense of a slight extra power consumption. Time-resolution is a function of the measured integrated noise ($T_{int,rms}$) [20]. Hence, we can say that the less measured integrated noise, the finer the time resolution is. Therefore, benefiting from multirating technique and third-order noise-shaping simultaneously, this work yields the lowest measured integrated noise and finest time resolution as shown in the Table 2. Another important parameter that is related to the measured integrated noise is dynamic range (DR) which can be interpreted as noise immunity of TDC over detection range and hence determines the shortest detectable time interval. Based on Table 2, superior DR belongs to the proposed third-order TDC compared to other works.

This work also demonstrates the superior FoM in the Table while in order to have a fair comparison, the FoM of this work was calculated with the power consumption considering the entire constituent units of the system including oscillators, PLLs and other utilized equipment of the FPGA board. It should be highlighted that the mentioned improvements have been achieved while this work utilizes lower number of bits for quantization. Thus, it can be inferred that superiority of the proposed design over previous works is due to

the optimization of all-digital design rather than increasing the number of bits that will increase the complexity of the design. In order to overcome the constraints of increasing the noise-shaping order we employ Multirating technique in the proposed structure which expands the design space and helps achieving higher SNR with lower hardware and complexity. Moreover, designing the proposed architecture using all-digital units and operating in time-domain facilitate benefiting from CMOS technology scaling and implementing that totally on-chip on the 40 nm Altera Stratix IV FPGA which subsequently result in a remarkable performance. It should be noted that this work is the first all-digital high-order FPGA-based $\Delta\sum$ TDC employing multirating presented so far.

VI. CONCLUSION

In this paper, a 5-bit time-domain multirate $\Delta\sum$ TDC with 1-1-1 MASH structure is presented. The advantages of using GSRO-based quantizers has been improved by employing multirating technique in this work. The prototype of the proposed design is implemented on a 40-nm Altera Stratix VI FPGA and verified through dynamic and static tests. Experimental results show 52 fs$_{\text{rms}}$ measured integrated noise, 0.18 ps time-resolution, 89.7 dB DR and 3 LSB INL. Demonstrating 180 dB FoM with 9.24 mW total power consumption along with the mentioned results imply competency of this work for applications such as smart vehicles and biosensors. Finally, we suggest incorporating extra cascaded stages to the proposed structure to improve performance further by constituting multirate $\Delta\sum$ TDCs with higher-order of noise-shaping for future works.

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