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Comparative Analysis and Energy-Efficient Write Scheme of Ferroelectric FET-Based Memory Cells

DONG HAN KO, (Graduate Student Member, IEEE), TAE WOO OH, (Graduate Student Member, IEEE), SEHEE LIM, (Graduate Student Member, IEEE), SE KEON KIM, (Graduate Student Member, IEEE), AND SEONG-OOK JUNG, (Senior Member, IEEE)
School of Electrical and Electronic Engineering, Yonsei University, Seoul 03722, South Korea

Corresponding author: Seong-Ook Jung (sjung@yonsei.ac.kr)

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ABSTRACT The ferroelectric field-effect transistor (FeFET) is one of the most promising candidates for emerging nonvolatile memory devices owing to its low write energy and high I_{ON}/I_{OFF} ratio. For FeFET applications as nonvolatile memory devices, 1FeFET, 1T-1FeFET, 2T-1FeFET, and 3T-1FeFET cells have been proposed. The 1FeFET cell exhibits the highest density but suffers from write disturbance. Although the 1T-1FeFET and 2T-1FeFET cells resolve the write disturbance, they use a write scheme with a negative write voltage (V_W), which requires voltage swings of many control signals, leading to a significantly high write energy consumption. The 3T-1FeFET cell uses a write scheme without a negative V_W; however, it exhibits the largest area overhead. Although the 1T-1FeFET cell resolves the write disturbance with a small area overhead; however, it exhibits high write energy consumption because of the use of a negative V_W. In this paper, to significantly reduce the write energy consumption, we propose a less control signal swing (LCSS) write scheme without using a negative V_W. Simulation results indicate that the worst, average, and best cases of the proposed LCSS write scheme can achieve 35%, 66%, and 96% lower write energy consumption, respectively, than the write scheme with a negative V_W in the 1T-1FeFET cell. We also identify the available sensing schemes for each FeFET cell in the read operation according to the FeFET threshold voltage distribution.

INDEX TERMS Control signal swing, ferroelectric field-effect transistor, hysteresis, nonvolatile memory, write disturbance.

I. INTRODUCTION

In the past decades, static and dynamic random-access memory (SRAM and DRAM, respectively) have been conventionally used as cache and main memory, respectively. The technology has been scaled down to satisfy the demand for a high memory density, a high speed, and low power dissipation [1], [2]. However, process variation makes technology scaling difficult [3]–[9]. Moreover, technology scaling causes a high leakage power in SRAM and DRAM [10], [11].

To overcome these limitations, researchers have developed emerging nonvolatile memory devices that have zero-leakage power, high-density, and high-scalability characteristics. Because of these characteristics, emerging nonvolatile devices are suitable for use as Internet of Things devices and in data-intensive applications such as edge computing and artificial-intelligence hardware devices.

In this context, nonvolatile memory devices such as phase-change memory (PCM), spin-transfer torque magnetic random-access memory (STT-RAM), and resistive random-access memory (ReRAM) have been studied. However, these memory devices face the following challenges. Because they use a current-based write scheme, a high write current flows during the write operation, which causes high write energy consumption [12]. Additionally, they have a low I_{ON}/I_{OFF} ratio, which causes a low read sensing margin [13]–[15]. The ferroelectric field-effect transistor (FeFET), which is a promising emerging nonvolatile memory device, can overcome these challenges. First, because the ferroelectric (FE) layer polarization is switched by the gate-to-source

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voltage (V_{GS}), a write current rarely flows during the write operation [16]. Most of the write energy is consumed by charge trapping and capacitor charging [17], [18]. Moreover, the FE layer in an FeFET has a fast switching time [19]. Therefore, the FeFET exhibits a low write energy consumption. Second, the FeFET has a high I_{ON}/I_{OFF} ratio [19], [20], leading to a high read-sensing margin.

To use the FeFET as a nonvolatile memory device, various FeFET cell structures have been proposed: 1FeFET [21], 1T-1FeFET [22], 2T-1FeFET [23], and 3T-1FeFET [24]. Each structure has advantages and limitations. The 1FeFET cell exhibits the highest density. However, it suffers from write disturbance in the array structure owing to the absence of an access transistor. To alleviate the write disturbance, the write voltage (V_W)/2 and V_W/3 inhibition bias (IB) schemes were proposed in [21], [25]; however, they still have the probability of write disturbance. In the 1T-1FeFET cell, one access transistor is added to the gate of the FeFET. This transistor allows selected and unselected rows to be distinguished; thus, the write disturbance problem can be solved. In the 2T-1FeFET cell, an additional access transistor is added at the drain of the FeFET. Thus, the 2T-1FeFET cell can read by selecting bits during the read operation. Moreover, the 1T-1FeFET and 2T-1FeFET cells use a write scheme with a negative write voltage (V_W). This causes increased control signal swing to prevent write disturbance in unselected rows. Thus, this write scheme exhibits a higher write energy consumption than the write scheme without a negative V_W. Additionally, in the 1FeFET, 1T-1FeFET, and 2T-1FeFET cells, the available sensing scheme varies according to the FeFET threshold voltage (V_{TH}) distribution because there is no access transistor at the FeFET source to block the sneak-current path. In the 3T-1FeFET cell, an additional access transistor is added at the source of the FeFET. Because the 3T-1FeFET cell uses a write scheme without a negative V_W, it exhibits a lower write energy consumption. Furthermore, both current- and voltage-based sensing schemes can be used regardless of the V_{TH} distribution. However, because three access transistors are used, the 3T-1FeFET cell exhibits the largest area overhead.

In this study, we comprehensively analyzed previous FeFET memory cells in terms of area, write scheme, and sensing scheme. Among these, the analyzed 1T-1FeFET cell not only solves the write disturbance problem but also exhibits a small area overhead. However, it also exhibits a high write energy consumption because it uses a negative V_W. To reduce the write energy consumption of the 1T-1FeFET cell, we propose a less control signal swing (LCSS) write scheme without using a negative V_W. Additionally, we analyzed the available sensing schemes in array structures according to V_{TH} distribution in the FeFET.

The remainder of this paper is organized as follows. The FeFET device characteristics, write and sensing schemes, and simulation model are introduced in Section II. Previous FeFET memory cells are reviewed in Section III. The characteristics and operation of the proposed LCSS write scheme are presented in Section IV, along with an analysis of the available sensing schemes based on the V_{TH} distribution in the FeFET. Previous FeFET memory cells are comprehensively analyzed in Section V; additionally, in this section, the proposed LCSS write scheme is compared with previous write schemes. Finally, Section VI concludes the paper.

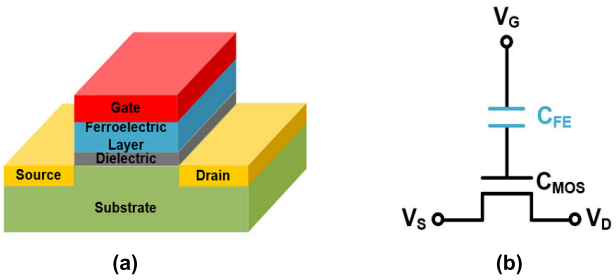

FIGURE 1. FeFET (a) structure and (b) equivalent circuit.

II. BACKGROUND

A. FeFET STRUCTURE AND CHARACTERISTICS

The FeFET structure is similar to that of a metal–oxide–semiconductor field-effect transistor (MOSFET). The difference is that in an FeFET, an FE layer is added between the gate metal and dielectric layer, as shown in Fig. 1(a). Additionally, the FeFET equivalent circuit structure has an FE-layer capacitance (C_{FE}) coupled with a MOSFET capacitance (C_{MOS}), as illustrated in Fig. 1(b). Because of the coupled capacitance (C_{FE} and C_{MOS}), an FeFET can be used as a nonvolatile memory device that exhibits hysteresis behavior based on the V_{GS} with a sufficient FE-layer thickness [20], [26]–[28]. The FeFET V_{TH} depends on its polarization state, which can be either the high V_{TH} (HVT) state corresponding to logic "0" or the low V_{TH} (LVT) state corresponding to logic "1." When a positive V_{GS} is applied to the FeFET, the polarization direction points to the channel. This causes electrons in the substrate to form a channel, which reduces the V_{TH}. Conversely, when a negative V_{GS} is applied to the FeFET, the polarization direction points to the gate metal. This prohibits the electrons in the substrate from forming a channel, which increases the V_{TH}.

B. FeFET WRITE AND SENSING SCHEMES

Based on the use of a negative voltage source, the FeFET write scheme can be divided into write schemes with and without a negative V_W [20], [24]. In the write scheme with a negative V_W, the source of the FeFET is driven to ground (GND), and its gate is driven to a positive or negative V_W, as shown in Fig. 2(a). In the write scheme without a negative V_W, the write data "1" operation is the same as that for the write scheme with a negative V_W. When writing the data "0" the source of the FeFET is driven to the positive V_W, and the gate is driven to GND to apply a negative V_{GS} without a negative V_W, as shown in Fig. 2(b).

The FeFET sensing schemes are illustrated in Fig. 3. The gate of the FeFET is driven to the gate read voltage (V_{GREAD}).

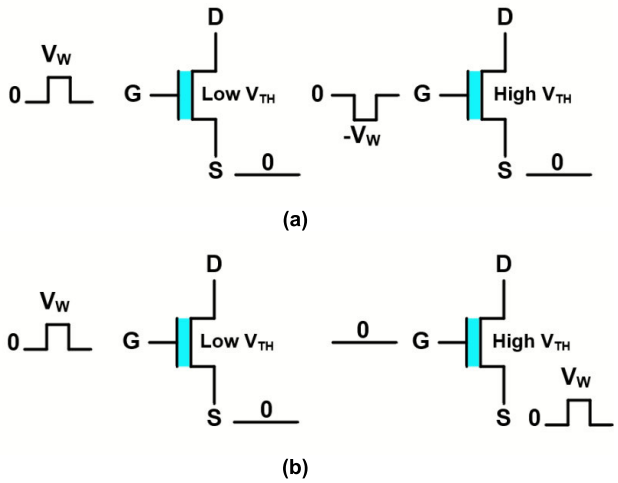

FIGURE 2. FeFET write schemes (a) with and (b) without a negative V_W [20], [24].

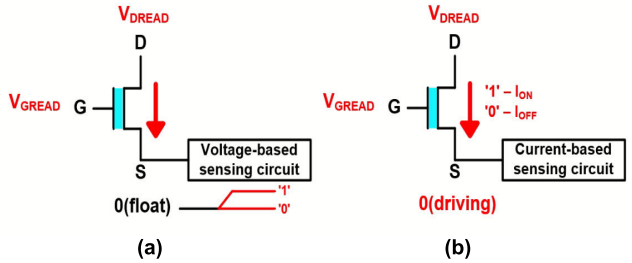

FIGURE 3. (a) Voltage- and (b) current-based FeFET sensing schemes.

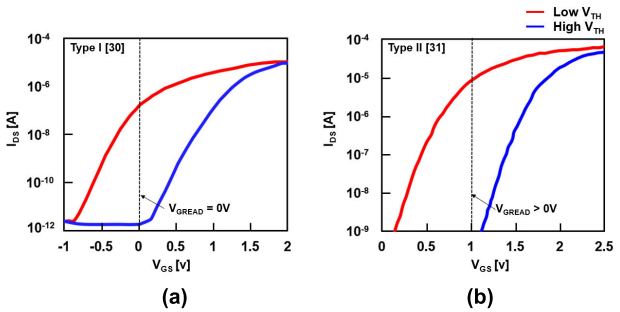

FIGURE 4. I_{DS} versus V_{GS} characteristics of the FeFET: (a) I_{DS}–V_{GS} curve of a type-I FeFET: experimentally measured data for a fabricated FeFET [30]; (b) I_{DS}–V_{GS} curve of a type-II FeFET: experimentally measured data for a fabricated FeFET [31].

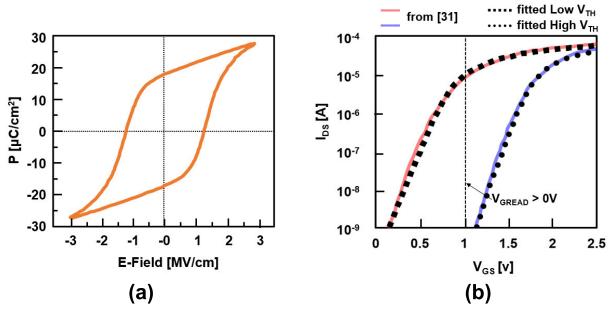

FIGURE 5. (a) Polarization versus electric field (P–E) hysteresis curve of a fabricated FeFET [31]. (b) Fitted I_{DS}–V_{GS} curves of a type-II FeFET (black dotted lines). The fitting was based on experimentally measured data for the fabricated FeFET (represented by red and blue solid lines) [31].

V_{GREAD} has a value within the memory window and is used for distinguishing the LVT and HVT states. When the drain of the FeFET is driven to the drain read voltage (V_{DREAD}), the I_{ON}/I_{OFF} current flows according to the stored data in the FeFET. This I_{ON}/I_{OFF} current can be sensed by the voltage- or current-based sensing scheme. When the source of the FeFET is floated to GND, the voltage of the source is altered by the I_{ON}/I_{OFF} current, and this is sensed by the voltage-based sensing circuit. When the source of the FeFET is driven to GND, the I_{ON}/I_{OFF} current is sensed by the current-based sensing circuit.

Previous FeFET memory cell structures use various write and sensing schemes. In Section III, we examine the advantages and disadvantages of these write and sensing schemes at the array level.

C. FeFET MODELING FOR SIMULATION

The V_{TH} of the FeFET can be shifted through body biasing or gate metal engineering [19], [28], [29]. Fig. 4 presents the drain–source current (I_{DS}) versus V_{GS} curves of FeFETs with different V_{TH} distributions [30], [31]. In this study, we divide FeFETs into two types according to the V_{TH} distribution: type-I has a negative LVT, whereas type-II has a positive LVT. These two FeFET types use 0 V and a voltage higher than 0 V as V_{GREAD}, respectively. Additionally, the available sensing scheme is determined by the V_{TH} distribution. When the FeFET has a positive LVT (type-II), both sensing schemes (current- and voltage based) can be used in all FeFET cells. This is discussed in detail in Section III.

In this study, we performed HSPICE simulations based on industry-compatible 28 nm complementary metal–oxide–semiconductor (CMOS) technology. The FeFET model used for the simulations is based on the type-II FeFET. Figs. 5(a) and (b), respectively, present the measured polarization versus electric field (P-E) hysteresis and I_{DS}–V_{GS} curves (red and blue solid lines) of a fabricated FeFET device with a 10 nm-thick Si:HfO_2 [31]. The FeFET model used in this study was fitted using a predictive technology model (PTM) [32] to mimic the measured I_{DS}–V_{GS} curves (red and blue solid lines) in Fig. 5(b). The fitting was performed by adjusting the PTM parameters values related to I_{ON}/I_{OFF}, V_{TH}, and the subthreshold slope. The black dotted lines in Fig. 5(b) represent the fitted I_{DS}–V_{GS} curves obtained using the FeFET model. According to the constant-current criteria (800 nA), the V_{TH} values for the LVT and HVT states in the fitted FeFET model are 0.67 and 1.58 V, respectively. Because V_{GREAD} is 1 V in the read simulation, the I_{ON} value was adjusted when V_{GS} in the fabricated FeFET device is 1 V. The V_{TH} and I_{ON}/I_{OFF} values obtained with the fitted FeFET model are within a 3% error range of those obtained in [31].

TABLE 1. Control signal information for the 1FeFET, 1T-1FeFET, 2T-1FeFET and 3T-1FeFET cells.

Cell	1FeFET				1T-1FeFET			2T-1FeFET			3T-1FeFET		
Operation	Hold	Write Phase 1	Write Phase 2	Read	Hold	Write	Read	Hold	Write	Read	Hold	Write	Read
WL (selected)	0	$-V_W$[a] ($-V_W$[b])	V_W (V_W)	V_{GREAD}	0	V_W	V_{DD}	0	V_W	V_{DD}	0	V_W	V_{DD}
WL (unselected)		$-V_W/2$ ($-V_W/3$)	$V_W/2$ ($V_W/3$)	0		$-V_W$	0		$-V_W$	0		0	0
BL (write '1')	0	$-V_W/2$ ($-2V_W/3$)	0	V_{DREAD}	0	V_W	V_{GREAD}	0	V_W	V_{GREAD}	0	V_W	V_{GREAD}
BL (write '0')		0	$V_W/2$ ($2V_W/3$)			$-V_W$			$-V_W$			0	
SL (write '1')	0	$-V_W/2$ ($-2V_W/3$)	0	0	0	0	0	0	0	0	0	V_W	V_{DD}
SL (write '0')		0	$V_W/2$ ($2V_W/3$)									0	0
RL (selected)	-				0	0	V_{DREAD}	0	0	V_{DREAD}	0	0	V_{DREAD}
RL (unselected)							0			0			0
DL	-				-			0	0	V_{DD}	0	0	V_{DD}
SSL (selected)	-				-			-			0	V_W	V_{DD}
SSL (unselected)												0	0

[a] $V_W/2$ IB scheme.
[b] $V_W/3$ IB scheme.

III. PREVIOUS FeFET MEMORY CELLS

The 1FeFET, 1T-1FeFET, 2T-1FeFET, and 3T-1FeFET memory cells were proposed in [21]–[23], and [24], respectively. Each cell uses its own write and sensing schemes according to the access transistor position. In this section, we review the structure and operation of these FeFET memory cells. The FeFET memory cells are in hold operation when they are neither in write nor read operation. In hold operation, the FeFET memory cell needs to maintain the stored data. This can be achieved by setting all control signals to 0 to make the FeFET V_{GS}s in all memory cells 0. The control signal information for all FeFET memory cells is presented in Table 1.

A. 1FeFET CELL

The 1FeFET cell has the highest density; however, it suffers from write disturbance owing to the absence of an access transistor. To alleviate the write disturbance, the $V_W/2$ and $V_W/3$ IB schemes were proposed in [21], [25]; however, they still have the probability of write disturbance.

The write operation of the 1FeFET cell is presented in Figs. 6(a) and (b). The write operation occurs in two phases. In phase 1, the data "0" are written to the cells in which data "0" are intended to be written, and in phase 2, the data "1" are written to the cells in which data "1" are intended to be written. Phase 1, which begins as the word line (WL) in the selected row, is set to $-V_W$ and the unselected WLs are set to $-V_W/2$ ($-V_W/3$). The bit and sense lines (BLs and SLs, respectively) in unselected cells are set to $-V_W/2$ ($-2V_W/3$) in the $V_W/2$ ($V_W/3$) IB scheme.

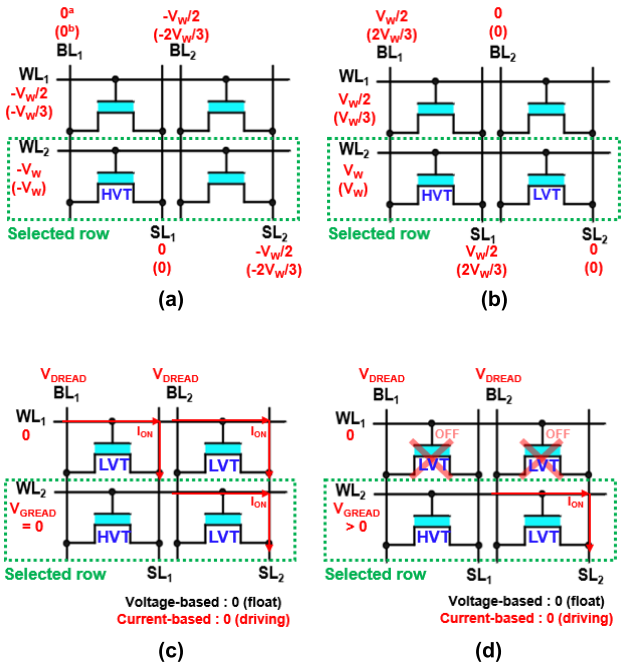

FIGURE 6. Array structure (2 × 2) of the 1FeFET cell: (a) write phase 1 and (b) write phase 2 ([a] $V_W/2$ IB and [b] $V_W/3$ IB schemes). Read operation of (c) type-I and (d) type-II FeFETs.

In phase 2, the selected WL is set to V_W, and the unselected WLs are set to $V_W/2$ ($V_W/3$). The BLs and SLs in unselected cells are set to $V_W/2$ ($2V_W/3$) in the $V_W/2$ ($V_W/3$) IB scheme.

Although both schemes were proposed to reduce the write disturbance, they are unable to completely solve the problem.

In the $V_W/2$ IB scheme, the disturbance voltage $V_W/2$ is applied to the half-selected cells, where either the WL or the BL and SL are selected. In the $V_W/3$ IB scheme, the disturbance voltage $V_W/3$ is applied to all cells except the selected cells. Although a low-level disturbance voltage occurs in the $V_W/3$ IB scheme, the number of disturbed cells and the routing cost increase owing to the large number of required voltage sources, such as $\pm V_W/3$, $\pm 2V_W/3$, and $\pm V_W$. Additionally, the swing of all BLs, SLs, and WLs occurs during the write operation, leading to high write energy consumption.

The available sensing scheme depends on the type of FeFET. The read operation of the 1FeFET cell is presented in Figs. 6(c) and (d). In the type-I FeFET, all BLs are set to V_{DREAD}, and the selected WL is set to V_{GREAD} (=0). Thereafter, the SL is floated to GND in a voltage-based sensing scheme or driven to GND in a current-based sensing scheme during the read operation. Because the LVT of the type-I FeFET is negative and the unselected WLs are set to GND during the read operation, the FeFETs in the LVT state in unselected rows are turned on. Thus, the read current flows from the unselected rows to the SL of the selected cell. Furthermore, in the 1FeFET cell, there is no access transistor at the source of the FeFET that can prevent the current path. Therefore, it is impossible to read the data in the selected row under both the voltage- and current-based sensing schemes. In the type-II FeFET, the selected WL is set to V_{GREAD} (a positive value), and the other control signals are assigned similar values to those in the type-I FeFET. Because the gate of the FeFET in the unselected rows is set to GND, the FeFETs in the unselected rows are completely turned off. Therefore, the read current does not flow to unselected rows, and both sensing schemes can be used in the type-II 1FeFET cell.

B. 1T-1FeFET CELL

The 1T-1FeFET cell has an access transistor at the gate of the FeFET, which can address the write disturbance problem by distinguishing between the selected and unselected rows.

The write operation of the 1T-1FeFET cell is presented in Fig. 7(a). The 1T-1FeFET cell uses a write scheme with a negative V_W. The write operation begins as the selected WL is set to V_W, and the unselected WLs are set to $-V_W$. Thereafter, BLs that write data "1" and "0" are set to V_W and $-V_W$, respectively. In the write scheme with a negative V_W, the unselected WLs must be set to $-V_W$ to prevent write disturbance to cells in unselected rows. Additionally, the swing of all BLs occurs during the write operation, leading to high write energy consumption.

The available sensing scheme also depends on the type of FeFET for the 1T-1FeFET cell. The current- and voltage-based sensing scheme operation in the 1T-1FeFET cell is presented in Figs. 7(b), (c), and (d). In the type-I FeFET, the selected WL is set to V_{DD}, and the selected read line (RL) is set to V_{DREAD}. Thereafter, all BLs are set to V_{GREAD}. The operation of the SL is identical to that in the 1FeFET cell. In the current-based sensing scheme, no sneak current flows

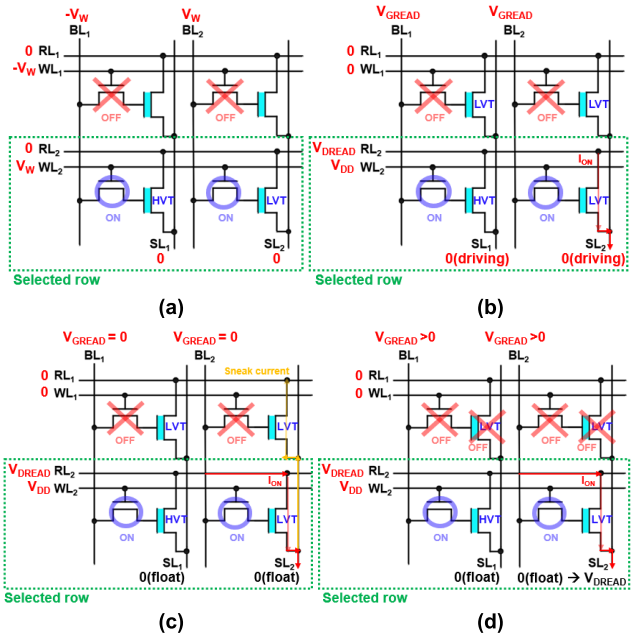

FIGURE 7. Array structure (2 × 2) of the 1T-1FeFET cell. (a) Write operation. (b) Current sensing scheme operation. (c) Voltage sensing scheme operation at type-I FeFET. (d) Voltage sensing scheme operation at type-II FeFET.

from the SL to the unselected RLs because the SL and the unselected RLs are driven to GND. Thus, a current-based sensing scheme can be used for the type-I FeFET. Conversely, in a voltage-based sensing scheme, the SL is floated to GND, and the SL voltage increases when the data "1" are read. Because the FeFETs in the LVT state in the unselected rows are turned on and there is no access transistor at the source of the FeFET in the 1T-1FeFET cell, sneak current can flow from the SL to unselected rows. Subsequently, the SL voltage decreases to GND; thus, it is impossible to read data "1". Therefore, the voltage-based sensing scheme cannot be used for the type-I 1T-1FeFET cell. In the type-II FeFET, no sneak current flows from the SL to unselected rows because the FeFETs in the LVT state in unselected rows are completely turned off. Thus, both sensing schemes can be used for the type-II 1T-1FeFET cell.

C. 2T-1FeFET CELL

The 2T-1FeFET cell has two access transistors connected to the gate and drain of the FeFET. It can control the read current path, which flows from the drain to the source of the FeFET owing to the access transistor at the drain of the FeFET. This allows the 2T-1FeFET cell to read the cell by selecting bits.

The write operation of the 2T-1FeFET cell is presented in Fig. 8(a). The 2T-1FeFET cell uses a write scheme with a negative V_W, and its write operation is the same as that of the 1T-1FeFET cell. Thus, all BLs and WLs swing during the write operation, leading to high write energy consumption.

The current- and voltage-based sensing scheme operation in the 2T-1FeFET cell is presented in Figs. 8(b), (c), and (d).

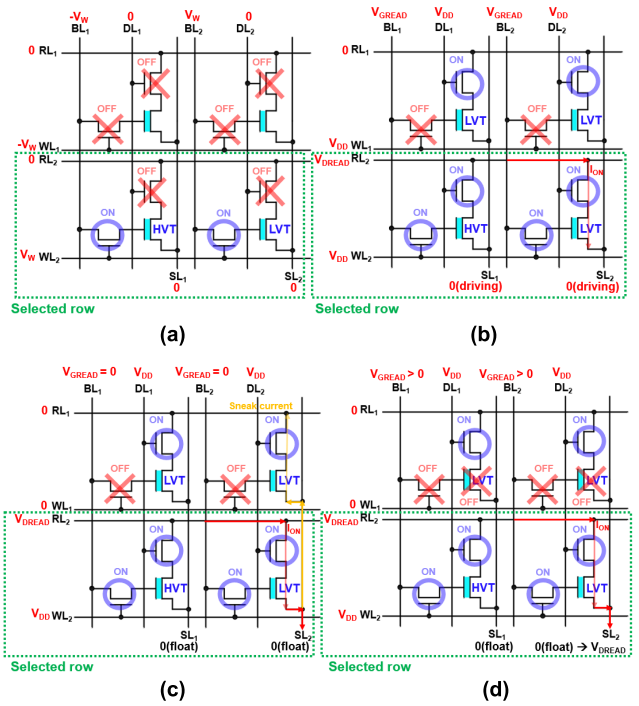

FIGURE 8. Array structure (2 × 2) of the 2T-1FeFET cell. (a) Write operation. (b) Current sensing scheme operation. (c) Voltage sensing scheme operation at type-I FeFET. (d) Voltage sensing scheme operation at type-II FeFET.

The 2T-1FeFET cell has no access transistor at the source of the FeFET. Thus, the current-based sensing scheme can be used for both types of FeFETs, and the voltage-based sensing scheme can only be used for the type-II FeFET, as with the 1T-1FeFET cell. The read operation begins as the selected WL and all data lines (DLs) are set to V_{DD}. The operation of the BL, RL, SL, and unselected WLs is identical to those for the 1T-1FeFET cell.

D. 3T-1FeFET CELL

In the 3T-1FeFET cell, an access transistor is connected to each of the three terminals of the FeFET. The access transistor at the source of the FeFET can prevent the sneak current path. Thus, a current- or voltage-based sensing scheme can be used regardless of the type of FeFET. However, the 3T-1FeFET cell has the largest area overhead.

The write operation of the 3T-1FeFET cell is presented in Fig. 9(a). This cell uses a write scheme without a negative V_W. The write operation begins with the WL and sense selected line (SSL) in the selected row being set to V_W. Thereafter, the BLs that write the data "1" are set to V_W and the SLs that write the data "0" are set to V_W. In the write scheme without a negative V_W, the swing of the unselected WLs can be eliminated. Thus, the 3T-1FeFET cell exhibits low write energy consumption.

Because of the access transistor at the source of the FeFET, both sensing schemes can be used regardless of the type of FeFET in the 3T-1FeFET cell. The read operation of the 3T-1FeFET cell is presented in Fig. 9(b), which begins as the

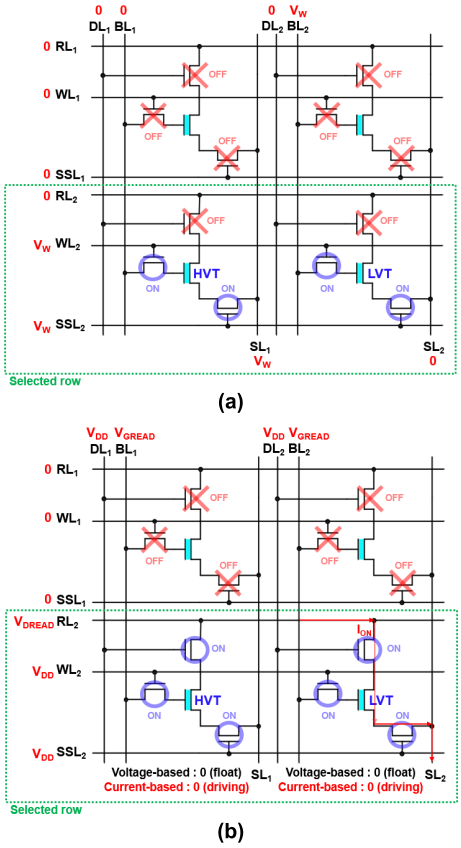

FIGURE 9. Array structure (2 × 2) of the 3T-1FeFET cell. (a) Write operation. (b) Read operation.

TABLE 2. Parameter values of the FeFET model.

Parameter	Description	FeFET LVT	FeFET HVT
V_{TH}	Threshold voltage	0.67 V	1.58 V
[a]I_{ON}	On-current	9.43 μA	0.05 nA
nfactor	Sub-threshold swing factor	9	8.5
E_{ta0}	[b]DIBL coefficient	0.004	0.006
μ_0	Low field mobility	32 $cm^2/V{\cdot}S$	200 $cm^2/V{\cdot}S$
V_{SAT}	Saturation velocity	15000 m/s	25000 m/s

[a]I_{ON} is measured at V_{GS} = 1V
[b]DIBL: Drain-induced barrier lowering

selected WL, the selected SSL, and all DLs are set to V_{DD}. Thereafter, all BLs are set to V_{GREAD}, and the selected RL is set to V_{DREAD}. The SL operation is identical to that in the 1T-1FeFET cell.

E. SENSING SCHEME ANALYSIS

As described in the preceding section, the available sensing scheme for the FeFET in an array structure depends on the type of FeFET. Table 3 presents the available sensing schemes for each type of FeFET memory cell. For the type-I FeFET, the 1FeFET cell cannot read data in the selected row because the data in the selected and unselected rows

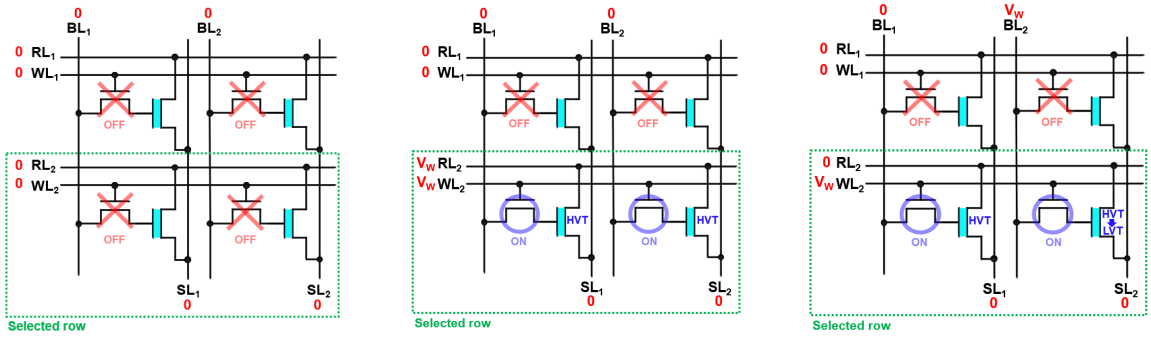

FIGURE 10. Operation of the proposed LCSS write scheme: (a) hold; (b) write phase 1: write data "0"; (c) write phase 2: write data "1."

TABLE 3. Available sensing schemes for each type of FeFET memory cell.

Type of FeFET	1FeFET	1T-1FeFET	2T-1FeFET	3T-1FeFET
type-I	Not available	Current-based	Current-based	All
type-II	All[a]	All	All	All

[a]All: both (current and voltage based) sensing schemes.

cannot be distinguished owing to the read current flowing from the FeFETs in the LVT state in the unselected rows to the SL in the selected cell. The 1T-1FeFET and 2T-1FeFET cells can use only the current-based sensing scheme because the data "1" cannot be read under the voltage-based sensing scheme owing to the sneak current flowing from the SL of the selected cell to unselected rows. The 3T-1FeFET cell can use both sensing schemes owing to the access transistor at the source of the FeFET. In contrast, in type-II FeFET, there is no sneak current because the FeFETs in the LVT state in the unselected rows are completely turned off. Thus, when the FeFET memory cell design is based on the type-II FeFET, both sensing schemes can be used for all FeFET memory cells.

IV. PROPOSED FeFET WRITE SCHEME

Previous FeFET memory cells have the following advantages and disadvantages. The 1FeFET cell exhibits the highest density but suffers from write disturbance. The 1T-1FeFET and 2T-1FeFET cells can address the write disturbance problem due to the presence of an access transistor at the gate of the FeFET. However, they use a write scheme with a negative V_W, which suffers from high write energy consumption because of the voltage swings of the many control signals. The 3T-1FeFET cell uses a write scheme without a negative V_W, which incurs low write energy consumption. However, it exhibits the largest area overhead. Although the 1T-1FeFET cell can address the write disturbance and has a small area overhead, it exhibits high write energy consumption due to the use of a negative V_W. Thus, to reduce the write energy consumption of the 1T-1FeFET cell, we propose an LCSS write scheme without using a negative V_W.

To significantly reduce the energy consumption without using a negative V_W during the write operation, the proposed LCSS write scheme consists of two phases. Furthermore, the row-wise RL acts as the source of the FeFET.

Fig. 10 illustrates the operation of the proposed LCSS write scheme. Write phase 1 begins as the selected WL is set to V_W to turn on the access transistor at the gate of the FeFET. Next, the selected RL is set to V_W to apply a negative V_{GS} to all cells in the selected row. Thus, the data "0" are written to all cells in the selected row. Write phase 2 begins as the selected RL falls to 0. Subsequently, the BLs that write the data "1" are set to V_W, and the data "1" are written to the cells in which the data "1" are intended to be written.

The proposed LCSS write scheme can eliminate the swing of unselected rows owing to the absence of a negative V_W. Additionally, because the data "0" are written owing to the swing of the selected RL, the swing of the BLs that write data "0" is also reduced. Therefore, the write energy consumption is significantly lower in the proposed write scheme than in the write scheme with a negative V_W at the expense of the overhead in write time.

V. PERFORMANCE ANALYSIS

In this section, we compare previous FeFET memory cells in terms of write energy, read time, read energy, and layout area. HSPICE simulations were performed using an industry-compatible 28 nm model for CMOS technology, and the FeFET model was fitted using the PTM [32], as described in Section II-C. The V_W and write time were set to 4 V and 10 ns, respectively [33], [34]. The V_{GREAD} and V_{DREAD} were set to 1 V, which is the value within a memory window. A metal capacitance of 0.21 fF/μm was considered for evaluating the delay and energy [35]. In this simulation, a 32 $\times$ 32 memory array was assumed. Table 4 presents the characteristics and performance of the FeFET memory cells.

TABLE 4. Characteristics and performance of the analyzed FeFET memory cells.

	1FeFET cell [21]		2T-1FeFET cell [23]		3T-1FeFET cell [24]		**1T-1FeFET cell [22]**		
Layout area (μm^2)	0.099		0.292		0.392		**0.14**		
Write scheme	V_W/2 IB	V_W/3 IB	with a negative V_W		without a negative V_W		with a negative V_W	**proposed LCSS**	
Negative V_W	yes		yes		no		yes	no	
Write disturbance	yes		no		no		no	no	
Write time	two-phase		one-phase		one-phase		one-phase	**two-phase**	
Write energy (pJ)	2.27	2.84	3.7		2.83		3.16	**worst**	**2.06**
								average	**1.09**
								best	**0.13**
Type of FeFET	type-**I**	type-II	type-**I**	type-II	type-**I**	type-II	type-**I**	**type-II**	
Available read scheme	not available	all[a]	current-based	all	all		current-based	**all**	
Read time (ns)[b]	-	0.279	-	0.326	0.510		-	**0.289**	
Read energy (pJ)[b]	-	0.03	-	0.107	0.128		-	**0.036**	

[a]All: both (current- and voltage-based) sensing schemes.
[b]Read time and energy are measured under the voltage-based sensing scheme.

A. WRITE ENERGY

The write energy of the FeFET can be divided into two portions: one is consumed by the switching current in the FE layer, and the other is consumed by the voltage swings of the control signals. Because the switching current in the FE layer occurs only in the selected row and is small [16], the energy consumed by it in the FE layer constitutes a small portion of the entire write energy. Conversely, because the swing of the control signals occurs in all lines, most of the write energy is consumed by the swing of the control signals. Thus, we evaluated the write energy consumed by the voltage swings of the control signals.

Fig. 11 presents the write energy for the previous FeFET memory cells and the proposed LCSS write scheme. In the proposed LCSS write scheme, because the data "0" are written into all cells connected to the selected row in write phase 1, the write energy consumption depends on the data portions that are "0" and "1" in the selected row. Thus, the write energy consumption is divided into three cases according to the data portions: the worst case is to write only "1", the average case is to write an equal number of "0"s and "1"s, and the best case is to write only "0".

In the write scheme with a negative V_W of the 1T-1FeFET and 2T-1FeFET cells, the swing of all WLs and BLs occurs during the write operation, whereas there is no swing of the unselected WLs and BLs for writing data "0" in the proposed LCSS write scheme. Thus, the 1T-1FeFET and

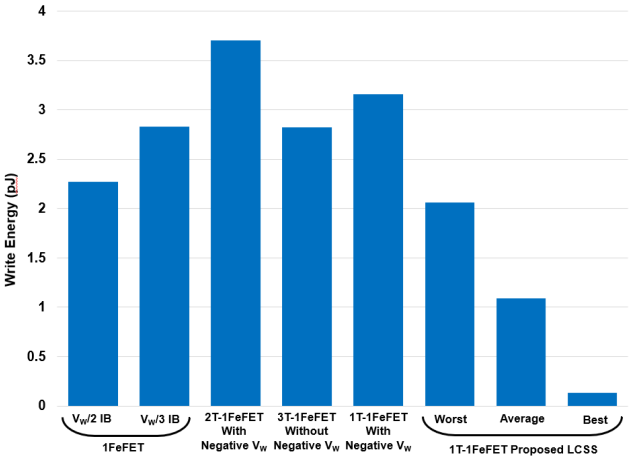

FIGURE 11. Write energy comparison.

2T-1FeFET cells consume 56% and 83% higher write energy, respectively, than the worst case of the proposed LCSS write scheme in the 1T-1FeFET cell.

In the V_W/2 and V_W/3 IB schemes of the 1FeFET cell, the swing of all WLs, BLs, and SLs occurs during the write operation. Thus, these schemes consume 12% and 40% higher write energy, respectively, than the worst case of the proposed LCSS write scheme in the 1T-1FeFET cell. Because the V_W/3 IB scheme in the 1FeFET cell uses a higher disturbance voltage ($2V_W$/3) in the BLs and SLs, it incurs in higher

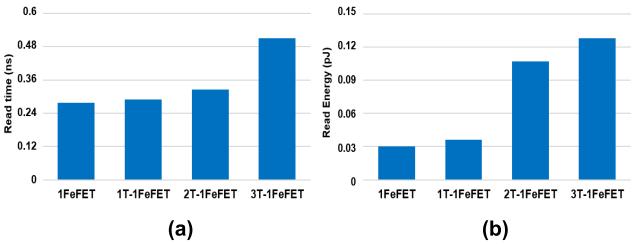

FIGURE 12. Read performance of FeFET memory cells based on the voltage-based sensing scheme: (a) Read time; (b) Read energy.

write energy consumption than the $V_W/2$ IB scheme in the 1FeFET cell.

The 3T-1FeFET cell uses a write scheme without a negative V_W, which can eliminate the swing of unselected rows. Thus, it results in lower write energy consumption than the write scheme with a negative V_W in the 1T-1FeFET and 2T-1FeFET cells. However, the 3T-1FeFET cell has a higher metal capacitance than the other FeFET memory cells. Thus, it consumes 40% higher write energy than the worst case of the proposed LCSS write scheme in the 1T-1FeFET cell.

The proposed LCSS write scheme can eliminate the swing of unselected WLs because it does not use a negative V_W. Additionally, it can eliminate the swing of BLs for writing "0" because the data "0" are written through the swing of the selected RL. Thus, the proposed LCSS write scheme can reduce the write energy consumption by 35%, 66%, and 96% in the worst, average, and best cases, respectively, relative to the write scheme with a negative V_W in the 1T-1FeFET cell. Moreover, even in the worst case, the proposed LCSS scheme consumes the lowest write energy compared to the other FeFET memory cells.

B. READ TIME AND ENERGY

As described in Section IV-B, type-I 1T-1FeFET and 2T-1FeFET cells can only use the current-based sensing scheme. In contrast, type-II FeFET memory cells can use both the current- and voltage-based sensing schemes in all FeFET memory cells. In the read simulation, we evaluated the read performance of type-II FeFET memory cells under the voltage-based sensing scheme.

Fig. 12(a) presents the read times of the FeFET memory cells. The read time of the 1T-1FeFET cell was 11% and 43.3% faster than that of the 2T-1FeFET and 3T-1FeFET cells, respectively, because its read path consists of an FeFET without an access transistor, and it has a low parasitic capacitance. The 1T-1FeFET cell exhibited a similar read time as the 1FeFET cell because both cells have the same read path.

Fig. 12(b) presents the read energy results for the FeFET memory cells. When the data in the selected row are read, the swing of the row-wise control signals (WL, RL, SSL) only occurs in the selected row. Conversely, the swing of the column-wise control signals (BL, SL, DL) occurs in all columns. Thus, the swing of the column-wise control signals

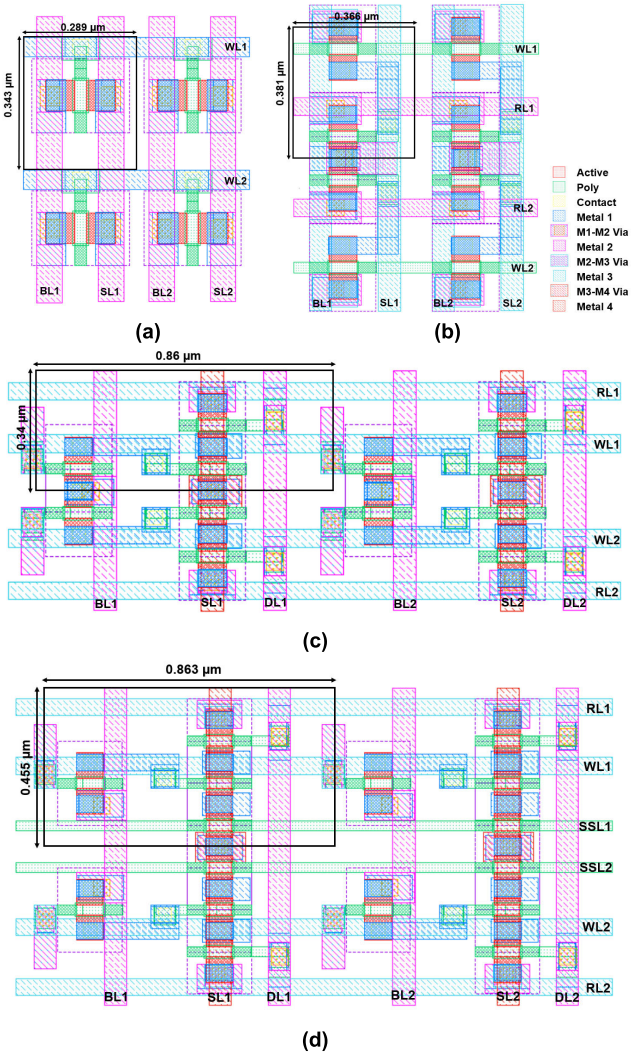

FIGURE 13. Layouts of 2 × 2 FeFET memory cells: (a) 1FeFET cell; (b) 1T-1FeFET cell; (c) 2T-1FeFET cell; (d) 3T-1FeFET cell.

dominates the read energy consumption. The 1T-1FeFET cell consumes 66% and 71.9% lower read energy than the 2T-1FeFET and 3T-1FeFET cells, respectively, because it has a small number of column-wise control signals and low parasitic capacitance. However, the 1T-1FeFET cell consumes 20% higher read energy than the 1FeFET cell because the 1T-1FeFET cell has an additional row-wise control signal (RL).

C. LAYOUT AREA

Fig. 13 presents the layouts of the 2 × 2 FeFET memory cells based on the industry-compatible 28 nm CMOS technology. The area of the 1T-1FeFET cell is 52% and 64% smaller than that of the 2T-1FeFET and 3T-1FeFET cells, respectively, because it has a small number of access transistors and simple metal routing. Although the area of the 1T-1FeFET cell is 41% larger than that of the 1FeFET cell owing to the access transistor at the gate of the FeFET, the 1T-1FeFET cell has the advantage that there is no write disturbance.

VI. CONCLUSION

Previous FeFET memory cells have advantages and limitations. The 1FeFET cell exhibits the highest density but suffers from write disturbance. Furthermore, the type-I 1FeFET cell cannot read data in the selected row. The 1T-1FeFET cell can address the write disturbance; however, it uses a write scheme with a negative V_W, which incurs high write energy consumption. The 2T-1FeFET cell can control the read current during the read operation; however, it also uses a write scheme with a negative V_W. Moreover, the type-I 1T-1FeFET and 2T-1FeFET cells can use only a current-based sensing scheme during the read operation. The 3T-1FeFET cell uses a write scheme without a negative V_W, which consumes a low amount of write energy, and can use both current- and voltage-based sensing schemes regardless of the type of FeFET; however, it exhibits the largest area overhead.

Compared with the other FeFET memory cells, under the proposed LCSS write scheme, the 1T-1FeFET cell addresses the write disturbance, has a smaller area overhead and the lowest write energy consumption by eliminating the negative V_W. Additionally, the available sensing scheme for each FeFET memory cell was identified according to the FeFET V_{TH} distribution. The analysis results indicated that when the FeFET memory cell is designed on the basis of the type-II FeFET, both sensing schemes can be used in all FeFET memory cells.

APPENDIX

The parameter values of the FeFET model are presented in table 2.

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DONG HAN KO (Graduate Student Member, IEEE) was born in Seoul, South Korea, in 1995. He received the B.S. degree in electrical and electronic engineering from Yonsei University, Seoul, in 2021, where he is currently pursuing the Ph.D. degree in electrical and electronic engineering. His current research interest includes ferroelectric FET-based nonvolatile circuit design.

TAE WOO OH (Graduate Student Member, IEEE) was born in Seoul, South Korea, in 1992. He received the B.S. degree in electrical and electronic engineering from Yonsei University, Seoul, in 2015, where he is currently pursuing the Ph.D. degree in electrical and electronic engineering. His current research interests include ferroelectric FET-based nonvolatile circuit design, next-generation semiconductor devices, low-power and high-speed SRAM, and processing-in-memory.

SEHEE LIM (Graduate Student Member, IEEE) was born in Seoul, South Korea, in 1994. She received the B.S. degree in systems biology and electrical and electronic engineering from Yonsei University, Seoul, in 2018, where she is currently pursuing the Ph.D. degree. Her current research interests include physically unclonable function design and ferroelectric FET-based logic IP design.

SE KEON KIM (Graduate Student Member, IEEE) was born in Seoul, South Korea, in 1996. He received the B.S. degree in electrical and electronic engineering from Yonsei University, Seoul, in 2021, where he is currently pursuing the Ph.D. degree in electrical and electronic engineering. His current research interest includes ferroelectric FET-based nonvolatile circuit design.

SEONG-OOK JUNG (Senior Member, IEEE) received the B.S. and M.S. degrees in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 1987 and 1989, respectively, and the Ph.D. degree in electrical engineering from the University of Illinois at Urbana–Champaign, Urbana, IL, USA, in 2002. From 1989 to 1998, he was affiliated with Samsung Electronics Company, Ltd., Hwaseong, South Korea, where he was involved in specialty memories, such as video, graphic, and window RAM, and merged memory logic. From 2001 to 2003, he was affiliated with T-RAM Inc., Mountain View, CA, USA, where he was the Leader of the Thyristor-Based Memory Circuit Design Team. From 2003 to 2006, he was affiliated with Qualcomm Inc., San Diego, CA, USA, where he was involved in high-performance low-power embedded memories, process variation-tolerant circuit design, and low-power circuit techniques. Since 2006, he has been a Professor with Yonsei University. His current research interests include process variation-tolerant, low-power, mixed-mode circuit design, and next-generation memory and technology.