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DC-DC High Voltage Gain Switched Capacitor Converter With Multilevel Output Voltage and Zero-Voltage Switching

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ABSTRACT This paper presents the concept and results of a novel resonant DC-DC converter which achieves high voltage gain at a low number of utilized switches, low voltage stress on transistors, ZVS and ZCS operation, high efficiency and variable voltage gain. The converter uses resonant switched-capacitors (SC) circuits with five switches which allows it to reach a six-fold voltage gain. By the application of adequate switching patterns, seven levels of voltage adjustment can be achieved. The basic operation mode of the converter is at zero current switching (ZCS) but a part of the existing transitions can be switched-on at a zero drain-source voltage. Zero voltage switching (ZVS) allows for a reduction of C_{oss} losses and a decrease in disturbances of voltages and currents. In the proposed converter, voltage stress on switches are noticeably lower than the output voltage which is beneficial from viewpoint the cost reduction and switching quality improvement. The converter output stage consists of two series connected capacitors which allows for a supply of 3-level NPC inverters. Resonant inductors, used in the proposed topology, store very low amount of energy and their volume is significantly lower than in case of chokes typically used in switch-mode converters. Qualities of the converter such as low switch count, efficiency, ZCS and ZVS operation as well as voltage gain variation are demonstrated in this paper. Furthermore, an impact of MOSFET transistors type on the efficiency of the converter is investigated. The design based on low C_{oss} superjunction (SJ) MOSFETs is compared with the implementation where $R_{ds(on)}$ of switches is minimized. Due to low voltage stress, application of Schottky rectifiers is also demonstrated in the converter. The concept of the topology and switching patterns is verified by the results of analysis, simulations and experiments.

INDEX TERMS Boost converters, DC-DC converters, high voltage gain converter, switched-capacitor circuit.

I. INTRODUCTION

HIGH voltage gain DC-DC converters are especially required in some applications such as low power photovoltaic grid-connected systems, fuel cell powered devices and mobility applications [2]–[9]. The origins of the growth of switched-capacitor (SC) converters can be found in micro-electronics [1]. Over time, this technology was adapted for power applications and has found a significant place for itself in the field of power electronics where research on its development is still being carried out. A converter with high-voltage gain can be effectively achieved with the use of mixed converters with switched capacitors and inductors [2], [4]–[16] as well as the pure ore resonant SC converters [1], [3], [10], [17]–[40]. The operation of SC converters is based on the energy transfer via capacitors in circuits, which are reconfigured with the use of semiconductor switches. The application of resonant inductors allows for it to achieve oscillatory currents during the process of switched capacitors recharging and zero current switching operation (ZCS). An adequate low volume resonant inductance can be achieved as a parasitic component, as well as a PCB planar coil or air choke [22], [24], [25]. An SC inductive-less converter can operate at a high temperature of components and environment, which might be an important characteristic in some applications [40]. Other benefits of SC based converters are associated with its simple switching logic and their modular topology. However, SC circuits have disadvantages related to the large number of switches, constant voltage gain and high C_{oss} losses [22], [26], [37].

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The majority of SC converters operates with a fixed voltage gain, especially in applications where a relatively high conversion ratio is needed [5], [23]–[26]. Yet, in some topologies the voltage gain can be changed to achieve various levels of output voltage [26]–[33]. In [26] and [27], it is accomplished on $n+1$ levels (where n is the number of switching cells in the voltage multiplier) by selecting a suitable active cell count. The variable voltage gain of the SC converter, with fractional precision, is presented in [28]. References [29]–[33] present converters and methods for continuous voltage gain regulation which is achieved by the variation of switching frequency. In the particular case of a ladder converter, presented in [29], the switching frequency adjustment helps to obtain a smoothly regulated voltage gain cofactor in the range from 1 to 3.

The converter proposed in this paper has the ability of output voltage regulation on 7 levels. It is achieved by the use of appropriate switching patterns.

A decrease in switch count is an important research trend in the field of SC converters and is presented in the literature [21]–[25]. The SC voltage multiplier analyzed in [21] requires $2n$ switches where the voltage gain equals n, which is relatively high. Reference [24], shows another kind of modular converter where high voltage gains as well as multilevel regulation has been obtained. The cascaded connection of SC converters is a very effective method of switch count reduction [25]. However, some transistors in this topology have to withstand a high amount of voltage stress. In [22], another modular converter was presented. In its basic configuration, this device uses 7 switches and allows for a seven-time increase in the gain of the voltage. Reference [23] presents the device where a four-fold voltage amplification is achieved with the use of just three transistors. LC based switched capacitor converter in [12] obtains an extremely high conversion ratio, which is an important merit. Yet, this converter utilizes high inductivity chokes which makes it unusual in the family of pure switched capacitor converters. The proportion of the number of switches to the voltage gain in the case of the converter presented in this paper is 5/6, which is very beneficial in comparison to the referenced converters.

Switching losses that are generated and which are associated with the output capacitance of transistors (C_{oss} losses) can be a crucial problem of SC converters. These kinds of losses are proportional to the value of a voltage on switches before their activation. In such a converter as the SCVM [25]–[27] voltage stress on switches are not equal and, in some applications, it reaches the level of the output voltage. Therefore, some switches generate very high C_{oss} losses. To overcome C_{oss} losses in certain SC resonant topologies, ZVS operation can be achieved [33]–[38]. In [36] and [37] the SC voltage-doubler operates above the resonant frequency which pushes a small amount of current through its internal diode. Simultaneously, a charge collected in the output capacitance of a transistor is discharged and the switch can be turned on without the charge dissipation.

In the novel converter proposed in this paper the following advantages have been achieved:

- High voltage gain. The converter can boost the input voltage six-fold ($G_{\text{Umax}} = 6$)
- A switch-capacitor structure. The resonant chokes are used to avoid inrush currents but their energy and volume is nearly negligibly small;
- Regulated voltage gain. The converter allows for an operation on seven levels of the output voltage
- Operation in ZCS
- Operation in ZVS mode of some transistors
- A low number of switches. The converter contains 5 active switches for $G_{\text{Umax}} = 6$ which is favorable in comparison to e.g. voltage multipliers presented in [10], [27];
- A low voltage stress on switches in comparison to the value of the converted voltage. This parameter is much better than in the case of a classic switch-mode boost converter and well-established SC voltage multipliers [27] where some switches should withstand the full output voltage stress. In the proposed converter the voltage stress on switches is in the range of (U_{in} to $U_{\text{out}}/2$);
- A low voltage stress on diodes. For the output voltage below 400 V all the diodes in the converter can be Shottky-type (with very low forward voltage, good performance and low cost). In some range of the output voltage above 400 V three diodes applied in the converter can be silicon Shottky-type;
- A low number of switched capacitors and resonant inductors. Only two switched capacitors are required which is much below then in the case of well-established SC voltage multipliers [27]. Two resonant inductors can be even designed as an air-based inductor composed of PCB tracks or parasitic inductance;
- Symmetrically divided output voltage which creates suitable supply conditions for A 3-level NPC inverter

A combination of such favorable characteristics in one converter brings an important contribution to the field of SC DC-DC converters.

Charge pumps may be considered in PV system where high gain is required. In [6] the high gain converter which utilizes the charge pump and coupled inductors is presented. The converter operates with the input voltage 20-70V with the voltage gain 2.9-10. In [8] the switched-capacitor integrated with the Z-source network is implemented in the DC-DC part of the PV system with 400V on the DC-link and 20V on the input. High voltage gain ability of the proposed converter can be a merit in system with low voltage renewable energy sources. In two stage systems composed of the DC-DC and DC-AC parts, step change of the voltage gain of the proposed converter allows to adjust the DC-link voltage to most adequate level as the source voltage varies. As vast majority of renewable energy systems are grid connected the MPPT (maximum power point tracking) algorithm can be realized by an inverter by its output current control. In [39] the step-up

voltage balancing converter is used in front of the DC-AC PV system. The converter has static threefold voltage gain and the MPPT is realized by the inverter. The MPPT controller determines the reference DC voltage. The error of DC voltage realization is utilized by the PI-type controller for the referenced component of the grid current control in the *dq*-frame settings. Similar approach to the MPPT, which determines the DC voltage, change can be found in [41], [42] for the PV with the stand-alone PV inverter, in [43] for the single-stage DC-AC converters, in [43] for the T-type 3-level inverter with two input PV modules. The converter proposed in this paper, operating with a static voltage gain, can be a part of the high voltage gain DC-AC system with the MPPT ability on the inverter side.

SC circuits are also implemented in high-gain DC-DC converters operating according to other concepts, such as coupled inductors-based [7], or Z-type [8]. The converters can achieve continuous voltage regulation and a smaller number of switches then the proposed pure SC converter. However, the converters use chokes of considerable inductors e.g., 2 devices of 3 mH in [2], 0.5mH in [4], 2 devices of 480 μH in [5], 2 devices of 94 μH in [7], 2 devices of 270 μH in [8], 330 μH and 1mH in [9], 430 μH in [12], 2 devices of 1mH in [13], 5 mH and 2 mH (case of CCM operation) in [14], 0.55 mH and 1.1 mH in [12]. The proposed circuit belongs to other family of converters from the principle of operation viewpoint. However, comparisons of some qualities such as efficiency and the input current ripple will be provided in this paper with these reference concepts.

This paper is organized in the following way. Section 2 presents the basic concept of the operation of the converter and the analysis of its voltage gain. The simulation results are presented in Section 3. The waveforms obtained demonstrate the converter operation concept and voltage stress on the switches. Section 4 describes the laboratory test setup of the converter as well as the results of the most relevant experiments. The tests were performed in the design approached to the case of operation with the use of two PV arrays with the maximum 70V and 600W as the input source. It gives nearly 400V DC voltage on the output of the DC-DC converter and majority of tests were performed for the six-fold gain. A single-phase grid-tied 230V bridge inverter can operate in such conditions of the DC-link voltage.

II. THE TOPOLOGY AND PRINCIPLE OF OPERATION

The proposed converter, presented in Fig. 1 is made up of two switched capacitors, five switches, five diodes and the output with a midpoint.

A. BASIC PRINCIPLE OF OPERATION IN ZCS MODE AND HIGH-VOLTAGE GAIN

The switched capacitors (C_2, C_3) charge and discharge in circuits with the participation of resonant inductances which provides an oscillatory current waveform, and the possibility of ZCS operation (Fig. 2 and Fig. 3). A changeover from ZCS

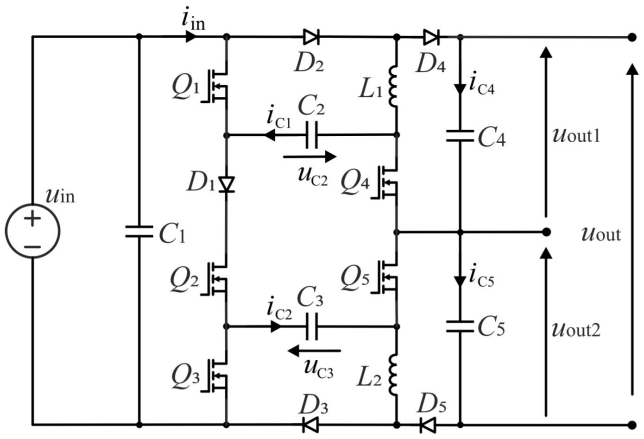

FIGURE 1. The proposed DC-DC high voltage gain converter.

to ZVS mode can be achieved by increasing the switching frequency of the transistors.

In the basic operation strategy, the converter operates with the voltage gain $G_{Umax} = 6$. To achieve that, each full switching period (T_S) consists of six consecutive stages (Fig. 2), which are described as follows:

- **1st** stage (T_{S1} subperiod, M1 mode): the upper switched capacitor (C_2) is charging from the source;
- **2nd** stage (T_{S2} time period, M2 mode): the lower switched capacitor (C_3) is charging from the source;
- **3rd** stage (T_{S3} time period, M3 mode): the output capacitor C_4 is charging in the circuit composed with the source, capacitors C_2 and C_3 connected in series;
- **4th** and **5th** stages in the time periods T_{S4} and T_{S5}: charging the C_2 and C_3 as in T_{S1} and T_{S2} (M1, M2);
- **6th** stage (T_{S6} time period, M4 mode): the output capacitor C_5 is charging in the circuit composed with the source, capacitors C_2 and C_3 are connected in series;

The output stage of the converter consists of two capacitors (C_4, C_5). To achieve the maximum voltage, gain the

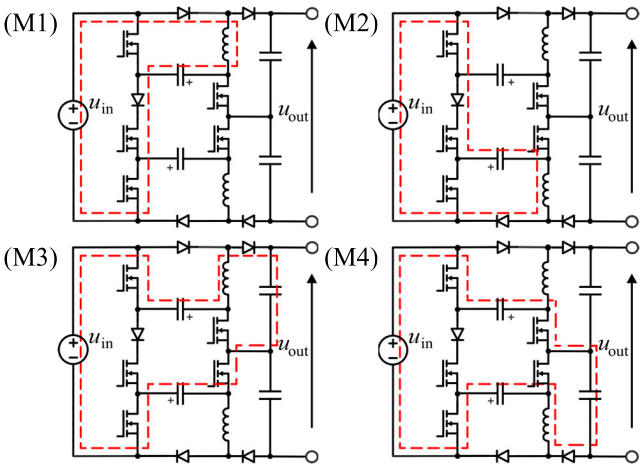

FIGURE 2. Basic modes (M1 – M4) of switching for operation with the highest voltage gain $G_U = 6$.

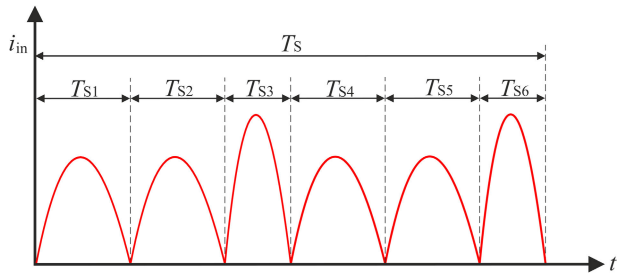

FIGURE 3. Switching frequency definition on the base of the input current waveform (i_{in}).

capacitors C_4 and C_5 are charged individually (Fig. 2, modes M3 and M4). Therefore, the final output voltage is a sum of the voltages across the capacitors (C_4 and C_5).

The converter operates using the switching pattern in the following order of modes: M1-M2-M3-M1-M2-M4. For further analysis, equal capacitance and average value of voltage on C_4 and C_5 is assumed. Moreover, it is also assumed that capacitance of resonant capacitors (C_2, C_3) is equal to each other, as well as the inductance of resonant inductors (L_1, L_2). Additionally, due to the fact that the whole circuit resistance is relatively small, its value has been neglected in further calculations.

When each of the switched capacitors is charged from the input voltage separately (Fig. 2, modes M1 or M2, Fig. 3, time intervals T_{S1} or T_{S2} or T_{S4} or T_{S5}) the voltage of the switched capacitors oscillates, which can be described by the following equations:

$$u_{C_n} = U_{in} + \left(U_{C_{min}} - U_{in}\right)\cos\omega_{ch}t \tag{1}$$

$$\omega_{ch} = \frac{1}{\sqrt{L_n C_n}} \tag{2}$$

where: u_{Cn} is the voltage on one of the resonant capacitor (C_2 or C_3), ω_{ch} is the pulsation of the LC circuit, L_{n} is the resonant inductance (L_1 or L_2), C_n is the resonant capacitance (C_2 or C_3), U_{Cmin} is one of the initial voltages value of resonant capacitor (C_2 or C_3).

Once the charging process of any resonant capacitor is complete (Fig. 2, modes M1 or M2) the voltage across its terminals reaches the following value:

$$U_{C_{max}} = U_{in} - \left(U_{C_{min}} - U_{in}\right) = 2U_{in} - U_{C_{min}} \tag{3}$$

In the discharging modes (Fig. 2, modes M3 or M4, Fig. 3 periods T_{S3} or T_{S6}), energy from two series connected switched capacitors is transferred to one of the output capacitors. In this stage the voltage on a switched capacitor is described by the following equation:

$$2u_{C_n} = (2U_{C_{max}} - \frac{U_{out}}{2} + U_{in})\cos\omega_{dis}t + \frac{U_{out}}{2} - U_{in} \tag{4}$$

Because the capacitances of C_2 and C_3 are equal, the following equations can be written:

$$C_2 = C_3 = C \tag{5}$$

$$\omega_{dis} = \frac{1}{\sqrt{L_n \frac{C}{2}}} \tag{6}$$

The voltage across a single switched capacitor during the discharging phase is described by the equation:

$$U_{C_{dis}} = \left(U_{C_{max}} - \frac{\frac{1}{2}U_{out} - U_{in}}{2}\right)cos\omega_{dis}t + \frac{\frac{1}{2}U_{out} - U_{in}}{2} \tag{7}$$

When the discharge process is complete, the voltage on each resonant capacitor is described by the following equation:

$$U_{C_{min}} = \frac{1}{2}U_{out} - U_{in} - U_{C_{max}} \tag{8}$$

From (3) and (8) the maximum voltage gain of the converter is:

$$U_{out} = 6U_{in}; \quad G = \frac{U_{out}}{U_{in}} = 6 \tag{9}$$

Another important issue related to the design of the converter is the consideration of voltage stresses across the switches. The stages M1 and M2 show that the voltage stress on switches Q_1 and Q_3 are:

$$U_{\mathrm{Q1max}} = U_{\mathrm{Q3max}} = U_{\mathrm{in}} \tag{10}$$

From the stages M3 and M4 voltage stress on the branch with the switch Q_2 and the diode D_1 can be described as:

$$U_{\mathrm{Q2max}} + U_{\mathrm{D1max}} = U_{\mathrm{in}} \tag{11}$$

The maximum voltage stresses on switches Q_4 and Q_5 occurs at the maximum voltage gain of the converter and can be estimated during the stages M3 and M4 as well. During the stage M3:

$$u_{\mathrm{Q4}} = u_{\mathrm{in}} + u_{\mathrm{C2}} + u_{\mathrm{C3}} \tag{12}$$

Assuming the operation with low voltage ripples on C_2 and C_3 capacitors the estimated value of the maximum voltage on the Q4 switch is described by following equation:

$$U_{\mathrm{Q4max\_ideal}} = U_{\mathrm{Q5max\_ideal}} = 3U_{\mathrm{in}} \tag{13}$$

Relations (10), (11) and (13) are very favourable because the voltage stress on switches can be significantly below the output voltage (9). To operate with low voltage stresses on Q_4 and Q_5, voltage ripples on C_2 and C_3 capacitors should be limited.

In the case of design where the deep discharge of the C_2 and C_3 capacitors are allowed, the voltage stress on Q_4 and Q_5 rise. In the worst case, the resonant capacitors can be charged up to the doubled input voltage ($2U_{\mathrm{in}}$). In this case the voltage stress is the highest and can reach the value $U_{\mathrm{Q4max}} = U_{\mathrm{Q5max}} = 5U_{\mathrm{in}}$. However, it can be easily avoided by the adequate design where C_2 and C_3 capacitances are adjusted to the power of the converter respecting low ripples of their voltages.

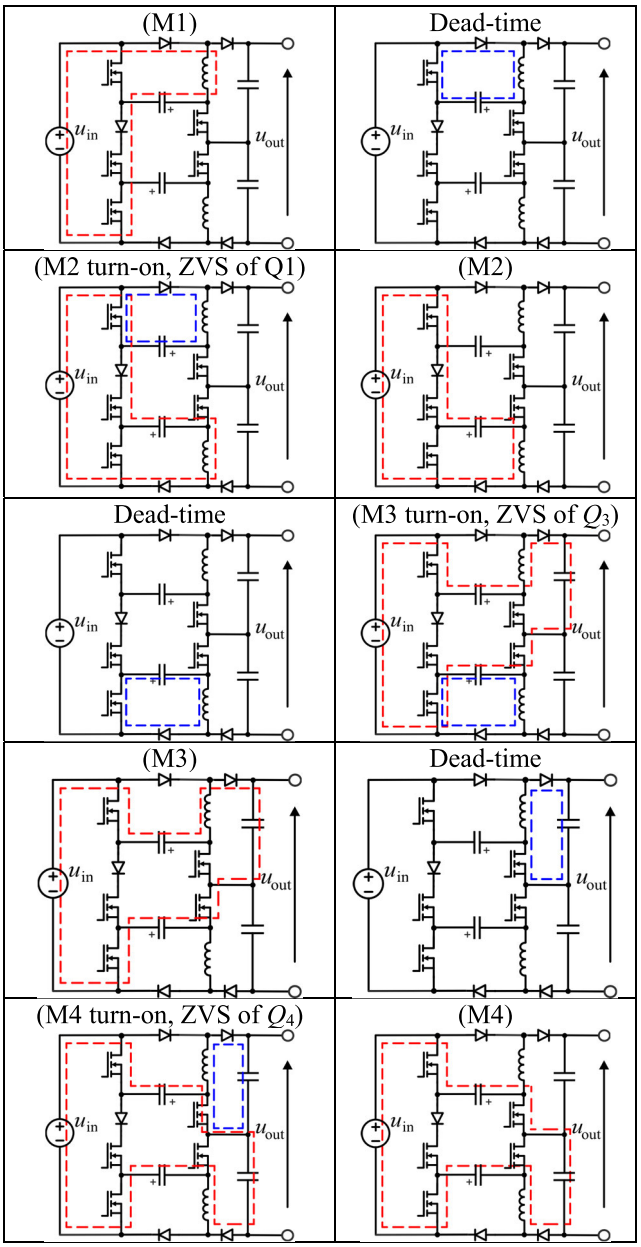

FIGURE 4. ZVS operation in a cycle of switching with $G = 6$.

B. OPERATION IN ZERO VOLTAGE SWITCHING MODE (ZVS)

ZVS during the transistor activation process allows for a significant reduction in switch output charge (Q_{oss}) dissipation. It leads to a limitation of switching related losses. These losses strongly depend on voltage stresses across transistors. The amount of power dissipated on each transistor rises with its increase in voltage. Therefore, the importance of the Q_{oss} reduction problem grows along with the voltage gain cofactor and gains the greatest importance when the converter works with the highest voltage gain $G_U = 6$. This case, with the ZVS introduced, is presented in Fig. 4.

The concept of ZVS operation presented in Fig. 4, shows that the switches Q_1, Q_2 and Q_3 operate in ZVS at its activation. ZVS can be accomplished in operation with a decreased voltage gain as well. Tab. 1 presents transitions for various voltage gains with indicated ZVS operation.

TABLE 1. Transitions with ZVS on particular levels.

Voltage gain	ZVS of	ZVS in stage
1.5	Q1	M6
2	Q1, Q3	M8
3	Q1	M2
4	Q1	M9
	Q3	M10
5	Q1	M9, M2
	Q3	M1, M4
6	Q1	M2
	Q3	M3, M4

TABLE 2. Switching patterns for seven-level operation.

Voltage gain G_U	Order of switching modes
1	All switches turned-off
1.5	M5-M6-M7-…
2	M5-M8-…
3	M1-M2-M8-…
4	M1-M9-M2-M10-…
5	M1-M9-M1-M2-M4-…
6	M1-M2-M3-M1-M2-M4-…

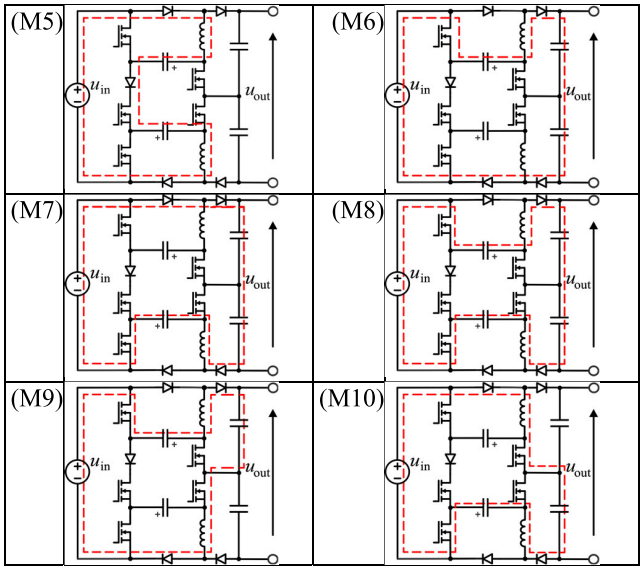

FIGURE 5. Modes (M5 – M10) of switching for operation with the partial voltage gain $G < 6$.

C. OPERATION WITH A VARIABLE VOLTAGE GAIN

The converter can operate with various voltage gain cofactors. The obtained gain (G_U) depends on the employed switching strategy. To accomplish the ability to operation with numerous voltage gain ratios, additional switching modes (Fig. 5) should be used. The possible voltage gains which can be achieved using the modes M1-M10 are presented in Table 2.

III. SIMULATION RESULTS

The simulation research was performed to demonstrate the principle of the operation of the converter, in the case when

the voltage gain of the device is set to the highest possible value ($G_U = 6$). Moreover, the simulation research also covered the analysis of voltage stress in the case of operation under nominal conditions. In addition, the simulation tests included an analysis of the ZVS operation mode and the examination of the voltage gain adjustment.

A. OPERATION WITH HIGH-VOLTAGE GAIN

Operation with the highest voltage gain was considered very important due to the presence of the highest voltage stress. All the assumed parameters used during this simulation and experimental research are listed in Table 3. The output voltage level that was obtained was around 400 V, which is suitable for a single-phase grid connected NPC inverter input. The input voltage 70 V can be found in a PV system composed of two series connected PV arrays operating with 35V at MPP (Maximum Power Point) with the power 200 – 300 W each.

Fig. 6 presents a set of control signals and basic waveforms of voltages and currents across components in the full converter working cycle. From these waveforms it might be seen that the converter operates as intended in its operation concept (Section 2).

TABLE 3. Parameters of the converter used for simulation and experimental tests.

Parameter	*Value*	*Symbol*
Input voltage	70 V	U_{in}
Switching frequency of the entire cycle composed of 6 switching states (T_s in Fig. 3)	21 kHz	f_s
Output voltage	ca. 405 V	U_{out}
Maximum output power	600 W	P_{out_max}
Inductance of resonant inductors	1.9 µH	L_1, L_2
Capacitance of resonant capacitors	4 µF	C_2, C_3
Output capacitances	9.4 µF	C_4, C_5
Ripples of voltages on C_2 and C_3	20V at P_{out}=600 W	$U_{C2C3ripple}$

Fig. 6 presents simulation results of voltage values across switches and capacitors in rated operation mode. From the recorded waveforms it shows that voltages across switches Q_4 and Q_5 are slightly above the ideal value ($3U_{in}$). Voltage stress on remaining transistors are always equal to the value of the input voltage.

Voltage stress is important from the perspective of appropriate switch selection, but the maximal turn-on voltage of the transistor is also important. This voltage value determines the C_{oss} losses. From the simulation results, we see that the voltage of Q_4 and Q_5 transistors during the activation process is significantly below the maximum voltage stress as it might occur on those switches, which is very favorable from the standpoint of C_{oss} losses limitation.

B. OPERATION WITH HIGH-VOLTAGE GAIN

Several switches of the presented converter might operate in ZVS mode which is proven by the waveforms presented in Fig. 8. In one particular case, the investigation of ZVS switching procedure of transistor Q_1 has been carried out.

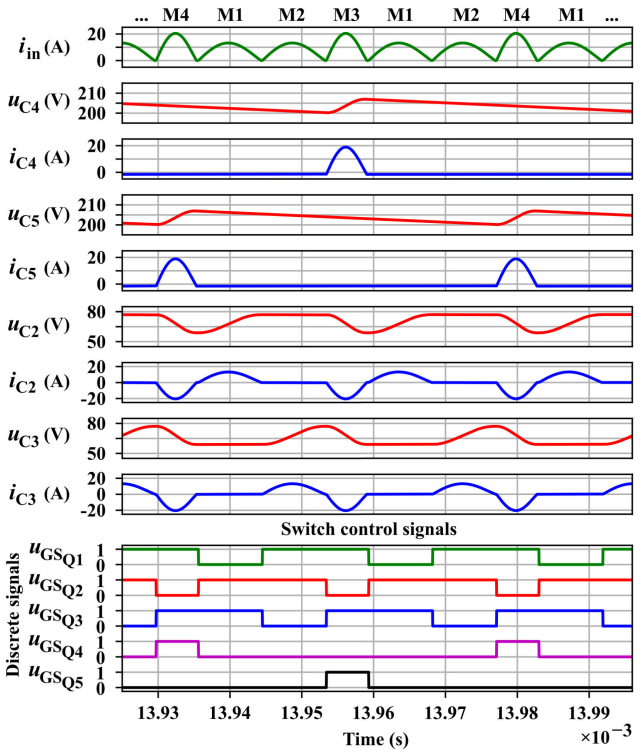

FIGURE 6. Steady state waveforms of voltages, currents and control signals of switches. $G = 6$. Order of switching states according to Table 2. $P_{out} = 600$W. Matlab/Simulink simulation results.

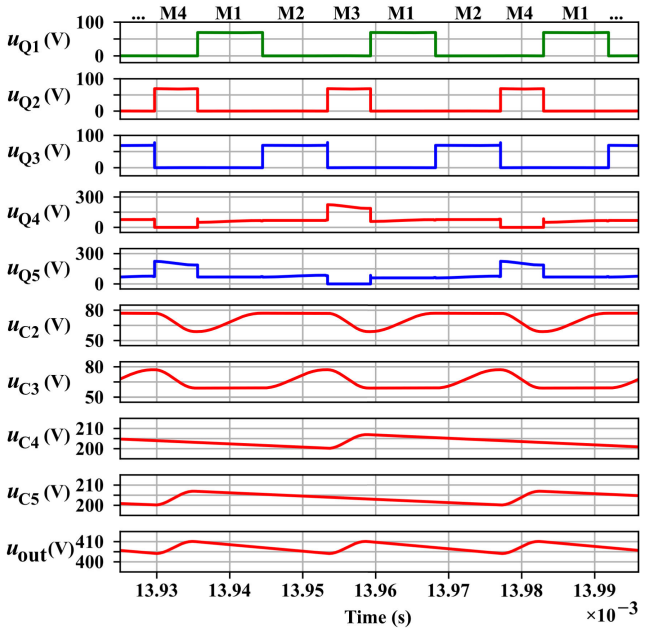

FIGURE 7. Waveforms of the voltages across transistors and capacitors, recorded under rated operation conditions of the converter ($G = 6$, $U_{out} = 410$V). $P_{out} = 600$W. Matlab/Simulink simulation results.

Fig. 8 clearly shows that Q_1 switch turning-on is proceeded by the reverse current flow. As soon as C_{oss} discharging process is finished the switch might be turn on without any additional power losses related to C_{oss} capacitance.

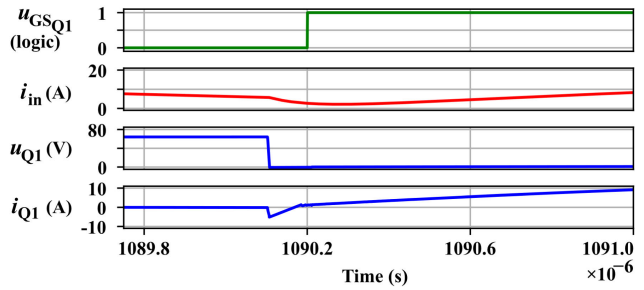

FIGURE 8. Zero-voltage turn-on of the Q_1 switch. Waveforms of the input current and signals associated with the Q_1 switch (the gate-source voltage, the drain-source voltage and the drain current). *LT* spice simulation results.

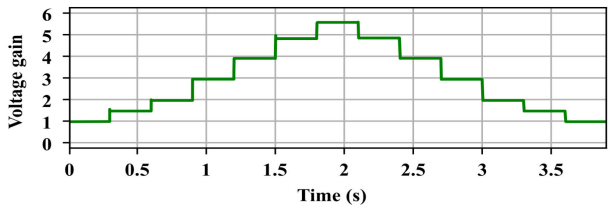

FIGURE 9. Level change of the output voltage by application of adequate order of switching modes presented in Tab. 2. Matlab/Simulink simulation results.

C. VOLTAGE GAIN ADJUSTMENT

The converter allows for the operation with 7 output voltage gain values (Tab. 2).

The results of the simulation research in this matter, presented in Fig. 9, confirms this ability. In order to visualize the voltage gain change of the converter, a stepwise steering pattern has been applied. During the whole simulation the constant value of resistive load (240 Ω) was applied.

D. THE INPUT CURRENT

Switching cells in the converter forces the pulsating current which flows to the input capacitor. Application of the input capacitor bank about approximately 100 μF capacitance and the input inductance 1.9 μH allows to suppress the current ripples of the source below 5% of the average input current (and below 2% of the currents' ripples in switching cells). Such inductance does not increase the volume of the converter

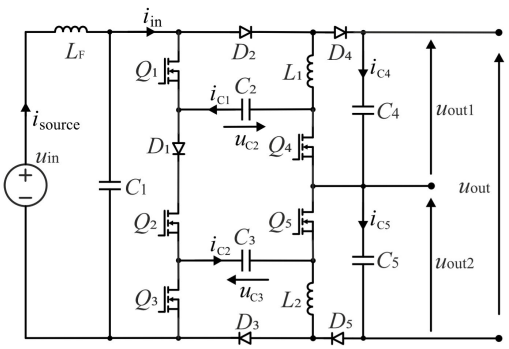

FIGURE 10. The diagram of the converter with the input filter.

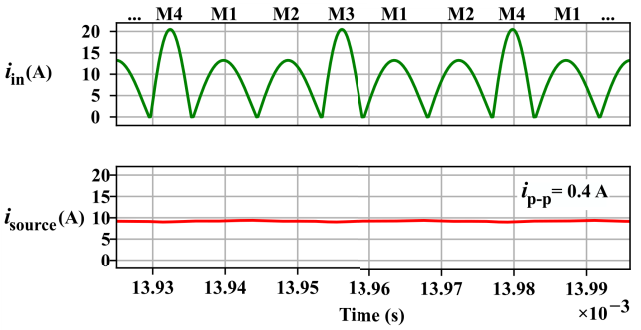

FIGURE 11. The input current of the resonant cells (i_{in}) and the current of the source (i_{source}). Input capacitor C_{in} = 102uF, the filter inductor L_{in} = 1.9uH, the input resistance (source and the filter's circuits) R_{in} = 10mΩ, G = 6, other parameters according to Table 3. P_{out} = 600W. Matlab/Simulink simulation results.

significantly. When the converter should be designed without ferrite cores (e.g., for high temperature operation) the filter inductance can be achieved in air-based choke, similarly to the resonant inductors.

The input current ripples or a discontinuity occur in majority types of switching step-up converters. The problem exists in typical switch-mode DC-DC converters (e.g., the boost in DCM mode), pure SC converter as well as high-gain DC-DC converters which utilize inductors in a topology. In recent concepts of high voltage gain converters, presented in [2], [4] or [7] an AC component in the input current is clearly demonstrated. In the high-gain converter proposed for PV system in [8] the input current is not continuous as its topology contain the diode on the input which conducts in selected switching states. In [7] the pulsating current is indicated for some of the topologies from the presented family.

TABLE 4. Components of the experimental test setup.

Components and parameters common for all hardware variants		
Component / parameter		*Type / value*
Input capacitor	C_1	2 x 4.7 µF polypropylene and 100 µF electrolytic
Output capacitor	C_4, C_5	5.7 µF polypropylene and 100 µF electrolytic
Switched capacitors	C_2, C_3	4 µF bank composed of CERALINK devices
Inductors	L_1, L_2	Fixed inductor 1.9 µH Wurth 7443556190
PCB board		FR4 - 35µm
Switching frequency ($1/T_S$) in Fig. 3		37 kHz
First variant (V_{out} = 420 V):		
Diodes	D_1, D_2, D_3	SI Schottky STPS60SM200C (V_F=640 mV)
	D_4, D_5	SiC Schottky IDW20G65C5B (V_F=1.5 V)
Transistors	Q_1 - Q_5,	CoolMOS IPW60R070CFD7 ($R_{DS(on)}$=70 mΩ)
Second variant (V_{out} = 420 V):		
Diodes	D_1, D_2, D_3	SI Schottky STPS60SM200C (V_F=640 mV)
	D_4, D_5	SiC Schottky IDW20G65C5B (V_F=1.5 V)
Transistors	Q_1, Q_2, Q_3	SI MOSFET IXFH130N15X3 ($R_{DS(on)}$=9 mΩ)
	Q_4, Q_5	CoolMOS IPW60R070CFD7 ($R_{DS(on)}$=70 mΩ)
Third variant (V_{out} = 800 V):		
Diodes	D_1	SI Schottky STPS60SM200C (V_F=640 mV)
	D_2 - D_5	SiC Schottky IDW20G65C5B (V_F=1.5 V)
Transistors	Q_1 - Q_5	CoolMOS IPW60R070CFD7 ($R_{DS(on)}$=70 mΩ)

IV. EXPERIMENTAL RESULTS

The experimental research was performed in the setup and the parameters presented in Tab. 4.

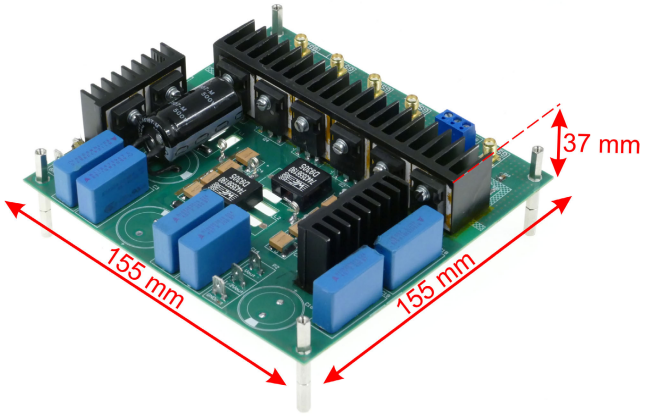

FIGURE 12. The laboratory experimental converter in the example configuration.

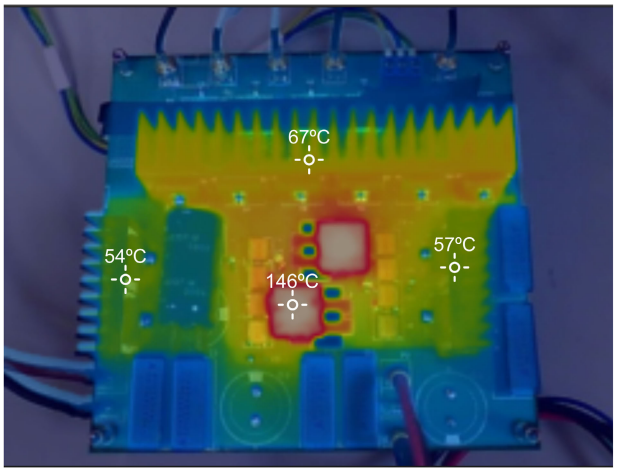

FIGURE 13. The thermographic result of the laboratory converter during the operation with $P_{out} = 600$W, $G = 6$ and $U_{in} = 70$V. No air flow forced.

The experimental tests of the proposed converter were carried out in order to verify the correct operation of the examined device. The ability to operate with the highest voltage gain (GU = 6), zero voltage switching feature as well as the output voltage adjustment was verified. Furthermore, design issues associated with efficiency of the converter are demonstrated. The converter's efficiency was tested in three configurations of selected switches and diodes (Tab. 4).

Fig. 12 presents the laboratory test setup of the converter. The converter is designed for convenient measurements rather than high volume. However, in the configuration with low output capacitances (as in the simulation results) it achieves the rated volumetric power density of 11 W/in^3 (calculated for P_{out} =600W).

Fig. 13 presents the thermographic result registered during the operation with P_{out} = 600W, G=6 and U_{in} = 70V. From this result it is also seen that the laboratory setup is oversized which gives the opportunity for further volume optimization. The only parts which reaches the limit of the temperature are resonant chokes, but heat sinks and PCBs can be considerably

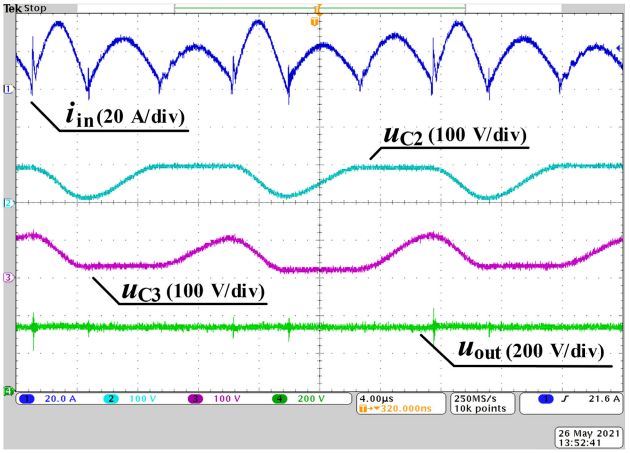

FIGURE 14. Steady state operation with the 1000 W input power. Waveforms of the input current, voltages on switched capacitors C_2 and C_3 and the output voltages for $U_{in} = 70$ V, $U_{out} = 340$ V.

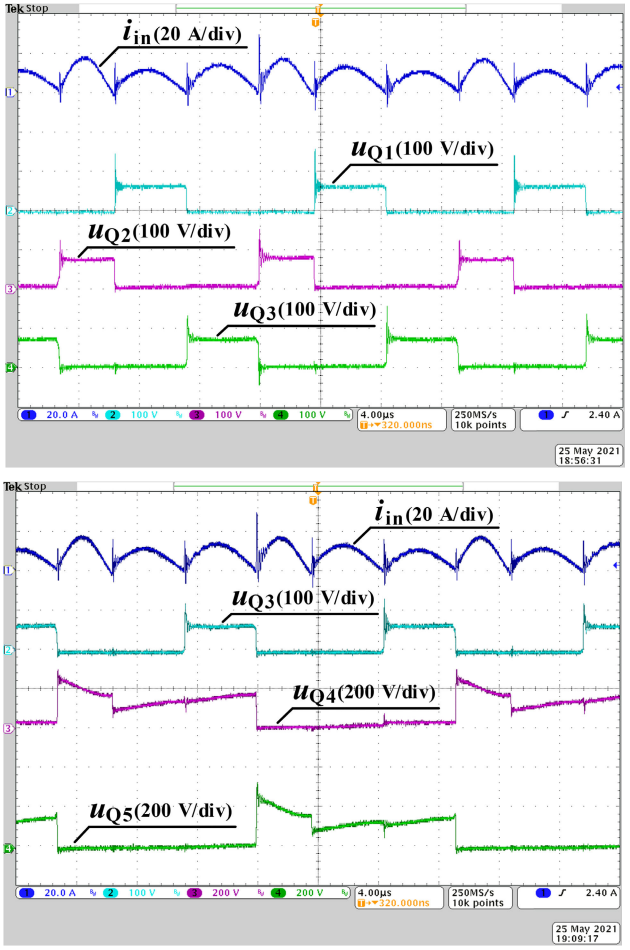

FIGURE 15. Voltage stresses on switches in a steady state. (a) Voltage on Q1, Q2 and Q3 switches (b) Voltage on Q3, Q4, and Q5 switches. $U_{in} = 70$ V, $U_{out} = 380$ V, $P_{out} = 620$ W.

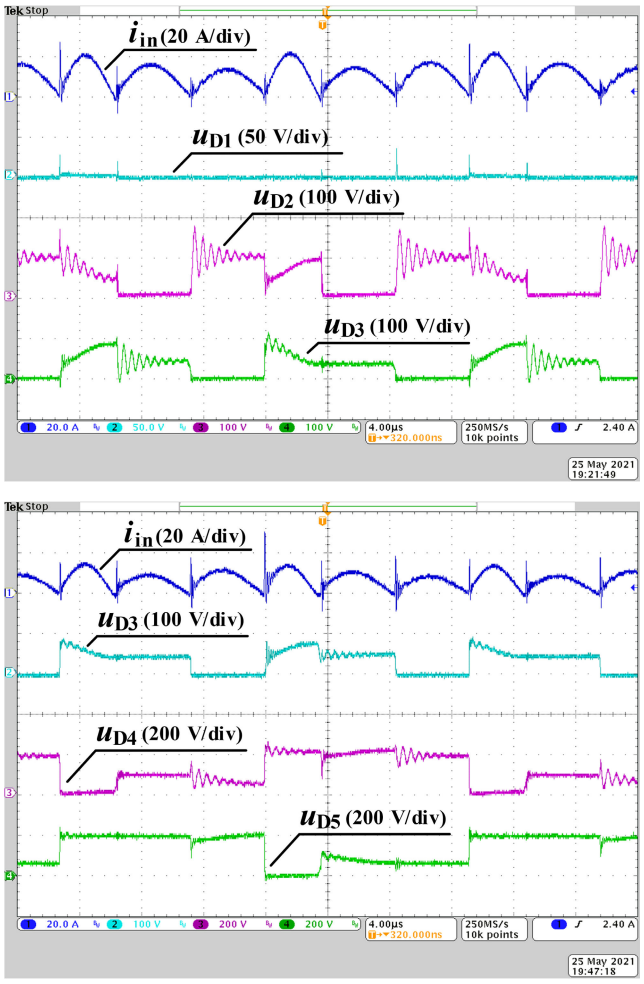

FIGURE 16. Voltage stresses on diodes in a steady state. (a) Voltage on D1, D2 and D3 diode (b) Voltage on D3, D4, and D5 diode. $U_{in} = 70$ V, $U_{out} = 380$ V, $P_{out} = 620$ W.

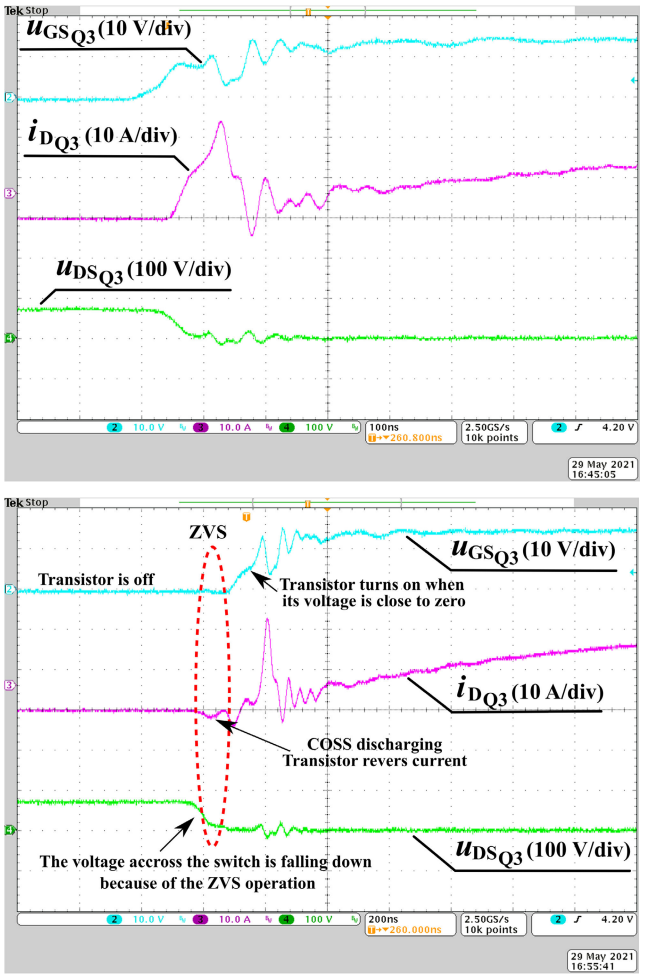

FIGURE 17. A detailed comparison of Q_3 transistor switching process in ZCS and ZVS operation mode of the converter. 2) Gate-source voltage of transistor Q_3, 3) Drain current of transistor Q_3 4) Drain-source voltage of transistor Q_3.

decreased in a low volume prototype (temperature of heat sinks are: ca. 60 °C). In the literature [40] an example power density of the SiC-based heat-sink less SC doubler which is 152 W/in^3.

A. HIGH-VOLTAGE GAIN OPERATION

The first set of the results (Figs. 14 - 16) presents waveforms that clearly illustrate the principle of operation of the proposed converter (ZCS mode). Those results prove that the converter is able to operate properly with the highest voltage gain value and the obtained waveforms are in in line with the concept and the simulations.

B. OPERATION IN ZERO VOLTAGE SWITCHING MODE (ZVS)

The next stage of the experimental research covered the verification of the converter operation in ZVS mode. Fig. 17 presents a comparison between ZCS and ZVS switching processes of the Q3 transistor in detail. In ZCS mode it is seen that the Q3 transistor turns on at a time when its drain-source voltage is relatively high. The output

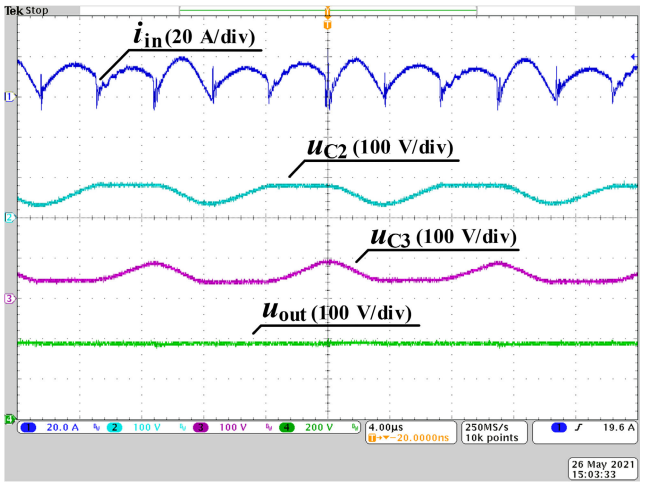

FIGURE 18. Steady state of converter operation in ZVS mode. waveforms of the input current voltages on switched capacitors C_2 and C_3 and the output voltages for $U_{in} = 70$ V, $U_{out} = 380$ V, $P_{out} = 620$ W.

capacitance is discharged in the transistor's structure during this process. The second oscillogram in Fig. 17 shows the

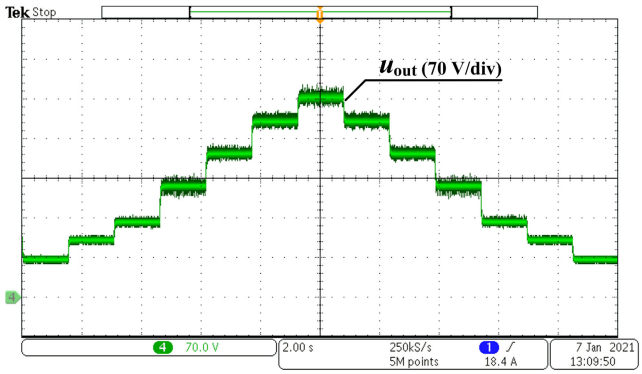

FIGURE 19. Level change of the output voltage by application of the adequate order of switching modes presented in Tab. 2.

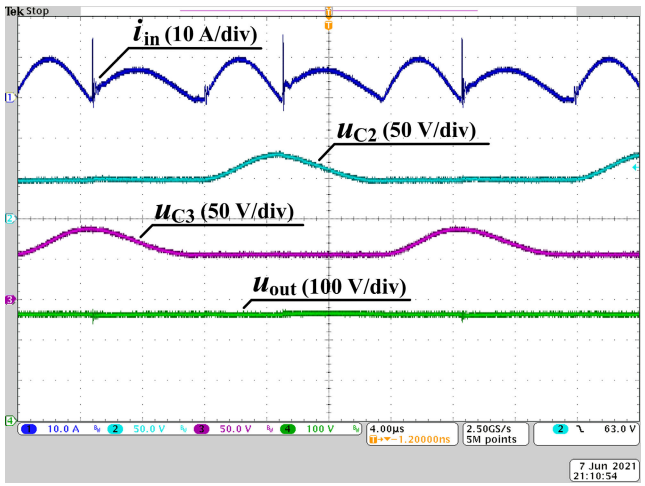

FIGURE 20. Steady state operation with the voltage gain $G = 4$. Waveforms of the input current, voltages on switched capacitors C_2 and C_3 and the output voltages for $U_{in} = 70$ V, $U_{out} = 270$ V, $P_{out} = 310$ W.

same switching process but in the case of converter operation in ZVS mode. In this case it is seen that the voltage on the Q3 switch is reduced to the value nearly equal to zero. It happens just before Q3 switch activation as it was assumed in section 2 (it is also expected that the current waveform in Fig. 17 is delayed several nanoseconds in relation to the drain-source voltage due to the current probe delay). Ringing which occurs after the turn-on process is significantly reduced in this case. The full operation cycle of the converter in ZVS mode is presented in Fig. 18. From those results it follows that the device works properly and the ZVS mode has any negative impact on the overall device operation.

C. VOLTAGE GAIN ADJUSTMENT

The ability of the output voltage adjustment has been verified in the experiment as well. The results obtained, presented in Fig. 19, confirms the concept of the output voltage change and the simulation results. During this test, the converter was loaded with 240 Ω of resistive load. The computation burden in the FPGA-based signal generator was not high. The required hardware resources were: 14% of available combinational functions and 3% of available logic registers for FPGA Cyclone III.

D. OPERATION WITH AN INTERMEDIATE VOLTAGE GAIN G=4

Fig. 20 presents waveforms in the case of operation with the four-fold voltage gain. The results confirm correctness of operation in the intermediate level.

E. EFFICIENCY AND VOLTAGE GAIN VS. OUTPUT POWER

Efficiency of the converter was tested in various configurations depending of selection of MOSFET transistors, diodes, switching methods and the input voltage. Even, when the converter operates with the output voltage above 400V ($U_{out} >$ 400V) three diodes can be selected as Schottky type due to low voltage stress (Tab. 4). Selection of switches should assume the trade of the C_{oss} and $R_{ds(on)}$ and was performed towards two figures of merit where the major optimization parameter is:

- Minimization of the output capacitance
- Minimization of the on-state resistance

In the first case all the transistors were selected as SJ MOSFET. In the second case, three switches (Q_1, Q_2, Q_3) were replaced by 200 V MOSFET with very low $R_{ds(on)}$. (Tab. 4). Comparison of the efficiency as well as the voltage gain versus the output power is presented in Figs. 21-25. The efficiency was further improved by introduction the method for ZVS in the converter which demonstrates that this concept is able to slightly increase converter efficiency especially in case of SJ MOSFET transistors utilization.

The efficiency and the converter output voltage versus the device output power have been registered with the utilization of the Yokogawa WT1800 power meter. Figs. 21-22 presents the measurements results which show that the peak efficiency for the converter equipped with SJ MOSFET transistors (Fig. 21) is ca. 91.5%, what has been obtained under the ZVS mode at the switching frequency $f_s = 48.7$ kHz. When the converter was controlled accordingly to ZCS method, it reaches of 91% efficiency at $f_s = 37$ kHz. In the case of the second variant of the converter's configuration (Tab. 4) the overall device efficiency rises up to 93% as a result of transistor conduction losses reduction (Fig. 22). ZVS operation mode of the converter brings insignificant improvement of the efficiency for higher power range. It was because standard MOSFET transistors usually have higher values of the output capacitance (C_{oss}) in comparison to the SJ devices. Furthermore, the converter's switching frequency was increased for ZVS operation. However, an increase of switching frequency allows to voltage ripples decrease on switched capacitors.

Fig 23. presents the results of the converter's efficiency examination in case of its operation with the output voltage value increased to 800 V (level of voltage adequate for some cases of a DC link configuration for inverters). this test the converter was configured accordingly to the third device variant (Tab. 4 – all SJ MOSFETS). A decrease of conduction

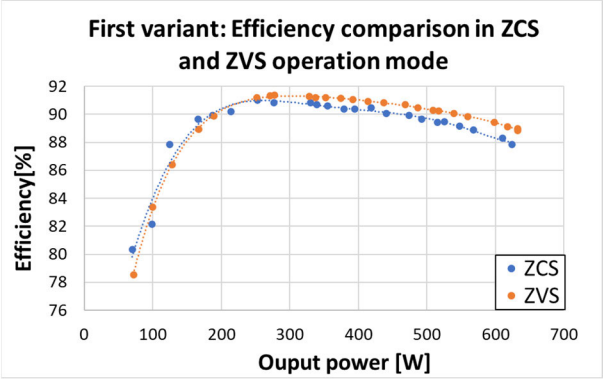

FIGURE 21. Converter efficiency comparison in case of its operation ZCS and ZVS mode. Hardware variant: *First* (Tab. 4), $U_{in} = 70$ V, $G = 6$.

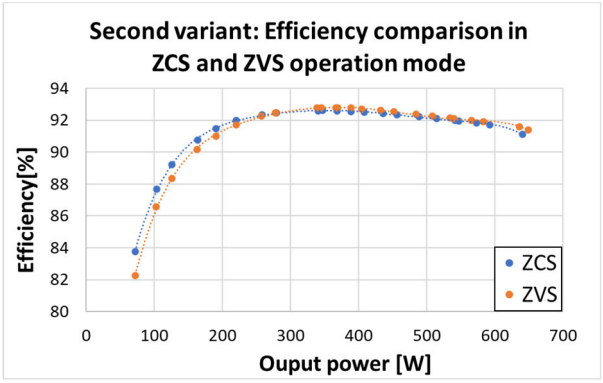

FIGURE 22. Converter efficiency comparison in case of its operation ZCS and ZVS mode. Hardware variant: *Second* (Tab. 4), $U_{in} = 70$ V, $G = 6$.

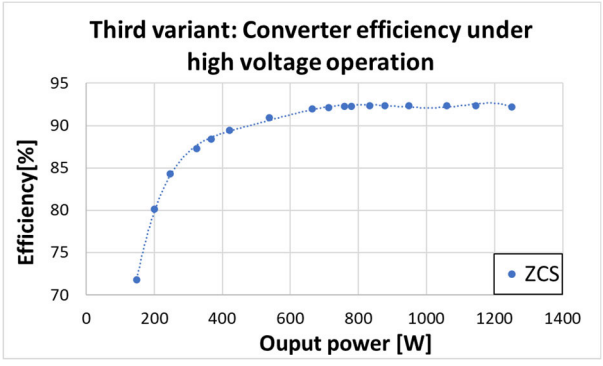

FIGURE 23. Converter efficiency under high voltage operation. Hardware variant: *Third* (Tab. 4), $U_{in} = 140$ V, $G = 6$.

losses exceeds an increase of C_{oss} losses in this test which shows higher efficiency of the converter and significantly higher power of the peak efficiency.

Beside the efficiency, during each test also converter output voltage was investigated. The results of it presents Fig. 24.

The efficiency and the converter output voltage versus the device output power have been registered with the utilization of the Yokogawa WT1800 power meter.

Efficiency of this converter can be further improved by:

- Decrease of parasitic resistances. The presented setup uses the 6-layer PCB board with 35 micrometer cooper width which is low-cost solution. In more expensive design application of the PCB board with e.g. 70 or 105 micrometer cooper width and larger number of layers could allow to decrease resistance of connections;
- Application larger amount of the switched capacitance. It allows to decrease switching frequency and losses. However, it increases cost of the converter and requires the design of the input filter for lower frequency which may increase it volume as well. Fig. 25 presents an impact of the switching frequency on the efficiency of the converter. A decrease of the switching frequency deteriorates the efficiency as the time period of the current oscillations becomes much shorter than the switching period. However, a decrease of the switching frequency together with an increase of the switched capacitance allows for the efficiency increase.
- Replacement the Q_4 and Q_5 switches by the devices with lower on-state resistance with comparable switching performance. For the tests results obtained in the setup in the second variant $R_{DS(on)} = 70$ mΩ for the Q_4 and Q_5 devices. In further tests the converter equipped with GaN Q_4 and Q_5 transistors could be tested (e.g. GS66516B with $R_{DS(on)} = 25$ mΩ). The decrease in transistor resistance results in converter efficiency increase. When the converter operates with the output

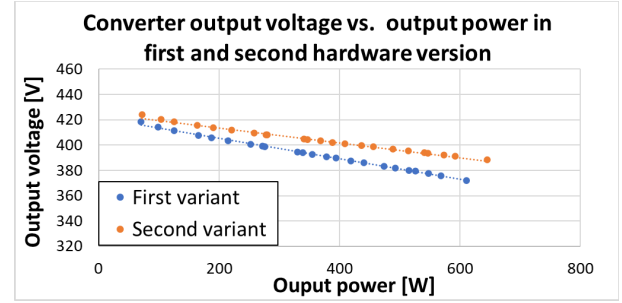

FIGURE 24. Efficiency and the output voltage of the converter versus the output power in two variants of the design (Tab. 4).

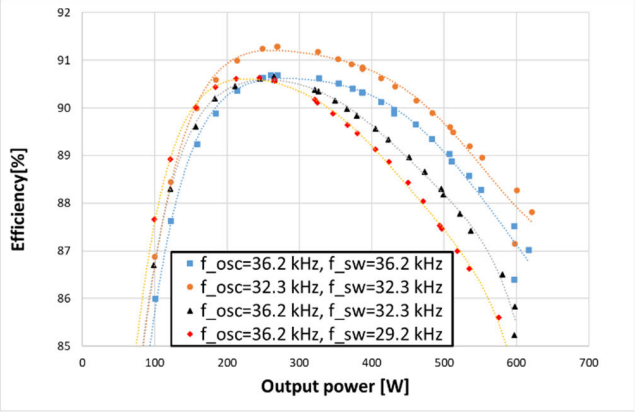

FIGURE 25. Efficiency of the converter versus the switching frequency and the switched capacitance. Hardware variant: *Second* (Tab. 4), $U_{in} = 70$ V, $G = 6$, ZCS.

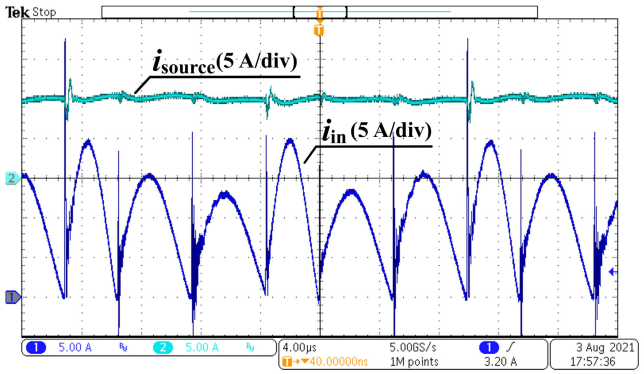

FIGURE 26. Experimental waveforms of the input current of the resonant cells (i_{in}) and the current of the source (i_{source}). Input capacitor $C_{in} = 102$uF, the filter inductor $L_{in} = 1.9$uH, $G = 6$, $P_{out} = 620$W, $f_s = 46$kHz.

TABLE 5. Comparison of parameters among high voltage gain sc converters.

Demonstrated parameters	Proposed	Ref. [18]	Ref [21]	Ref. [22]	Ref. [23] (Fig. 1b)	Ref. [29]	Ref. [30]	Ref. [37]
Gain	6	$2n$	6	7	4	n	3	2
Switch count	5	$4{\cdot}n{\cdot}p$	12	7	3	2	3	2
Diode count	5	0	0	5	5	$2(n-1)$	4	2
Voltage stress across switches	min: U_{in} max: $U_{out}/2$	min: U_{in} max: U_{out}/n	min: U_{in} max: $2U_{in}$	min: U_{in} max: $(4/7)U_{out}$	min: U_{in} max: $U_{out}/2$	U_{in}	min: U_{in} max: $2U_{in}$	U_{in}
Inductor count	2x 1.9µH	stray L only	stray L only	3x 2.97 µH	3x 0.5µH	1x 22µH	1x10µH, 1x2.5µH	1x 10.4 µH
Switched capacitor count	2	$2{\cdot}n{\cdot}p$	6	3	3	n-1	2	1
Output voltage control	+	-	-	-	-	+	+	+
Peak Efficiency [%]	92.8	96	96.5	91.9	91	97.6	95.7	99.2

n – number of series connected basic modules
p – number of interleaved converters
+ – possible characteristic

TABLE 6. Efficiency comparison to high voltage gain converters composed of sc technique and the inductor-based circuits.

Case	Reference number											
	Proposed	[2]	[4]	[5]	[6]	[7]	[9]	[11]	[12]	[13]	[15]	[16]
Max Efficiency [%]	92.8	94	93.7	96.1	97.4	96.7	95	92	90-93*	94.5	96	93

* Data estimated from a chart (93 % at low power, around 90% at rated power)

power $P_{out} = 600$W and the input voltage $U_{in} = 70$V, the RMS current of Q_4 and Q_5 switches is equal to 5 A (on the basis of waveforms from Fig. 6, where $i_{C4} = i_{Q5}$ and $i_{C5} = i_{Q4}$). A decrease in the $R_{DS(on)}$ resistance of these switches from 70 mΩ to 25 mΩ allows to reduce the overall power losses about 2.25 W.

The achieved efficiency is satisfied in comparison to others pure SC converters (Table 5), but also to recent concepts of high-gain converters with magnetic components. Efficiency comparison of the proposed converter with high voltage gain converters in topologies which integrates inductors and switched capacitors is presented in Table 5. From this comparison it is seen that the proposed converter efficiency is on the acceptable level among high voltage gain converters.

F. THE INPUT CURRENT

Fig. 26 presents waveforms of the input current of the switching cells (i_{in}) and the sources' current (i_{source}).

The converter operated with the 100uF of capacitor on the input and 1.9 μH input inductance (Fig. 26). The waveforms confirm the simulation results (Fig. 11) and show that at the applied switching frequency a very low volume inductance is sufficient for the effective source current filtering and the total volume of inductors remains on a very low level in the converter.

V. CONCLUSION

From the presented concept, analysis of the operation and results of the simulation and experiments performed, many following features of the proposed converter can be confirmed:

- The converter uses five switches and the voltage gains six-fold, which is an advantageous proportion in comparison to established SC topologies;
- Voltage stress on the switches are significantly below the output voltage, which is a positive characteristic from the cost, volume and efficiency point of view. In the converter with the output voltage 420 V three Schottky rectifiers were used. Operation with low voltage MOSFETs (200 V devices with very low $R_{ds(on)}$) was demonstrated as well.
- The ZVS can be implemented for some switching operations which decreases C_{oss} losses and can be especially important for operation with the high voltage gain. Operation with the switching frequency above the resonant frequency allows for efficiency improvement and EMI reduction associated with switching operations. The converter uses ZCS as well;
- The voltage gain of the converter may be fixed on seven levels, which is an important functional quality of a SC based system;
- The start of the converter may utilize the preliminary output capacitors charging and the gradual output voltage increase (appropriate steering pattern);
- The implementation of a switching algorithm according to the presented concepts is relatively simple;
- The converter is able to operate with low volume and low-cost resonant inductances. Energy is transferred through the switched capacitors. The resonant inductances (below 2 microhenry) are introduced to the circuits to avoid inrush currents. It is very positive characteristic in comparison to switch-mode DC-DC converters where ferrite-core chokes of several hundred microhenry may be required for demonstrating the similar range of power and voltages;
- Efficiency of the converter reached nearly 93% for $G = 6$. That is good result and it could be further improved by parasitic resistances reduction. It the

presented setup the converter was assembled on the 6-layer PCB board about 35 micrometer cooper width. Such an approach demonstrates a low-cost implementation of the kW scale converter but it can introduce the considerable amount of parasitic resistance;

- A decrease of switching frequency allows for the efficiency of the converter improvement. However, it increases the prospective cost of an input filter and switched capacitors.

The presented features from this concept shows that the converter incorporates various required qualities such as high voltage gain, low number of switches, low voltage stress on switches, ZVS/ZCS transition, high efficiency, variable voltage gain and quasi inductiveless design.

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