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Current Reused 8:1 Injection Locked Frequency Divider Using Unbalanced Ring Oscillator Frequency Divider

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ABSTRACT This paper proposes and analyzes a CMOS divide-by-8 injection locked frequency divider (ILFD) with a divide-by-2 ring oscillator stacked on a capacitive cross-coupled oscillator used as an *LC* divide-by-4 ILFD. The divide-by-8 ILFD in the TSMC 0.18 μm 1P6M CMOS process has a locking range from 15.5 GHz to 17.8 GHz at the power consumption of 10 mW. The varactorless divide-by-8 ILFD occupies a small area of 0.8044×0.72 mm^2. The ILFD can be used in divide-by-4 mode and has a locking range from 4.8 GHz to 10.6 GHz at the power consumption of 10.43 mW. The ring oscillator based frequency divider (FD) is designed with a pair of differential outputs so that the whole divide-by-8 ILFD provides differential output. The ring oscillator FD uses unbalanced component parameters to optimize the circuit performance and it supplies two unbalanced tail currents to the *LC* ILFD, which also provide unbalanced outputs despite the circuit topology is a symmetric one. The unbalanced approach offers design flexibility.

INDEX TERMS CMOS, ring oscillator, divide-by-8 injection locked frequency divider, harmonic mixer, locking range.

I. INTRODUCTION

DIVIDE-by-eight frequency dividers (FDs) are used in sliding-IF receivers [1], [2] and phase-locked loops as shown in Fig. 1 [3], [4]. Normally they can be designed with three ÷2 current mode logic (CML) flip-flop-based frequency dividers (FDs) [5]–[7] or three ÷2 LC-tank injection-locked frequency dividers (ILFDs). The former has the merit of wide locking range without frequency tuning mechanism and compact size but it expenses high energy at very high frequencies. The latter consumes low power at high frequency, but it occupies larger area at low frequency. Hybrid combination of CML, *LC* ILFD and other FDs take advantage of each circuit technology, and high-modulus ILFD with high input frequency, low output frequency and small die area can be designed.

This paper designs a hybrid current reused divide-by-8 ILFD. The designed ÷8 ILFD uses an *LC* tank ÷4 sub-ILFD stacking below a low frequency ÷2 sub-FD. Three shunt ÷2 sub-FDs perform the divide-by-8 function at low supply voltage. Three stacking ÷2 sub-FDs are not preferred because of voltage headroom caused by each sub-FD. Many possible current- reused circuit topologies are shown in Fig. 2. The first ÷8 ILFD in Fig. 2(a) uses a high frequency ÷2 ILFD followed by a low frequency ÷4 ILFD. The external injection signal is applied to the ÷2 ILFD with an output used as the input of the ÷4 ILFD, which provides the low frequency output signal. The second circuit shown in Fig. 2(b) shows a divide-by-8 ILFD with a high frequency ÷4 ILFD followed by a low frequency ÷2 ILFD. The two ILFDs affect each other. Fig. 2(c) and Fig. 2(d) are obtained from Fig. 2(a) and Fig. 2(b) respectively by switching the locations of ÷4 ILFD and ÷2 ILFD. Two sub-FDs share the same dc current path for current reuse and concurrent design of the two sub-FDs are mandatory, because the amount of common current affects the voltage headroom (V_{DD} -V_{DF}) and V_{DF}. Pure *LC* type current-reused ÷8 ILFD [8], [9] uses the circuit architecture in Fig. 2(b) with a high frequency ÷4 ILFD stacked under a

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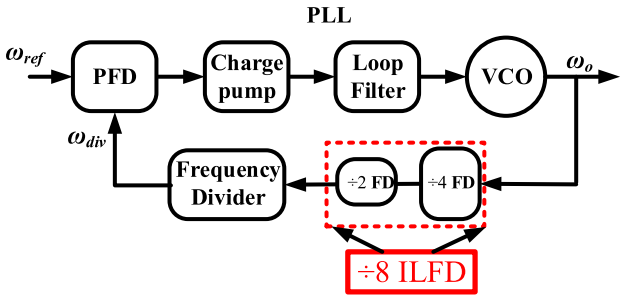


FIGURE 1. Block-diagram of a typical high-speed PLL.

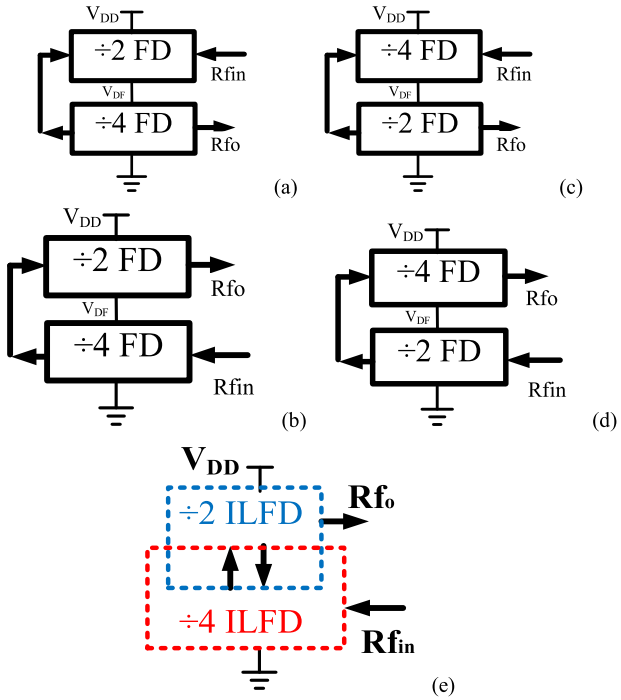


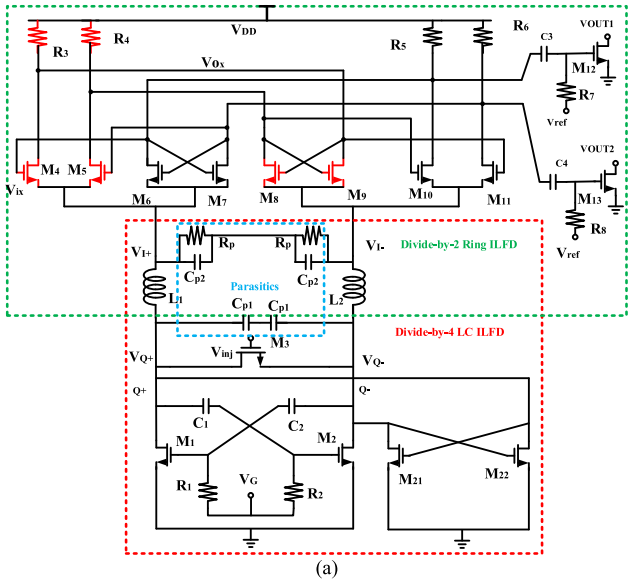
FIGURE 2. Block diagram of current–reused divide-by-8 FDs. Rf_{in}: input signal. Rf_o output signal. The arrows indicate the signal flow direction.

low frequency ÷2 ILFD. The frequency alignment between two sub-ILFDs and die area deserve the attention. A ÷8 regenerative frequency divider [10] has wide locking range at the cost of high power consumption.

This paper proposes a ÷8 *LC* ILFD with the architecture shown in Fig. 2(e) using a tail-injected ring oscillator based divide-by-2 FD stacking on a high frequency capacitive cross-coupled direct injection divide-by-4 *LC* ILFD. Both sub-FDs shares some components. The ring oscillator based FD has wide locking range to relax the problem of frequency alignment between two sub-FDs. Even with Fig. 2(b) or Fig. 2(e) there are many design options for the tail-injected divide-by-2 FD. Naturally, we may opt to the sub-circuits with differential outputs as an example shown previously [8], [9]. In this work, we design the ring oscillator based FD with unbalanced component parameters to optimize the circuit performance and the FD provides a pair of differential outputs. The *LC* FD uses a balanced schematic, but it provides two unbalanced outputs, which is caused by the unbalanced tail currents driving the *LC* FD. The measured locking range of the proposed current reused ÷8 ILFD at 0 dBm input power is 2.3 GHz, from the incident frequency 15.5 GHz to 17.8 GHz at the power consumption of 10 mW. The newly designed circuit is also used as a ÷4 ILFD with wide locking range while the *LC* FD serves as a ÷2 ILFD. Finally the explanation of the circuit operation principle is verified by simulated and experimental results.

II. CURRENT REUSED CIRCUIT

The whole designed ÷8 CMOS ILFD circuit is depicted in Fig. 3(a). The circuit consists of a low frequency tail injection ÷2 ring oscillator and a high frequency direct-injection ÷4 *LC* ILFD. The output of the latter is used as the input of the former. No buffer stage between the two FDs is used. This can improve the locking range of ÷4 *LC* ILFD because of less capacitive loading. The output of 8:1 ILFD is taken from the buffer output of the low frequency FD.



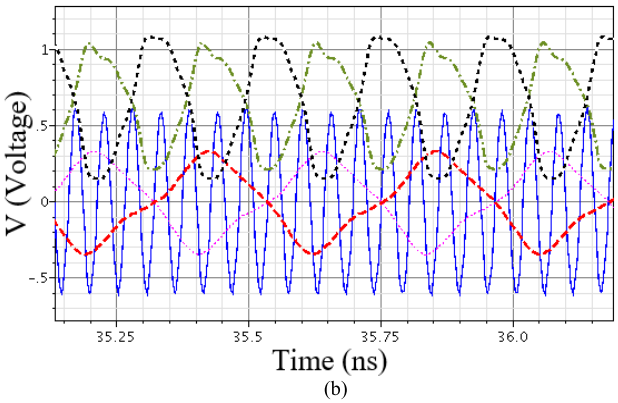


FIGURE 3. (a). Schematic of the studied ÷8 ILFD. (b). Simulated voltage transients for the ÷8 ILFD in CMOS. V_{DD} = 1.4V, V_G = 0.6 V and V_{inj} = 1.0 V. V_{buffer} = 0.8 V, V_{ref} = 0.8 V. Injection frequency f_{inj} = 18.6 GHz and injection power P_{inj} = 0 dBm. Red: (V_{OUT1}, V_{OUT2}). Black and green: (V_{Q+}, V_{Q-}). Solid blue: injection signal.

The ÷4 *LC* ILFD is made of the FET pair (M_1, M_2), a direct injection FET M_3 used as harmonic mixer, and a resonator composed of inductors L_1 and L_2, C_{p1}, a parasitic capacitor in shunt with the drains of the switching FETs with dc gate bias V_G and C_{p2}, a parasitic capacitor connected between the outputs of inductors L_1 and L_2. C_{p2} is due to the source to ground capacitance associated with the ring FETs. In general C_{p2} can be replaced by an admittance composed of C_{p2} and R_{p2} representing the parasitic due to the ring oscillator circuit. (C_1, C_2) are dc isolation capacitors and (R_1, R_2) are dc biasing resistors. M_3 with dc gate bias V_{inj} accepts a gate injection signal. The direct FET pair (M_{21}, M_{22}) are also used to provide energy to the resonator. By controlling the gate bias V_G the tradeoff between the power consumption and locking range can be pursued.

The low frequency ÷2 FD consists of a ring oscillator and an injection composite. In the ring oscillator, the circuits consists of two delay stages and the components in red color are the first subcircuit and the black counterparts are the 2nd subcircuit. M_4 and R_3, M_5 and R_4 form the first differential amplifier. The pair (M_8, M_9) is a negative resistance. M_{10} and R_5, M_{11} and R_6 form a second differential amplifier and the pair (M_{10}, M_{11}) is a negative resistance. The output of the 2nd amplifier is used as the input of the 1st amplifier and the output of the 1st amplifier is used as the input of the 2nd amplifier, this inverted connection generates required phase delay for oscillation. Transistors (M_{12}, M_{13}) are buffers with dc gate bias V_{ref}. (C_3, C_4) are dc isolation capacitors and (R_7, R_8) are dc biasing resistors. The injection method can be a direct injection approach or a tail injection method. The latte approach is used for simple bias structure. Two similar stages injected by signals with differential phases provided by the ÷4 *LC* ILFD, the output frequency of the low frequency FD is precisely locked to half of the injection frequency. The input signals (V_{I+}, V_{I-}) are from the inductors of the ÷4 *LC* ILFD. Parasitic C_{p2} affects the current injection to the ring oscillator, the locking range of ring oscillator and the free running oscillation frequency of *LC* ILFD. Fig. 3(b) shows simulated voltage transients for the ÷8 ILFD. Two outputs (V_{Q+}, V_{Q-}) of *LC* ILFD are unbalanced, this is caused by the unbalanced current through inductors L_1 and L_2. The outputs (V_{OUT1}, V_{OUT2}) of ÷8 ILFD buffers are differential. The whole designed ILFD circuit in Fig. 3(a) also can be used as a ÷4 CMOS ILFD circuit by using the *LC* ILFD as a ÷2 ILFD, where M_3 plays the role of linear mixer with higher dc gate bias than that used for the ÷4 LC ILFD. Table 1 shows the design parameters for comparison of four ÷4 ILFDs with same architecture as shown in Fig. 3(a) by varying ring oscillator component parameters. In Case 1, the ILFD outputs are asymmetric (V_{Q+}, V_{Q-}) and has the largest locking range percentage, so these parameters are used to design the ÷8 *LC* ILFD. Case 4 is a large locking range ÷4 ILFD with differential outputs.

The free running oscillation frequency of the ÷4 *LC* ILFD is designed to align to the center frequency of ÷2 frequency divider. According to the simulation at $V_{DD} = 1.4$ V and $V_{inj} = 1.0$ V, the dc drain bias V_{I+} for the *LC* ILFD at $V_G = 0.6$ V is about 0.726 V, the free running *LC* ILFD oscillation frequency is 4.59 GHz. The ÷8 locking range is from 17.7 GHz to 19.1 GHz. According to the symmetric design Case 4 at $V_{DD} = 1.4$ V and $V_{inj} = 1.0$ V, the dc drain bias V_{I+} for the *LC* ILFD at $V_G = 0.6$ V is about 0.699 V, the free running *LC* ILFD oscillation frequency is 4.799 GHz. The locking range is from 18.8 GHz to 19.8 GHz.

TABLE 1. Design parameters and performance of 4 simulated ÷4 *LC* ILFDs.

Design Parameters of Proposed FD Case 1 (asymmetric) W/L=		Parameters of Simulated FD Case 2 (symmetric)	
$M_{1,2}$	70/0.18 μm	$M_{1,2}$	70/0.18 μm
M_3	40/0.18 μm	M_3	40/0.18 μm
$M_{4,5,6,7}$	96/0.18 μm	$M_{4,5,10,11}$	48/0.18 μm
$M_{8,9,10,11}$	48/0.18 μm	$M_{6,7,8,9}$	96/0.18 μm
$M_{12,13}$	160/0.18 μm	$M_{12,13}$	160/0.18 μm
$M_{21,22}$	32/0.18 μm	$M_{21,22}$	32/0.18 μm
$R_{1,2,3,4}$	150 Ω	$R_{1,2,3,4}$	150 Ω
V_{DD}	1.4 V	V_{DD}	1.4 V
Lock Range (GHz)	5.4~13(82.6%)		4.8~10.8 (76.9%)
Parameters of Simulated FD Case 3 (asymmetric)		Simulated Parameters Case 4 (symmetric)	
$M_{1,2}$	70/0.18 um	$M_{1,2}$	70/0.18 um
M_3	40/0.18 um	M_3	40/0.18 um
$M_{4,5,6,7}$	48/0.18 um	$M_{4,5,10,11}$	96/0.18 um
$M_{8,9,10,11}$	96/0.18 um	$M_{6,7,8,9}$	48/0.18 um
$M_{12,13}$	160/0.18 um	$M_{12,13}$	160/0.18 um
$M_{21,22}$	32/0.18 um	$M_{21,22}$	32/0.18 um
Lock Range (GHz)	5.4~12.8(81.3%)		5.8~13.2(76.6%)

The resonator of the ÷4 *LC* ILFD can be transformed to a parallel *RLC* network if C_{p2} is large to ensure the swing signal $V_{Q+} > V_{I+}$, and this has been verified by the simulation in the present design. According to the equivalent parallel *RLC* resonator, the locking range (LR) of the ÷4 ILFD is derived as [11]

$$\omega - 4\omega_o = \frac{2\omega_o}{Q}\frac{I_{inj}/I_{OSC}}{\sqrt{1-[I_{inj}/I_{OSC}]^2}} \tag{1a}$$

$$Q = \frac{R_{inj}}{\omega L_1} \quad \omega_o = \frac{1}{\sqrt{C_{p1}L_1}} \tag{1b}$$

R_{inj} is the channel resistance of injection MOSFET. I_{inj} is the fundamental injection current of injection MOSFET, and I_{osc} is the fundamental drain current ($I_{D1} + I_{D2}$) of MOSFETs M_1 and M_{22}. Changing V_G shifts the drain current I_{D1} of M_1 and the injection current I_{inj} because the variation of ILFD voltage swing. If R_p is considered, then the admittance of the network C_{p2}, R_p, and L_1 is

$$Y_{in1} = \frac{1}{sL_1 + \frac{1}{G_p + sC_{p2}}} \equiv g_{eq} + \frac{1}{sL_{eq}} \tag{2a}$$

$$Y_{in1} = \frac{G_p\{1-\omega^2 L_1 C_{p2} + \omega^2 C_{p2} L_1 G_p\}}{[(1-\omega^2 L_1 C_{p2})]^2 + \omega^2\{L_1 G_p\}^2} - s\frac{G_p L_1 G_p - C_{p2}(1-\omega^2 L_1 C_{p2})}{[(1-\omega^2 L_1 C_{p2})]^2 + \omega^2\{L_1 G_p\}^2} \tag{2b}$$

Then the locking range in (1b) is modified as

$$Q = \frac{1/(1/R_{inj} + G_{eq})}{\omega L_{eq}}, \quad \omega_o = \frac{1}{\sqrt{C_{p1} L_{eq}}} \tag{3}$$

If the locking range (LR) of the ÷4 ILFD falls in the locking range of the ÷2 ring oscillator, then the ÷8 LR is determined by the ÷4 LR. Therefore it is important to get wide locking range for the *LC* ILFD. Eq. (1a) is an approximation because it is based on balanced ILFD output voltages.

In Fig. 3(a), the peak-to-peak voltage of V_{Q+} is larger than that of V_{I+}. As V_G increases, the swing of V_{Ox} increases because of high drain current, the startup dc value of V_{Q+} decreases, the oscillation frequency increases because the gate overdrive of M_1 increases. To offset the tuning of V_G, the voltage V_{inj} decreases to maintain the gate overdrive of M_1 at a fixed value for maximum locking range of the ÷4 *LC* ILFD because the locking range is dependent on the gate overdrive of injection MOSFET. As V_G increases, the dc voltage of ($V_{DD} - V_{I+}$) increases, the ring oscillator property shifts. The channel width of M_1 is 32 μm and the channel width of M_{21} is 70 μm. M_{21} has high dc-ac power conversion efficiency than M_1 because of lower dc gate bias. It is well known that class *C* amplifier has higher efficiency than class *AB* amplifier because of lower dc gate bias.

The whole circuit in Fig. 3(a) can be used as a divide-by-4 ILFD. In the past many ÷4 CMOS ILFD have been proposed [12]–[15]. Harmonic mixer approach were used in [12], [13]. Linear mixer approach was used in [14] and current reuse approach was used in [15] with two ÷2 FDs. In this operation mode, the injection FET is used as a linear mixer.

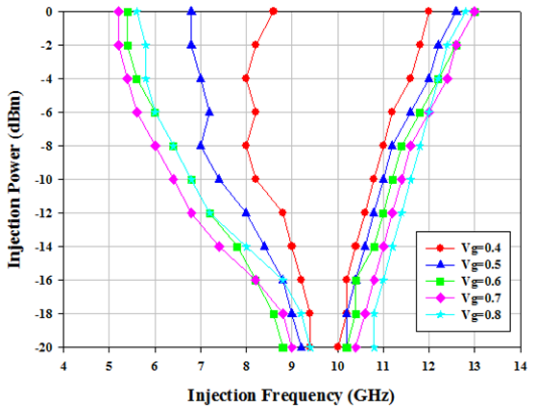


FIGURE 4. Simulated input sensitivity. V_{DD} = 1.4V, V_G = 0.4 V~0.8 V and V_{inj} = 1.2 V. V_{buffer} = 0.8 V, V_{ref} = 0.8 V. ÷4 ILFD.

Fig. 4 shows the simulated input sensitivity for the ÷4 ILFD biased at V_{DD} = 1.4V, V_G = 0.4 V~0.8 V, V_{inj} = 1.2 V, V_{buffer} = 0.8 V, and V_{ref} = 0.8 V. The simulated ÷4 locking range at V_G = 0.65 V is from 5.2 GHz to 13.3 GHz. At V_G = 0.4 V M_1 and M_2 are biased in the class-C mode. The simulated locking range at V_G = 0.5 V is from 8.2 GHz to 12.8 GHz. Locking range at V_G = 0.7 V is maximum, away from V_G = 0.7 V the locking range decreases, this explains the measured V_G-dependent locking range shown later. V_G is used to control the ration of I_{inj}/I_{osc} used in Eq. (1a).

Now we separately analyze the ring oscillator FD and *LC* ILFD. Fig. 5 shows schematics of ring oscillator. Fig. 5(a) is a simplified version of ring oscillator in [16]. Fig. 5(b) is modified from Fig. 5(a) by replacing pMOSFEs ($M_{R3} \sim M_{R6}$) with resistors ($R_3 \sim R_6$). A direct injection ring oscillator FD is obtained by using a pair FETs in shunt with drains of (M_4, M_5) and (M_{10}, M_{11}). A tail-injection ring-oscillator FD is obtained by using a pair of FETs in series with sources of (M_4, M_5, M_6, M_7) and (M_8, M_9, M_{10}, M_{11}). Fig. 5(c) shows a quarter-circuit small-signal equivalent circuit of Fig. 5(b). Because the pairs (M_4, M_5) and (M_6, M_7) are differential the common–source node of these FETs is a common ground for the fundamental, the ratio of output voltage to the input voltage for the first amplifier stage is

$$\frac{v_{ou1}}{v_{in}} = \frac{-g_{m4}}{sC_{L1} + g_4 - g_{m6}} \tag{4}$$

where V_{in} is the input voltage of M_4 with transconductance g_{m4} and V_{ou1} is the output voltage. g_{m6} is the transconductance of M_6 and C_{L1} is the capacitive load of M_4, g_4 is the inverse of R_4. Similarly, the ratio of the second stage is

$$\frac{v_{ou2}}{v_{ou1}} = \frac{-g_{m10}}{sC_{L2} + g_{10} - g_{m8}} \tag{5}$$

g_{m8} (g_{m10}) is the transconductance of M_8 (M_{10}) and C_{L2} is the capacitive load of M_8, g_{10} is the inverse of R_{10}. Applying

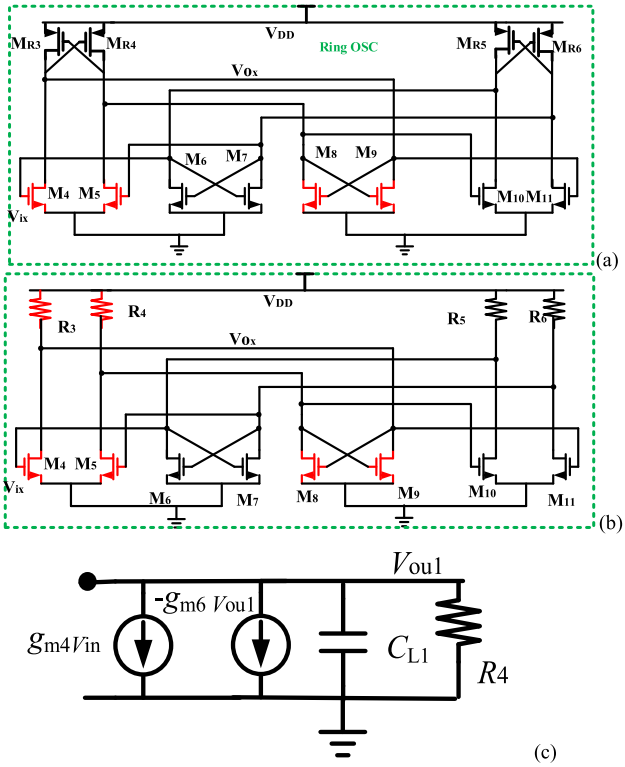


FIGURE 5. Schematics of ring-oscillator (a) and (b). Equivalent circuit (c).

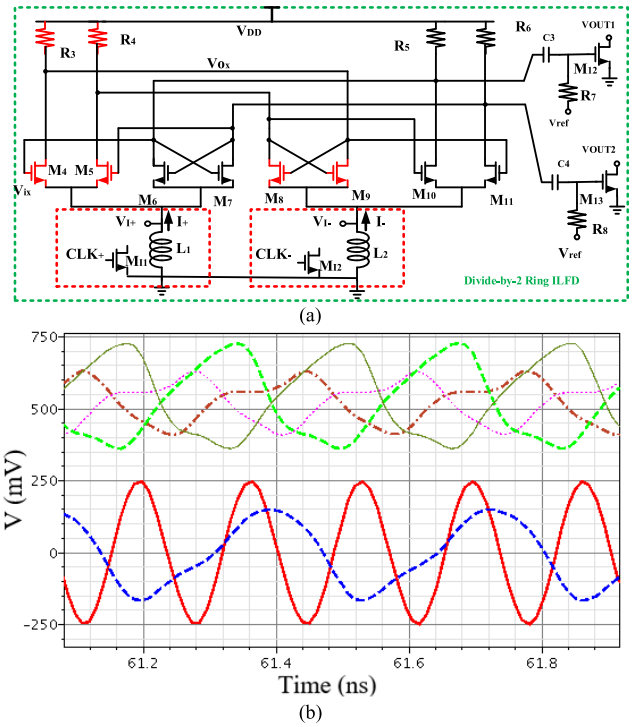


FIGURE 6. (a). Schematic of the ring oscillator based ÷2 FD. (b). Simulated voltage transients of the ÷2 FD. $V_{DD} = 0.75$ V. $V_{buffer} = 0.8$ V, $V_{ref} = 0.8$ V. $f_{inj} = 6$ GHz and injection power $P_{inj} = -5$ dBm. Blue: V_{OUT1}. Red: injection signal. Tope four curves are drain voltages of M_4, M_5, M_{10}, and M_{11}.

the phase criteria for oscillation, we can get the oscillation frequency

$$\omega = \sqrt{\frac{(g_{10} - g_{m8})(g_4 - g_{m6}) + g_{m10}g_{m4}}{C_{L1}C_{L2}}} \tag{6}$$

The oscillation frequency f_{OSC} increases by decreasing C_{L2} and increasing transconductance such as g_{m4}.

Fig. 6(a) shows schematic of ring oscillator ÷2 FD with tail inductors L_1 and L_2. It is different from Fig. 5(a) and Fig. 5(b) because of L_1 and L_2 and one buffer stage. Under normal operation, the circuit provides free running signal. Tail injection forces the circuit become an injection locked oscillator. Capacitive coupled injection signals (V_{I-}, V_{I+}) are applied to inductors L_1 and L_2. Alternatively FETs (M_{I1}, M_{I2}) replace inductors L_1 and L_2 and are used to converter the voltage signal (CLK$_-$, CLK$_+$) to current signal (I$_-$, I$_+$). The present simulation uses the tail inductor method. The speed and division bandwidth depend on the value of ring components. In a symmetric design approach, the first subunit and the 2nd subcircuit use the same circuit components, and the ring oscillator ÷2 FD and its derivative ÷8 ILFD can provide quadrature outputs. Alternatively, the ÷2 FD and its derivative ÷8 ILFD will provides differential outputs, because the two pairs of ring oscillator output voltages are unbalanced and the 1st and 2nd subcircuits use different circuit components. This also fits the design with the ring oscillator FD using only two output buffers. Fig. 6(b) shows the simulated voltage

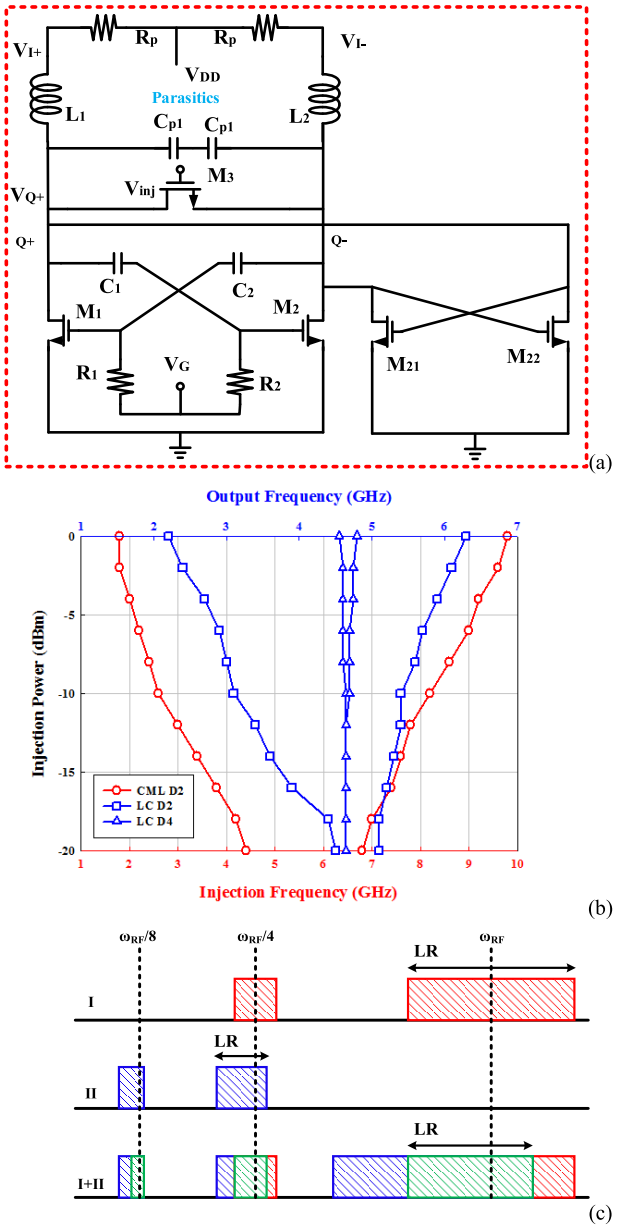


FIGURE 7. (a) Schematic. (b) Simulated output sensitivity of the *LC* ILFD. $V_{DD} = 0.75$ V, $V_G = 0.6$ V and $V_{inj} = 1.2$ V. $R_p = 20$ Ω. ÷2 *LC* ILFD. Simulated input sensitivity of the ring-oscillator FD. $V_{DD} = 0.75$ V, $V_B = 0.8$ V and $V_{ref} = 0.8$ V. (c) Locking ranges of the ÷8 ILFD.

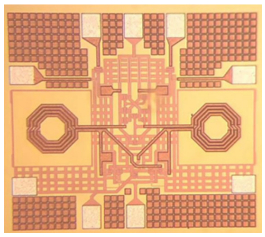


FIGURE 8. Chip micrograph of the ÷8 ILFD.

waveforms. The component parameters are the same as those used in the designed ÷8 ILFD. The drain voltages of M_4, M_5, M_{10}, and M_{11} are asymmetric because of unbalanced

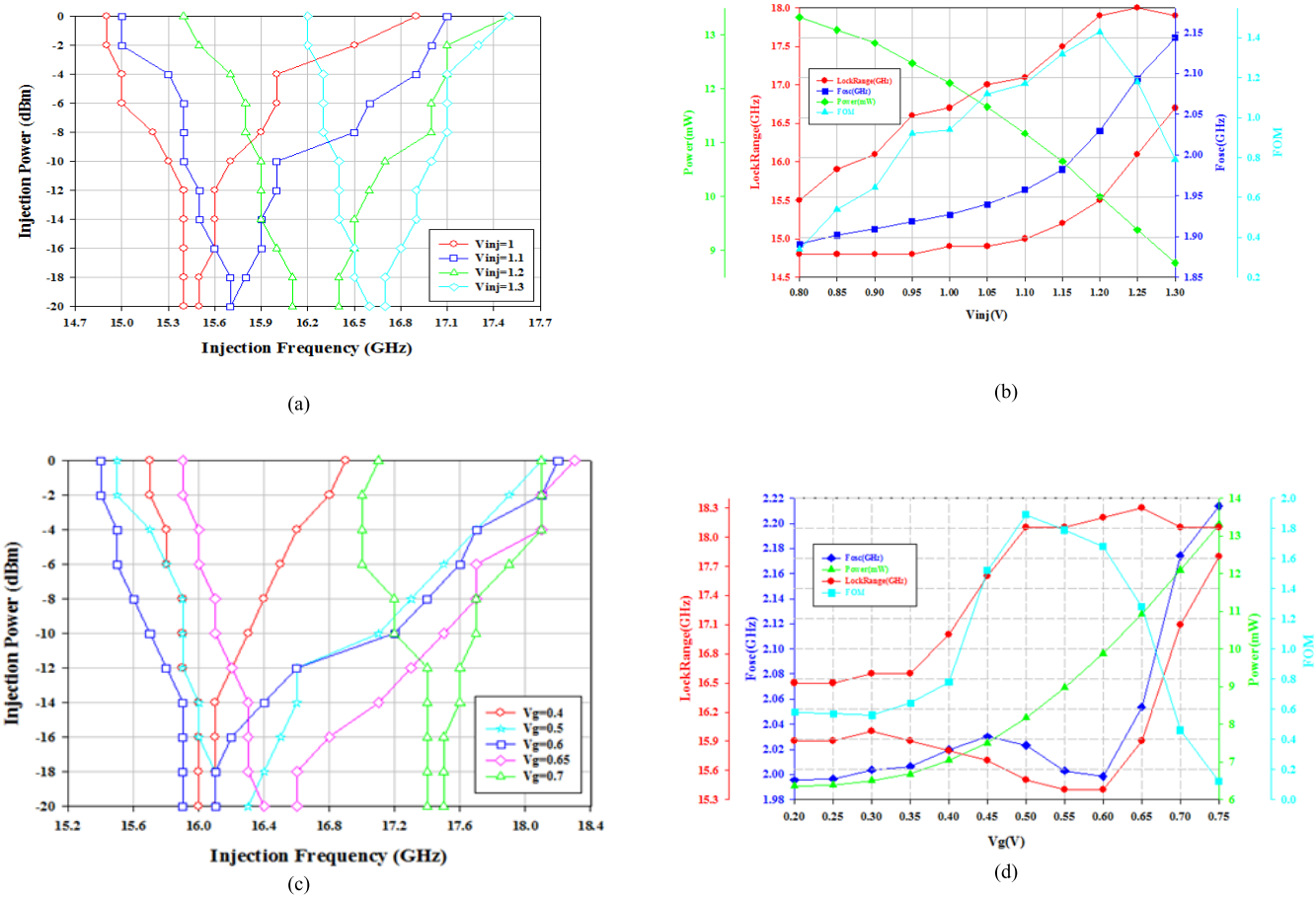


FIGURE 9. (a). Measured input sensitivity for the ÷8 ILFD. V_{DD} = 1.4 V, V_G = 0.6 V and V_{inj} = 1.0V ~1.4 V. V_{buffer} = 0.8 V, V_{ref} = 0.8. V. (b). Measured oscillation frequency, power consumption, locking range at 0 dBm and FOM versus injection gate bias. V_{DD} = 1.4 V, V_G = 0.6 V and V_{inj} = 0.8 V ~1.3 V. V_{buffer} = 0.8 V, V_{ref} = 0.8 V. ÷8 ILFD. (c). Measured input sensitivity for the ÷8 ILFD. V_{DD} = 1.4 V, V_G = 0.4 V ~0.7 V and V_{inj} = 1.2 V. V_{buffer} = 0.8 V, V_{ref} = 0.8 V. (d). Measured oscillation frequency, power consumption, locking range at 0 dBm and FOM versus switching gate bias. V_{DD} = 1.4V, V_G = 0.15 V ~ 0.75 V and V_{inj} = 1.2 V. V_{buffer} = 0.8 V, V_{ref} = 0.8 V. ÷8 ILFD.

device parameters. In appendix, the operation principle of ring-oscillator in the ÷8 FD is more closely described.

The input locking range of an ILFD is defined as the input frequency range in which the ILFD is able to divide properly the frequency of the incoming signal by the desired ratio. The output locking range is equal to the input locking range divided by the division ratio. Fig. 7(a) shows one ÷2 *LC* FD schematic and its simulated output sensitivity of the *LC* ILFD with the same components and sizes as the counterparts shown in Fig. 3(a). $R_p = 20\ \Omega$ is used to consider the effect of R_p in Fig. 3(a), the simulated locking range is from 2.2 GHz to 6.4 GHz. Fig. 7(b) also shows the input sensitivity of the ring oscillator FD shown in Fig. 6(a). This indicates that the output locking range (LR) of the ÷2 (÷4) *LC* ILFD falls in the locking range of the ÷2 ring FD, the LR is limited by the ÷2 LR of *LC* ILFD. In general, the ring oscillator FDs achieve a wide bandwidth and is more robust to the process variations than other types of FDs at low-to-medium range of frequencies. Fig. 7(c) shows the frequency alignment method of the two sub-FDs. The first I-plot shows the input locking range (LR) and output frequency of the ÷4 ILFD. The II-plot shows the input locking range (LR) and output frequency of the ÷2 FD. The III-plot shows the input locking range (LR) and output frequency of the ÷8 ILFD. The green frequencies represent the effective ÷8 locking range, the output frequency range of the ÷4 ILFD and the output frequency range of the ÷2 ILFD. A good design is to avoid false locking by designing larger locking range for the divide-by-4 ILFD and ensuring less frequency mismatch between the two subFDs without increased power consumption. Fig. 7(b) indicates a good design robust to frequency misalignment.

III. MEASUREMENT OF THE ILFD

The ÷8 ILFD has been designed and fabricated in the TSMC 0.18 μm 1P6M CMOS technology. The die micrograph occupying an area of 0.8044 × 0.72 mm^2 is shown in Fig. 8. Fig. 9(a) shows the measured input sensitivity for the ÷8 ILFD biased at V_{DD} = 1.4 V, V_G = 0.6 V, V_{inj} = 1.0 V ~ 1.4 V, V_{buffer} = 0.8 V, and V_{ref} = 0.8 V. At V_{inj} = 1.1 V, an external injected signal power P_{inj} of 0 dBm provides one locking range from 15 GHz to 17.2 GHz. As V_{inj} increases, *LC* ILFD voltage swing decreases, the oscillation

frequency increases and the locking range shifts to higher frequency.

Fig. 9(b) shows measured oscillation frequency, power consumption, locking range at 0 dBm and Figure of merit (FOM) versus injection gate bias. Maximum FOM is measured at $V_{\text{inj}} = 1.2$ V and the locking range is from 15.5 GHz to 17.8 GHz. The power consumption is 10 mW and it decreases with increasing V_{inj}.

Fig. 9(c) shows measured sensitivity plot as a function of gate bias for the ÷8 ILFD. As V_{G} increases, the operation range shifts to higher frequency, because the free-running oscillation frequency increases. Maximum locking range is measured at $V_{\text{G}} = 0.6$ V. Fig. 9(d) shows measured oscillation frequency, power consumption, locking range at 0 dBm and FOM versus switching gate bias. If $V_{\text{G}} < 0.6$ V, as V_{G} decreases, the power consumption decreases and the locking range decreases too. Maximum FOM is measured at $V_{\text{G}} = 0.5$ V slightly below the threshold voltage.

Fig. 10(a) superposes measured output spectrum of the free-running ILFD and the output spectrum of the locked ÷8 ILFD. The ÷8 locked output spectrum shows a lower output power at offset frequency from the carrier indicating lower ILFD phase noise. Fig. 10(b) displays the gauged phase noises of the injection-locked ÷8 ILFD and the injection RF reference. At 1 MHz frequency offset from the carrier, the phase noise of the injection-reference is −121.642 dBc/Hz. At 1 MHz frequency offset from the carrier, the phase noise of the locked ILFD is −138.966 dBc/Hz.

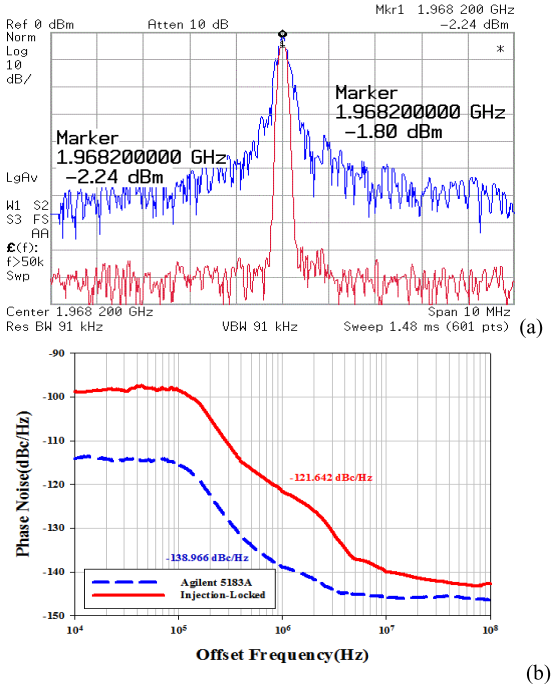


FIGURE 10. (a). Measured spectra of the free running ILFD and the locked ILFD. Injection signal $f_{inj} = 15.8$ GHz and divider output $f_o = 1.968$ GHz. $P_{\text{inj}} = 0$ dBm. (b). Measured phase noises of the locked ILFD and the reference. The ÷8 ILFD at $V_{\text{DD}} = 1.4$V, $V_{\text{G}} = 0.6$ V and $V_{\text{inj}} = 1.1$V. $V_{\text{buffer}} = 0.8$ V, $V_{\text{ref}} = 0.8$ V.

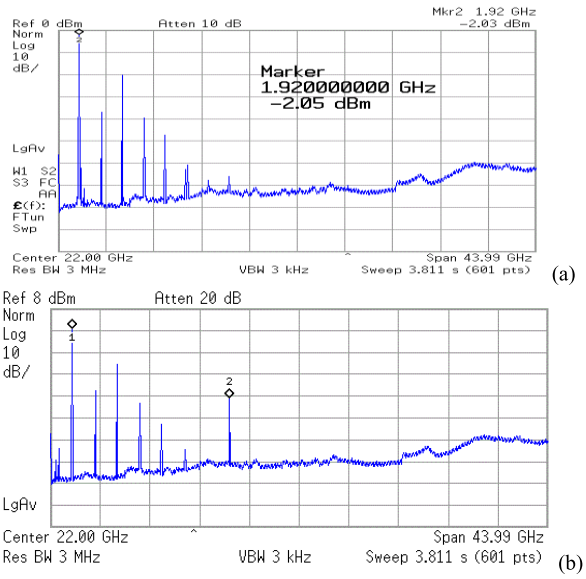


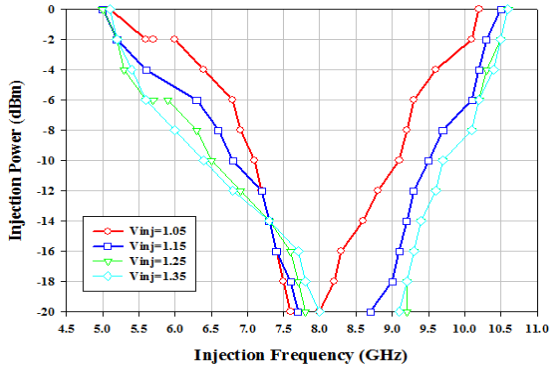
FIGURE 11. Measured full-span spectra of the free-running ILFD (a) and the locked ILFD (b). $f_{inj} = 15.8$ GHz and $f_o = 1.968$ GHz. $P_{inj} = 0$ dBm. The ÷8 ILFD at $V_{\text{DD}} = 1.4$V, $V_{\text{G}} = 0.6$ V and $V_{\text{inj}} = 1.1$V. $V_{\text{buffer}} = 0.8$ V, $V_{\text{ref}} = 0.8$ V.

The phase noise value of the locked ÷8 ILFD is less than the injection RF signal by 17.324 dB at 1MHz offset frequency. Fig. 11 shows measured full-span spectra of the free-running ILFD (a) and the locked ILFD (b). The injection signal is present in the ILFD output, it passes through both FDs to appear at output, but it is smaller than the carrier by 31.93 dBm.

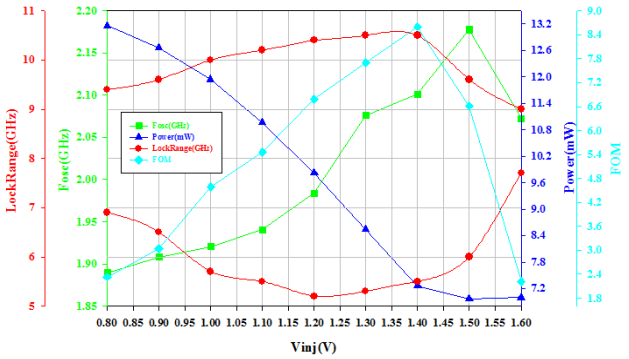
Fig. 12(a) shows the measured input sensitivity for the ÷4 ILFD biased at $V_{\text{DD}} = 1.4$V, $V_{\text{G}} = 0.65$ V, $V_{\text{inj}} = 1.25$ V, $V_{\text{buffer}} = 0.8$ V, and $V_{\text{ref}} = 0.8$ V. An external injected signal power P_{inj} of 0 dBm provides one locking range from 4.8 GHz to 10.6 GHz. At P_{inj} of −20 dBm, the center frequency of locking range is 8.6 GHz. Fig. 12(b) shows measured oscillation frequency, power consumption, locking range at 0 dBm and FOM versus injection gate bias. Maximum FOM occurs at $V_{\text{inj}} = 1.4$ V. Maximum locking range occurs at $V_{\text{inj}} = 1.3$ V. Away from $V_{\text{inj}} = 1.3$ V, the locking range decreases because of reduced conversion gain.

Fig. 13 shows measured oscillation frequency, power consumption, locking range at 0 dBm and figure of merit (FOM) versus gate bias. The power consumption increases with V_{G}. The maximum FOM is measured at $V_{\text{G}} = 0.6$ V. The maximum locking range is measured at $V_{\text{G}} = 0.65$ V. At $V_{\text{G}} = 0.45$ V, the power consumption is 5.8 mW and the locking range is from 7 GHz to 10 GHz. At $V_{\text{G}} < 0.5$ V, two locking range curves are measured and they are dependent on measurement from low input frequency or from high input frequency, this memory effect of parasitic varactor capacitance.

Fig. 14(a) are measured output spectra of the free running ILFD and the locked ÷4 ILFD. The locked output power



(a)



(b)

FIGURE 12. (a). Measured operation frequency vs input power. V_{DD} = 1.4V, V_G = 0.6 V and V_{inj} = 1.05 V ∼ 1.35 V. V_{buffer} = 0.8 V, V_{ref} = 0.8 V. ÷4 ILFD. (b). Measured oscillation frequency, power consumption, locking range at 0 dBm and FOM versus injection gate bias. V_{DD} = 1.4 V, V_G = 0.6 V and V_{inj} = 0.8∼1.6 V. V_{buffer} = 0.8 V, V_{ref} = 0.8 V. ÷4 ILFD.

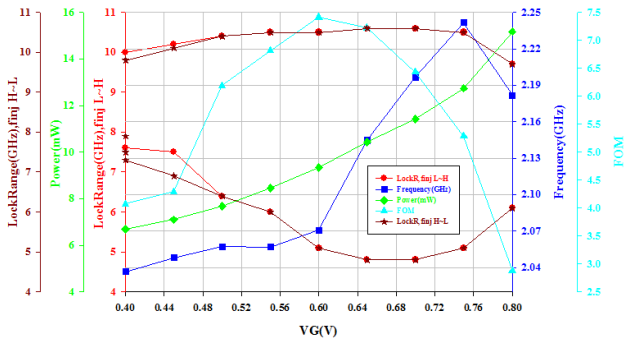


FIGURE 13. Measured oscillation frequency, power consumption, locking range at 0 dBm and FOM versus switching gate bias. V_{DD} = 1.4 V, V_G = 0.4 V ∼0.8 V and V_{inj} = 1.25 V. V_{buffer} = 0.8 V, V_{ref} = 0.8 V. ÷4 ILFD.

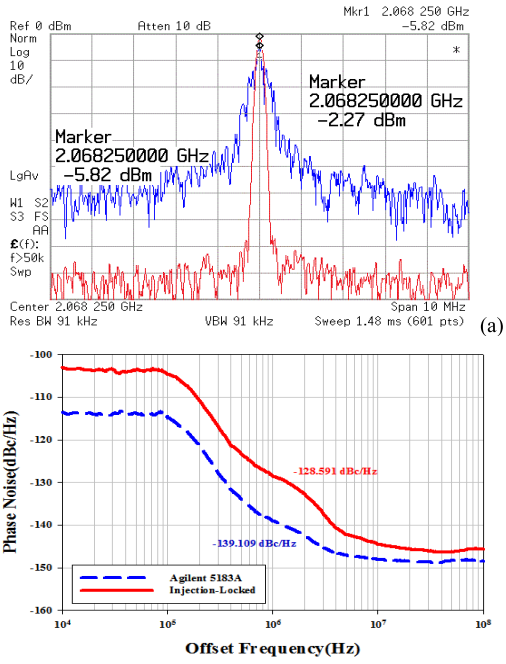


FIGURE 14. (a). Measured spectra of the free running ILFD and the locked ILFD. f_{inj} = 8.3 GHz and f_o = 2.068 GHz. P_{inj} = 0dBm. (b). Measured phase noises of the locked ILFD and the reference. The ÷4 ILFD at V_{DD} = 1.4 V, V_G = 0.6 V and V_{inj} = 1.25V. V_{buffer} = 0.8 V, V_{ref} = 0.8 V.

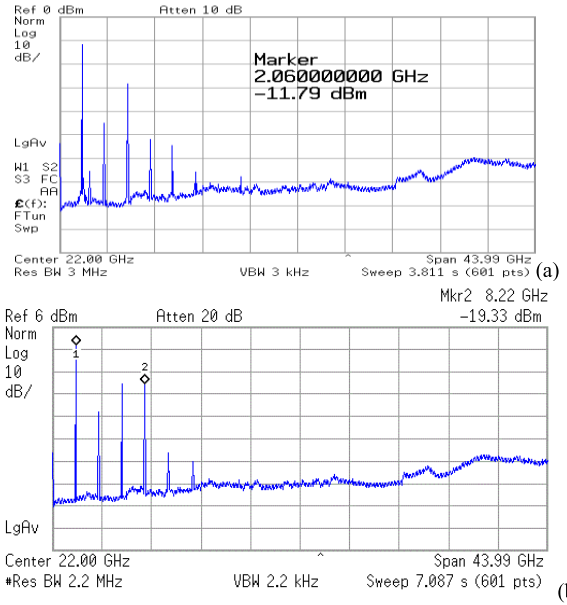


FIGURE 15. Measured spectra of the free-running ILFD (a) and the locked ILFD (b). f_{inj} = 8.3 GHz and f_o = 2.068 GHz. P_{inj} = 0dBm. The ÷4 ILFD at V_{DD} = 1.4 V, V_G = 0.6 V and V_{inj} = 1.25V. V_{buffer} = 0.8 V, V_{ref} = 0.8 V.

at offset frequencies is smaller than that of the free running one. Fig. 14(b) displays the two phase noises owing to the locked ÷4 ILFD and the injection-reference. At 1 MHz frequency offset, the phase noise of the locked ILFD is −139.109 dBc/Hz, while the phase noise of the injection-reference is −128.591 dBc/Hz at 1MHz offset frequency. The phase noise value of the locked ILFD is less than the injection signal by 10.52 dB/Hz at 1MHz offset frequency. Fig. 15 shows measured full-span spectra of the free-running ILFD (a) and the locked ÷4 ILFD (b). The injection signal is present in the ILFD output and it is smaller free-running ILFD (a) and the locked ÷4 ILFD (b). The injection signal is

TABLE 2. Performance comparison of CMOS ÷8 and ÷4 *LC* ILFDs.

Ref.	Tech. (μm)	Pin (dBm)	Vdd(V) Pdis(mW)	FOM	Locking Range (GHz) (%)
[17] ÷8	0.13	0	2/12.5	0.06	19.85~20(0.75)
[18] ÷8	0.18	0	1.8/6.8	0.29	14.4~14.7(2)
This÷8	0.18	0	1.4/8.17	1.89	15.5~17.8 (13.8)
[10] ÷4	0.09		0.5/10.08	3.27	13.2 ~ 18.4 (33.07)
[13]÷4	0.18	0	0.8/7.09	5.29	13~ 19(37.5)
[15]÷4	0.13	0	1.48/7.3	10.58	13.5~ 30.5(77.3)
This÷4	0.18	0	1.4/7.26	8.6	5.5~10.5 (62.5)

*GaAs, Figure of merit (FOM)=Locking Range Percent/Power Con. in mW.

present in the ILFD output and it is smaller than the carrier by 17.2 dBm. Table 2 is the performance comparison of ÷4 ILFDs and ÷8 ILFDs.

IV. CONCLUSION

This paper designs and analyzes a CMOS ÷8 ILFD consisted of a high-frequency direct injection ÷4 capacitive cross-coupled *LC* ILFD stacked under a low-frequency tail injection oscillator based ÷2 FD. The ÷4 *LC* sub-ILFD uses no buffer and varactors for locking range enhancement because of reduced buffer loading and the ÷2 oscillator based FD has large locking range to align the locking range to the ÷4 *LC* ILFD output frequency. With this approach, the designed ÷8 ILFD has good phase noise performance, wide locking range and compact size, and is robust to process and voltage variation. For the present ÷8 design, harmonic mixer ÷4 *LC* ILFD is demonstrated, the locking range can be further extended while replacing the harmonic mixer with a linear mixer. The particular part of this design adopts unbalanced parameters for the ring oscillator based ÷2 FD and this has no negative effect to the ILFD operation. Because the top low frequency ÷2 FD supplies unbalanced currents to both arms of the bottom ÷4 *LC* sub-FD, the ÷4 ILFD outputs a pair of signals with unbalanced amplitudes. Then the injection FET supplies unbalanced injection currents to the two ports of the *LC* tank, and the injection voltages to the top ÷2 FD are unbalanced. The interaction of both sub-FDs leads to a consistent manner. The output buffers are connected to one pair of differential amplifier of the low frequency sub-ILFD, and a pair of balanced differential outputs is generated. For measurement reason, the ILFD is designed to operate at low Giga Hertz region, the principle is applicable to millimeter wave ÷8 ILFDs. The designed ILFD can be used as a ÷4 ILFD with only differential outputs, it also shows good performance measured from the differential outputs. And the advantage of using the capacitive cross-coupled structure and unbalanced ring oscillator to get wide ÷8 locking range is also experimentally verified. This current-reuse circuit also reduces the circuit number by sharing the devices.

APPENDIX

Fig. 16 shows a reference oscillator and frequency divider altered from the designed ÷8 FD shown in Fig. 3(a) by disabling the cross-coupling of the bottom *LC* ILFD and by

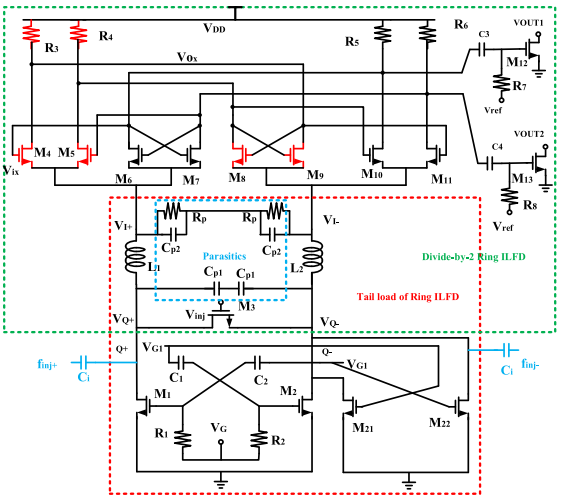


FIGURE 16. Schematic of a reference ring-oscillator and ÷2 ILFD.

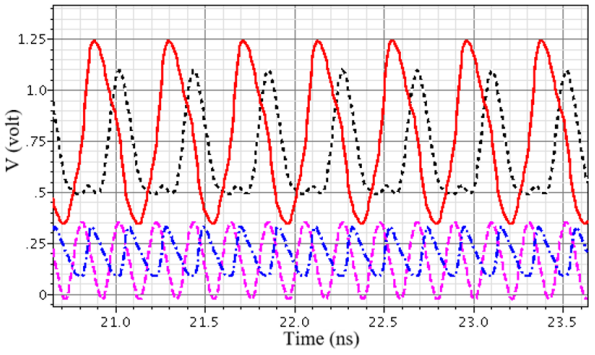


FIGURE 17. Voltage waveforms of the free-run oscillator. $V_{DD} = 1.4$ V, $V_G = V_{G1} = 1$ V and $V_{inj} = 0$V. $V_{buffer} = 0.8$ V, $V_{ref} = 0.8$ V. Red solid: M_4 drain, purple dashed: M_4 source. Black dotted: M_{10} drain, blue dotted-dashed: M_{10} source. Oscillation frequency = 2.4 GHz.

dc biasing the switching FETs and including two injection signal ports. It is used to explain the operation of the ring-oscillator ILFD. Fig. 17 shows the voltage waveforms of the free-run oscillator without the injection source. The outputs of ring-oscillator and the tails of cross-coupled pairs are unbalanced. Fig. 18 shows the voltage waveforms of the ÷2 ring-oscillator ILFD subject to an injection signal. The ILFD provides two pairs of differential outputs and the simulated locking range is from 3.9 GHz to 5.9 GHz. The injection voltages at ω_{RF+} and ω_{RF-} changes the currents through inductors L_1 and L_2. The ÷2 input-output frequency relation of the M_4 mixer is given by $\omega_{RF+} - \omega_{o+} = \omega_{o+}$, where ω_{o+} is the frequency of mixer M_4 gate and drain output signals. Similarly, the ÷2 input-output frequency relation of the mixer M_{10} is given by $\omega_{RF-} - \omega_{o*} = \omega_{o*}$, where ω_{o*} is the frequency of mixer M_{10} output signal. If the ring-oscillator is in a balanced structure, then the signals at ω_{o+} and ω_{o*} are quadrature and the ring-oscillator ILFD outputs are in quadrature. The tail load of ring-oscillator shown in Fig. 3(a) is different from that of Fig. 16 because cross-coupled FETs switches the load periodically. The operation principle of ring-oscillator shown in Fig. 3(a) is similar to that shown in

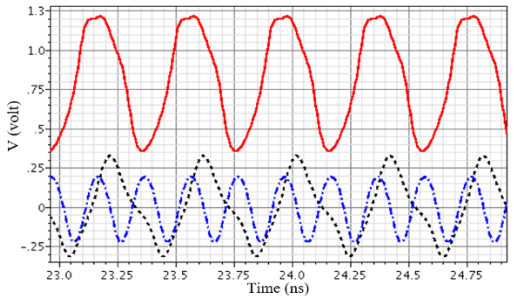


FIGURE 18. Voltage waveforms of the studied ÷2 ILFD used as a free-run oscillator. $V_{DD} = 1.4$ V, $V_G = V_{G1} = 1$ V and $V_{inj} = 1$V. $V_{buffer} = 0.8$ V, $V_{ref} = 0.8$ V. Red solid: M_4 drain. Black dotted: M_{12} output buffer, blue dotted-dashed: injection signal. Oscillation frequency = 2.33 GHz. $f_{inj} =$ 5 GHz and $P_{inj} = 0$ dBm.

Fig. 16, but some differences exist by considering the effect of the *LC* ILFD. In Fig. 3(a), the ac voltage swing of M_1 is larger, so the injection current swings through L_1 and L_2 are larger, the locking range is larger and V_G is smaller to operate so lower power consumption is used for the ring-oscillator ILFD to function. In Fig. 6, dc power consumption is wasted in M_1, M_2 and M_{21}, M_{22}.

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