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Hierarchical Yield-Aware Synthesis Methodology Covering Device-, Circuit-, and System-Level for Radiofrequency ICs

ANTÓNIO CANELAS[1], FÁBIO PASSOS[1], NUNO LOURENÇO[1], (Member, IEEE), RICARDO MARTINS[1], (Member, IEEE), ELISENDA ROCA[2], RAFAEL CASTRO-LÓPEZ[2], (Member, IEEE), NUNO HORTA[1], (Senior Member, IEEE), AND FRANCISCO V. FERNÁNDEZ[2], (Member, IEEE)

[1]Instituto de Telecomunicações, 1049-001 Lisbon, Portugal
[2]Instituto de Microelectrónica de Sevilla, Universidad de Sevilla and CSIC, 41092 Seville, Spain

Corresponding author: António Canelas (antonio.canelas@lx.it.pt)

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ABSTRACT This paper presents an innovative yield-aware synthesis strategy based on a hierarchical bottom-up methodology that uses a multiobjective evolutionary optimization algorithm to design a complete radiofrequency integrated circuit from the passive component level up to the system level. Within it, performances' calculation aims for the highest possible accuracy. A surrogate model calculates the performances for the inductive devices, with accuracy comparable to full electromagnetic simulation; and, an electrical simulator calculates circuit- and system-level performances. Yield is calculated using Monte-Carlo (MC) analysis with the foundry-provided models without any model approximation. The computation of the circuit yield throughout the hierarchy is estimated employing parallelism and reducing the number of simulations by performing MC analysis only to a reduced number of candidate solutions, alleviating the computational requirements during the optimization. The yield of the elements not accurately evaluated is assigned using their degree of similitude to the simulated solutions. The result is a novel synthesis methodology that reduces the total optimization time compared to a complete MC yield-aware optimization. Ultimately, the methodology proposed in this work is compared against other methodologies that do not consider yield throughout the system's complete hierarchy, demonstrating that it is necessary to consider it over the entire hierarchy to achieve robust optimal designs.

INDEX TERMS Electronic design automation, Monte Carlo analysis, multiobjective optimization, optimization-based design, radiofrequency integrated circuit.

I. INTRODUCTION

The design of radiofrequency (RF) integrated circuits (ICs) and systems in nanometer-scale technologies is challenging due to their high operating frequencies, passive component design, and degrading effects of parasitics and variability. Automatic design methodologies that promote the optimal design of RF ICs support circuit designers, with several optimization-based methodologies for simple circuits reported in the literature. Nevertheless, scaling these approaches to more complex circuits or systems is not trivial as the optimization time does not scale well with the circuit size/complexity. Therefore, most proposed optimization-based approaches are only adequate for tackling simple blocks, and hierarchical automation tools still show severe limitations, particularly when considering variability effects. Variability and yield are critical aspects of IC design, and their consideration in the design automation flow is mandatory. As RF circuit design demands time-consuming simulations, such as electromagnetic (EM), periodic steady-state,

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or S-parameter simulations, the overall execution time of simulation-based optimization approaches increases as the circuits' complexity grows. Many reported approaches had used first-order equations for circuit/system performances and analytical models for passives to speed up the optimization process [1]–[15], but they lack accuracy. Moreover, in nanometer technologies, accurate yield estimation is of utmost importance. However, optimization-based methodologies do not effectively handle such estimation due to the need for intensive Monte-Carlo (MC) simulations that degrade even further its efficiency [1]–[8].

For the first time in literature, this paper proposes a hierarchical yield-aware bottom-up (BU) approach covering the entire device-, circuit-, and system-level design for RF circuits, including an accurate and efficient estimation of each circuit performance, including yield, at each level. Furthermore, by considering the yield of each low-level block, the hierarchical optimization becomes robust to variability, where at each level, the performances already account for the performance degradation caused by variability.

The rest of this paper is organized as follows. Section II discusses the related work. Section III explains the proposed hierarchical yield-aware optimization methodology, exposing the challenges and the solutions proposed to address them. In Section IV, as experimental results, an RF front-end composed of a low-noise amplifier (LNA), a voltage-controlled oscillator (VCO), and a mixer (MIX) is designed using the presented methodology, and finally, in Section V, conclusions are drawn.

II. RELATED WORK

Several works have been proposed where optimization-based methodologies are endorsed as a strategy to design and achieve optimal RF circuits automatically [1]–[15]. Most works only tackle simple circuits such as LNAs and VCOs and cannot handle more complex designs [1]–[8]. Even the ones that tackle more complex circuit-level topologies [9] evaluate passive devices (i.e., inductors) with analytical models that, although fast, tend to be inaccurate. These errors lead to discrepancies between the circuit performances estimated with the passive component model and the circuit performances when the passives are simulated with an accurate evaluator (e.g., an EM simulator) [10]. Other works propose strategies to tackle more complex RF systems; however, most of them are focused on RF budget analyzers, architecture comparison tools, or high-level system specifications tools [11]–[15].

In addition, some tools are intended for design space exploration at the system architecture level, given the target system performances [11]–[13]. In these top-down approaches, the circuits that compose the system are modeled with behavioral models [11], [12] or analytical equations [13]. The difficulties in using these methods are on the modeling of all circuits' nonidealities. Therefore, the system-level specifications may not hold once circuits are sized, leading to redesign cycles. Some approaches address this issue, designing RF systems by sizing all devices simultaneously [14], [15]. However, they use first-order analytical equations to estimate circuit performances that do not account for all nonidealities and use ideal models, which are inaccurate, for passive components.

In [16], a hierarchical bottom-up (BU) approach that uses pre-optimized circuits for the subblocks enables the RF systems' accurate and effective hierarchical design. It starts at the lowest level, where the smaller sub-circuits are optimized individually, and then, results are composed up the hierarchy until reaching the system level. In this approach, simulation-based evaluation ensures the accuracy of the performance estimation.

A. RF IC VARIABILITY-AWARE SYNTHESIS

None of the previously mentioned methodologies consider the impact of process variations and mismatch, which is unbearable in modern nanometer technologies. In the past, the lack of mature RF yield-aware design techniques led to the adoption of typical digital IC design techniques, like process, voltage, and temperature (PVT) corner analysis, and some works included such corner analysis in the optimization-based techniques [17]. However, such techniques are not the best suited since RF ICs are particularly sensitive to local or intra-die variations, which are not considered by the PVT analysis. Several techniques have been proposed to estimate parametric yield, such as MC analysis, which revealed to be the most reliable and accurate method to estimate circuit yield, and is still considered the gold standard for yield prediction.

However, the MC analysis's main downside is the considerable number of circuit simulations needed to provide an accurate yield estimation. This fact is even more problematic when dealing with population-based optimization techniques where hundreds or thousands of simulations must be executed to evaluate typical performances.

Nevertheless, methodologies that increase efficiency and include process variations and mismatch in the optimization, especially for the analog baseband, have been reported in the literature [18]–[26]. Some works propose a mixed approach between corner and MC analysis, where only the parameters that highly degrade the circuit performances are varied [18], [19]. Such methodologies identify which physical/design parameter influences the circuit performances and perform MC analysis with a predefined standard deviation over such parameters. For example, in [18], the oscillation frequency is set as the circuit performance to be optimized, which shows a strong dependence on the threshold voltage, V_{th}, and gate oxide thickness, T_{ox}. Hence, the MC analysis considered only changes on these parameters and the supply voltage. However, in general, foundry-provided models consider a few dozen variation parameters per device in their models. It can be difficult or impossible to identify only a small set of parameters that accurately cause performance variations.

Alternatively, selecting a subset of candidate solutions for MC simulation and the number of simulations in each MC is a common approach to reduce MC simulations' time impact in optimization-based methodologies. In [20], the candidate solutions during optimization are subject to a variable number of MC simulations. The first stage of the methodology is to perform a few MC simulations for all feasible candidate solutions, which provides their ranking. In the second stage, based on such rank, the algorithm allocates a higher number of MC simulations to the best candidate solutions, as more accurate yield estimation is required for the solutions that have more probability of being optimal. In [21], a similar methodology is proposed, where the candidate solutions are subject to a small number of MC simulations to perform variability analysis, which allows allocating a different number of MC simulations to different candidate solutions from a total budget. In [22], clustering is used to select a subset of the representative solutions to be subject to MC analysis at each iteration. Some other works adopted low-discrepancy sequences methods to reduce the necessary number of MC samples; however, their use in optimization-based methodologies still demands many simulations [23], [24]. In [25], [26], system-level designs considering the yield estimation are reached. However, they share some of the limitations of the system-level tools reported in [11]–[15], where behavioral models are considered both for yield and for circuit performances, and therefore is it not possible to ensure that the estimated performances will be met at the device level.

B. CONTRIBUTIONS

Despite the studies that show that, in a limited amount of time, BU methodologies achieve superior results in terms of optimality when compared with a completely flat optimization of the entire system at once [16], reported works do not consider yield when using accurate circuit simulation for performance evaluation. Therefore, there is still the need for a methodology that proposes a complete hierarchical sizing approach starting at the device level up to the system level, considering process and mismatch variability effects caused by a non-ideal manufacturing process, and estimating the performances accurately to avoid re-design iterations. Moreover, it is imperative to consider a yield-aware strategy in the synthesis methodology that maintains a fair accuracy-efficiency tradeoff.

This work presents an innovative hierarchical bottom-up design considering variability effects since the lowest levels of the hierarchy. The variability effects are minimized by optimizing the yield of all potential circuit solutions at every level of the hierarchy. In addition, an innovative parallel yield estimation technique that split the number of candidate solutions being evaluated over several processing threads is used to reduce the time impact of the MC simulations on the overall optimization process. Moreover, only a small number of potential solutions are subject to full MC analysis on each thread.

III. YIELD-AWARE HIERARCHICAL BOTTOM-UP DESIGN METHODOLOGY

Most automatic IC sizing methodologies use an optimization algorithm to determine the circuits' and devices' sizes. The sizing of a circuit can be formulated as the following multi-objective optimization problem in (1),

$$\begin{aligned} &\textit{minimize } f\,(x)\,; \quad f\,(x) \in \mathbb{R}^m \\ &\textit{subject to } g\,(x) \leq 0; \quad g\,(x) \in \mathbb{R}^k \\ &\qquad x \in \Omega \in \mathbb{R}^n \end{aligned} \tag{1}$$

where $f(\mathrm{x})$ is the set of m objective functions, $g(\mathrm{x})$ is the set of k constraints, and x is the n-dimensional design vector on the search space Ω. Circuit design commonly targets the optimization of two or more performance figures ($m > 1$ in (1)), while subject to several constraints, leading to a constrained multiobjective optimization problem. Therefore, some key concepts of dominance-based constrained multi-objective optimization are needed to support the proposed methodology's description. For a more in-depth description, refer to [27].

1) CONSTRAINED-DOMINANCE

a point $y \in \Omega$ constrained-dominates point z if and only if y show less constraint violation than z, or, if both solutions meet all constraints, $f_i(y) \leq f_i(z)$, for every $i \in \{1, \ldots, m\}$ and $f_j(y) < f_j(z)$ for at least one index $j \in \{1, \ldots, m\}$.

2) PARETO OPTIMALITY

a point $y \in \Omega$ is Pareto-optimal if it is not constrained-dominated by any other point in Ω.

3) PARETO SET

the group of all Pareto-optimal points in the search space is known as the Pareto set, Ω^*.

4) PARETO OPTIMAL FRONT (POF)

The values $f(\Omega^*)$, in the objective space, form the Pareto-optimal front (POF).

This work applies the NSGA-II [27] evolutionary algorithm (EA) to solve the optimization problem proposed in this work. NSGA-II is based on the evolution of a population of candidate solutions guided by the concept of Pareto dominance at each iteration.

A. MULTIOBJECTIVE BOTTOM-UP SYNTHESIS METHODOLOGY

Whereas the general formulation in (1) applies to any circuit, for large circuits, the number of design variables increases with the number of devices, leading to an exponential growth of the size of the design space. This complexity may also be reflected in a considerable increase in the simulation time of each candidate solution. However, in circuit design, hierarchical decomposition is naturally performed, limiting the correlation among design variables.

Therefore, the natural sparseness in the design space favors decomposition without compromising global optimality. Since circuit design is inherently about balancing tradeoffs, using multiobjective optimization hierarchically and passing a POF representing the best tradeoffs available for a given circuit (e.g., gain versus noise figure in an LNA) rather than a single solution to the upper level in the hierarchy, mitigates the need for re-design cycles.

Fig. 1 illustrates the BU design methodology for the RF front-end addressed in this paper. Moreover, this type of BU methodologies provides some lower-level blocks' hierarchical reusability. When a new system has to be designed (e.g., for a different communication standard), there are already multiple designs that can be reused for the lower level blocks, increasing the entire process's efficiency.

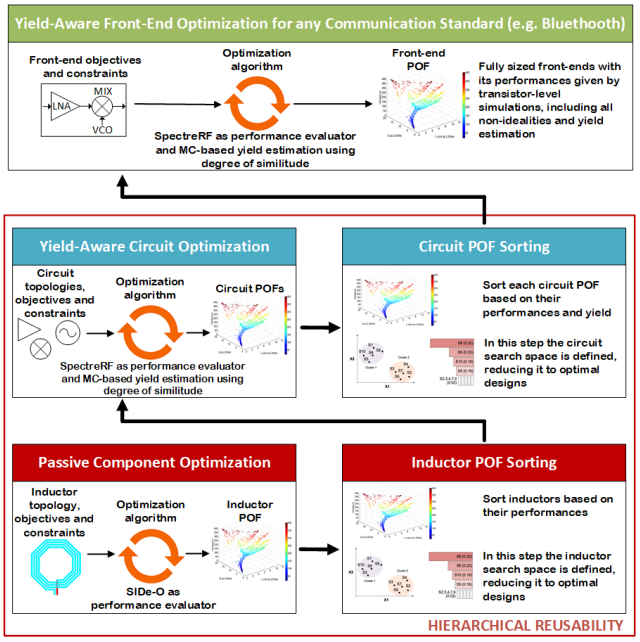

FIGURE 1. Overview of the BU design methodology for the RF front-end tackled in this paper.

B. LOWEST HIERARCHY LEVEL: PASSIVE DEVICES

How to model/evaluate passive components such as inductors and transformers is a particular characteristic of RF IC design. Typically, accurate inductor performance is estimated using EM simulations. However, including hundreds/thousands of EM simulations in automated circuit design is not practical and leads to long execution times. Hence, we use a state-of-the-art machine learning (ML) technique to model inductors [28]. It is a MATLAB toolbox (SIDe-O), which allows the designer to perform inductor design and optimization within milliseconds [29]. The model achieves less than 1% error compared to EM simulations and does not impact the accuracy of the inductor design. We follow the approach in [29], and the passive component design is considered an additional level of the hierarchy.

SIDe-O model is used to optimize the inductors that are used later during circuit optimization. The model saves weeks in the execution time of the inductor optimization. Since this work aims for the highest possible accuracy, as long as the execution time is reasonable, the inductors that result from the model optimization are simulated using accurate EM simulations, and their correspondent S-parameter files are stored and used when simulating the higher levels of the circuit hierarchy.

C. YIELD ESTIMATION ACROSS THE HIERARCHY

When building a system hierarchically, considering yield in the design flow brings its challenges. Reference [25] proposes a simplistic approach to generate low-level block POFs with a given yield and considers that the solution points will have the same yield level as building blocks after the system-level optimization. However, this approach may not work correctly, as it does not capture the statistical correlations between the different low-level blocks since each subblock is optimized independently. So, such simple yield-aware synthesis methodologies increase robustness at the low level of the design but do not ensure the complete statistical information to determine the total system yield. Moreover, the relationship between hierarchical lower levels' yield and the system yield can be non-monotonic and complex. Then, when transforming from low-level circuit performances to system-level performances, the yield may not sustain. Therefore, the yield must be calculated at low- and higher-levels circuits to have a reliable yield estimation.

In our approach, at each hierarchy level, the yield estimation methodology adopted is based on MC analysis. The adopted methodology only performs MC simulations for a reduced number of candidate solutions at each generation of the optimization to prevent the massive amount of circuit simulations required to estimate the yield using MC simulations for all candidate solution points. The newly developed yield estimation technique adopts a parallel approach where the new EA candidate solutions at each iteration are assigned among several processing threads for evaluation, as illustrated in Fig. 2. Notice that this parallelism refers to the optimization loop and should not be confused with the multithreading capabilities already available in many circuit simulators. Moreover, the multithreaded simulation capabilities of modern circuit simulations are fully compatible with the proposed technique. The criterion for the assignment of the candidate solutions is to divide the population among the threads randomly. An alternative method using clustering in the variable space to guide the assignment was also considered. However, a preliminary trial on optimizing the LNA with both these methods shows that the random assignment presents better results in terms of workload.

Moreover, each thread has the same number of individuals to evaluate and, on average, a similar number of individuals per thread. Table 1 summarizes the number of candidate solutions subject to MC analysis for five execution runs of each method. The Random-based assignment leads to only

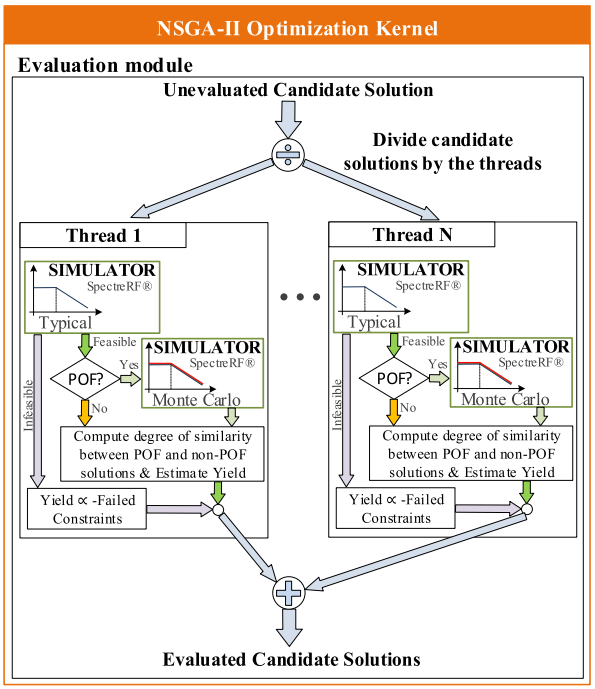

FIGURE 2. Multi-thread optimization kernel evaluation for yield estimation.

TABLE 1. The number of solutions subject to Monte-Carlo analysis during the optimization of the LNA with a population of 800 elements and 400 iterations using random-based and cluster-based assignment to 4 threads.

Run	Random-based Performed MC/Thread	Cluster-based Performed MC/Thread
1	6032	11293
2	7637	12051
3	7019	11299
4	6699	11760
5	6508	10698
Mean	*6779*	*11420*

8.5% of the candidate solutions being subject to MC analysis. Whereas the cluster-based lead to 14% of feasible candidate solutions being subject to MC analysis.

At each thread, the evaluation of the candidate solutions uses a two-stage process. In the first stage, the individuals are subject to electrical simulations to estimate typical performance. Then, it is possible to classify individuals as feasible or infeasible (under typical conditions). Infeasible solutions are removed from the second stage of the evaluation process, where the yield is estimated. However, instead of merely assigning them a zero yield, a negative yield value proportional to their constraint violations is used, allowing a more meaningful constrained dominance ranking of the population's infeasible solutions and improving the optimization algorithm's convergence.

Following, a POF, local to the thread, is computed at the second stage based on typical values of the objectives being optimized. Then, all individuals belonging to that POF have their yield accurately estimated via MC analysis. Circuit desired specifications are implemented in the optimization problems as constraints. The computed yield estimates the percentage of circuits expected to comply with the circuit's desired specifications (optimization constraints) when variability is considered. When the yield is optimized, i.e., the percentage of solutions expected to comply with the desired specifications, the variability of the objectives is implicitly reduced as the design is centered. As such, we did not explicitly consider the variability of the objectives when evaluation yield. Fig. 3 shows the typical behaviour of the standard deviation of an objective *versus* the yield value. Nevertheless, if needed, the yield can be computed considering the variability of the optimization objectives explicitly, as done in [24] instead.

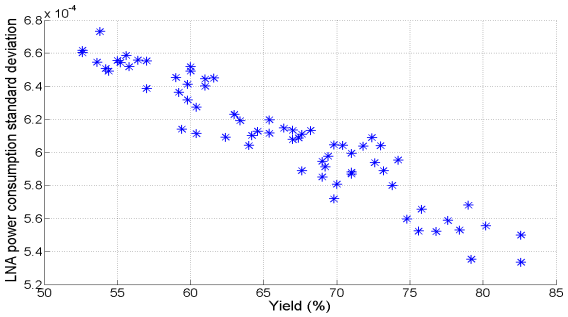

FIGURE 3. LNA power consumption standard deviation vs. yield.

Once the yield of the POF solutions is computed by MC analysis, the yield of the remaining candidates is assigned using their degree of similitude to the ones in the POF. Although these dominated solutions are never presented to the circuit designer, they are important to improve diversity during the evolutionary process. Their yield, $\hat{Y}_{x_j}$, is estimated by summing the product of the similitude degree with the accurate yield value of the simulated solutions:

$$\hat{Y}_{x_j} = \sum_{i=1}^{k} u_{ij} Y_i \tag{2}$$

where Y_i is the yield of the i-th POF simulated solution, and u_{ij} is the similitude among solution $\mathbf{x}_j$ with respect to solution $\boldsymbol{p}_i$ based on the Euclidean distance computed between $\mathbf{x}_j$ and $\boldsymbol{p}_i$ in the variable space and is given by:

$$u_{ij} = \frac{1}{\sum_{p=1}^{k} \left(\frac{\|\boldsymbol{x}_j - \boldsymbol{p}_i\|_2^2}{\|\boldsymbol{x}_j - \boldsymbol{p}_p\|_2^2} \right)} \tag{3}$$

subject to:

$$\begin{aligned} & u_{ij} \in [0, 1] \\ & \textstyle\sum_{i=1}^{k} u_{ij} = 1, \quad \forall j \in 1, \ldots, n \\ & 0 < \textstyle\sum_{j=1}^{n} u_{ij} < n, \quad \forall i \in 1, \ldots, k \end{aligned}$$

with:

$$k = |POF\ solutions|$$

$$n = |Thread\ individuals|$$
$$i = 1, \ldots, k; \quad j = 1, \ldots, n$$
$$\|\cdot\|_2 \text{ Euclidean distance}$$

The Euclidean distance is computed in the variable design space as it is expected that variability affects neighbor solutions, i.e., solutions with similar devices' sizes, similarly. So, the estimated yield value, $\hat{Y}_{x_j}$, has more significant contributions from the closest POF solutions. Based on the described flow, it is possible to implement an MC-based analysis methodology for yield estimation with a reduced time impact in population-based optimization algorithms as not all potential solutions/individuals require time-expensive MC analysis.

D. EXPLORING LOWER LEVEL POFS DURING OPTIMIZATION

The system is composed bottom-up during the hierarchical synthesis, along its hierarchy, exploring the lower-level POFs [30]. These lower-level POFs greatly prune the design space towards the most promising regions, i.e., optimized sub-block, and ensure diversity of solutions. Therefore, one of the problematic issues in BU synthesis methodologies is how to explore low-level POFs while going up in the hierarchy during the optimization. Since most heuristic/stochastic optimization algorithms rely on concepts such as slight movements or neighborhoods, searching these low-level POFs must be done carefully. EAs, for example, consider mutation to create small local perturbations, where a slight movement in the design space should represent a small change in the component's parameter.

Consequently, a slight component variation is usually associated with a small performance variation of the circuit. However, this is not the case when exploring through low-level POFs, where two consecutive randomly indexed circuits can have completely different performances leading to essentially different system performances. Thus, it is clear that the low-level POFs must be organized intelligently so that the optimization algorithm can search through them effectively and not perform random selections of a point in the lower-level POF that have small chances of finding optimal results. The approach taken to index the low-level POFs during the system-level assembling follow a parameterless decaying neighborhood to implement slight local variations. It identifies the points by one integer but considers the distance between points in the related indexing variables. For each point, i, in a low-level POF, the probability of point j to be selected in a random local move around i is defined by

$$p_i(j) = \frac{\frac{1-d_{i,j}}{d_{i,j}}}{\sum_{k=1}^{N} \frac{1-d_{i,k}}{d_{i,k}}} \tag{4}$$

where $d_{i,j} \in (0, 1]$ is the normalized Euclidean distance from solution i to solution j, and N is the total number of points in the POF. Fig. 4 illustrates the higher probability of selecting closer designs in the performance design space of the currently used design. Higher probabilities are shown in red, while lower probabilities are shown in blue.

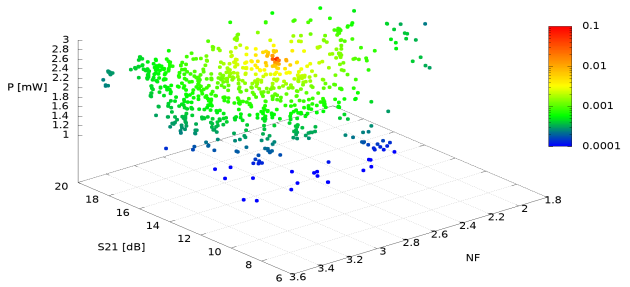

FIGURE 4. Illustration of the LNA probability of selection using the proposed operator for the neighborhood of the solution marked in red.

IV. EXPERIMENTAL RESULTS

This section shows experimental synthesis results for a low-IF RF front-end receiver on the ISM radio bands in 65-nm CMOS technology. The front-end receiver is composed of an LNA, a VCO, and a MIX. The LNA (source degenerated LNA) was implemented with asymmetrical inductors, whereas symmetrical inductors are used for the VCO (cross-coupled double differential VCO). The topologies for both circuits and passives are presented in Fig. 5. In the first level of the hierarchical partition are the passives (inductors). The LNA and VCO are considered for optimization in the second level, whereas the Gilbert cell MIX is considered at the system level for impedance matching purposes. Optimizing the MIX at the system level improves the impedance matching between blocks (LNA-MIX and VCO-MIX), by assuring that each low-level device/circuit delivers good performance figures for the entire 2.4–2.5 GHz ISM band. The low-level POFs can be used when designing other receivers working in this band (e.g., ZigBee, Bluetooth, Wi-Fi/WLAN, Bluetooth low energy, among others). Still, the methodology is independent of the circuit, foundry, or communication standard.

The optimization processes were set to run on a computer server with an Intel Xeon E5-2630 CPU. All optimizations were parallelized using 4 processing threads.

A. DEVICE-LEVEL OPTIMIZATIONS

Following the synthesis flow shown in Fig.1, the first step was to optimize the integrated inductors at the lowest hierarchical level. The asymmetrical and symmetrical octagonal inductors illustrated in Fig. 6 (a) and (b), respectively, were considered. In both cases, their design parameters are the number of turns, N; the inner diameter, D_{in}, the turn width, W. The inductor's search space that was considered for the optimization is presented in Table 2.

The ranges for the design parameters and the grid size were derived from the design rules of the technology process and are reasonably comprehensive, considering inductance values used commonly. The inductor optimization is performed using surrogate models that present less than 1% error vs.

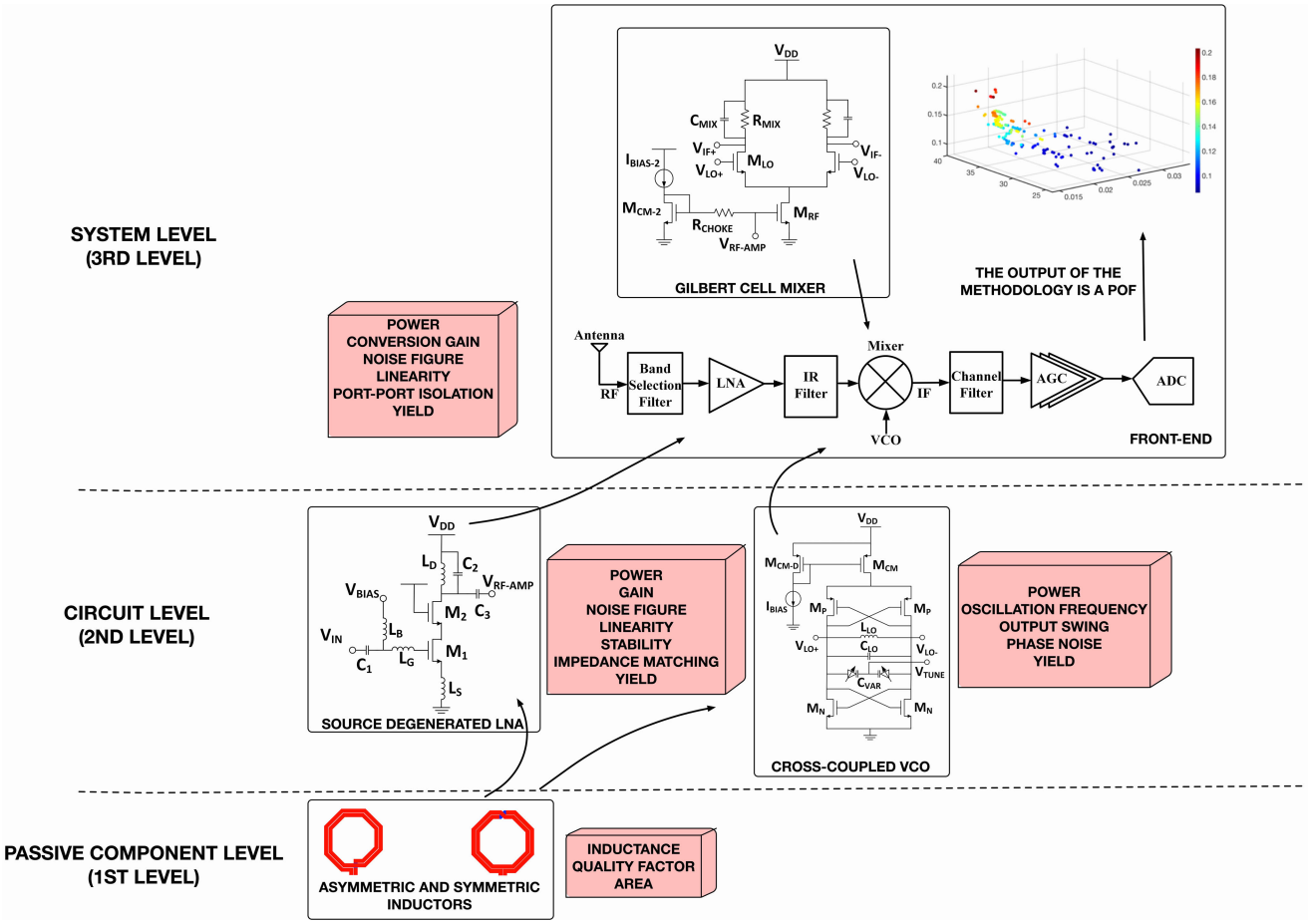

FIGURE 5. Hierarchical decomposition of the RF front-end into passive components, LNA and VCO. The MIX as is optimized at the system level. Apart from the presented topologies, other topologies can be considered together enabling not only the design selection but also topological selection.

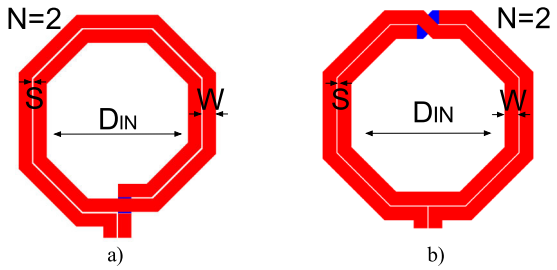

FIGURE 6. a) Octagonal asymmetric topology used in the LNA and b) octagonal symmetric topology used in the VCO.

TABLE 2. Design variables for the inductors.

N			D_{in} (µm)			W (µm)		
Min	Max	Grid	Min	Max	Grid	Min	Max	Grid
1	5	1	20	200	0.05	5	15	0.05

EM simulations. This is a highly accurate estimation that will introduce only a negligible deviation during inductor optimization.

Both topologies were optimized to maximize quality factor, Q, and inductance, L, and minimize the area. Furthermore, additional constraints were imposed to guarantee the proper behavior of inductors at the entire frequency band. Such constraints impose that the inductor operates in a relatively robust area of the performance curve (i.e., inductor flat-bandwidth area), decreasing the device's sensitivity over fabrication variability [28]. Still, once the optimization is complete, the solutions obtained were simulated in an EM simulator for increased accuracy, and the resulting POFs are shown in Fig. 7. The individuals of these POFs (each dot in the figure) represent fully-sized inductors that present the best tradeoffs over L, Q, and area at the selected technology node and working frequency—implying that for a given L and area, the obtained inductor has the highest Q value.

B. CIRCUIT LEVEL OPTIMIZATION

The next step in the proposed hierarchical synthesis is to optimize at the circuit level the LNA and VCO. The MIX is sized on the top level to adapt its impedance to the pre-optimized LNA and VCO. An alternative approach would be to optimize the MIX separately but to constrain the impedances on all

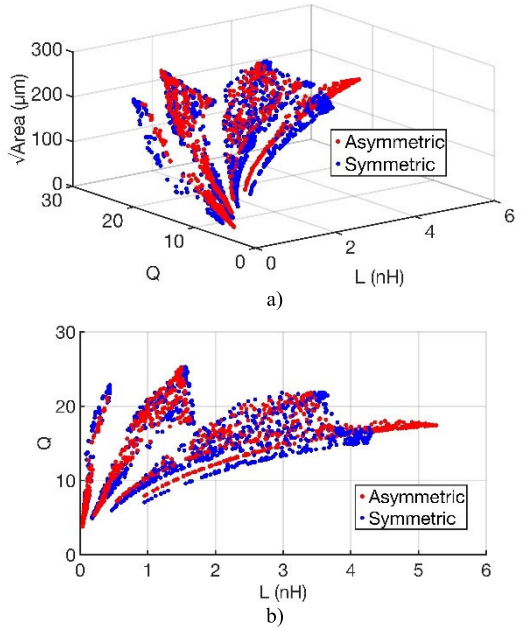

FIGURE 7. a) Comparison between the asymmetric and symmetric inductors POFs. b) 2-D projection of the POFs illustrating *L* vs. *Q*.

circuits. The electrical circuit simulations were done using SpectreRF, but the methodology is independent of the electrical simulator. Finally, the yield is estimated using the multi-thread algorithm, as explained previously.

The source degenerated LNA, shown in Fig. 5, is powered by a 1.2V supply, and its target operating frequency is the ISM band (2.4-2.5GHz). The target performance figures of the LNA that need to be considered during optimization are, gain S_{21}, power consumption P_{DC}, noise figure NF, third-order intercept point IIP_3, input matching coefficient S_{11}, output matching coefficient S_{22}, Rollet stability factor k (if smaller than 1, the LNA is potentially unstable) and the yield.

Two optimizations were performed: one considering only typical performances (no yield considerations) and another considering process and mismatch using MC models (yield-aware optimization) with a 95% yield constraint. The 95% (two sigmas) was selected to give some latitude to explore the lower levels, as there might be compensation at the system level. On an excellent accuracy-efficiency tradeoff, 100 MC iterations adopting low discrepancy sampling (LDS) are considered during the yield-aware optimizations. The lower-level POFs for the inductors are organized using the method discussed in section III.C, and they constitute the inductor design space for the circuit optimizations. In Table 3 the design variables for all optimizations, which define the search space, are presented.

The LNA optimization had three objectives: maximization of S_{21} and minimization of NF and P_{DC}. The other circuit specifications (i.e., constraints) are shown in Table 4, columns one and two., and the result of the optimization is shown in Fig. 8.It can be observed in Fig. 8 b) and c) that typically, in the yield-aware optimization, the LNA consumes more power in order to achieve the same NF and S_{21} values. Also, superior NF values can be achieved when the yield is not considered.

TABLE 3. Design variables for all optimizations.

Variables	Min	Step	Max
Transistor width (μm)	0.6	0.1	4
Transistor length (nm)	60	5	120
Transistor number of fingers	2	1	32
Transistor multiplicity	1	1	8
Capacitors (F)	3f	1f	4.8p
Varactor width (in VCO) (m)	400n	100n	3.2μ
Varactor length (in VCO) (m)	200n	100n	3.2μ
Resistors (Ω)	10	10	10k
Voltage source (in LNA) (V)	0.55	0.01	1.2
Current source (in VCO) (mA)	0.1	0.1	3

The same operation is performed for the VCO. The VCO is intended to oscillate at a frequency of 2.5GHz with a supply voltage of $V_{DD} = 1.2V$, and its target performances are the power consumption (P_{DC}), the oscillation frequency (f_{osc}), the phase noise (PN), the output swing (V_{OUT}), which is an important performance parameter especially when the VCO is connected to a mixer, and, finally, the yield. The VCO was optimized for the minimization of PN and P_{DC} and the maximization of V_{OUT}. Again, the VCO specifications are shown in Table 4 (columns three and four), and the design variables are also listed in Table 3. The optimization results are shown in Fig. 9.

It can be observed that for the VCO, it is possible to obtain designs with less P_{DC}(less than 0.6mW) and lower PN (less than -125 dBc/Hz) when the yield is not considered. Overall, and not surprisingly, both LNA and VCO solution space shrinks as yield is considered in the optimization, resulting in tighter POF.

C. SYSTEM-LEVEL OPTIMIZATION

After the circuit level optimizations, it is possible to perform the system-level optimization to reach the front-end design [31]. Again, the lower-level POFs, for the VCO and LNA are organized using the method discussed in section III.C, and they constitute the design space considered during the front-end optimization. Two different optimizations were performed, one without considering yield and another considering 95% yield (as in the low-level optimizations). The objectives and constraints, shown in Table 4, are established so that the front-ends comply with both the Bluetooth Low Energy (BLE) and Wi-Fi standards [32]. The results are shown in Fig. 10, where it is possible to observe that the "no-yield" POF achieves far superior results, especially in terms of NF and P_{DC} (Fig. 10.b)). This can be explained by observing Fig. 10.c), where the "no-yield" circuits achieve better NF performances. These results are expected, since by considering the yield in the optimization process, circuit performances are centered into a more conservative region of space, further away from the boundaries of nominal feasibility. Including the yield during the optimization degrades the efficiency of the entire process.

TABLE 4. Specifications for the LNA, VCO, mixer, and front-end optimizations.

LNA		VCO		Front-end	
Performance	Specifications	Performance	Specifications	Performance	Specifications
S_{11} @ 2.45; 2.5; 2.55 GHz	< -12 dB	f_{osc}	> 2.45 GHz	CG @ 10 MHz	> 10 dB
S_{22} @ 2.45; 2.5; 2.55 GHz	< -12 dB	f_{osc}	< 2.55 GHz	CG @ 40 MHz	**Maximize** (> 10 dB)*
S_{21} @ 2.45; 2.5; 2.55 GHz	**Maximize** (>7 dB)*	PN @ 3MHz offset	< -110 dBc/Hz	P_{DC}	**Minimize** (< 5 mW)*
k	> 1	PN @ 1MHz offset	**Minimize** (< -105 dBc/Hz)*	NF @ 10 MHz	< 8 dB
NF @ 2.45; 2.5; 2.55 GHz	**Minimize**	P_{DC}	**Minimize** (< 2 mW)*	NF @ 40 MHz	**Minimize** (< 8 dB)*
P_{DC}	**Minimize** (< 2 mW)*	V_{OUT}	**Maximize** (> 150mV)*	IIP_3	> -10 dBm
IIP_3	> -10 dBm	V_{OUT}	< 1.1V	yield	>95%
yield	>95%	yield	>95%		

*Although this performance is given as an objective a constraint is also imposed.

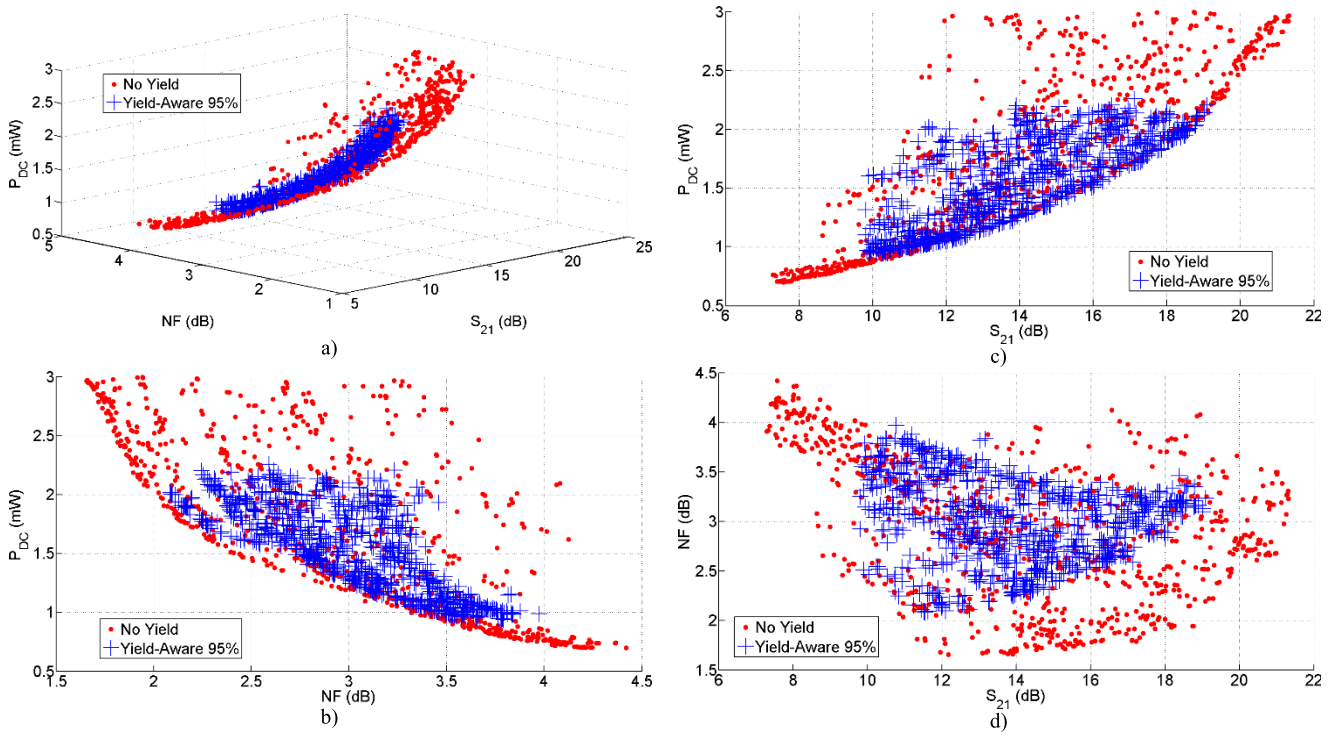

FIGURE 8. a) Comparison between the obtained LNA POFs considering typical performances versus yield-aware performances. b) 2-D projection of the POF illustrating NF vs. P_{DC}. c) 2-D projection of the POF illustrating S_{21} vs. P_{DC}.ing L vs. Q. d) 2-D projection of the POF illustrating S_{21} vs. NF.

However, using the methodology proposed in this paper, it is still possible to perform the optimization-based design without reaching unbearable times.

The run time of all optimizations performed in the paper is shown (no-yield and yield-aware optimizations) and compared with an estimation of how much time it would take for the yield-aware optimization using a complete MC analysis for all individuals during a given optimization (to estimate the time reduction by using the approach proposed in this work). Table 5 shows the time comparisons for all the circuits optimized in this work, where it is possible to observe that the time reduction of our methodology is hundreds of hours per optimization compared to a complete MC yield-aware optimization.

The full MC yield-aware optimization time is estimated as follows. The time needed for performing just the MC simulation with 100 iterations is on average 8s, 274s and 306s elapsed time per solution, respectively, for the LNA, VCO, and Front-End & MIX. Exemplifying for the LNA circuit optimization, the number of circuit evaluations required during the optimization of the LNA is the number of iterations

TABLE 5. Time for all optimizations performed in this work.

Circuit	Pop.[1]	Iter.[2]	No Yield	Yield-aware	
				this work	full MC
Inductor	1000	80	~10min.	~	~
LNA	800	400	~4h	~19h	~178h (x9)*
VCO	600	300	~46h	~171h	~3425h (x20)*
Front-End + MIX	256	1000	~26h	~95h	~5440h (x57)*

[1] NSGA-II population size [2] NSGA-II iterations' count
*Between the method proposed in this work and a full MC optimization-based methodology

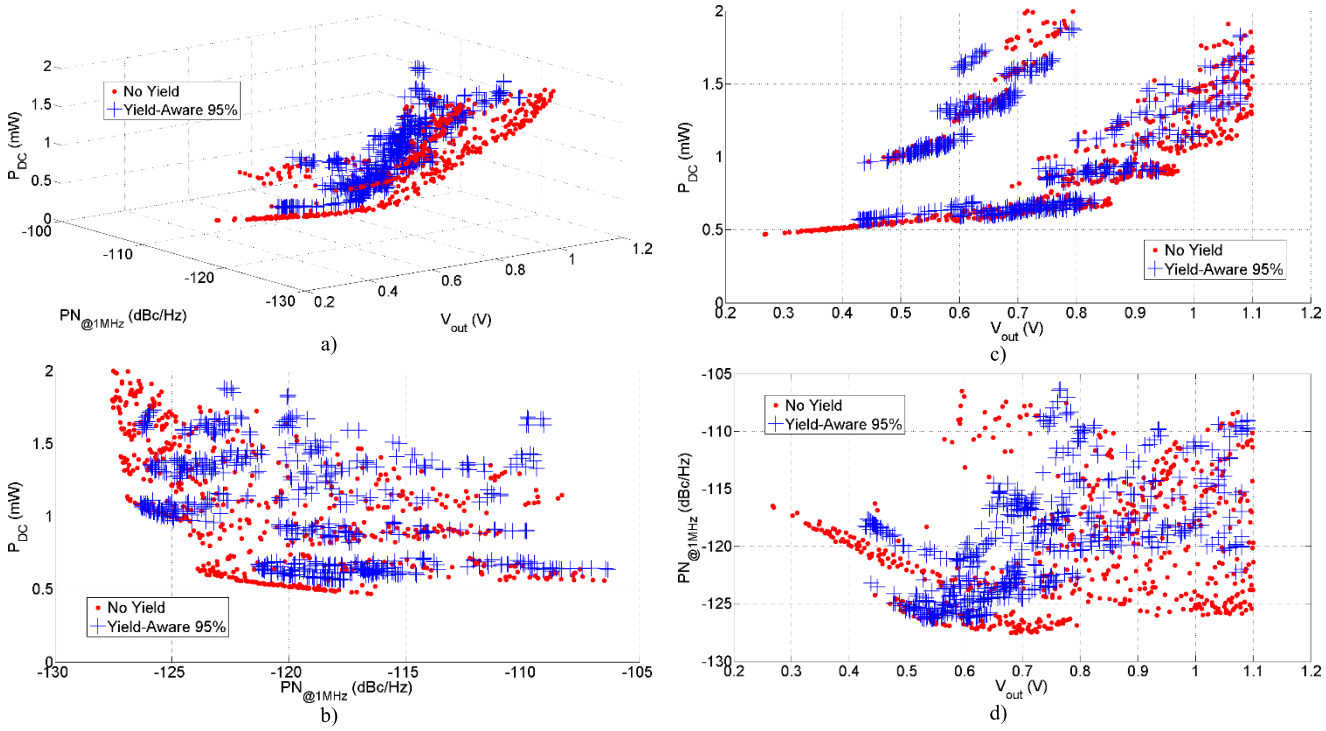

FIGURE 9. a) Comparison between the obtained VCO POFs considering typical performances versus yield-aware performances. b) 2-D projection of the POF illustrating PN vs. P_{DC}. c) 2-D projection of the POF illustrating V_{OUT} vs. P_{DC}. d) 2-D projection of the POF illustrating V_{out} vs PN.

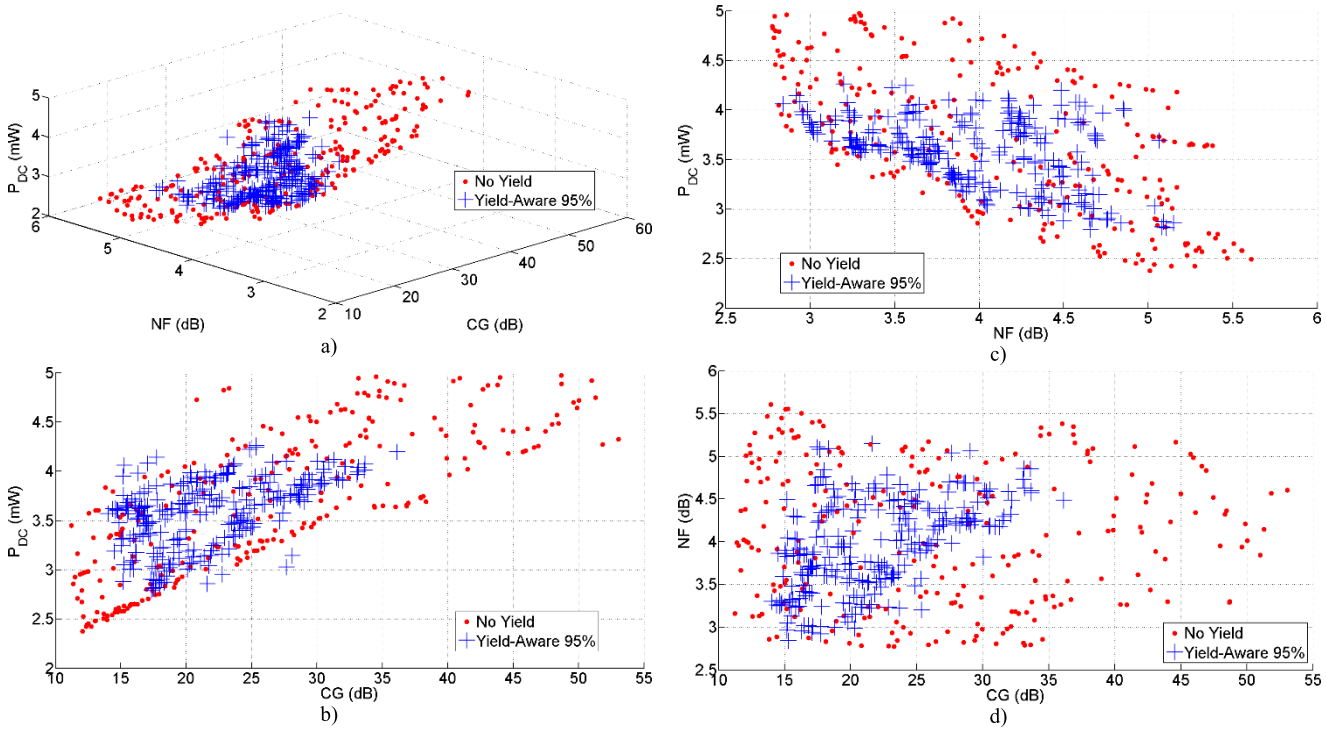

FIGURE 10. a) Comparison between the obtained front-end POFs considering typical performances versus yield-aware performances. b) 2-D projection of the POF illustrating CG vs. P_{DC}. c) 2-D projection of the POF illustrating NF vs. P_{DC}. d) 2-D projection of the POF illustrating CG vs. NF.

times the population size (i.e., $800 \times 400 = 320,000$). The total time in a yield-aware optimization-based using a full MC methodology is the number of iterations times the population size times the execution time of an MC simulation, which in our case was 8s (i.e., $800 \times 400 \times 8 = 2,560,000s$). Therefore, is it possible to conclude that the yield-aware

optimization with only MC analysis of all candidate solution points would last approximately 711 hours for the LNA. But, considering that the optimization was running on 4 threads, the time is 711/4 = 178 hours, which compared to our yield-aware approach, which took around 19 hours, is still 6 days increase. Therefore, our methodology proves to be very efficient due to the new multi-thread yield estimation technique.

D. IMPORTANCE OF ENSURING YIELD AT EACH LEVEL OF THE HIERARCHY

One additional test was performed to show the importance of considering the yield calculation at each hierarchy level to show the importance of the yield calculation at the system level. As explained in section III.B, some works only considered the yield at the low level and then assumed that the yield value would be valid for the system level. Therefore, optimization was performed where the low-level POFs had a 95% yield, and no yield was ensured at the high level. This optimization run with a population of 300 elements and 150 iterations. The obtained results can be seen in Fig. 11. It shows the yield calculated for each point in the POF after the optimization was complete. Even though each circuit in the low-level POFs had at least a 95% yield after the circuits are used in a system, the total system yield was as low as 50%. From the entire POF seen in Fig. 11, only two designs comply with a 95% yield. Therefore, such an experiment clearly shows the importance of considering yield at all levels of the hierarchy.

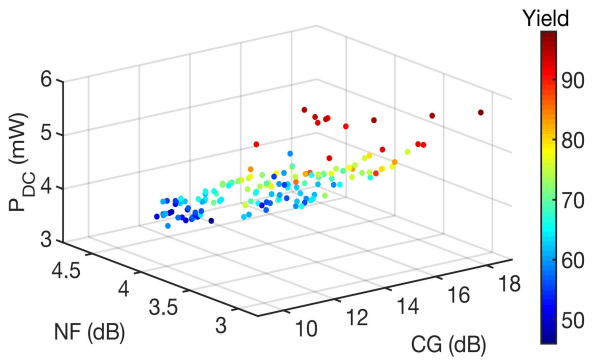

FIGURE 11. System level optimization where the low-level POFs have at least 95% yield but no yield constraint was imposed during the system-level optimization.

V. CONCLUSION

In this paper, an optimization-based hierarchical bottom-up yield-aware methodology is proposed to design robust RF ICs. The methodology combines ML techniques with EAs to undertake the complex task of automating the design of RF circuits while taking yield into account.

The methodology uses a surrogate model to accurately and efficiently model inductors, which are still a bottleneck of RF circuits. Moreover, a multiobjective optimization algorithm is used to obtain circuit POFs, and then, a bottom-up methodology is used to reach system designs. Also, to efficiently consider the circuit yield and perform yield-aware optimizations, throughout the entire hierarchy a new multi-thread yield estimation technique is used to reduce the necessary number of MC simulations and therefore reducing the total optimization time when compared to a full MC yield-aware optimization. Ultimately, this work proves that it is necessary to consider the circuit yield over the entire hierarchy, achieving fully optimal designs. This was proven by comparing the methodology proposed in this work against other methodologies that do not consider yield throughout the complete hierarchy of the system.

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ANTÓNIO CANELAS received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the Instituto Superior Técnico, University of Lisbon, Portugal, in 2010, 2012, and 2019, respectively. In 2011, he held a research position at the Instituto de Telecomunicações, where he was working on time series analysis and pattern discovery. He is currently a Postdoctoral Researcher at the Instituto de Telecomunicações, where he is working in the area of analog and mixed-signal IC design automation and evolutionary computation techniques.

FÁBIO PASSOS received the Ph.D. degree from the Universidad de Sevilla, Seville, Spain, in 2018. At the same time, he was conducting his work at the Instituto de Microelectroìnica de Sevilla (IMSE-CNM), Seville. He has performed research stays in several academic and industrial institutions, such as the IMEC, the Instituto de Telecomunicações, the University of Barcelona, and Analog Devices. He is currently a Marie Curie Postdoctoral Fellow with the Instituto de Telecomunicações, Lisbon, Portugal. His current research interests include the development of automated design methodologies for RF and mm-Wave circuits. He was a recipient of several best paper awards, the EDA Competition Award in SMACD 2016, and the Prestigious Outstanding Dissertation Award from the European Design and Automation Association (EDAA), in 2019. He was a recipient of Postdoctoral Marie Skłodowska-Curie Individual Fellowship, in 2019.

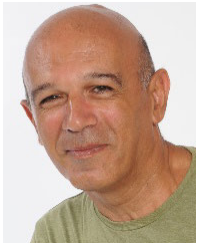
NUNO LOURENÇO (Member, IEEE) received the Licenciado, M.Sc., and Ph.D. degrees in electrical and computer engineering from the Instituto Superior Técnico, University of Lisbon, Portugal, in 2005, 2007, and 2014, respectively. He was an Invited Assistant Professor with the Department of Electrical and Computer Engineering, IST-UL, from 2015 to 2019, where he was distinguished with two "IST Outstanding Teaching Awards." He has been with the Instituto de Telecomunicações, Lisbon, since 2005, where he is currently a Researcher. He has authored or coauthored and supervised over 80 international scientific publications, and is/was a Supervisor of two Ph.D. thesis and eight M.Sc. dissertations. He has participated in several scientific projects with national and international universities and companies, and is the PI of the ongoing internal HAICAS Project funded by IT. His current research interests include AMS/RF IC design, evolutionary computation and machine learning applied to electronic design automation, and applied artificial intelligence. He has received 12 scientific awards and distinctions, including several Best Paper Awards and the Best EDA Tool from SMACD'15 Competition, and the 2010 IET DesignVision Award on the category of Semiconductor IP. He is/was involved in the Organizing Committee of several international conferences, such as IEEE ISCAS'15 and PRIME'16-21 or SMACD'16-21, and he is/was the Publication Co-Chair of the International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design 2016, 2017, 2019 and 2021, and the Conference on Ph.D. Research in Microelectronics and Electronics (PRIME) 2016, 2019, and 2021, technically sponsored by IEEE, IEEE CEDA, and IEEE CAS societies.

RICARDO MARTINS (Member, IEEE) received the Ph.D. degree in electrical and computer engineering from the Instituto Superior Técnico–University of Lisbon (IST–UL), Portugal, in 2015. He was also an Invited Assistant Professor with the Department of Electrical and Computer Engineering, IST-UL. He is conducting his research at the Instituto de Telecomunicações. He has participated in several scientific projects with national and international Institutes, Universities and Companies, and is the Principal Investigator of the ongoing LAY(RF)^2. He has authored or coauthored and supervised more than 70 international scientific publications. His research interests include electronic design automation tools for analog, mixed-signal, radio-frequency and millimeter wave integrated circuits, deep nanometer integration technologies, applied soft computing, and machine and deep learning. He is/was involved in the Organizing Committee of several international conferences. He has received ten scientific awards and distinctions, including best paper awards and best EDA tool for his oral presentations and live demonstrations. In July 2019, he was the General Chair of the International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD) held at the École Polytechnique Fédérale de Lausanne, Switzerland, technically sponsored by IEEE, IEEE CEDA, and IEEE CAS societies.

ELISENDA ROCA received the Ph.D. degree in physics from the Universidad de Barcelona, Spain, in 1995. Since 1995, she has been with the Instituto de Microelectrónica de Sevilla (IMSE-CNM-CSIC), Seville, Spain, where she is currently a Tenured Scientist. She has been involved in several national and international research projects with different institutions, such as CEC, ESA or ONR-NICOP. She has also coauthored more than 150 papers in international journals, books, and conference proceedings. Her research interests include modeling and design methodologies for analog, mixed-signal and RF integrated circuits, and reliability circuit design.

RAFAEL CASTRO-LÓPEZ (Member, IEEE) received the Ph.D. degree in microelectronics from the Universidad de Sevilla, Seville, Spain, in 2005. Since 1998, he has been a Researcher with the Instituto de Microelectrónica de Sevilla (IMSE-CNM), where he holds the position of a Tenured Scientist. He has participated as a Researcher in several national and international research and development projects. He has coauthored more than 100 international journals and conferences, and has authored or edited five books and book chapters. His current research interests include the design and design methodologies of analog, mixed-signal, and RF circuits, and reliable circuit design. He has served as the general chair and participated in the Program Committee of several international conferences. He is currently serving as an Associate Editor for the *Integration, the VLSI Journal* (Elsevier), and as an Expert Collaborator in the ICT area of the State Research Agency.

NUNO HORTA (Senior Member, IEEE) received the Licenciado, M.Sc., Ph.D., and Habilitation degrees in electrical and computer engineer from the Instituto Superior Técnico (IST), University of Lisbon, Lisbon, Portugal, in 1989, 1992, 1997, and 2014, respectively. In 1998, he joined the Department of Electrical and Computer Engineering, IST, where he is currently an Associate Professor with Habilitation. Since 1998, he has been with the Instituto de Telecomunicações, Lisbon, where he is also the Head of the Integrated Circuits Group. He has supervised over 100 post-graduation works between the M.Sc. and Ph.D. theses. He has also participated as a Researcher or a Coordinator in several National and European research and development projects. He has authored or coauthored over 200 publications as books, book chapters, international journals articles, and conferences papers. His current research interests include analog and mixed-signal IC design, analog IC design automation, soft computing, and data science. He was the General Chair of AACD 2014, PRIME 2016, and SMACD 2016 and is/was a member of the organizing and technical program committees of several other conferences, such as IEEE ISCAS, IEEE LASCAS, DATE, and NGCAS. He is an Associate Editor of *Integration, the VLSI Journal* (Elsevier), and usually acts as a Reviewer of several prestigious publications, such as IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, IEEE TRANSACTIONS ON EVOLUTIONARY COMPUTATION, *IEEE Circuits and Systems Magazine*, *ESWA*, and *ASC*.



FRANCISCO V. FERNÁNDEZ (Member, IEEE) received the Ph.D. degree in microelectronics from the Universidad de Sevilla, Spain, in 1992. In 1993, he worked as a Postdoctoral Research Fellow at KUL (Belgium) funded by the European Commission. From 1995 to 2009, he was an Associate Professor with the Department of Electronics and Electromagnetism, Universidad de Sevilla, where he was promoted to a Full Professor, in 2009. He is currently the Head of the Department at IMSE-CNM (Universidad de Sevilla and CSIC). He has authored or edited five books and has coauthored more than 250 papers in international journals and conferences. His research interests include microelectronics reliability, and design and design methodologies of analog, and mixed-signal and radiofrequency circuits. He has served as the general chair for three international conferences and regularly serves at the committees for several international conferences. He was the Editor-in-Chief of *Integration, the VLSI Journal* (Elsevier), from 2005 to 2015.