A New Transformerless Ultra High Gain DC–DC Converter for DC Microgrid Application

SHAHRUKH KHAN[1], (Student Member, IEEE), **MOHAMMAD ZAID**[1], (Member, IEEE),
ARSHAD MAHMOOD[1], **ABBAS SYED NOORUDDIN**[1], (Student Member, IEEE),
JAVED AHMAD[2], **MAMDOUH L. ALGHAYTHI**[3], (Member, IEEE),
BASEM ALAMRI[4], (Member, IEEE), **MOHD TARIQ**[1], (Senior Member, IEEE),
ADIL SARWAR[1], (Senior Member, IEEE), **AND CHANG-HUA LIN**[2], (Member, IEEE)

[1]Department of Electrical Engineering, Zakir Husain College of Engineering and Technology (ZHCET), Aligarh Muslim University, Aligarh 202002, India
[2]Department of Electrical Engineering, National Taiwan University of Science and Technology, Da'an, Taipei 10607, Taiwan
[3]Department of Electrical Engineering, College of Engineering, Jouf University, Sakaka, Aljouf 72388, Saudi Arabia
[4]Department of Electrical Engineering, College of Engineering, Taif University, Taif 21944, Saudi Arabia

Corresponding author: Mohammad Zaid (mohammad.zaid@zhcet.ac.in)

ABSTRACT High gain dc-dc converters are used in several applications which include solar photovoltaic system, switch-mode power supplies and fuel cells. In this paper, an ultra-high gain dc-dc boost converter is proposed and analyzed in detail. The converter has a gain of six times as compared with the boost converter. The high gain is achieved by utilizing switched inductors and switched capacitors. A modified voltage multiplier cell (VMC) with switched inductors is proposed. The converter has a single switch which makes its operation easy. Moreover, the voltage across the switch, diodes and capacitors are less than the output voltage which increases the overall efficiency of the converter. The converter performance in steady-state is analyzed in detail and it is compared with other latest high gain converters. The working of the converter in non-ideal conditions is also discussed in detail. The loss analysis is done using PLECS software by incorporating the real models of switches and diodes from the datasheet. To confirm and validate the working of the proposed converter a hardware prototype of 200 W is developed in the laboratory. The converter achieves high gain at low duty ratios and its performance is found to be good in open and closed loop conditions.

INDEX TERMS Boost converter, DC microgrid, duty cycle, ultra high gain, voltage stress.

I. INTRODUCTION

Power electronics play an important role to extract maximum energy from renewable and clean energy sources. Figure 1 shows a schematic of a DC microgrid. High gain dc-dc converters act as a medium between the load and the source and boost the low voltage(12V-60V) generated by the battery, solar photovoltaic (PV) and fuel cell to high DC voltage(200-300V). Moreover, a high gain dc-dc converter in a DC microgrid maintains the dc-link voltage to the desired value [1]. A combination of supercapacitors and a high gain dc-dc converter is also employed nowadays in a DC microgrid because supercapacitors have high power density but a low voltage rating. High gain converters are nowadays used in

level three fast charging of electric vehicle (EV). A combination of a high gain converter with an inverter can be used to feed AC loads in islanded mode operation of a DC microgrid. High gain converters have gained prominence because the traditional boost converters and their variants [1] are associated with poor efficiency and high duty cycle operation to achieve the high gain. Also, there is a problem of reverse recovery in the diode at an increased duty cycle. These converters are broadly classified into isolated and non-isolated structures. Isolated converters isolate the output from the input electrically dividing circuit into two separate sections preventing the direct flow of current. This is achieved by using a high-frequency transformer but it increases the size and cost [3]–[6] of the converter. Isolated topologies are favoured in high power applications and where common ground between source and load is required.
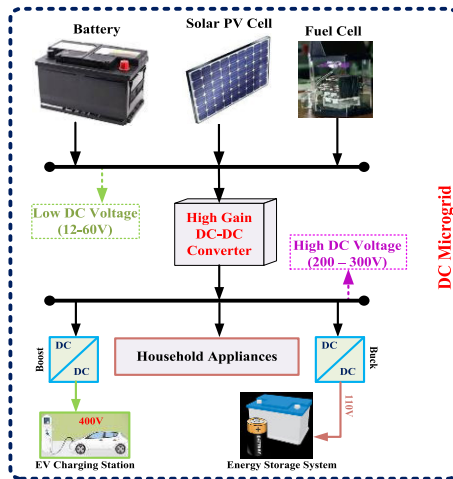
FIGURE 1. Simple schematic of DC microgrid.

Non-isolated converters are favoured where isolation of input from output is not required. They can be classified as coupled and non-coupled types [7]. The coupled inductor topologies can produce very high voltage gain with low stress on the semiconductor switch but the problems with leakage inductance can result in large voltage spikes across the switch for which a clamped circuit needs to be designed. To achieve a high gain capacitor-diode voltage multiplier cell and cascading of two or more converters is employed. Several new and modified topologies use voltage multiplier circuit (VMC) made of switched capacitors and inductors to increase the gain of the converter. The quadratic boost (QBC) and cubic boost topologies can produce high gain at low duty cycles with reduced stress on switching devices [8]–[10] but at higher duty ratios the efficiency may decrease with an increase in current. Further, the inductor core is more prone to enter saturation at higher duty cycles. In [11] a new quadratic boost converter is proposed with lower inductor current ripple and low stress across the switch. Another class of high gain boost converter is a quasi-z-source or z-source converter that is used to increase the gain of the converter where the inductor is replaced by an impedance network but these converters have a restricted duty cycle [12], [13] operation. Interleaved boost converters are being used to acquire high output voltage and high efficiency [14] with a lesser number of switches. In a multiphase interleaved converter is introduced along with a z-source network to achieve high gain. The input current ripple is low therefore there the need for an input filter does not arise. The problem with interleaved converters is that a voltage boost circuit is needed at the end to increase the gain [15] of the converter. Several new converter topologies have been discussed in [16] with the well-known Cockcroft-Walton voltage multiplier cell. A new single-ended primary inductor converter (SEPIC) is presented in [17] with a single switch is used to achieve high gain. Another new SEPIC converter with both buck and boost topology is presented in [18]. Single input multiport output is a good way of getting different output voltage using a single input. These converters have

better voltage regulation capability and low stress across the output capacitor as compared to single input [19], [20] single-output (SISO) converter. They can be used as individual SISO converters.

A quadratic boost converter is proposed by using the voltage lift technique (VL) in [21]. In [22] VL technique is used to get desired value of gain but the converter utilizes two switches that are switched alternately. A hybrid converter based on voltage multiplier cell (VMC) and switched capacitor cells with high gain is presented in [23]. It overcomes shortcomings such as high voltage and current stress on the power devices. A converter with a similar gain is presented by authors in [24] but the stress on two switches is different and it uses the diode voltage capacitor multiplier and switched inductor voltage multiplier to achieve high gain. A high step-down interleaved converter is presented in [25] using a similar concept of switched/series capacitor using six switches. A novel switched impedance network-based converter is presented in [26]. It utilizes a voltage doubler-switched capacitor network to achieve higher gain at lower duty ratios. A multistage structure can significantly increase the gain but efficiency can be low due to a greater number of components. A hybrid zeta boost converter with a switched inductor is proposed in [27] but its voltage gain is not very high. A new tranformerless active switched network is presented in [28] by using two switches but the gain achieved is lower than the proposed topology in this paper. A switched capacitor network-based topology is presented in the paper [29]. In [30] the switched inductor topology has used two inductor and two switches but the voltage gain is not very high. A modified SEPIC converter is presented in [32] to achieve high voltage gain. In [34] the converter uses parallel input and series output (PISO) technique to increase voltage gain. Furthermore, the stress voltage of switches and diodes has been reduced.

In this article, the proposed high gain converter has a VMC made up of switched inductors. A combination of switched capacitors and VMC achieves ultra-high gain with only one switch and two inductors. High gain topologies proposed in [28]–[31] utilize two switches and have much less voltage gain as compared with the proposed converter in this paper. The attractive features of the proposed converter are

- The converter achieves a voltage conversion ratio of six times that of the conventional boost converter.
- The converter uses a single switch that has low voltage stress i.e. one-third of output voltage.
- A coupled inductor is not used so the problem of leakage inductance is avoided.
- The voltage stress on all the semiconductor devices is equal. The devices with a uniform rating and low internal resistance can be used.

The paper discusses the structure and principle of operation of the converter in section II. Steady-state operation of the proposed converter in the continuous and discontinuous mode of operation is presented in section III and IV respectively. In section V and VI non-ideal gain analysis
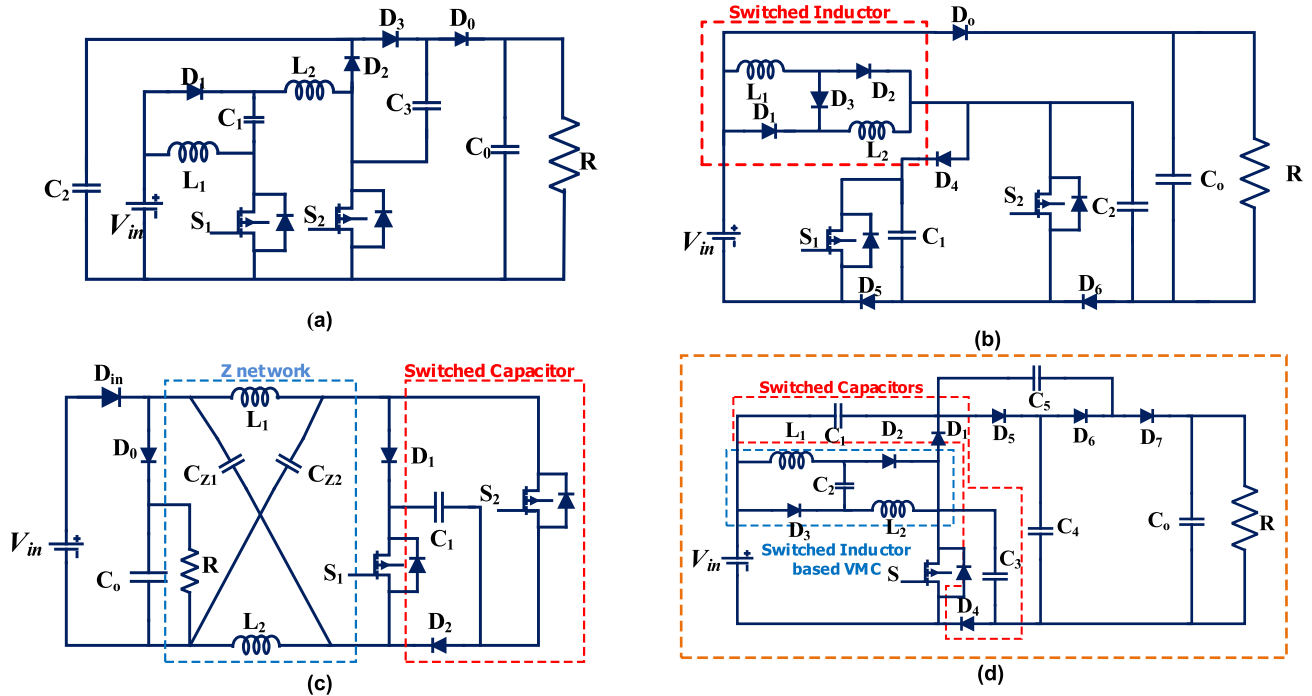
FIGURE 2. (a) Active switch inductor in [28] (2021) (b) Switched Inductor (SL-DS-DC) in [29] (2021) (c) Switched-capacitor with Z network in [30] (2021) (d) Proposed (SC-SL-DC) converter.
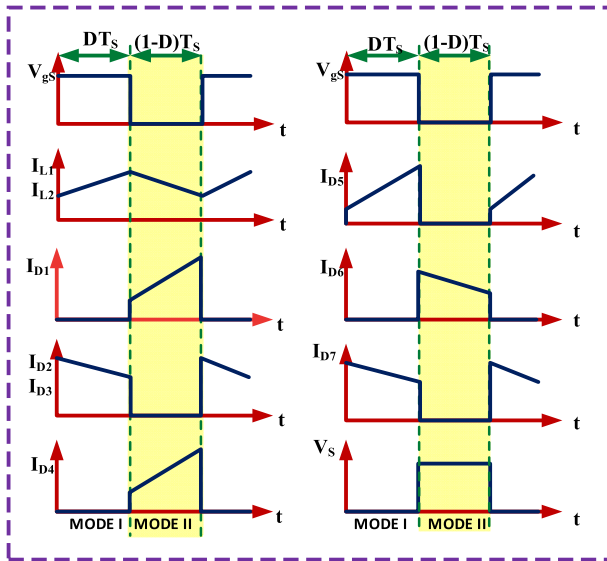

FIGURE 3. Waveforms associated with the converter in CCM.

and comparative study of the proposed structure is presented respectively. Experimental results and efficiency of the converter are shown in section VII. In section VIII conclusion is presented.

II. OPERATING PRINCIPLE OF PROPOSED CONVERTER (SC-SL-DC)

A. CIRCUIT DESCRIPTION

The proposed dc-dc converter topology is presented in Figure 2. The converter consists of a single switch (S), two
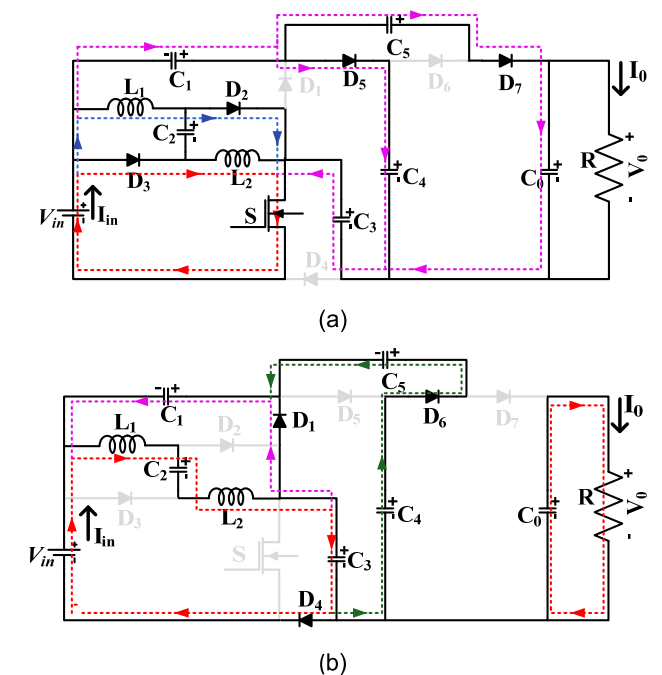

FIGURE 4. Modes of operations for the proposed converter (a) When the switch is ON (b) When the switch is OFF

inductors (L_1 and L_2), seven diodes (D_1, D_2, ..., D_7) and six capacitors including one capacitor C_o as an output filter which filters the output pulsating current and provide a smoothed output voltage. The combination of (L_1, L_2, D_1, D_2 and C_1) is a modified switched capacitor cell while the

combination of (C_1, D_1, C_3 and D_4) is switched capacitor cell. Some important waveforms for the proposed converter are shown in Figure 3. All capacitors are sufficiently large, therefore the voltage across capacitors is assumed to be constant. And all components are assumed as ideal.

B. MODES OF OPERATION
This converter can be operated in both CCM and DCM modes of operation. The CCM operation of the proposed converter has two modes. In the first mode when the switch is conducting and the second one is analyzed when the switch is turned OFF. Analysis of the proposed converter for one switching period under CCM mode and in steady-state is as follows

1) MODE I: WHEN SWITCH IS ON ($0 < t < DT_S$)
Mode I of operation is shown in Figure 4(a). In this interval, the switch is turned ON and the diodes D_2, D_3, D_5 and D_7 are forward biased. The voltage across inductors L_1 and L_2 is equal to the input voltage (V_{in}) by which they are magnetized and therefore, inductor currents I_{L1} and I_{L2} increase linearly. In this mode, Capacitor C_1 discharges and transfer its energy through capacitor C_5 and load. During this interval, C_2 and C_3 discharge through L_2 and C_4. Thus, related equations can be drawn out as follows:

The voltage across inductors appears as shown (1)

$$\begin{cases} V_{L1} = L_1 \dfrac{dI_{L1}}{dt} = V_{in} \\ V_{L2} = L_2 \dfrac{dI_{L2}}{dt} = V_{in} \end{cases} \quad (1)$$

The voltage across capacitors is derived from Figure 4(a) using KVL and KCL as follows:

$$\begin{cases} V_{C2} = -V_{in} \\ V_{C4} + V_{C5} = V_o \\ V_{C1} + V_{C5} + V_{C3} = V_o - V_{in} \end{cases} \quad (2)$$

Current relations through capacitors, inductors, diodes and switch can be estimated as follows:

$$\begin{cases} C_1 \dfrac{dV_{C1}}{dt} = I_{C1} = I_{in} - I_{L1} - I_{D3} \\ C_2 \dfrac{dV_{C2}}{dt} = I_{C2} = I_{L1} - I_{D2} \\ C_3 \dfrac{dV_{C3}}{dt} = I_{C3} = I_{L2} + I_{D2} - I_S \\ C_4 \dfrac{dV_{C4}}{dt} = I_{D5} \\ C_0 \dfrac{dV_{C0}}{dt} = I_{Co} = I_{C5} - I_o \end{cases} \quad (3)$$

C. MODE II: WHEN SWITCH IS OFF ($DT_S < t < T_S$)
In this interval, the switch is turned OFF and the diodes D_1, D_4 and D_6 are forward biased and the other three diodes are reversed biased. The circuit diagram is shown in Figure 4(b). During this interval, V_{in} charges C_1 and L_1 charges C_2. Inductor L_2 transfer its stored energy to C_3. Output capacitor C_0 transfer its energy to load R.

Using KVL and KCL in mode II, the voltage across inductors come out as follows:

$$V_{L1} + V_{L2} = L_1 \frac{dI_{L1}}{dt} + L_2 \frac{dI_{L2}}{dt} = V_{in} - V_{C2} - V_{C3} \quad (4)$$

In (2), it is derived that

$$V_{C2} = -V_{in}$$

Equation (4) can now be written as

$$V_{L1} + V_{L2} = 2V_{in} - V_{C3} \quad (5)$$

The voltage across the capacitors can be written by applying KVL in Figure 4(b)

$$\begin{cases} V_{C4} - V_{C5} = V_{C3} \\ V_{C3} - V_{C1} = V_{in} \end{cases} \quad (6)$$

Current passing through capacitors relations can be shown as follows:

$$\begin{cases} C_1 \dfrac{dV_{C1}}{dt} = I_{C1} = I_{in} - I_{L1} \\ C_2 \dfrac{dV_{C2}}{dt} = I_{C2} = I_{L1} = I_{L2} \\ C_3 \dfrac{dV_{C3}}{dt} = I_{C3} = I_{L1} - I_{D1} \\ C_4 \dfrac{dV_{C4}}{dt} = C_5 \dfrac{dV_{C5}}{dt} = I_{C4} = I_{C5} = I_{C1} - I_{D1} \\ C_0 \dfrac{dV_{C0}}{dt} = I_{C0} = -I_0 \end{cases} \quad (7)$$

III. STEADY STATE ANALYSIS IN CCM
A. CALCULATION OF CAPACITOR VOLTAGES AND VOLTAGE GAIN
Applying the principle of volt-second balance on inductors L_1 and L_2 and using (1), (2), (4) and (6) the voltage conversion ratio, M can be derived as shown.

$$\int_0^{DT_S} (V_{L1} + V_{L2}) \, dt + \int_{DT_S}^{T_S} (V_{L1} + V_{L2}) \, dt = 0$$

where, T_S is switching time period.

Using this equation following results can be drawn out as.

$$2V_{in}D + (2V_{in} - V_{C3})(1 - D) = 0 \quad (8)$$

It is clear from (8), that

$$V_{C3} = \frac{2V_{in}}{(1 - D)} \quad (9)$$

From (6) it can be written that

$$V_{C4} - V_{C5} = V_{C3}$$

Using (9) in (6) the following equation can be written

$$V_{C4} - V_{C5} = \frac{2V_{in}}{(1 - D)} \quad (10)$$

Again from (2)

$$V_{C4} + V_{C5} = V_o \quad (11)$$

Solving (10) and (11), it can be shown that

$$\begin{cases} V_{C4} = \dfrac{V_0}{2} + \dfrac{V_{in}}{(1-D)} = \dfrac{2V_0}{3} \\ V_{C5} = \dfrac{V_0}{2} - \dfrac{V_{in}}{(1-D)} = \dfrac{V_o}{3} \end{cases} \quad (12)$$

From (2) again,

$$V_{C1} + V_{C5} + V_{C3} = V_o - V_{in} \quad (13)$$

Also, from (6)

$$V_{C1} = V_{C3} - V_{in} \quad (14)$$

Putting this value in equation (13), it can be shown that

$$V_{C5} + 2V_{C3} = V_o \quad (15)$$

Using (12) and (15), it can be drawn out easily.

$$V_{C3} = \frac{V_0}{4} + \frac{V_{in}}{2(1-D)} = \frac{V_o}{3} \quad (16)$$

From (9) and (16), voltage gain is derived as,

$$M = \frac{V_0}{V_{in}} = \frac{6}{(1-D)} \quad (17)$$

According to (17), it can be seen that the voltage gain of the proposed converter is six times higher than that of the conventional boost converter.

B. VOLTAGE AND CURRENT STRESSES OF POWER DEVICES

In Figure 4, by applying KVL the voltage appeared across the switch (V_{SW}), diodes (V_D) and capacitors (V_C) when they are not conducting, can be expressed as

$$\begin{cases} V_{SW} = V_{C3} = \dfrac{V_0}{3}, & V_{D1} = V_{C4} - V_{C3} = \dfrac{V_0}{3} \\ V_{D2} = V_{D3} = \dfrac{V_0}{3}, & V_{D4} = V_{C3} = \dfrac{V_0}{3} \\ V_{D5} = V_{D6} = V_{C5} = \dfrac{V_0}{3}, & V_{D7} = V_0 - V_{C4} = \dfrac{V_0}{3} \end{cases} \quad (18)$$

The stress on different semiconductor devices is shown in Figure 9.

Assuming a lossless circuit, it can be written

$$P_{in} = P_{out} \Rightarrow V_{in}I_{in} = V_oI_o \quad (19)$$

where I_{in} and I_0 are input and output currents respectively. From (19) and (17), it can be written down:

$$\frac{I_{in}}{I_0} = \frac{V_0}{V_{in}} = M = \frac{6}{(1-D)} \quad (20)$$

From (20), dc input current can be calculated as,

$$I_{in} = \left(\frac{6}{1-D}\right)I_0 \quad (21a)$$

Applying the principle of current balance on the capacitors C_1 and C_2 and using (3) and (7) it can be written as:

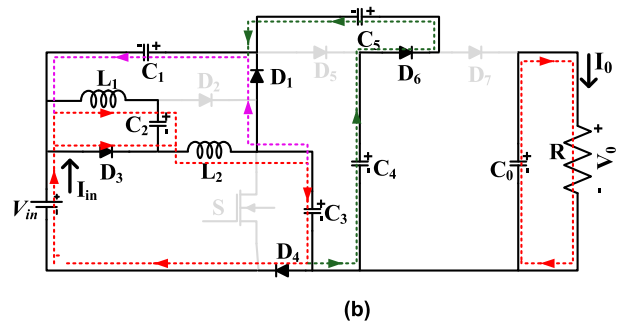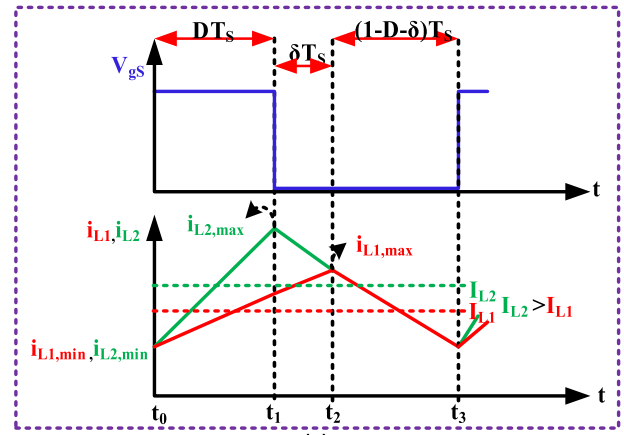$$\int_0^{DT_S} (I_{in} - I_{L1} - I_{D3}) \, dt + \int_{DT_S}^{T_S} (I_{in} - I_{L1}) \, dt = 0$$

FIGURE 5. (a) Inductor current waveforms when L1 > L2 (b) Mode II.

$$\int_0^{DT_S} (I_{L1} - I_{D2}) \, dt + \int_{DT_S}^{T_S} (I_{L1}) \, dt = 0 \quad (21b)$$

After solving the above equation, the average current through inductors can be found out as

$$I_{L1} = I_{L2} = I_L = \left(\frac{3}{1-D}\right)I_o \quad (22)$$

The dc values of current through the semiconductor devices can be found as

$$\begin{cases} I_{SW_{avg}} = \dfrac{5+D}{1-D}I_O \\ I_{D1} = I_{D2} = I_L = \left(\dfrac{3}{1-D}\right)I_o \\ I_{D3} = I_{D4} = I_{D5} = I_{D6} = I_{D7} = I_o \end{cases} \quad (23)$$

C. SELECTION OF INDUCTORS AND CAPACITORS

For a given suitable value of ripple of inductor currents ΔI_{L1} and ΔI_{L2} at a fixed value of switching frequency f_s for this converter, inductances can be extracted from (1) as:

$$\begin{cases} L_1 = \dfrac{V_{in}D}{\Delta I_{L1}f_s} \\ L_2 = \dfrac{V_{in}D}{\Delta I_{L2}f_s} \end{cases} \quad (24)$$

Moreover, within the valid range of voltage ripple, the value of capacitances can be calculated from

(3) and (7) as:

$$\begin{cases} C_1 = \dfrac{3V_0}{\Delta V_{C1}f_sR}, & C_2 = \dfrac{3V_0}{\Delta V_{C2}f_sR} \\[2mm] C_3 = \dfrac{2V_0}{\Delta V_{C3}f_sR}, & C_4 = \dfrac{V_0}{\Delta V_{C4}f_sR} \\[2mm] C_5 = \dfrac{V_0}{\Delta V_{C5}f_sR}, & C_o = \dfrac{V_0}{\Delta V_{C0}f_sR} \end{cases} \tag{25}$$

To obtain the desired output voltage at the given input voltage, duty cycle D can be calculated. From (17), the duty cycle is:

$$D = \frac{V_0 - 6V_{in}}{V_0} \tag{26}$$

IV. EFFECT OF UNEQUAL INDUCTANCES ON VOLTAGE GAIN

The operation of the converter depends on the inductance values of inductor L_1 and L_2. The current through the inductor will have different slopes and it will change the current waveform of the inductor due to different values of inductances of L_1 and L_2.

A. IF INDUCTANCE VALUE L_1 IS LARGER THAN L_2

The current waveform through the inductor L_1 and L_2 is shown in Figure 5. The converter SC-SL-DC is operated in three modes.

1) MODE I: WHEN SWITCH IS ON (0 < t < t₁)

The Switch is turned ON. This mode is same as Mode I and the equivalent circuit is shown in Figure 4(a). Diode D_1, D_4, D_6 are reverse biased while the diodes D_2, D_3, D_5 and D_7 are forward biased. The voltage across the inductors L_1 and L_2 is equal to input voltage by which they are magnetized and therefore, inductor currents I_{L1} and I_{L2} increase linearly with different slopes. The slope of inductor currents of L_1 and L_2 can be achieved as

$$\frac{dI_{L1}}{dt} = \frac{V_{in}}{L_1} \tag{27}$$

$$\frac{dI_{L2}}{dt} = \frac{V_{in}}{L_2} \tag{28}$$

In this mode the current through L_1 is less than current through L_2 because the inductance value of $L_1 > L_2$.

2) MODE II: WHEN SWITCH IS ON (t₁ < t < t₂)

Switch is just turned OFF. This mode occurs for a very duration of δT_S as shown in Figure 5(a). The equivalent circuit in this mode is shown in Figure 5(b). Diode D_1, D_3, D_4 and D_6 are forward biased while the diodes D_2, D_5 and D_7 are reverse biased. Inductor current I_{L1} is smaller than I_{L2} as shown in Figure 5(a). The current through L_1 has positive slope and magnetizes in this period and the current L_2 has large negative slope and discharge in this period. The current through D_3 will be difference between inductor current I_{L2} and I_{L1}.

The slope of inductor currents of L_1 and L_2 can be achieved as

$$\frac{dI_{L1}}{dt} = \frac{-V_{C2}}{L_1} = \frac{V_{in}}{L_1} \tag{29}$$

$$\frac{dI_{L2}}{dt} = \frac{V_{in} - V_{C3}}{L_2} \tag{30}$$

In this mode the current through L_1 is less than current through L_2 because the inductance value of $L_1 > L_2$ and this mode ends when $I_{L1} = I_{L2}$ and converter operates in Mode III.

3) MODE III: SWITCH IS OFF (t₂ < t < DT_s)

Switch is OFF. The equivalent circuit is same as Mode II in CCM as shown in Figure 4(b). Diode D_1, D_4, D_6 are forward biased while the diodes D_2, D_3, D_5 and D_7 are reverse biased. The inductors L_1 and L_2 are in series and the current through inductors L_1 and L_2 are equal and demagnetize with equal negative slope which can be achieved as follows

$$\frac{dI_{L1}}{dt} = \frac{2V_{in} - V_{C3}}{L_1 + L_2} \tag{31}$$

$$\frac{dI_{L2}}{dt} = \frac{2V_{in} - V_{C3}}{L_1 + L_2} \tag{32}$$

The average of voltage across the inductor is zero. Therefore,

$$L_1 \rightarrow D\,(V_{in}) + \delta\,(V_{in}) + \frac{L_1\,(2V_{in} - V_{C3})}{L_1 + L_2}$$
$$\times\,(1 - D - \delta) = 0 \tag{33}$$

$$L_2 \rightarrow D\,(V_{in}) + \delta\,(V_{in} - V_{C3}) + \frac{L_2\,(2V_{in} - V_{C3})}{L_1 + L_2}$$
$$\times\,(1 - D - \delta) = 0 \tag{34}$$

Also,

$$V_{C3} = \frac{V_O}{3} \tag{35}$$

On solving (33)-(35), the voltage gain of proposed converter SC-SL-DC can be obtained as

$$\left.\frac{V_0}{V_{in}}\right|_{L1>L2} = \frac{6}{(1 - D)} \tag{36}$$

The voltage gain is same as equation (17) but the average value of inductor current L_1 is less than inductor current L_2.

B. IF INDUCTANCE VALUE L_2 IS LARGER THAN L_1

The current waveform through the inductor L_1 and L_2 is shown in Figure 6. The converter SC-SL-DC is operated in three modes as discussed below

1) MODE I: WHEN SWITCH IS ON (0 < t < t₁)

The Switch is turned ON. This mode is same as Mode I and the equivalent circuit is shown in Figure 4(a). Diode D_1, D_4, D_6 are reverse biased while the diodes D_2, D_3, D_5 and D_7 are forward biased. The voltage across the inductors L_1 and L_2 is equal to input voltage by which they are magnetized and therefore, inductor currents I_{L1} and I_{L2} increase linearly with
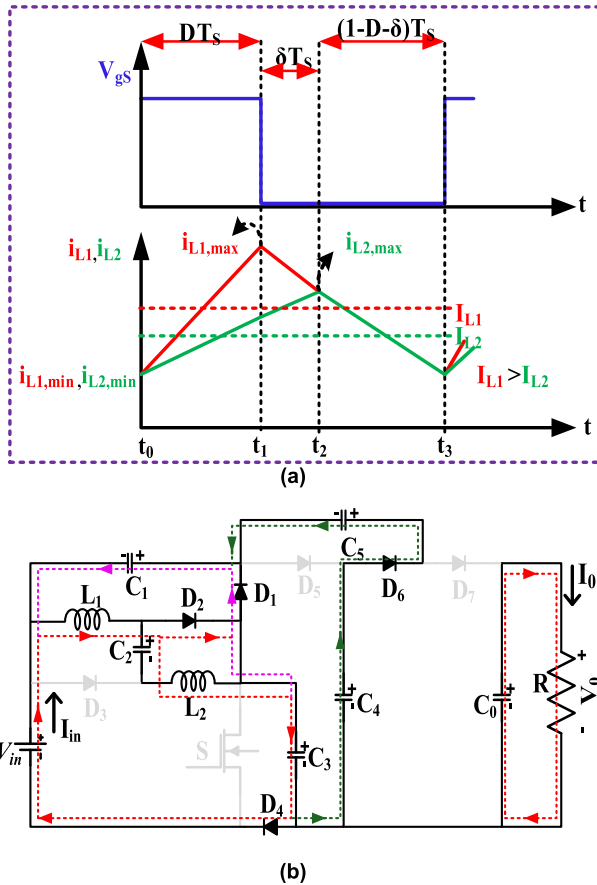
FIGURE 6. (a) Inductor current waveforms when L1 < L2 (b) Mode II.

different slopes. The slope of inductor currents of L_1 and L_2 can be achieved as

$$\frac{dI_{L1}}{dt} = \frac{V_{in}}{L_1} \tag{37}$$

$$\frac{dI_{L2}}{dt} = \frac{V_{in}}{L_2} \tag{38}$$

In this mode the current through L_2 is less than current through L_2 because the inductance value of $L_1 < L_2$.

2) MODE II: WHEN SWITCH IS ON ($t_1 < t < t_2$)
Switch is just turned OFF. This mode occurs for a very duration of δT_S as shown in Figure 6(a). The equivalent circuit in this mode is shown in Figure 6(b). Diode D_1, D_2, D_4 and D_6 are forward biased while the diodes D_3, D_5 and D_7 are reverse biased. Inductor current I_{L2} is smaller than I_{L1} as shown in Figure 6(a). The current through L_2 has positive slope and magnetizes in this period and the current L_1 has large negative slope and discharge in this period. The current through D_2 will be difference between inductor current I_{L1} and I_{L2}.

The slope of inductor currents of L_1 and L_2 can be achieved as

$$\frac{dI_{L1}}{dt} = \frac{V_{in} - V_{C3}}{L_1} \tag{39}$$

$$\frac{dI_{L2}}{dt} = \frac{-V_{C2}}{L_2} = \frac{V_{in}}{L_2} \tag{40}$$

In this mode the current through L_2 is less than current through L_1 because the inductance value of $L_1 < L_2$ and this mode ends when $I_{L1} = I_{L2}$ and converter operates in Mode III.

3) MODE III: SWITCH IS OFF ($t_2 < t < DT_s$)
Switch is OFF. The equivalent circuit is same as Mode II in CCM as shown in Figure 4(b). Diode D_1, D_4, D_6 are forward biased while the diodes D_2, D_3, D_5 and D_7 are reverse biased. The inductors L_1 and L_2 are in series and the current through inductors L_1 and L_2 are equal and demagnetize with equal negative slope which can be achieved as follows

$$\frac{dI_{L1}}{dt} = \frac{2V_{in} - V_{C3}}{L_1 + L_2} \tag{41}$$

$$\frac{dI_{L2}}{dt} = \frac{2V_{in} - V_{C3}}{L_1 + L_2} \tag{42}$$

The average of voltage across the inductor is null. Therefore,

$$L_1 \rightarrow D(V_{in}) + \delta(V_{in} - V_{C3}) + \frac{L_1(2V_{in} - V_{C3})}{L_1 + L_2}$$
$$\times (1 - D - \delta) = 0 \tag{43}$$

$$L_2 \rightarrow D(V_{in}) + \delta(V_{in}) + \frac{L_2(2V_{in} - V_{C3})}{L_1 + L_2}$$
$$\times (1 - D - \delta) = 0 \tag{44}$$

Also,

$$V_{C3} = \frac{V_O}{3} \tag{45}$$

On solving (43)-(45), the voltage gain of proposed converter SC-SL-DC can be obtained as

$$\left.\frac{V_0}{V_{in}}\right|_{L2>L1} = \frac{6}{(1 - D)} \tag{46}$$

From equation (36) and (46) it can be seen that the voltage gain is unaffected with unequal values of inductances L_1 and L_2 i.e. six times the traditional boost converter (TBC). However, the average value of current through the inductors are changed.

V. STEADY STATE ANALYSIS IN DCM
A. MODE I: WHEN SWITCH IS ON ($0 < t < DT_S$)
This mode is the same as Mode I of CCM mode and equivalent circuitry is depicted in Figure 4(a). Both the inductors L_1 and L_2 are magnetized by the input source voltage V_{in}. The current rises from zero to maximum value in both the inductors till the time, $t_1 = DT$.

B. MODE II: WHEN SWITCH IS OFF ($DT_S < t < D_1T_S$)
This mode is equivalent to mode II of CCM. All the inductors demagnetize from their maximum value to zero at time $t_2 = D_1T$.

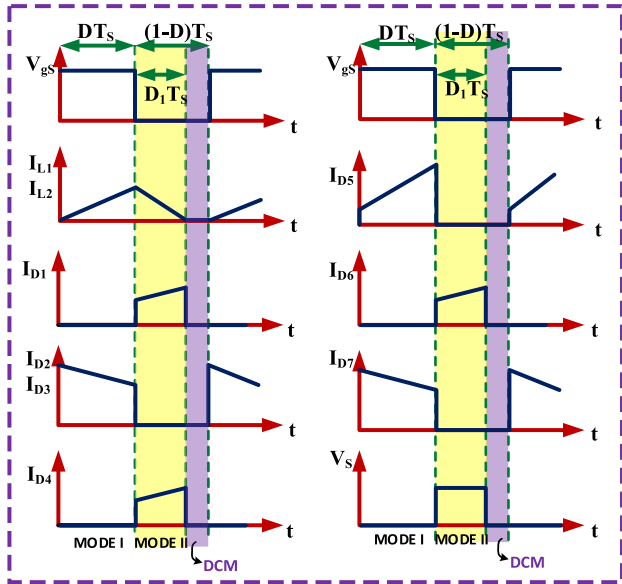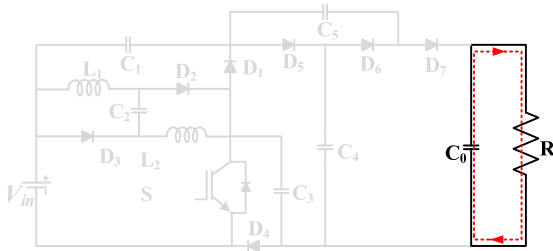FIGURE 7. Waveforms associated with the converter in DCM.

FIGURE 8. Conduction diagram in DCM mode (mode III).

C. MODE III: WHEN SWITCH IS OFF AND INDUCTOR CURRENT IS ZERO ($D_1 T_S < t < T_S$)

In this mode, all diodes D_1-D_7 are reverse biased. Inductor current in this interval ($t_2 < t < t_3$) is zero. Energy is provided by capacitor C_o to load R. The equivalent circuit diagram and associated waveforms are depicted in Figure 7 and Figure 8.

Applying the volt-sec balance principle on the inductors yields the following relation

$$D_1 = \frac{6D}{\frac{V_O}{V_{in}} - 6} \quad (47)$$

$$I_L = I_{D1} + I_{D4} + I_{D6} = 3I_O \quad (48)$$

$$\frac{3V_O}{R} = \frac{1}{2}D(D + D_1)\frac{V_{in}}{Lf_S} \quad (49)$$

$$\frac{V_o}{V_{in}} = \frac{D(D + D_1)R}{6Lf_S} \quad (50)$$

Using the value of D_1 from (47) in (50) the following quadratic equation is obtained

$$\left(\frac{V_O}{V_{in}}\right)^2 - 6\frac{V_O}{V_{in}} - \frac{6D^2}{\beta} = 0 \quad (51)$$
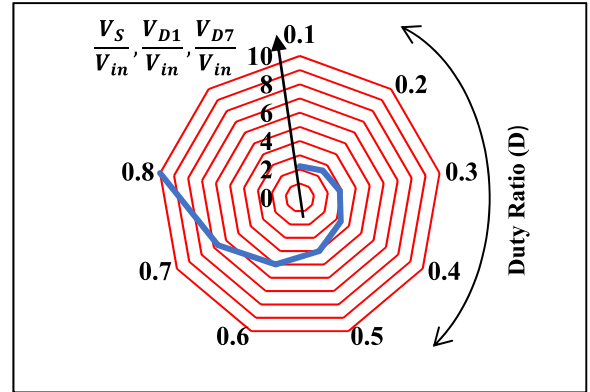

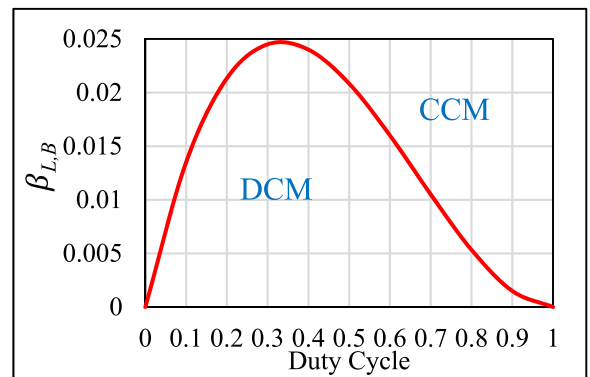FIGURE 9. Semiconductor stress plot at different values of duty cycle.

FIGURE 10. Normalized inductor time constant at the boundary versus duty cycle curve.

Defining $\beta_L = \frac{6Lf_S}{R}$ as normalized inductor time constant, the ideal voltage gain (M_{DM}) in DCM mode is calculated as

$$M_{DM} = \frac{V_O}{V_{in}} = 3 + \sqrt{9 + \frac{6D^2}{\beta_L}} \quad (52)$$

If the converter is to be operated at the boundary of CCM and DCM, then the voltage gain of both modes will be equal. The normalized inductor time ($\beta_{L,B}$) constant at the boundary is calculated as

$$\beta_{L,B} = \frac{D(1 - D)^2}{6} \quad (53)$$

A plot between $\beta_{L,B}$ and duty ratio D is shown illustrated in Figure 8. The converter operates in CCM mode if $\beta_L > \beta_{L,B}$ and the reverse is true for DCM mode.

VI. PRACTICAL MODEL OF THE PROPOSED CONVERTER

The equivalent circuit of the proposed converter is shown in Figure 11. R_L is the equivalent series resistance (ESR) of the inductor R_{SW} is the switch ON-state resistance, R_{DS} and V_{CN} denote the diode internal resistance and voltage drop respectively. R_C is the equivalent series resistance (ESR) of the capacitors.
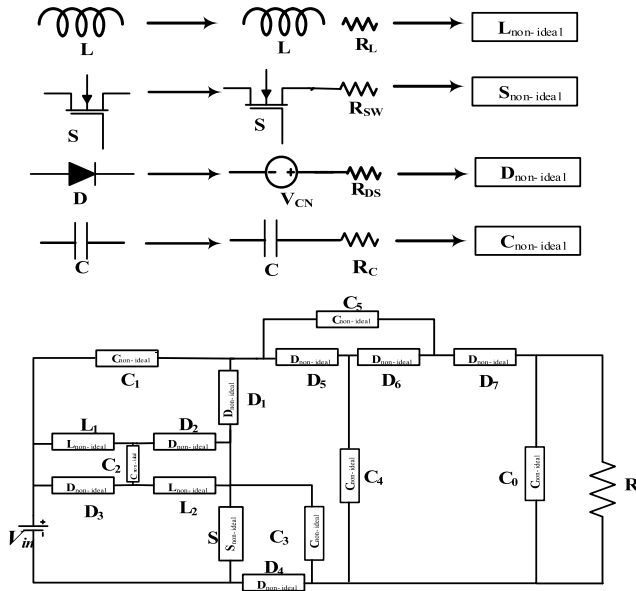
FIGURE 11. Non-ideal model with parasitic elements.

A. EFFECT OF NON-IDEALITIES ON VOLTAGE GAIN

1) EFFECT OF NON-IDEAL INDUCTORS ON VOLTAGE GAIN

The effect of non-ideal inductors having parasitic resistances on voltage gain is analysed and other elements are assumed ideal.

The voltage across inductor L_1 and L_2 in both modes can be found as:

MODE I: The useful voltage relations are:

$$\begin{cases} V_{L1} = V_{in} - I_{L1}R_{L1} \\ V_{L1} = V_{in} - I_{L2}R_{L2} \\ V_{C2} = -V_{in} \end{cases} \tag{54}$$

MODE II: The useful voltage relations are:

$$\begin{cases} V_{L1} + V_{L2} = V_{in} - V_{C2} - V_{C3} - I_{L1}(R_{L1} + R_{L1}) \\ V_{C3} = \dfrac{V_o}{3} \end{cases} \tag{55}$$
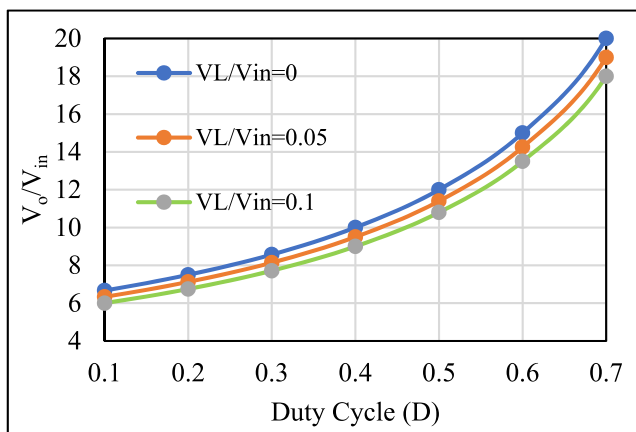

FIGURE 12. Drop across inductor ESR is varied to analyse the non-ideal effect of the inductor on voltage gain.
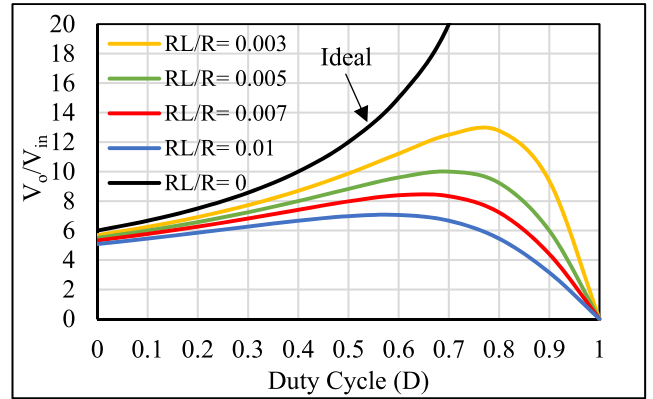

FIGURE 13. Variation of voltage gain with different ratio of ESR resistance at a different duty cycle.

If $R_{L1} = R_{L1} = R_L$ Then $V_{L1} = V_{L2}$.
Therefore,
MODE I: The inductor voltages are

$$V_{L1} = V_{L2} = V_{in} - I_L R_L \tag{56}$$

MODE II: The inductor voltages are

$$V_{L1} = V_{L2} = V_{in} - I_L R_L - \frac{V_O}{6} \tag{57}$$

Since the average value of the voltage inductor is zero in the switching time interval.

$$D(V_{in} - I_L R_L) + (1 - D)(V_{in} - I_L R_L - \frac{V_O}{6}) \tag{58}$$

The ratio of output voltage to the input voltage is derived using (58)

$$\frac{V_o}{V_{in}} = \frac{6\left(1 - \frac{I_L R_L}{V_{in}}\right)}{(1 - D)} = \frac{6\left(1 - \frac{V_{LD}}{V_{in}}\right)}{(1 - D)} \tag{59}$$

where $I_L R_L = V_{LD}$ is the drop across R_L
Using the value of I_L from expression (22)

$$\frac{V_o}{V_{in}} = \frac{6\left(1 - \frac{\frac{3V_O}{(1-D)}\frac{R_L}{R}}{V_{in}}\right)}{(1 - D)} \tag{60}$$

$$\frac{V_o}{V_{in}} = \frac{6}{(1 - D)\left[1 + \frac{18}{(1-D)^2}\frac{R_L}{R}\right]} \tag{61}$$

The effect of non-idealities on voltage gain is given by (59) and (61) in the CCM mode of operation of the converter and the plot of both the expression is presented in Figure 12 and Figure 13.

2) EFFECT OF NON-IDEAL SWITCH ON VOLTAGE GAIN

The voltages across the inductors in both modes can be found as:

MODE I: The useful voltage relations are:

$$\begin{cases} V_{L1} = V_{in} - I_{SW}R_{SW} \\ V_{L2} = V_{in} - I_{SW}R_{SW} \end{cases} \tag{62}$$

MODE II: The useful voltage relations are:

$$V_{L1} = V_{L2} = \frac{V_{in} - V_{C2} - V_{C3}}{2} \quad (63)$$

$$V_{C2} = -V_{in} + I_{SW}R_{SW} \quad (64)$$

Since the average value of voltage across the inductor is zero. Therefore, the expression can be derived as follows

$$D(V_{in} - I_{SW}R_{SW}) + (1-D)(\frac{V_{in} - V_{C2} - V_{C3}}{2}) \quad (65)$$

$$D(V_{in} - I_{SW}R_{SW}) + (1-D)(\frac{2V_{in} - I_{SW}R_{SW} - \frac{V_o}{3}}{2}) \quad (66)$$

The ratio of output voltage to the input voltage is derived using (66)

$$\frac{V_o}{V_{in}} = \frac{6\left(1 - \frac{I_S R_{Sw}(1+D)}{2V_{in}}\right)}{(1-D)} = \frac{6\left(1 - \frac{V_{SD}(1+D)}{2V_{in}}\right)}{(1-D)} \quad (67)$$

where $I_S R_{Sw} = V_{SD}$ is the voltage drop across the switch. Using the value of I_{SW} from expression (23)

$$\frac{V_O}{V_{in}} = \frac{6\left(1 - \frac{\frac{(5+D)(1+D)V_o}{2(1-D)}\frac{R_{SW}}{R}}{V_{in}}\right)}{(1-D)} \quad (68)$$

$$\frac{V_O}{V_{in}} = \frac{6}{(1-D)\left[1 + \frac{3(5+D)(1+D)}{(1-D)^2}\frac{R_{SW}}{R}\right]} \quad (69)$$

The effect on voltage gain is given by (67) and (69) and the plot of both the expressions are shown in Figure 14 and 15a respectively. From Figure 15a it can be inferred that the gain rapidly decreases with an increase in the parasitic resistance of the switch, especially at higher duty ratios.

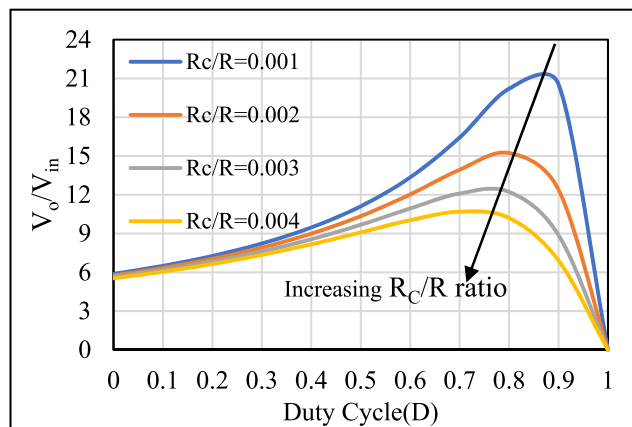### 3) EFFECT OF NON-IDEAL DIODES ON VOLTAGE GAIN
The effect of non-ideal diodes (D_1-D_7) having parasitic resistance (R_D) and forward cut in voltage (V_{CN}) on voltage gain is analysed and other elements are assumed ideal.
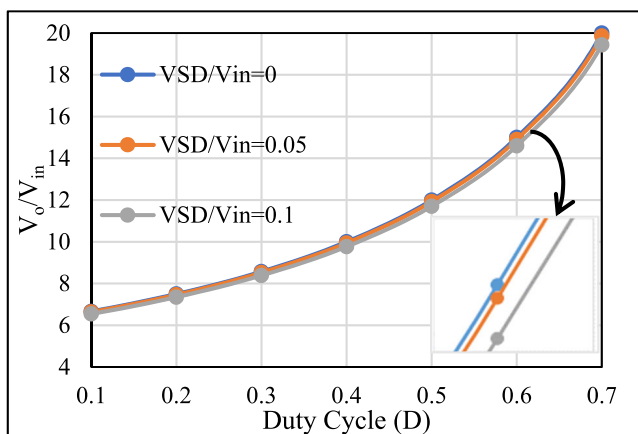
FIGURE 14. Effect of the voltage drop across switch resistance on voltage gain.
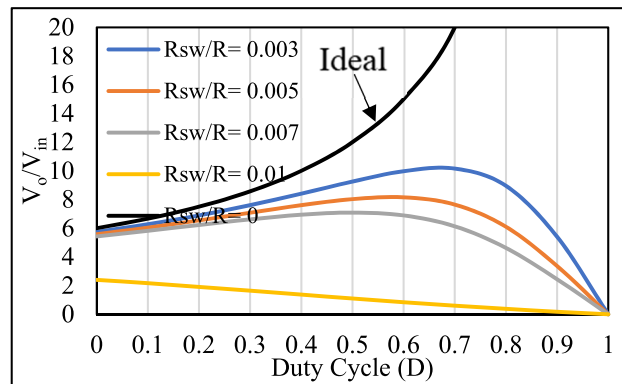
(a)

(b)

FIGURE 15. (a) Variation of voltage gain when the ON-state resistance of the switch is increased. (b) Variation of voltage gain when the capacitive resistance is increased.

MODE I: The inductor voltage relations are:

$$\begin{cases} V_{L1} = V_{in} - I_L R_D - V_{CN} \\ V_{L2} = V_{in} - I_L R_D - V_{CN} \end{cases} \quad (70)$$

MODE II: The inductor voltage relations are:

$$V_{L1} = V_{L2} = \frac{V_{in} - V_{C2} - V_{C3} - V_{CN} - \frac{I_o R_D}{(1-D)}}{2} \quad (71)$$

$$V_{C2} = -V_{in} + \frac{2I_L R_D}{D} + 2V_{CN} \quad (72)$$

$$V_{C3} = \frac{V_O}{3} \quad (73)$$

Since the average value of voltage across the inductor is null. Therefore, the expression can be derived as follows

$$D(V_{in} - I_L R_D - V_{CN}) + (1-D) \\ \times \left(\frac{V_{in} - V_{C2} - V_{C3} - V_{CN} - \frac{I_o R_D}{(1-D)}}{2}\right) \quad (74)$$

The effect on voltage gain is given by (75)

$$\frac{V_O}{V_{in}} = \frac{6\left(1 - \frac{V_{CN}}{V_{in}}\right)}{(1-D)\left[1 + \frac{(6+D-D^2)}{D(1-D)^2}\frac{R_D}{R}\right]} \quad (75)$$

4) EFFECT OF ESR OF CAPACITORS ON VOLTAGE GAIN

The ON and OFF state current through the capacitors is found using (3) and (7).

The effect of ESR of capacitors (C_1 to C_5) on voltage gain is analysed and other elements are assumed ideal.

The voltage across inductor L_1 and L_2 in both modes can be found as:

MODE I: The useful voltage relations are:

$$V_{L2} = V_{L2} = V_{in} \tag{76}$$

$$V_{C2} = -V_{in} + \frac{3I_O R_{C2}}{D} \tag{77}$$

$$V_{C4} + V_{C5} = V_O - \frac{I_O R_{C4}}{D} + \frac{I_O R_{C5}}{D} \tag{78}$$

$$V_{C1} + V_{C3} + V_{C5} = V_O - V_{in} + \frac{2I_o}{D}(R_{C1} + R_{C3} + R_{C5}) \tag{79}$$

MODE II: The useful voltage relations are:

$$V_{L1} = V_{L2} = \frac{V_{in} - V_{C2} - V_{C3} - \frac{3I_O R_{C2}}{(1-D)} - \frac{2I_O R_{C3}}{(1-D)}}{2} \tag{80}$$

$$V_{C4} - V_{C5} = V_{C3} + \frac{2I_o R_{C3}}{(1-D)} + \frac{I_O R_{C4}}{(1-D)} + \frac{I_O R_{C5}}{(1-D)} \tag{81}$$

$$V_{C3} - V_{C1} = V_{in} + \frac{2I_o(R_{C1} - R_{C3})}{(1-D)} \tag{82}$$

Since the average value of voltage across the inductor is zero. Therefore, the expression can be derived as follows

$$D(V_{in}) + (1-D)(\frac{V_{in} - V_{C2} - V_{C3} - \frac{3I_O R_{C2}}{(1-D)} - \frac{2I_O R_{C3}}{(1-D)}}{2}) \tag{83}$$

$$\frac{2V_{in}}{(1-D)} = V_{C2} + V_{C3} + \frac{3I_O R_{C2}}{(1-D)} + \frac{2I_O R_{C3}}{(1-D)} \tag{84}$$

Using (77) in (84)

$$\frac{2V_{in}}{(1-D)} = V_{C3} + \frac{3I_O R_{C2}}{D(1-D)} + \frac{2I_O R_{C3}}{(1-D)} \tag{85}$$

V_{C1}, V_{C3}, V_{C5} are obtained using (77),(78) and (79) and putting these relations in (80) the effect of ESR values of capacitors on voltage gain is obtained as (86), as shown at the bottom of the page.

For simplicity, it is assumed that

$$R_{C1} = R_{C2} = R_{C3} = R_{C4} = R_{C5} = R_C$$

$$\frac{V_O}{V_{in}} = \frac{6}{(1-D)} - \frac{(21-2D)I_O R_C}{D(1-D)V_{in}} \tag{87}$$

$$\frac{V_O}{V_{in}} = \frac{6}{(1-D)\left[1 + \frac{(21-2D)}{D(1-D)} \frac{R_C}{R}\right]} \tag{88}$$

Figure 15(b) shows the variation in gain when the capacitor resistance is increased. The gain decreases especially at higher duty ratios and low value of load resistance.

5) COMBINED EFFECT OF NON-IDEALITIES ON VOLTAGE GAIN

The combined effect of all parasitic elements on voltage gain can be found by considering all the non-idealities of components of the proposed converter.

The deviation from voltage gain can be obtained as follows

$$\frac{V_O}{V_{in}} = \frac{6}{(1-D)} - \frac{18I_O R_L}{V_{in}} - \frac{3(5+D)(1+D)I_O R_{SW}}{2V_{in}}$$
$$- \frac{6}{(1-D)}\frac{V_{CN}}{V_{in}} - \frac{(6+D-D^2)I_O R_D}{D(1-D)^2 V_{in}}$$
$$- \frac{(21-2D)I_O R_C}{D(1-D)V_{in}} \tag{89}$$

where $I_O = \frac{V_O}{R}$ is output load current.

The combined effect of non-idealities on the voltage gain can be derived as

$$\frac{V_O}{V_{in}} = \frac{6\left(1 - \frac{V_{CN}}{V_{in}}\right)}{(1-D)\left[1 + a\frac{R_L}{R} + b\frac{R_{SW}}{R} + c\frac{R_D}{R} + d\frac{R_C}{R}\right]} \tag{90}$$

where,

$$\begin{cases} a = \dfrac{18}{(1-D)^2}, & b = \dfrac{3(5+D)(1+D)}{(1-D)^2} \\ c = \dfrac{(6+D-D^2)}{D(1-D)^2}, & d = \dfrac{(21-2D)}{D(1-D)} \end{cases}$$

B. POWER LOSS ANALYSIS OF THE PROPOSED CONVERTER

1) LOSSES IN PROPOSED CONVERTER DUE TO SWITCH

The practical power switch has conduction and switching losses.

The conduction loss in the switch during the ON state by the parasitic resistance R_{SW}.

$$P_{Sw_{cond}} = I_{SW_{rms}}^2 \times R_{SW} \tag{91}$$

where $I_{SW_{rms}}$ is root mean square value of switch current and it is equal to

$$I_{SW_{rms}} = \frac{5+D}{\sqrt{D(1-D)}}I_o \tag{92}$$

$$P_{Sw_{cond}} = \frac{(5+D)^2}{D(1-D)^2}I_o^2 R_{SW} \tag{93}$$

$$P_{Sw_{cond}} = \frac{(5+D)^2}{D(1-D)^2}\frac{R_{SW}}{R}P_o \tag{94}$$

where P_O is the output power of the resistive load.

$$\frac{V_O}{V_{in}} = \frac{6}{(1-D)} - \frac{1}{D(1-D)}\left(\frac{4I_O R_{C1} + 9I_O R_{C2} + 4I_O R_{C3} + I_O R_{C4} + (3-2D)I_O R_{C5}}{V_{in}}\right) \tag{86}$$

The switching loss ($P_{Sw_{switching}}$) of the power switch can be calculated with the approximate relation shown in (95).

$$P_{Sw_{switching}} = \frac{(t_r + t_f)\left(I_{SWavg}V_{Sw}\right) * f_s}{2} \tag{95}$$

where, t_r = total rise time of the switch, t_f = total fall time, f_s = switching frequency.

$$V_s = \frac{V_o}{3}, \quad I_{SW_{avg}} = \frac{5+D}{1-D}I_o \tag{96}$$

$$P_{Sw_{switching}} = \frac{(t_r + t_f)(5+D)V_o^2 f_s}{3R(1-D)} \tag{97}$$

Total loss in the switch ($P_{SW_{loss_{total}}}$) is the sum of conduction and switching loss and can be expressed as

$$P_{SW_{loss_{total}}} = P_{Sw_{cond}} + P_{Sw_{switching}} \tag{98}$$

$$\begin{cases} P_{SW_{loss_{total}}} \\ = \left(\dfrac{(5+D)^2}{D(1-D)^2}\dfrac{R_{SW}}{R} + \dfrac{(t_r + t_f)(5+D)f_s}{3(1-D)}\right)P_o \\ P_{SW_{loss_{total}}} \\ = 3.2W \end{cases} \tag{99}$$

2) LOSSES IN PROPOSED CONVERTER DUE TO SEVEN DIODES (D$_1$-D$_7$)

As compared to conduction loss the switching loss in the diode is neglected and only conduction losses are taken into consideration. It is assumed that all diodes have equal resistance R_{DS} and equal cut in voltage V_{CN}.

The conduction loss due to parasitic resistance (P_{D_r}) is calculated using

$$P_{D_r} = I_{D_{rms}}^2 R_{DS} \tag{100}$$

The conduction loss ($P_{D_{CN}}$) due to cut in voltage in forward biased is calculated using

$$P_{D_{CN}} = V_{CN}I_{D_{dc}} \tag{101}$$

Total conduction loss in the diode ($P_{D_{loss}}$) is the sum of both losses

$$P_{D_{loss}} = P_{D_r} + P_{D_{CN}} = I_{D_{rms}}^2 R_{DS} + V_{CN}I_{D_{dc}} \tag{102}$$

Total conduction losses due to in the proposed converter is the sum of all losses in the diodes

$$P_{D_{loss_{total}}} = \sum_{i=1}^{7} P_{Di,loss} = \sum_{i=1}^{7} (I_{Di_{rms}}^2 R_{DS} + V_{CN}I_{Di_{dc}}) \tag{103}$$

The root mean square value of current through the diodes is expressed as below

$$I_{D1_{rms}} = I_{D4_{rms}} = I_{D6_{rms}} = \frac{I_o}{\sqrt{(1-D)}} \tag{104}$$

$$I_{D2_{rms}} = I_{D3_{rms}} = \frac{3I_o}{(1-D)\sqrt{D}} \tag{105}$$

$$I_{D5_{rms}} = I_{D7_{rms}} = \frac{I_o}{\sqrt{D}} \tag{106}$$

$$\begin{cases} P_{D1,loss} = \dfrac{I_O^2}{(1-D)}R_{DS} + V_{CN}I_o \\ = \left(\dfrac{1}{(1-D)}\dfrac{R_{DS}}{R} + \dfrac{V_{CN}}{V_O}\right)P_o \\ P_{D2,loss} = \dfrac{9I_O^2}{D(1-D)^2}R_{DS} + V_{CN}I_o \\ = \left(\dfrac{9}{D(1-D)^2}\dfrac{R_{DS}}{R} + \dfrac{V_{CN}}{V_O}\right)P_o \\ P_{D3,loss} = P_{D2,loss} \\ P_{D4,loss} = P_{D6,loss} = P_{D1,loss} \\ P_{D5,loss} = P_{D7,loss} \\ = \dfrac{I_O^2}{D}R_{DS} + V_{CN}I_o = \left(\dfrac{1}{D}\dfrac{R_{DS}}{R} + \dfrac{V_{CN}}{V_O}\right)P_o \end{cases} \tag{107}$$

$$\begin{cases} P_{D_{loss_{total}}} = \sum_{i=1}^{7} P_{Di,loss} \\ = \left(\dfrac{(20-D-D^2)}{D(1-D)^2}\dfrac{R_{DS}}{R} + \dfrac{7V_{CN}}{V_o}\right)P_o \\ P_{D_{loss_{total}}} = 9.48W \end{cases} \tag{108}$$

3) LOSSES IN PROPOSED CONVERTER DUE TO TWO INDUCTORS (L$_1$ AND L$_2$)

The total conduction losses in the two inductors are

$$P_{L_{loss_{total}}} = I_{L1_{rms}}^2 r_{L1} + I_{L2_{rms}}^2 r_{L2} \tag{109}$$

Using equation (22) to find the value of root mean square (rms) value of inductor currents.

$$P_{L_{loss_{total}}} = \frac{9I_O^2}{(1-D)^2}(r_{L1} + r_{L2}) \tag{110}$$

or it can be equivalently written as

$$P_{L_{loss_{total}}} = \frac{9}{(1-D)^2}\left(\frac{r_{L1}}{R} + \frac{r_{L2}}{R}\right)P_O \tag{111}$$

It is assumed that the ESR value of both the inductors are equal ($r_{L1} = r_{L2} = r_L$) then total loss in the inductor can be expressed as

$$\begin{cases} P_{L_{loss_{total}}} = \dfrac{18}{(1-D)^2}\left(\dfrac{r_L}{R}\right)P_O \\ P_{SW_{loss_{total}}} = 5.8W \end{cases} \tag{112}$$

4) LOSSES IN PROPOSED CONVERTER DUE TO SIX CAPACITORS (C$_O$-C$_5$)

The power loss in the capacitors due to series resistance is

$$P_{C_{loss}} = I_{C_{rms}}^2 \times R_C \tag{113}$$

The total losses in the proposed converter are the sum of losses due to all the capacitors i.e.

$$P_{C_{loss_{total}}} = \sum_{i=0}^{5} P_{Ci_{loss}} = \sum_{i=0}^{5} (I_{Ci_{rms}}^2 \times R_{Ci}) \tag{114}$$

The rms value of current through capacitors can be calculated using the formula

$$I_{C_{rms}} = \sqrt{\frac{1}{T_S}\left(\int_0^{DT_s} I_{C_{ON}}^2 dt + \int_{DT_s}^{T_s} I_{C_{OFF}}^2 dt\right)} \quad (115)$$

The values of rms currents through capacitors can be earned using (3), (7) and (115)

$$\begin{cases}
I_{C1_{rms}} = \dfrac{2I_O}{\sqrt{D(1-D)}}, & P_{C1_{loss}} = \dfrac{4I_O^2 R_{C1}}{D(1-D)} \\
& \qquad\quad = \dfrac{4}{D(1-D)}\dfrac{R_{C1}}{R}P_O \\[4pt]
I_{C2_{rms}} = \dfrac{3I_O}{\sqrt{D(1-D)}}, & P_{C2_{loss}} = \dfrac{9I_O^2 R_{C2}}{D(1-D)} \\
& \qquad\quad = \dfrac{9}{D(1-D)}\dfrac{R_{C2}}{R}P_O \\[4pt]
I_{C3_{rms}} = \dfrac{3I_O}{\sqrt{D(1-D)}}, & P_{C3_{loss}} = \dfrac{9I_O^2 R_{C3}}{D(1-D)} \\
& \qquad\quad = \dfrac{9}{D(1-D)}\dfrac{R_{C3}}{R}P_O \\[4pt]
I_{C4_{rms}} = \dfrac{I_O}{\sqrt{D(1-D)}}, & P_{C4_{loss}} = \dfrac{I_O^2 R_{C4}}{D(1-D)} \\
& \qquad\quad = \dfrac{1}{D(1-D)}\dfrac{R_{C4}}{R}P_O \\[4pt]
I_{C5_{rms}} = \dfrac{I_O}{\sqrt{D(1-D)}}, & P_{C5_{loss}} = \dfrac{I_O^2 R_{C5}}{D(1-D)} \\
& \qquad\quad = \dfrac{1}{D(1-D)}\dfrac{R_{C5}}{R}P_O \\[4pt]
I_{CO_{rms}} = \sqrt{\dfrac{1-D}{D}}I_O, & P_{C0_{loss}} = \dfrac{(1-D)I_O^2 R_{CO}}{D} \\
& \qquad\quad = \dfrac{1-D}{D}\dfrac{R_{CO}}{R}P_O
\end{cases} \quad (116)$$

Summation of all individual losses occurring in capacitor gives total losses occurring due to capacitors in the proposed converter

$$P_{C_{loss_{total}}} = P_{C1_{loss}} + P_{C2_{loss}} + P_{C3_{loss}} + P_{C4_{loss}} + P_{C5_{loss}} \quad (117)$$

If it is assumed that

$$R_{C1} = R_{C2} = R_{C3} = R_{C4} = R_{C5} = R_{CO} = R_C$$

Then

$$\begin{cases}
P_{C_{loss_{total}}} = \dfrac{(D^2 - 2D + 25)}{D(1-D)}\dfrac{R_C}{R}P_O \\
P_{C_{loss_{total}}} = 2.52W
\end{cases} \quad (118)$$

Hence total in the proposed converter is the sum of all the losses occurring in the proposed converter that is
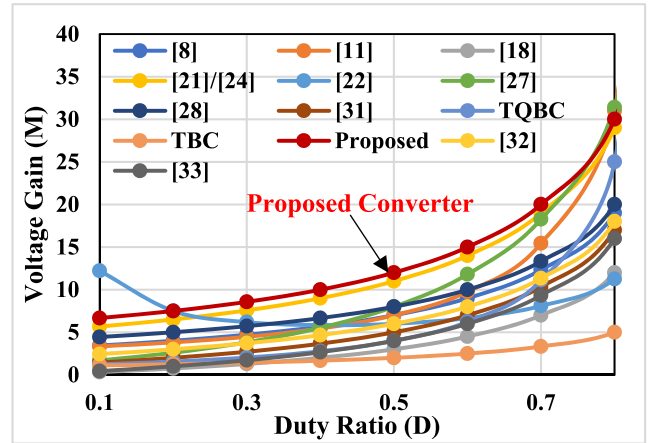
FIGURE 16. Voltage gain curve at different duty cycle for comparison.
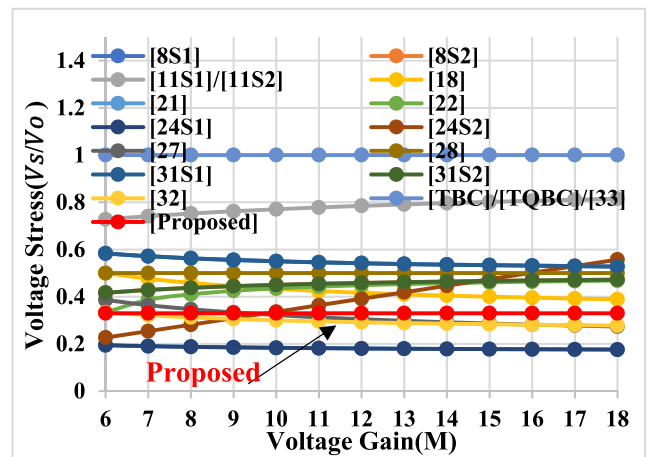

FIGURE 17. Switch voltage stress curve at different duty cycle for comparison.

expressed below.

$$P_{loss_{total}} = P_{SW_{loss_{total}}} + P_{D_{loss_{total}}} + P_{L_{loss_{total}}} + P_{C_{loss_{total}}} \quad (119)$$

$$P_{loss_{total}} = \left(\frac{f_S C_S R}{9} + a\frac{R_{SW}}{R} + b\frac{R_{DS}}{R} + c\frac{r_L}{R} \right.$$
$$\left. + d\frac{R_C}{R} + \frac{7V_{CN}}{V_o}\right)P_O \quad (120)$$

where

$$\begin{cases}
a = \dfrac{(5+D)^2}{D(1-D)^2}, & b = \dfrac{(20-D-D^2)}{D(1-D)^2} \\
c = \dfrac{18}{(1-D)^2}, & d = \dfrac{(D^2 - 2D + 25)}{D(1-D)}
\end{cases}$$

The efficiency (η) of the proposed converter can be expressed as below

$$\eta = \frac{P_O}{P_O + P_{loss_{total}}} \quad (121)$$

$$\eta = \cfrac{1}{1 + \frac{f_S C_S R}{9} + a\frac{R_{SW}}{R} + b\frac{R_{DS}}{R} + c\frac{r_L}{R} + d\frac{R_C}{R} + \frac{7V_{CN}}{V_O}}$$
(122)

VII. PERFORMANCE ANALYSIS WITH SIMILAR CONVERTERS

A detailed comparative analysis has been carried out and two traditional topologies and a few very recent high gain converter topologies have been considered. The analysis is based on the number of components, voltage gain and voltage stress across switches as given in Table 1. When compared to conventional boost and conventional quadratic boost converter the proposed topology can obtain a higher gain and the switch stress is considerably low. The converter in [8], adopts two switches and four inductors but its voltage gain is found to be lower than the proposed converter. The converter in [11] also has a lower voltage gain and higher switch stress than the proposed topology. The converter in [18] uses a total of four inductors which makes the converter bulky and the voltage gains are also low. Converters in [21], [22] and [28] have a relatively lower component count but the voltage gains are substantially less. The converter in [24], has a total of three switches (which could make the control of the converter complicated) but the voltage gains are less and switch stress is found to be higher. In [27] the topology has employed five inductors, two switches and a total of 18 components, and the increased count of components results in increased size of the converter and inefficiency and its voltage gain is quite low as compared to the proposed topology. Voltage gains of the converter proposed in [31] are also considerably less than the proposed converter. The converter in [32] has a total component count of 16 equal to the proposed converter including 3 inductors and 7 capacitors, but the voltage gains are considerably less than the proposed topology. Converter in [4] has adopted a total of 4 switches in its proposed circuit which can make the converter control very complex as compared to a single switch in the topology in this literature and even then, the voltage gains are lower.

For comparison, a plot of the voltage gain(M) versus the duty ratio(D) for the proposed topology and other similar converters is shown in Figure 16. It can be observed that the proposed topology gives the highest voltage gain even at low values of the duty ratio(D). A gain of almost ten times can be achieved at a duty of 0.4. High gain at a lower duty ratio reduces the current stress of the converter. The voltage gain of converters in [27], [11] is slightly higher than the proposed topology when it is operated at duty ratio values close to D = 0.8 but the switch stress is also high at these extreme values of the duty ratio. The plot of voltage stress vs the voltage gain is shown in Figure 17. It can be inferred from this plot that the proposed converter has one of the lowest voltage stresses across the switch.

Based on the comparison results the proposed converter topology is more advantageous as it can achieve high voltage gain, low voltage stress and is controlled by a single switch.

VIII. STATE SPACE MODEL OF THE PROPOSED CONVERTER

To derive the small signal state space model small resistances with capacitors C_1, C_2 and C_5 are considered. These resistances are used to simplify the analysis and to eliminate the invalid variables from the state space representation. Assuming the same value of inductors, the inductor current is represented by a single state variable. All the capacitors except the output capacitor have same value. The dynamic equations in ON and OFF state can be represented as shown in equation (123) and equation (124).

A. ON STATE

$$
\begin{bmatrix} \dot{i_L} \\ \dot{v_{C1}} \\ \dot{v_{C2}} \\ \dot{v_{C3}} \\ \dot{v_{C4}} \\ \dot{v_{C5}} \\ \dot{v_{Co}} \end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & \frac{1}{rC} & 0 & \frac{1}{rC} & -\frac{1}{rC} & 0 & 0 \\
0 & 0 & -\frac{1}{rC} & 0 & 0 & 0 & 0 \\
0 & \frac{1}{rC} & 0 & \frac{1}{rC} & -\frac{1}{rC} & 0 & 0 \\
0 & \frac{1}{rC} & 0 & \frac{1}{rC} & -\frac{2}{rC} & -\frac{1}{rC} & -\frac{1}{rC} \\
0 & 0 & 0 & 0 & \frac{1}{rC} & \frac{1}{rC} & -\frac{1}{rC} \\
0 & 0 & 0 & 0 & \frac{1}{rC_o} & \frac{1}{rC_o} & \frac{r+R}{C_o rR}
\end{bmatrix}
$$

$$
\times
\begin{bmatrix} i_L \\ v_{C1} \\ v_{C2} \\ v_{C3} \\ v_{C4} \\ v_{C5} \\ v_{Co} \end{bmatrix}
+
\begin{bmatrix} \frac{1}{L} \\ \frac{1}{rC} \\ \frac{1}{rC} \\ \frac{1}{rC} \\ \frac{1}{rC} \\ \frac{1}{rC} \\ 0 \\ 0 \end{bmatrix} v_{in}
$$

$$
v_o(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}
\begin{bmatrix} i_L \\ v_{C1} \\ v_{C2} \\ v_{C3} \\ v_{C4} \\ v_{C5} \\ v_{Co} \end{bmatrix}
$$
(123)

B. OFF STATE

$$
\begin{bmatrix} \dot{i}_L \\ \dot{v}_{C1} \\ \dot{v}_{C2} \\ \dot{v}_{C3} \\ \dot{v}_{C4} \\ \dot{v}_{C5} \\ \dot{v}_{Co} \end{bmatrix} = \begin{bmatrix} \frac{-r}{2L} & 0 & 0 & -\frac{1}{2L} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{rC} & 0 & 0 & 0 \\ \frac{1}{rC} & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{rC} & 0 & 0 & \frac{-2}{rC} & \frac{1}{rC} & \frac{1}{rC} & 0 \\ 0 & 0 & 0 & -\frac{1}{rC} & \frac{1}{rC} & \frac{1}{rC} & 0 \\ 0 & 0 & 0 & -\frac{1}{rC} & \frac{1}{rC} & \frac{1}{rC} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{RC_o} \end{bmatrix}
$$

$$
\times \begin{bmatrix} i_L \\ v_{C1} \\ v_{C2} \\ v_{C3} \\ v_{C4} \\ v_{C5} \\ v_{Co} \end{bmatrix} + \begin{bmatrix} \frac{1}{2L} \\ \frac{1}{rC} \\ \frac{1}{rC} \\ \frac{1}{rC} \\ \frac{1}{rC} \\ \frac{1}{rC} \\ 0 \\ 0 \end{bmatrix} v_{in}
$$

$$
v_o(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ v_{C1} \\ v_{C2} \\ v_{C3} \\ v_{C4} \\ v_{C5} \\ v_{Co} \end{bmatrix} \quad (124)
$$

The converter operates in ON mode with a time $d(t)$ and in OFF mode with a time $(1-d(t))$. The averaged model by combining (123) and (124) can be obtained and written as shown in (125), as shown at the bottom of the next page.

After perturbation when all the state variables are written in terms of dc signal and small signals as shown in (126), as shown at the bottom of page 17, the small signal model of the proposed converter neglecting the dc terms can be obtained as shown in (127), as shown at the bottom of page 17.

The open loop dynamic response of $\frac{\tilde{v}_o(s)}{\tilde{d}(s)}$ obtained through PLECS software, plotted in MATLAB for the same values as shown in Table 2. is depicted in Figure 18. From the bode plot of uncompensated system it can be observed that the phase margin at the gain crossover frequency is only 10º

(a)
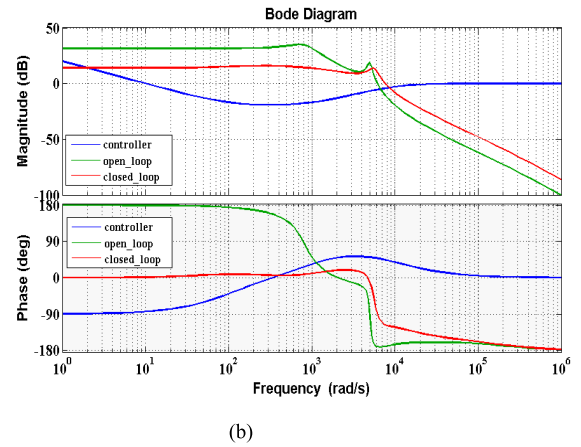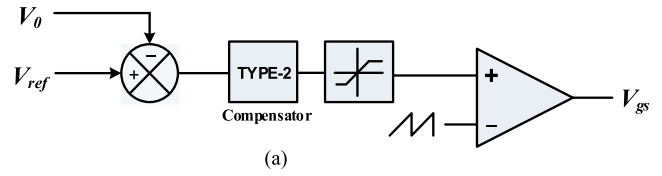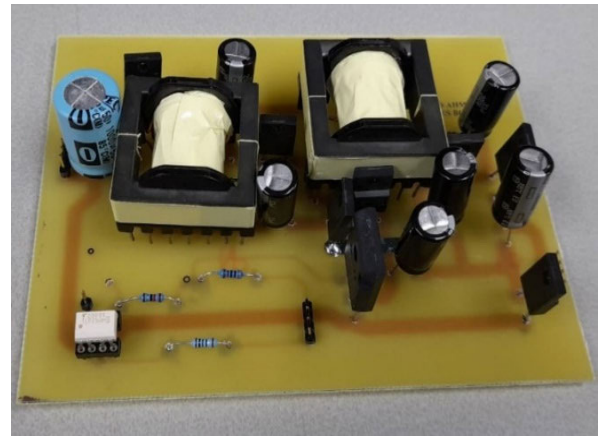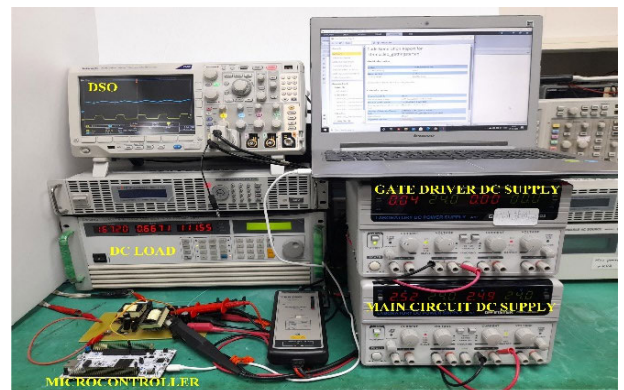

(b)

FIGURE 18. (a) Voltage control Loop. (b) Bode plots of open loop, closed loop and compensator.

(a)

(b)

FIGURE 19. (a) Hardware prototype of the proposed converter. (b) Experimental set-up.

which is not desirable. For closed loop stability of the system, the desirable phase margin should be between 45º to 65º to achieve good step response of the system.

1) VOLTAGE CONTROLLER DESIGN USING PLECS SOFTWARE

Using PLECS software the uncompensated bode plot can be observed and a proper controller can be designed. A PI controller usually works well for the lower order system. From the uncompensated bode plot it can be observed that the system is stable but it has zeroes in right half plane. To achieve proper phase margin a compensator is designed to remove the steady state error and remove the disturbances at high frequencies, for which the poles are added up at 0 rad/s and 10000 rad/s respectively. Zeroes are added at frequencies of 100rad/s and 1000 rad/s to achieve the desired phase margin. The compensator transfer function is given by (128)

$$G_c(s) = \frac{K(s + 1/\omega_{z1})(s + 1/\omega_{z2})}{s(s + 1/\omega_{P1})}$$

$$G_c(s) = \frac{10(s + 1/100)(s + 1/1000)}{s(s + 1/10000)} \tag{128}$$

From the Figure 18 of the compensated closed loop plot it can be observed that phase margin of closed loop system is 63º at the gain crossover frequency which shows that the closed loop system is stable.

IX. LABORATORY PERFORMANCE OF THE PROPOSED CONVERTER

The performance of the proposed converter is determined by building the hardware prototype as shown in Figure 19(a) in the laboratory. The converter is operated at a duty ratio of 40% and 30% in continuous conduction mode at a switching frequency of 50kHz. The design specifications of the presented

$$
\begin{bmatrix}
\dot{i_L} \\
\dot{v_{C1}} \\
\dot{v_{C2}} \\
\dot{v_{C3}} \\
\dot{v_{C4}} \\
\dot{v_{C5}} \\
\dot{v_{Co}}
\end{bmatrix}
=
\begin{bmatrix}
-\dfrac{(1-d)r}{2L} & 0 & 0 & -\dfrac{(1-d)}{2L} & 0 & 0 & 0 \\
0 & \dfrac{d}{rC} & 0 & \dfrac{1}{rC} & -\dfrac{d}{rC} & 0 & 0 \\
\dfrac{1-d}{C} & 0 & -\dfrac{d}{rC} & 0 & 0 & 0 & 0 \\
\dfrac{1-d}{C} & 0 & 0 & \dfrac{3d-2}{rC} & \dfrac{1-2d}{rC} & \dfrac{1-d}{rC} & 0 \\
0 & \dfrac{d}{rC} & 0 & \dfrac{2d-1}{rC} & \dfrac{1-3d}{rC} & \dfrac{1-2d}{rC} & \dfrac{d}{rC} \\
0 & 0 & 0 & -\dfrac{(1-d)}{rC} & \dfrac{1}{rC} & \dfrac{1}{rC} & -\dfrac{d}{rC} \\
0 & 0 & 0 & 0 & \dfrac{d}{rC} & \dfrac{d}{rC} & \dfrac{d(R+r)}{RC_o}
\end{bmatrix}
\times
\begin{bmatrix}
i_L \\
v_{C1} \\
v_{C2} \\
v_{C3} \\
v_{C4} \\
v_{C5} \\
v_{Co}
\end{bmatrix}
+
\begin{bmatrix}
\dfrac{1+D}{2L} \\
\dfrac{2D-1}{rC} \\
\dfrac{D}{rC} \\
\dfrac{1}{rC} \\
\dfrac{D}{rC} \\
0 \\
0
\end{bmatrix}
v_{in}
$$

$$
v_o(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}
\begin{bmatrix}
i_L \\
v_{C1} \\
v_{C2} \\
v_{C3} \\
v_{C4} \\
v_{C5} \\
v_{Co}
\end{bmatrix}
\tag{125}
$$

converter are listed in Table 2 and the experimental set-up is shown in Figure 19(b).

As depicted in Figure 20 measured input and output voltage are 12V and 117V respectively. The output voltage is reduced due to the effect of the parasitic resistance of the

diodes, switch, capacitors and inductors. In the same Figure, the ripple observed in the output capacitor (C_o) is two per cent (2%) of V_o that is about 2.24V. The drain to source voltage of the power MOSFET (S) is presented in Figure 20 with respective gate to source signals (V_{gs}). The maximum value

$$
\begin{cases}
i_L = I_L + \tilde{i}_L \\
v_{C1} = V_{C1} + v_{\tilde{C}1} \\
v_{C2} = V_{C2} + v_{\tilde{C}2} \\
v_{C3} = V_{C3} + v_{\tilde{C}3} \\
v_{C4} = V_{C4} + v_{\tilde{C}4} \\
v_{C5} = V_{C5} + v_{\tilde{C}5} \\
v_{Co} = V_{Co} + v_{\tilde{C}o}
\end{cases}
\tag{126}
$$

$$
\begin{bmatrix} \dot{\tilde{i}}_L \\ \dot{v_{\tilde{C}1}} \\ \dot{v_{\tilde{C}2}} \\ \dot{v_{\tilde{C}3}} \\ \dot{v_{\tilde{C}4}} \\ \dot{v_{\tilde{C}5}} \\ \dot{v_{\tilde{C}o}} \end{bmatrix} =
\begin{bmatrix}
-\dfrac{(1-D)r}{2L} & 0 & 0 & -\dfrac{(1-D)}{2L} & 0 & 0 & 0 \\
0 & \dfrac{D}{rC} & 0 & \dfrac{1}{rC} & -\dfrac{D}{rC} & 0 & 0 \\
\dfrac{1-D}{C} & 0 & -\dfrac{D}{rC} & 0 & 0 & 0 & 0 \\
\dfrac{1-D}{C} & 0 & 0 & \dfrac{3D-2}{rC} & \dfrac{1-2D}{rC} & \dfrac{1-D}{rC} & 0 \\
0 & \dfrac{D}{rC} & 0 & \dfrac{2D-1}{rC} & \dfrac{1-3D}{rC} & \dfrac{1-2D}{rC} & \dfrac{D}{rC} \\
0 & 0 & 0 & -\dfrac{(1-D)}{rC} & \dfrac{1}{rC} & \dfrac{1}{rC} & -\dfrac{D}{rC} \\
0 & 0 & 0 & 0 & \dfrac{D}{rC} & \dfrac{D}{rC} & \dfrac{D(R+2r)-r}{RrC_o}
\end{bmatrix}
$$

$$
\times \begin{bmatrix} \tilde{i}_L \\ v_{\tilde{C}1} \\ v_{\tilde{C}2} \\ v_{\tilde{C}3} \\ v_{\tilde{C}4} \\ v_{\tilde{C}5} \\ v_{\tilde{C}o} \end{bmatrix} +
\begin{bmatrix} \dfrac{1+D}{2L} \\ \dfrac{2D-1}{rC} \\ \dfrac{D}{rC} \\ \dfrac{1}{rC} \\ \dfrac{D}{rC} \\ 0 \\ 0 \end{bmatrix} v_{in} +
\begin{bmatrix}
\dfrac{r}{2L} & 0 & 0 & \dfrac{1}{2L} & 0 & 0 & 0 \\
0 & \dfrac{1}{rC} & 0 & 0 & -\dfrac{1}{rC} & 0 & 0 \\
\dfrac{-1}{C} & 0 & -\dfrac{1}{rC} & 0 & 0 & 0 & 0 \\
\dfrac{-1}{C} & 0 & 0 & \dfrac{3}{rC} & \dfrac{2}{rC} & \dfrac{-1}{rC} & 0 \\
0 & \dfrac{1}{rC} & 0 & \dfrac{2}{rC} & \dfrac{-3}{rC} & \dfrac{-2}{rC} & \dfrac{1}{rC} \\
0 & 0 & 0 & \dfrac{1}{rC} & 0 & 0 & -\dfrac{1}{rC} \\
0 & 0 & 0 & 0 & \dfrac{1}{rC} & \dfrac{1}{rC} & \dfrac{R+2r}{RrC_o}
\end{bmatrix}
\begin{bmatrix} I_L \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \\ V_{C5} \\ V_{Co} \end{bmatrix} .\tilde{d}(t) +
\begin{bmatrix} \dfrac{1}{2L} \\ \dfrac{2}{rC} \\ \dfrac{1}{rC} \\ 0 \\ \dfrac{1}{rC} \\ 0 \\ 0 \end{bmatrix} V_{in}\tilde{d}
$$

$$
\tilde{v}_o(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}
\begin{bmatrix} i_L \\ v_{C1} \\ v_{C2} \\ v_{C3} \\ v_{C4} \\ v_{C5} \\ v_{Co} \end{bmatrix}
\tag{127}
$$

TABLE 1. Comparison of proposed converter with other high gain converters.

Converters	Switch Count (S_C)	Inductor count (L_C)	Capacitor count (C_C)	Diode count (D_C)	$M\left(\frac{V_s}{V_{in}}\right)$	M at D=0.5	Voltage Stress $\left(\frac{V_s}{V_o}\right)$
TBC	1	1	1	1	$\frac{1}{(1-D)}$	2	1
TQBC	1	2	2	3	$\frac{1}{(1-D)^2}$	4	1
[8]	2	4	3	7	$\frac{3+D}{(1-D)}$	7	$S_1: \frac{2}{3+D}, S_2: \frac{1+D}{3+D}$
[11]	2	2	4	6	$\frac{3-3D+D^2}{(1-D)^2}$	7	$S_{1,2}: \frac{1}{3-3D+D^2}$
[18]	1	4	6	3	$\frac{3D}{(1-D)}$	3	$\frac{1}{3D}$
[21]	2	2	4	5	$\frac{5+D}{(1-D)}$	11	$\frac{1}{5+D}$
[22]	2	2	2	4	$\frac{1+D}{D(1-D)}$	6	$\frac{D}{1+D}$
[24]	3	4	2	5	$\frac{5+D}{(1-D)}$	11	$S_1: \frac{1}{5+D}; S_2: \frac{1}{(1-D)(5+D)}$
[27]	2	5	3	8	$\frac{1+5D+2D^2}{(1-D)}$	8	$\frac{1+D}{1+5D+2D^2}$
[28]	2	2	4	4	$\frac{4}{(1-D)}$	8	$\frac{1}{2}$
[31]	2	4	1	9	$\frac{1+3D}{(1-D)}$	5	$S_1: \frac{1+D}{1+3D}, S_2: \frac{2D}{1+3D}$
[32]	1	3	7	5	$\frac{2+2D}{(1-D)}$, n=2	6	$\frac{1}{2+2D}$
[33]	4	2	4	7	$\frac{4D}{(1-D)}$, m=3	4	1
Proposed	1	2	6	7	$\frac{6}{(1-D)}$	12	$\frac{1}{3}$

TABLE 2. Hardware specifications of the converter.

Elements	Specification
Maximum Power	200W
Input Voltage	12V/16V
Switching Frequency	50kHz
Duty Ratio	30% and 40%
Load Resistance	R=400-600 Ω
Inductors	$L_1=L_2=330\mu H$
Capacitors	$C_2=100\mu F/63V$, $C_1=C_3=C_4=$ $C_5=47\mu F/200V$ & $C_O=68\mu F/350V$
Power MOSFET	SPW52N50C3
Diodes	SF8L60USM
Gate Drivers IC	TLP250H
Microcontroller	STM32 Nucleo H743ZI2

FIGURE 20. Output voltage (V_0), source voltage (V_{in}) and V_{gs}.

is found to be 40V which is approximately 34% of the output voltage (V_o). When the power switch is triggered using the respective gate signal both the inductor L_1 and L_2 magnetize from 1.2A to 1.6A.

The inductor current peak to peak ripple is about 0.2A (15%) which is near to the value used to design the inductors and when the MOSFET is turned OFF the inductor demagnetize with the effect to reduce current linearly. The average value of both the indu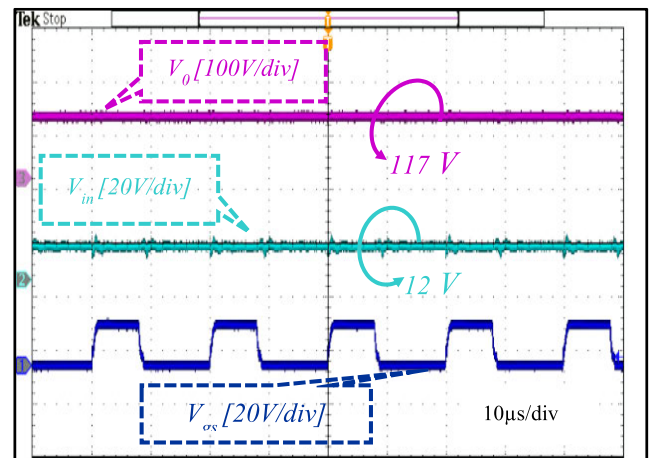ctor current is found to be 1.36A. The inductor currents are found to be continuous. Figure 22 and 23 shows the voltage across the capacitors C_1, C_2, C_3, C_4 and C_5 and is found to be 25.8V, 10.5V, 38.8V, 78.2 and 35.5V respectively with very low voltage ripple and is much less than the output voltage. The voltage across the output diode D_7 is shown and equal to 40V which is the same as the stress across the switch and less than the output voltage equal to 34%. All the results show that the converter is smoothly working in continuous conduction mode.
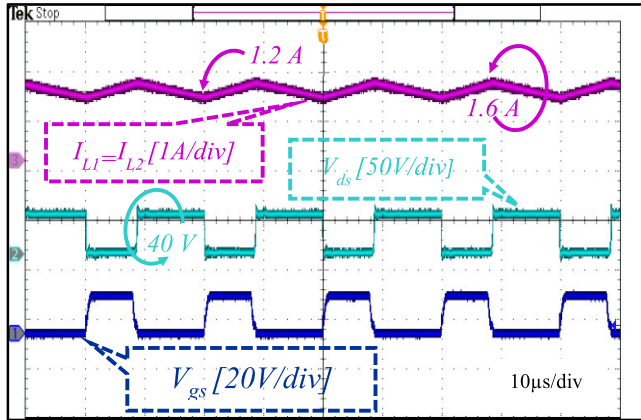
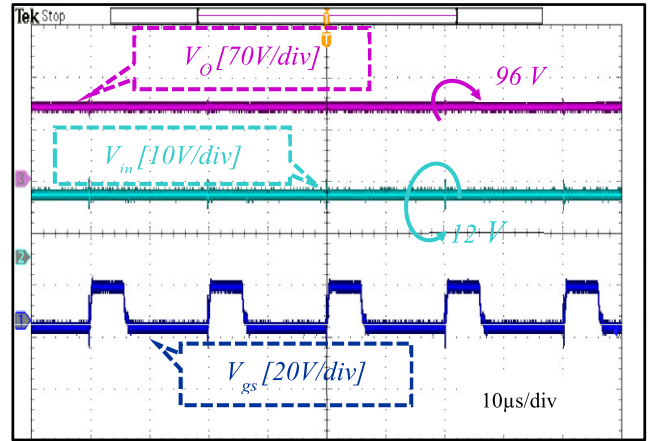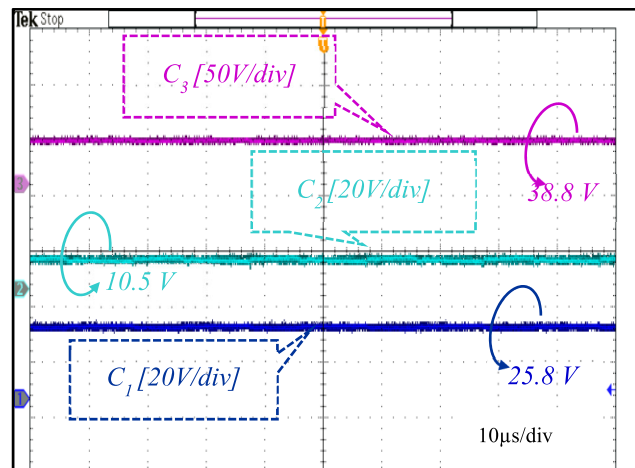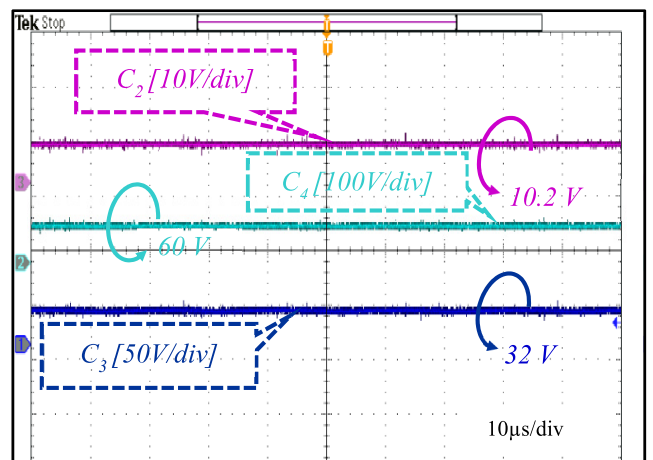**FIGURE 21.** Inductors current (I_{L1} and I_{L2}), at D = 0.4.

FIGURE 22. Voltage across capacitors C_1, C_2 and C_3 at D = 0.4.

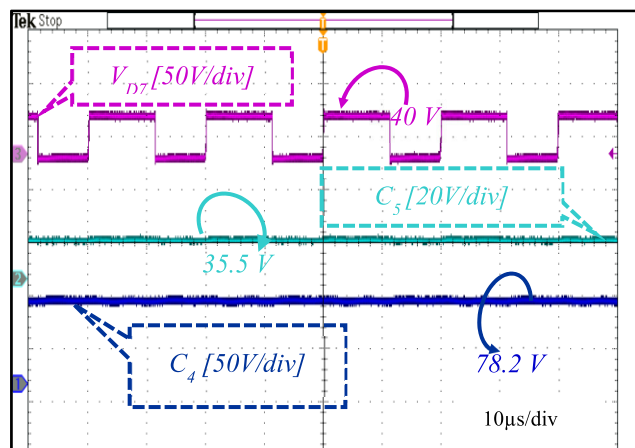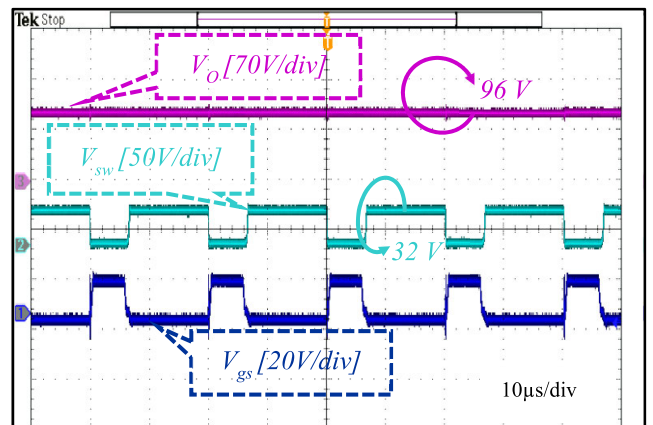**FIGURE 23.** Voltage across capacitors C_4, C_5 and output diode D_7 at D = 0.4.

FIGURE 24. Output voltage (V_O), input voltage (V_{in}) at D = 0.3.

FIGURE 25. Voltage across capacitors C_2, C_4 and C_3 at D = 0.3.

FIGURE 26. Output voltage and the voltage across switch at D = 0.3.

found to be 10.2 V, 32 V and 60 V respectively. The capacitor voltages are constant with ripple in the voltage close to 2 V.

As can be seen from Figure 26, the voltage stress across the switch (V_{sw}) is observed to be 32 V which is one-third of the V_o.

The converter performance is also tested in dynamic conditions when the duty cycle is changed from D = 0.3 to

Additional results to verify the working are obtained at D = 0.3 and V_{in} = 12V. As depicted in Figure 24 for an input of 12 V the output voltage is found to 96 V. The drop in the voltage is due to parasitic and ON state resistances. As shown in Figure 25, the voltage across capacitors C_2, C_3 and C_4 are
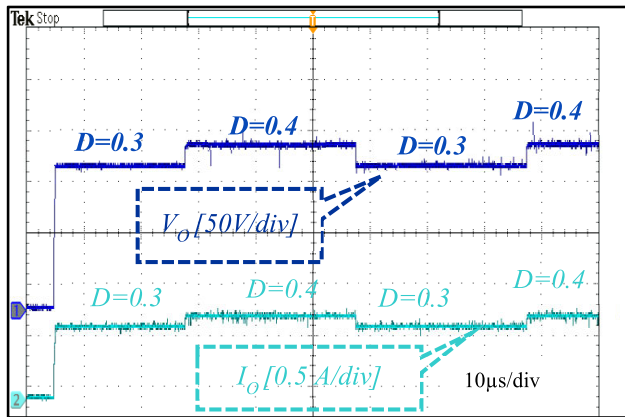
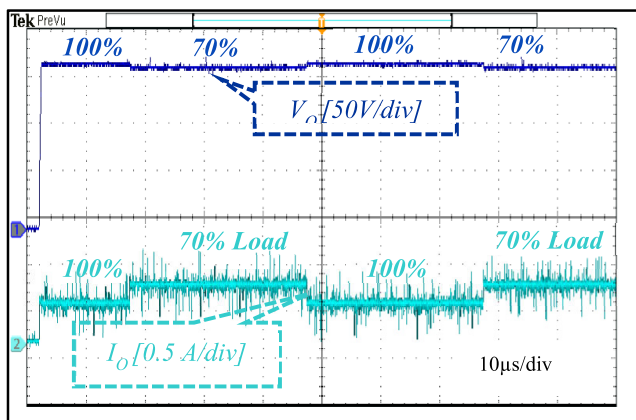**FIGURE 27.** Output voltage and the output current when D is changed from 0.3 to 0.4.

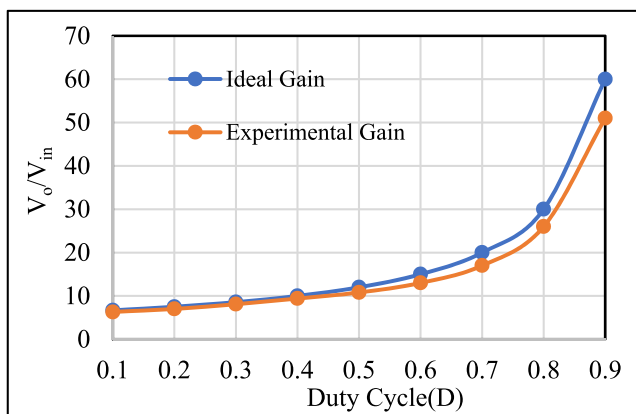**FIGURE 28.** Effect of the change in loading at V_{in} = 15 V and D = 0.45.

FIGURE 29. Ideal and experimental gain at different duty ratios.

FIGURE 30. Efficiency variation with output power.

FIGURE 31. Distribution of losses among components.

converter is good when load is changed. The output voltage is maintained between 160 V and 150V. Figure 29 shows the experimental voltage gain with the change in the duty cycle. For the same value of load resistance, the gain decreases at a higher duty cycle due to an increase in losses. The efficiency at different values of output power is shown in Figure 30. It can be seen from the plot that at constant output power as the voltage is increased from 12V to 24V the efficiency of the converter increases. This is because to achieve the same power output the current decreases with the increase in output voltage. As a result, the conduction losses decreases and efficiency increases. The power loss in different components in percentage is shown in Figure 31. The maximum loss occurs in diodes as shown in Figure 32. The selection of devices with a low value of parasitic resistances increases the overall efficiency of the converter.

A. CLOSED LOOP VALIDATION USING TYPHOON-HIL REAL TIME EMULATOR

The performance of in closed loop operation is tested using hardware in loop (HIL) operation using Typhoon-HIL-402 real time emulator. The Typhoon-real time emulator is designed to check the performance of controller in real time. The results with change in input voltage and change in load are shown in Figure 32 and Figure 33. From Figure 32 it can be observed that as the input voltage is changed from

D = 0.4 at V_{in} = 16 V. From Figure 27, it can be seen that the output voltage varies from 132 V at D = 0.3 to 150 V at D = 0.4. From the experimental results, it can be concluded that the converter performance is satisfactory in both steady-state and dynamic conditions. Figure 28 shows the response of the converter when load is decreased to 70% at D = 0.45 at Vin = 15V. Also, the load current is increased as depicted in the same Figure. This shows that the regulation of the

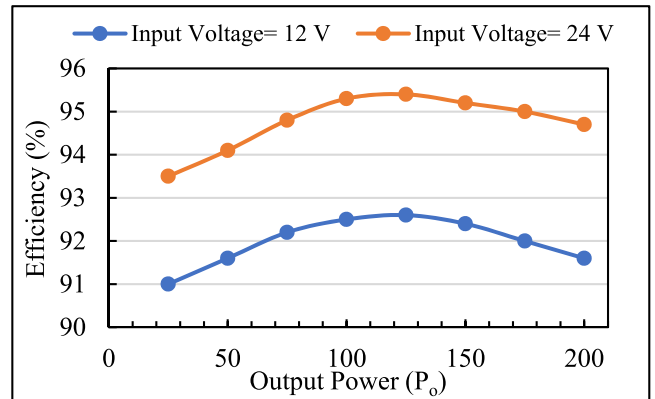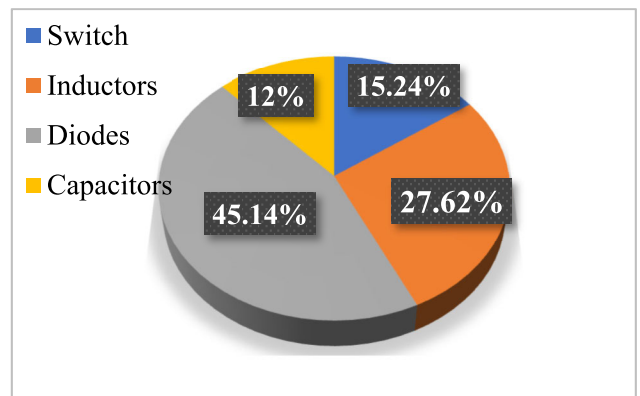**FIGURE 32.** Effect of change in V_{in} from 12V to 17V on V_o.

FIGURE 33. Effect of load change from 100Ω to 54.45Ω ohm at V_{in} = 15 V on V_o.

12 V to 17 V the output voltage is held constant at 120 V. Similarly, when load current is increased from 1.2 A to 2.2 A by decreasing the load resistance from 120 Ω to 55 Ω the output voltage is held constant by the voltage controller as shown in Figure 33. It can be concluded that the voltage controller is able to maintain the V_o at reference value.

X. CONCLUSION

In the proposed work, the converter (SC-SL-DC) has produced a voltage gain with a single switch and voltage multiplier cell made up of switched inductors. The voltage gain of the converter is found to be near 9.75 times at a duty ratio of 0.4 and 8 times at a duty of 0.3. which is high as compared with the quadratic boost converter and other high gain converters. The converter utilizes only two inductors which makes the converter light in weight. It is found that the high value of parasitic resistance of switch and inductors decreases the gain of the converter. Low voltage stress across capacitors leads to the selection of low voltage rating capacitors, which increases the efficiency and decreases the cost of the converter. The converter stress profile is also good as the stress across switch and diodes is one-third of the output voltage. The efficiency of the converter is found to improve if the input voltage is increased. The maximum efficiency is found to be 95.4%. The experimental results show that the converter is working in continuous current mode and the results match with the theoretical analysis. The proposed converter belongs to the non-isolated category and hence is suitable for medium power applications.

REFERENCES

[1] F. Blaabjerg and D. M. Ionel, "Renewable energy devices and systems—State-of-the-art technology, research and development, challenges and future trends," *Electr. Power Compon. Syst.*, vol. 43, no. 12, pp. 1319–1328, Jul. 2015.

[2] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, "Step-up DC–DC converters: A comprehensive review of voltage-boosting techniques, topologies, and applications," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9143–9178, Dec. 2017.

[3] M. F. Guepfrih, G. Waltrich, and T. B. Lazzarin, "High step-up DC-DC converter using built-in transformer voltage multiplier cell and dual boost concepts," *IEEE J. Emerg. Sel. Topics Power Electron.*, early access, Mar. 4, 2021, doi: 10.1109/JESTPE.2021.3063060.

[4] V. R. K. Kanamarlapudi, B. Wang, N. K. Kandasamy, and P. L. So, "A new ZVS full-bridge DC-DC converter for battery charging with reduced losses over full-load range," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 571–579, Feb. 2018.

[5] H.-L. Jou, J.-J. Huang, J.-C. Wu, and K.-D. Wu, "Novel isolated multilevel DC–DC power converter," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2690–2694, Apr. 2016.

[6] G. Catona, E. Bianconi, R. Maceratini, G. Coppola, L. Fumagalli, G. Petrone, and G. Spagnuolo, "An isolated semiresonant DC/DC converter for high power applications," *IEEE Trans. Ind. Appl.*, vol. 53, no. 3, pp. 2200–2209, May 2017.

[7] M. Forouzesh, K. Yari, A. Baghramian, and S. Hasanpour, "Single-switch high step-up converter based on coupled inductor and switched capacitor techniques with quasi-resonant operation," *IET Power Electron.*, vol. 10, no. 2, pp. 240–250, Feb. 2017.

[8] S. Khan, A. Mahmood, M. Tariq, M. Zaid, I. Khan, and S. Rahman, "Improved dual switch non-isolated high gain boost converter for DC microgrid application," in *Proc. IEEE Texas Power Energy Conf. (TPEC)*, Feb. 2021, pp. 1–6, doi: 10.1109/TPEC51183.2021.9384956.

[9] J. Ahmad, M. Zaid, A. Sarwar, C.-H. Lin, M. Asim, R. K. Yadav, M. Tariq, K. Satpathi, and B. Alamri, "A new high-gain DC-DC converter with continuous input current for DC microgrid applications," *Energies*, vol. 14, no. 9, p. 2629, May 2021, doi: 10.3390/en14092629.

[10] J. Ahmad, C.-H. Lin, M. Zaid, A. Sarwar, S. Ahmad, M. Sharaf, M. Zaindin, and M. Firdausi, "A new high voltage gain DC to DC converter with low voltage stress for energy storage system application," *Electronics*, vol. 9, no. 12, p. 2067, Dec. 2020, doi: 10.3390/electronics9122067.

[11] A. Kumar, Y. Wang, X. Pan, M. Raghuram, S. K. Singh, X. Xiong, and A. K. Tripathi, "Switched-LC based high gain converter with lower component count," *IEEE Trans. Ind. Appl.*, vol. 56, no. 3, pp. 2816–2827, May 2020, doi: 10.1109/TIA.2020.2980215.

[12] M. M. Haji-Esmaeili, E. Babaei, and M. Sabahi, "High step-up quasi-Z source DC-DC converter," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10563–10571, Dec. 2018.

[13] P. Kumar and M. Veerachary, "Z-network plus switched-capacitor boost DC–DC converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 791–803, Feb. 2021, doi: 10.1109/JESTPE.2019.2959078.

[14] A. Chub, D. Vinnikov, E. Liivik, and T. Jalakas, "Multiphase quasi-Z-source DC–DC converters for residential distributed generation systems," *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 8361–8371, Oct. 2018, doi: 10.1109/TIE.2018.2801860.

[15] M. Meraj, M. S. Bhaskar, A. Iqbal, N. Al-Emadi, and S. Rahman, "Interleaved multilevel boost converter with minimal voltage multiplier components for high-voltage step-up applications," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 12816–12833, Dec. 2020, doi: 10.1109/TPEL.2020.2992602.

[16] O. Abdel-Rahim, H. Funato, and J. Haruna, "A comprehensive study of three high-gain DC-DC topologies based on cockcroft-walton voltage multiplier for reduced power PV applications," *IEEJ Trans. Electr. Electron. Eng.*, vol. 13, no. 4, pp. 642–651, Apr. 2018.

[17] S. Hasanpour, M. Forouzesh, Y. Siwakoti, and F. Blaabjerg, "A new high gain, high-efficiency SEPIC-based DC-DC converter for renewable energy applications," *IEEE J. Emerg. Sel. Topics Ind. Electron.*, early access, Apr. 27, 2021, doi: 10.1109/JESTIE.2021.3074864.

[18] M. R. Banaei and S. G. Sani, "Analysis and implementation of a new SEPIC-based single-switch buck–boost DC–DC converter with continuous input current," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10317–10325, Dec. 2018, doi: 10.1109/TPEL.2018.2799876.

[19] M. R. A. Pahlavani and E. S. Asl, "DC–DC SIDO converter with low-voltage stress on switches: Analysis of operating modes and design considerations," *IET Power Electron.*, vol. 13, no. 2, pp. 233–247, Feb. 2020, doi: 10.1049/iet-pel.2018.6184.

[20] M. Farhadi-Kangarlu, A. M. Khiavi, and Y. Neyshabouri, "A non-isolated single-input dual-output boost DC–DC converter," *IET Power Electron.*, vol. 14, no. 5, pp. 936–945, Apr. 2021, doi: 10.1049/pel2.12076.

[21] S. Khan, M. Zaid, A. Mahmood, J. Ahmad, and A. Alam, "A single switch high gain DC-DC converter with reduced voltage stress," in *Proc. IEEE 7th Uttar Pradesh Sect. Int. Conf. Electr., Electron. Comput. Eng. (UPCON)*, Nov. 2020, pp. 1–6, doi: 10.1109/UPCON50219.2020.9376578.

[22] F. M. Shahir, E. Babaei, and M. Farsadi, "Analysis and design of voltage-lift technique-based non-isolated boost DC–DC converter," *IET Power Electron.*, vol. 11, no. 6, pp. 1083–1091, May 2018, doi: 10.1049/iet-pel.2017.0259.

[23] A. M. S. S. Andrade, T. Faistel, R. A. Guisso, and A. Toebe, "Hybrid high voltage gain transformerless DC-DC converter," *IEEE Trans. Ind. Electron.*, early access, Mar. 23, 2021, doi: 10.1109/TIE.2021.3066939.

[24] M. Zaid, S. Khan, M. D. Siddique, A. Sarwar, J. Ahmad, Z. Sarwer, and A. Iqbal, "A transformerless high gain DC–DC boost converter with reduced voltage stress," *Int. Trans. Electr. Energy Syst.*, vol. 31, no. 5, May 2021, Art. no. e12877, doi: 10.1002/2050-7038.12877.

[25] S. P. Syrigos, G. C. Christidis, T. P. Mouselinos, and E. C. Tatakis, "A non-isolated DC-DC converter with low voltage stress and high step-down voltage conversion ratio," *IET Power Electron.*, vol. 14, no. 6, pp. 1219–1235, May 2021, doi: 10.1049/pel2.12115.

[26] T. Shanthi, S. U. Prabha, and K. Sundaramoorthy, "Non-isolated *n*-stage high step-up DC-DC converter for low voltage DC source integration," *IEEE Trans. Energy Convers.*, vol. 36, no. 3, pp. 1625–1634, Sep. 2021, doi: 10.1109/TEC.2021.3050421.

[27] M. S. Bhaskar, N. Gupta, S. Selvam, D. J. Almakhles, P. Sanjeevikumar, J. S. M. Ali, and S. Umashankar, "A new hybrid zeta-boost converter with active quad switched inductor for high voltage gain," *IEEE Access*, vol. 9, pp. 20022–20034, 2021, doi: 10.1109/ACCESS.2021.3054393.

[28] S. Sadaf, N. Al-Emadi, P. K. Maroti, and A. Iqbal, "A new high gain active switched network-based boost converter for DC micro-grid application," *IEEE Access*, vol. 9, pp. 68253–68265, 2021, doi: 10.1109/ACCESS.2021.3077055.

[29] J. Zhao and D. Chen, "Switched-capacitor high voltage gain Z-source converter with common ground and reduced passive component," *IEEE Access*, vol. 9, pp. 21395–21407, 2021, doi: 10.1109/ACCESS.2021.3054880.

[30] D. Bao, A. Kumar, X. Pan, X. Xiong, A. R. Beig, and S. K. Singh, "Switched inductor double switch high gain DC-DC converter for renewable applications," *IEEE Access*, vol. 9, pp. 14259–14270, 2021, doi: 10.1109/ACCESS.2021.3051472.

[31] N. Gupta, M. S. Bhaskar, D. Almakhles, P. Sanjeevikumar, U. Subramaniam, Z. Leonowicz, and M. Mitolo, "Novel non-isolated quad-switched inductor double-switch converter for DC microgrid application," in *Proc. IEEE Int. Conf. Environ. Electr. Eng., IEEE Ind. Commercial Power Syst. Eur. (EEEIC/I CPS Eur.)*, Madrid, Spain, Jun. 2020, pp. 1–6, doi: 10.1109/EEEIC/ICPSEurope49358.2020.9160839.

[32] E. Babaei, T. Jalilzadeh, M. Sabahi, M. Maalandish, and R. S. Alishah, "High step-up DC-DC converter with reduced voltage stress on devices," *Int. Trans. Electr. Energy Syst.*, vol. 29, no. 4, p. e2789, Apr. 2019, doi: 10.1002/etep.2789.

[33] R. S. Alishah, M. Y. Hassani, S. H. Hosseini, K. Bertilsson, and M. Babalou, "Analysis and design of a new extendable SEPIC converter with high voltage gain and reduced components for photovoltaic applications," in *Proc. 10th Int. Power Electron., Drive Syst. Technol. Conf. (PEDSTC)*, Feb. 2019, pp. 492–497, doi: 10.1109/PEDSTC.2019.8697249.

[34] M. Babalou, M. Dezhbord, R. S. Alishah, and S. H. Hosseini, "A soft-switched ultra high gain DC-DC converter with reduced stress voltage on semiconductors," in *Proc. 10th Int. Power Electron., Drive Syst. Technol. Conf. (PEDSTC)*, Feb. 2019, pp. 677–682, doi: 10.1109/PEDSTC.2019.8697533.

SHAHRUKH KHAN (Student Member, IEEE) is currently pursuing the B.Tech. degree with the Department of Electrical Engineering, Zakir Husain College of Engineering and Technology (ZHCET), Aligarh Muslim University (AMU), Aligarh, India. He has published and presented research papers on power electronic DC/DC converters in various international/ overseas conferences and in reputed journals. His research interests include design and control of power electronic converters, interleaved converters, multi-level converters, and maximum power point techniques algorithms. He is the Joint Secretary of IEEE Student Branch, AMU, from 2020 to 2021. He has won the Best Paper Award in one of his conference proceedings. He served as a reviewer for various IEEE international conferences.

MOHAMMAD ZAID (Member, IEEE) received the bachelor's and master's degrees from Zakir Husain College of Engineering and Technology (ZHCET), Aligarh Muslim University (AMU), Aligarh, India. He is currently working as an Assistant Professor with the Department of Electrical Engineering, ZHCET, AMU. He is also a Branch Counselor with the IEEE Student Branch of the College. He has published research papers in the fields of DC/DC converters, multi-level inverters, and DG placement. His current research interest includes developing new topologies of high gain DC/DC converters for renewable energy applications.

ARSHAD MAHMOOD is currently pursuing the B.Tech. degree in electrical engineering with Zakir Husain College of Engineering and Technology, Aligarh Muslim University, Aligarh, India. He has submitted and presented several papers on power electronics DC/DC converters in various conference proceedings and journals. His research interests include high gain dc to dc converter, solar PV systems, and maximum power point techniques. In one of his proceeding, he has won the Best Paper Award.

ABBAS SYED NOORUDDIN (Student Member, IEEE) is currently pursuing the B.Tech. degree with the Department of Electrical Engineering, ZHCET, Aligarh Muslim University, Aligarh, India. He has held various voluntary positions. He is currently serving as a Secretary for the IEEE Student Branch, AMU. He has worked on various research projects on high gain DC-DC converters. His research interests include design and development of power converters, solar photovoltaic systems, blockchain applications in electric vehicles, and smart grids. He is a member of the Student Activity Committee (SAC), IEEE UP Section(R-10).

JAVED AHMAD received the B.Tech. degree in electrical engineering from Aligarh Muslim University, Aligarh, India, in 2017, and the M.E. degree in electrical power from Universiti Teknologi Malaysia, Johor Bahru, Malaysia, in 2019. He is currently pursuing the Ph.D. degree with the National Taiwan University of Science and Technology (Taiwan Tech), Taipei, Taiwan. His research interests include managing hybrid energy storage systems, DC to DC converters, interleaved converters, multi-level inverter, and power conversion for electric vehicle applications.
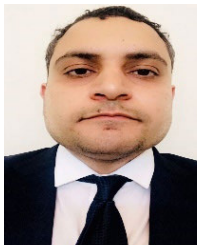
MAMDOUH L. ALGHAYTHI (Member, IEEE) received the B.S. degree in electrical engineering from Jouf University, Sakakah, Saudi Arabia, in 2012, the M.S. degree in electrical engineering from Southern Illinois University, Carbondale, IL, USA, in 2015, and the Ph.D. degree in electrical engineering from the University of Missouri, Columbia, MO, USA, in 2020. He is currently an Assistant Professor with the Electrical Engineering Department, Jouf University. His current research interests include power electronics, renewable energy systems, high step-up dc-dc converters, microgrids, and power converters. He is a member of the IEEE Power Electronics.

BASEM ALAMRI (Member, IEEE) received the B.Sc. degree (Hons.) in electrical engineering from King Fahd University of Petroleum and Minerals (KFUPM), in 2001, the first M.Sc. degree in sustainable electrical power from Brunel University London, London, U.K., in 2007, the second M.Sc. degree (Hons.) in electrical power systems from King Abdulaziz University, Jeddah, Saudi Arabia, in 2008, and the Ph.D. degree in electrical power engineering from Brunel University London, in 2017. He is currently an Assistant Professor of electrical engineering with the College of Engineering, Taif University. His research interests include power systems, power quality, power filter design, and smart grids, with a particular emphasis on the integration of renewable energy sources with power grids. He is a member of many international and local professional organizations. He is also a Certified Energy Auditor (CEA Ⓡ), a Certified Energy Manager (CEM Ⓡ), and a Certified Measurement and Verification Professional (CMVP Ⓡ) of the Association of Energy Engineers (AEE), USA. He has received many awards and prizes, including a certificate from Advance Electronics Company (AEC) in recognition of the Outstanding Academic Achievement during the B.Sc. degree with KFUPM. He also received the National Grid (NG) Prize and the Power Grid Operator, U.K., for being the top distinction student of the M.Sc. degree of the SEP Program with Brunel.

MOHD TARIQ (Senior Member, IEEE) received the bachelor's degree in electrical engineering from Aligarh Muslim University, Aligarh, the master's degree in machine drives and power electronics from the Indian Institute of Technology (IIT)-Kharagpur, and the Ph.D. degree in electrical engineering with a focus on power electronics and control from Nanyang Technological University (NTU), Singapore.

He has worked as a Researcher at the Rolls-Royce-NTU Corporate Laboratory, Singapore, where he has worked on the design and development of power converters for more electric aircraft. Before joining his Ph.D., he has worked as a Scientist with the National Institute of Ocean Technology, Chennai, under the Ministry of Earth Sciences, Government of India, where he has worked on the design and development of BLDC motors for the underwater remotely operated vehicle application. He also worked as an Assistant Professor at Maulana Azad National Institute of Technology (MANIT), Bhopal, India. He is currently working as an Assistant Professor with Aligarh Muslim University, where he is directing various international and national sponsored research projects and leading a team of multiple researchers in the domain of power converters, energy storage devices, and their optimal control for electrified transportation and renewable energy application. He has authored more than 150 research papers in international journals/conferences, including many articles in IEEE TRANSACTIONS/journals. He is the inventor of approximately 25 patents granted/published by the patent offices of USA, Australia, GB, EP, India, and China.

He was a recipient of the 2019 Premium Award for Best Paper in *IET Electrical Systems in Transportation* journal for his work on more electric aircraft and the Best Paper Award from the IEEE Industry Applications Society's (IAS) and the IEEE Industrial Electronic Society (IES), Malaysia Section-Annual Symposium (ISCAIE-2016) held in Penang, Malaysia, and many other best paper awards in different international conferences. He is a Young Scientist Scheme Awardee supported by the Department of Science and Technology, Government of India, in 2019, and a Young Engineer Awardee by the Institution of Engineers, India, in 2020. He is also the Founder Chair of the IEEE AMU Student Branch and the IEEE SIGHT AMU.

ADIL SARWAR (Senior Member, IEEE) received the B.Tech., M.Tech., and Ph.D. degrees from Aligarh Muslim University, in 2006, 2008, and 2012, respectively. He was associated with the Department of Electrical Engineering, Galgotia College of Engineering and Technology, Greater Noida, India, from 2012 to 2015. He has been working with the Department of Electrical Engineering, Aligarh Muslim University, Aligarh, India, since 2015. He is also working on world-bank sponsored research projects. He has contributed a chapter in Handbook of *Power Electronics* (Fourth Edition by M. H. Rashid). He has published more than 50 research papers in international journals and conferences. He is a Life Member of the Systems Society of India.

CHANG-HUA LIN (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electronic engineering from the National Taiwan University of Science and Technology, Taipei, Taiwan, in 1989, 1991, and 2000, respectively. He joined the Department of Electrical Engineering, National Taiwan University of Science and Technology, in 2016. He has engaged in research and teaching in the areas of power electronics and electronic circuit design. He has developed eight Taiwan patents and six U.S. patents. His major research interests include energy storage system design, battery management system design, and high voltage impulse circuit design. He is a member of the IEEE Power Electronics and Industrial Electronics Societies. He received the Young Researcher Award and the Best Paper Award from the National Science Council, in 2005.

• • •