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Resonance Suppression Method for Grid-Connected Converter With LCL Filter Under Discontinuous PWM

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ABSTRACT This paper presents a resonance suppression method that reduces current oscillation incurred by the *LCL*-filtered grid-connected converter's discontinuous PWM (DPWM). First, the cause of *LCL* resonance is analyzed with an aspect of frequency and time domain for DPWM scheme. Then, voltage references are manipulated to decrease the resonance problem. In the proposed method, pole voltage references at the edge of offset voltage are slightly adjusted to reduce the current oscillation. In addition, a perturb and observe (P&O) technique is adopted to search the magnitude of an edge voltage. Through the simulation and experimental tests, the current oscillation is dramatically reduced while keeping the advantages of DPWM scheme. The proposed method can minimize the switching frequency under the grid harmonics regulation.

INDEX TERMS Discontinuous PWM (DPWM), grid-connected converter, LCL resonance, active damping, search algorithm.

I. INTRODUCTION

Voltage source converters (VSCs) have largely penetrated electric power grids to interface renewable energy sources (RES), distributed generations (DG), and energy storage systems (ESS). A passive filter is installed for grid-connected converter systems to minimize high-frequency harmonics incurred by a pulse-width modulation (PWM) of the converter. Compared to the simple inductive (*L*) filter, the inductive-capacitive-inductive (*LCL*) filter has better harmonic attenuation performance, which not only minimizes the size, weight, and cost of the filter inductor but also improves the dynamics of the system [1], [2]. However, the resonance of *LCL* filter could cause unexpected current harmonics to the grid and even instability of the converter itself.

Various damping algorithms have been proposed to suppress *LCL* resonance. In general, existing literature can be classified into two groups: passive damping [3]–[5] and active damping methods [6]–[15]. Passive damping methods are quite simple and robust; however, they result in additional losses at a damping resistor. In addition, they reduce the filter attenuation ratio at PWM switching frequency. As an alternative, active damping methods have been proposed to simulate virtual damping resistors. They pass resonant frequency by adding an additional feedback loop to the current controller, which minimizes the losses on the filter. In [10]–[12], a digital delay due to sampling and computation was modeled to ensure the robustness of active damping methods. In [13]–[15], a resonance interaction between paralleled converters was analyzed to maintain system stability. These researches alleviate inherent resonant characteristics of *LCL* filters where the harmonic source exists. However, they were only focused on a current controller's stability analysis coupled with a damping algorithm, where the converter is assumed as an ideal voltage source. Thus, they did not consider a resonance problem provoked by PWM schemes of the converter and harmonic source itself.

In respect to the PWM scheme, it is essential to minimize power losses under the stringent regulation of grid standards. Current harmonics incurred by the PWM switching are subject to harmonic regulations such as IEEE 519 or BDEW [16], [17]. They describe maximum allowable harmonic currents at each harmonic number. In the worst case,

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the maximum harmonic current is 0.3 % of the rated current for harmonic numbers higher than 35 [16]. Therefore, *LCL* filter should be designed and damped to satisfy the harmonic regulation where harmonic spectra of PWM methods are carefully considered.

In [18], the impacts of PWM methods were analyzed based on power loss and power density for two-level three-phase converter with *LCL* filter. 60° discontinuous PWM (DPWM) has better performance compared with continuous PWM (CPWM) in most aspects, i.e., lower total power losses while keeping the harmonic standard. Not only semiconductor losses but also core loss of the filter inductor and cooling conditions are analyzed to optimize the weight of *LCL* filter. However, it did not consider a current oscillation provoked by abrupt changes of an offset voltage.

In [19] and [20], the resonance problem from DPWM was discussed through a frequency domain analysis. The low-order harmonics under a half of the switching frequency were triggered when the offset voltage is abruptly changed. These moments are generated every 60° in the conventional DPWM. As an alternative, a hybrid PWM method mixed with DPWM and CPWM was proposed to alleviate the cause of the resonance problem. In [21], an adaptive DPWM method was proposed to increase the ratio of CPWM to DPWM when the modulation index (MI) is low. It could be regarded as one of the hybrid PWM methods. However, the hybrid PWM methods in [19]–[21] increases switching losses compared to DPWM method because the region of CPWM is inserted to minimize the harmonics.

In this paper, the resonance problem incurred by DPWM is analyzed through *LCL* filter modeling in the frequency domain and harmonic spectra analysis according to the modulation schemes. Then, voltage references are modified to suppress the current oscillation while maintaining the merits of DPWM scheme. In the proposed method, the voltage references at the edges of offset voltage are moved closer to the optimal point by applying a perturb and observe (P&O) algorithm. Moreover, practical implementations and gain settings are analyzed to improve the performance of the proposed algorithms. The effectiveness of the proposed method is verified with the simulation and experimental results. Compared to the previous research work [22], the implementation and gain setting processes are clearly described. Besides, more simulation and experimental results are added to clarify the effectiveness of the proposed method.

II. ANALYSIS OF RESONANCE PROBLEM

A. LCL FILTER MODELING

Fig. 1 shows the circuit topology of a grid-connected converter with *LCL* filter. L_{fc}, $L_g \equiv L_{fg} + L_{grid}$, and C_f represent a converter-side inductance, a grid-side inductance, and a filter capacitance, respectively. The filter admittances from converter voltage, v_{conv}, to converter current, i_{conv}, and to grid current, i_{grid}, are defined by

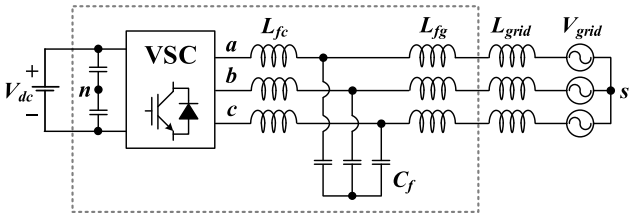

FIGURE 1. Configuration of *LCL*-filtered grid-connected converter.

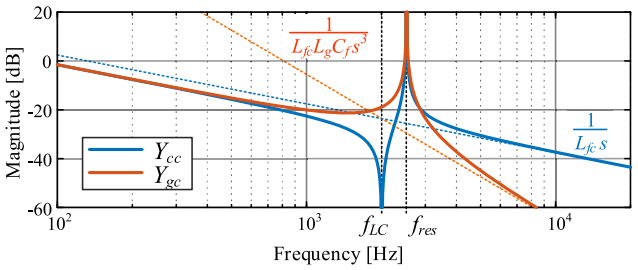

FIGURE 2. Frequency response of *LCL* filter admittances when $L_{grid} = 0$.

TABLE 1. System parameters.

Parameter	Value
Rated power, P_{rated}	5 kW
Rated current, I_{rated}	18.5 A_{peak}
Grid voltage, V_{grid}	220 $V_{l\text{-}l,rms}$, 60 Hz
Filter inductance on converter side, L_{fc}	1.2 mH
Filter capacitance, C_f	9 μF
Filter inductance on grid side, L_{fg}	0.7 mH
Resonant frequency, f_{res} ($L_{grid} = 0$)	2.52 kHz
Switching frequency, f_{sw}	7.20 kHz
Sampling frequency, f_{samp}	7.20 kHz

the following equations, respectively:

$$Y_{cc}(s) = \frac{i_{conv}(s)}{v_{conv}(s)} = \frac{L_gC_fs^2+1}{L_{fc}L_gC_fs^3+(L_{fc}+L_g)s} = \frac{1}{L_{fc}}\frac{s^2+\omega_{LC}^2}{s(s^2+\omega_{res}^2)}, \quad (1)$$

$$Y_{gc}(s) = \frac{i_{grid}(s)}{v_{conv}(s)} = \frac{1}{L_{fc}L_gC_fs^3+(L_{fc}+L_g)s} = \frac{1}{L_{fc}+L_g}\frac{\omega_{res}^2}{s(s^2+\omega_{res}^2)}, \quad (2)$$

where $\omega_{res} = 2\pi f_{res} = \sqrt{\frac{L_{fc}+L_g}{L_{fc}L_gC_f}}$, and $\omega_{LC} = 2\pi f_{LC} = \sqrt{\frac{1}{L_gC_f}}$. Here, f_{res} is the resonant frequency of *LCL* filter and f_{LC} is the *LC* resonant frequency of grid-side.

Fig. 2 depicts the frequency response of the filter admittances where *LCL* filter parameters are given in Table 1. Y_{gc} has 20 dB/dec of attenuation rate in a low frequency range, i.e., −20 dB/dec for $f < f_{res}$, and 60 dB/dec attenuation rate in a high frequency range, i.e., −60 dB/dec for $f > f_{res}$. The magnitude of Y_{gc}, $|Y_{gc}(s)|$, becomes very large at the resonant frequency, f_{res}. This result means that voltage harmonics around f_{res} can provoke large current oscillation and violate the harmonic regulation. Thus, f_{res} should be far

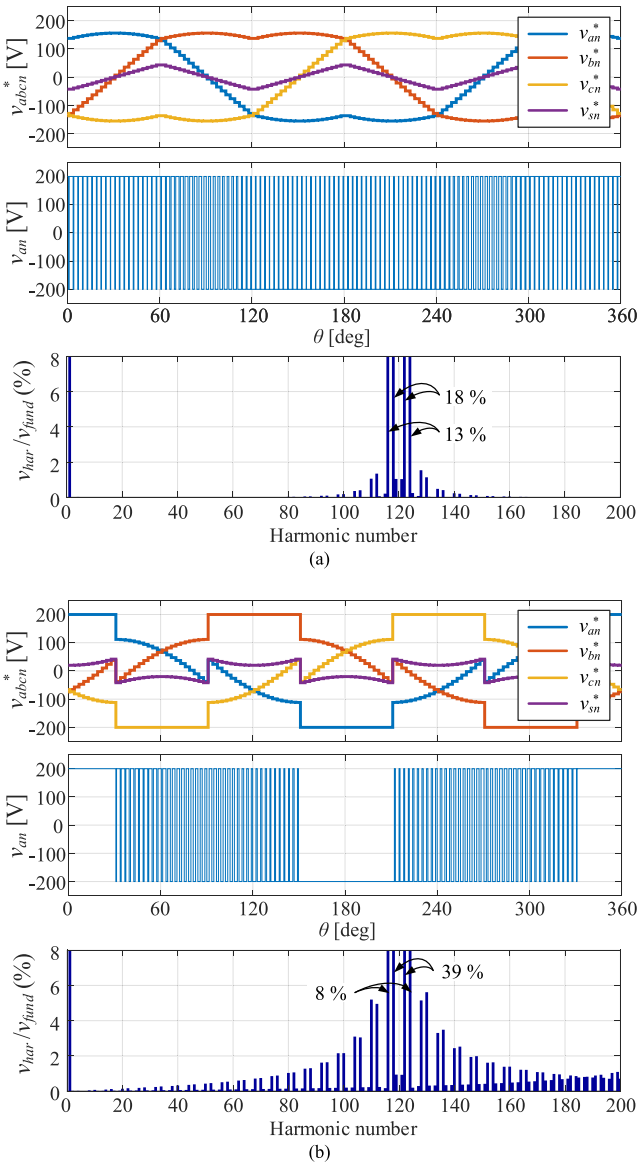

FIGURE 3. Pole voltage references, PWM waveforms, and harmonic spectra of v_{as} when MI = 0.9, f_{sw} = 7.2 kHz. (a) CPWM. (b) DPWM.

away from the switching frequency, f_{sw}, and its sideband frequencies.

B. HARMONIC SPECTRA ANALYSIS

Harmonic characteristics are changed based on the PWM schemes, which induce different voltage harmonics, v_{har}. Thus, harmonic spectra analysis for different PWM schemes is required to improve a system efficiency under given constraints, e.g., the harmonic regulation. The harmonic spectra of PWM can be derived by an analytical method such as the double Fourier integral method. It is widely applied to calculate the magnitude of each v_{har} as

$$C_{mn} = \frac{V_{dc}}{2\pi^2}\int_{-\pi}^{\pi}\int_{x_r}^{x_f} e^{j(mx+ny)}dxdy, \tag{3}$$

where m and n are carrier and baseband integer indices, respectively [23].

Fig. 3 shows the pole voltage references, PWM waveforms and harmonic spectra of a-phase phase voltage, defined as v_{as}, when MI and f_{sw} are set to 0.9 and 7.2 kHz, respectively. Here, MI is defined as the ratio between a fundamental component of the phase voltage, v_{s1}, and a half of dc-link voltage as follows:

$$\text{MI} = \frac{v_{s1}}{0.5V_{dc}}. \tag{4}$$

As shown in Fig. 3(a), the offset voltage of CPWM, v^*_{sn}(CPWM), which is equivalent to SVPWM [24], is defined as

$$v^*_{sn}(\text{CPWM}) = -0.5(v^*_{\max} + v^*_{\min}), \tag{5}$$

where v^*_{max}, v^*_{min} represent the maximum and minimum pole voltage reference, respectively.

The offset voltage of DPWM, v^*_{sn}(DPWM), is defined as follows as shown in Fig. 3(b).

$$v^*_{sn}(\text{DPWM}) = \begin{cases} +0.5V_{dc} - v^*_{\max} \equiv v^*_{sn,pos}, & (v^*_{\max} + v^*_{\min} \geq 0) \\ -0.5V_{dc} - v^*_{\min} \equiv v^*_{sn,neg}. & (v^*_{\max} + v^*_{\min} < 0). \end{cases} \tag{6}$$

Harmonic spectra of v_{an} in Fig. 3 show that DPWM has larger and widespread sideband harmonics near f_{sw} compared with CPWM. In this case, the sideband harmonics of f_{sw} and resonant frequency band near f_{res} can be overlapped, which would provoke severe harmonic oscillation [20].

An effective f_{sw} of DPWM is two-thirds of that of CPWM, and the switching loss of DPWM is almost half of that of CPWM owing to no switching at near maximum current. Thus, f_{sw} of DPWM can increase up to twice that of CPWM under the given limitation of the switching loss depending on a power factor angle [25], [26]. However, in spite of increasing f_{sw}, sideband harmonics around f_{sw} conspicuously increase when DPWM is applied. Therefore, v_{har} components near f_{res} should be avoided by changing PWM schemes or revising control algorithms.

When DPWM is applied, v^*_{sn} abruptly changes from $v^*_{sn,pos}$ to $v^*_{sn,neg}$ or vice versa, 6 times per an electrical period. Fig. 3(b) shows that a pulse width of v_{an} abruptly varies at rising and falling edge of v^*_{an} contrary to the case of SVPWM in Fig. 3(a), which induces more sideband harmonics around f_{res}. In the aspect of time domain, it could be comprehended that the harmonic oscillation occurs at each v^*_{sn} edge, triggering the oscillation not only in converter currents but also in grid currents. Consequently, the grid currents start to oscillate at an interval of 60° for DPWM and that cannot be easily suppressed with the conventional methods for the grid-connected converter with *LCL* filter.

III. PROPOSED RESONANCE SUPPRESSION METHOD

A. CONCEPT OF PROPOSED METHOD

To suppress the harmonic oscillation incurred by DPWM, v_{har} components near f_{res} should be avoided. v_{har} spectra are

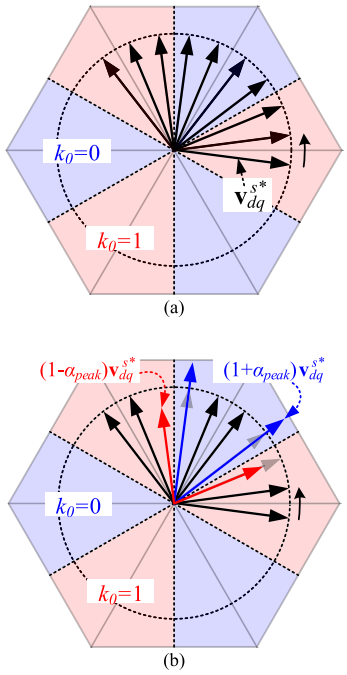

FIGURE 4. Traces of $\mathbf{v}_{dq}^{s*}$ at steady-state in space vector diagram. (a) Conventional method. (b) Proposed method.

determined by pole voltage references, $\mathbf{v}_{abcn}^*$, which means that $\mathbf{v}_{abcn}^*$ can be modified to change v_{har} near f_{res}. The pole voltage references, $\mathbf{v}_{abcn}^*$, is the sum of phase voltage references, $\mathbf{v}_{abcs}^*$, and offset voltage reference, v_{sn}^*. Here, $\mathbf{v}_{abcs}^*$ is set up by d-q voltage references, $\mathbf{v}_{dq}^*$, which is the output of the current controller. On the other hand, v_{sn}^* is determined by the PWM method. The PWM method can be changed to suppress sideband harmonics near f_{res} as mentioned previously [19]–[21]. However, the modification of v_{sn}^* is not desirable because a transition from DPWM to other PWMs would degrade the system's efficiency due to increased switching loss. Thus, the focus is on modifying $\mathbf{v}_{dq}^*$ to suppress the harmonic oscillation while the current controller operates without interruption.

Fig. 4(a) shows the traces of d-q voltage references in a stationary reference frame, $\mathbf{v}_{dq}^{s*}$, at a steady-state under the conventional current controller. The magnitude of $\mathbf{v}_{dq}^{s*}$ remains constant at the instant of v_{sn}^* edge because the bandwidth of the current controller is too low to catch up with the current harmonics near f_{res}. f_{res} is about one-third of f_{sw}, i.e., a few kHz, in the case of the LCL-filtered converter to satisfy the harmonic regulation. It is far from the current controller bandwidth, usually set to a few hundred Hz, e.g., 200 Hz. To damp the LCL resonance, a feedforward voltage, $\alpha_{peak}\cdot\mathbf{v}_{dq}^{s*}$, can be added or subtracted at the output of the current controller as shown in Fig. 4(b). Since the dominant voltage harmonics, i.e., v_{har} near f_{res}, are induced at v_{sn}^* edge, the feedforward voltage is applied at the edge of v_{sn}^* in the direction of damping the resonance. The feedforward voltage before the edge of v_{sn}^* is compensated after the edge of v_{sn}^* to maintain $\mathbf{v}_{dq}^{s*}$ on the average.

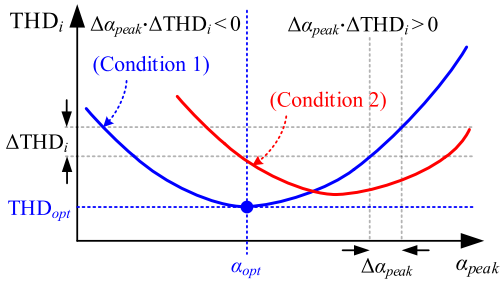

FIGURE 5. Relationship between α_{peak} and THD$_i$.

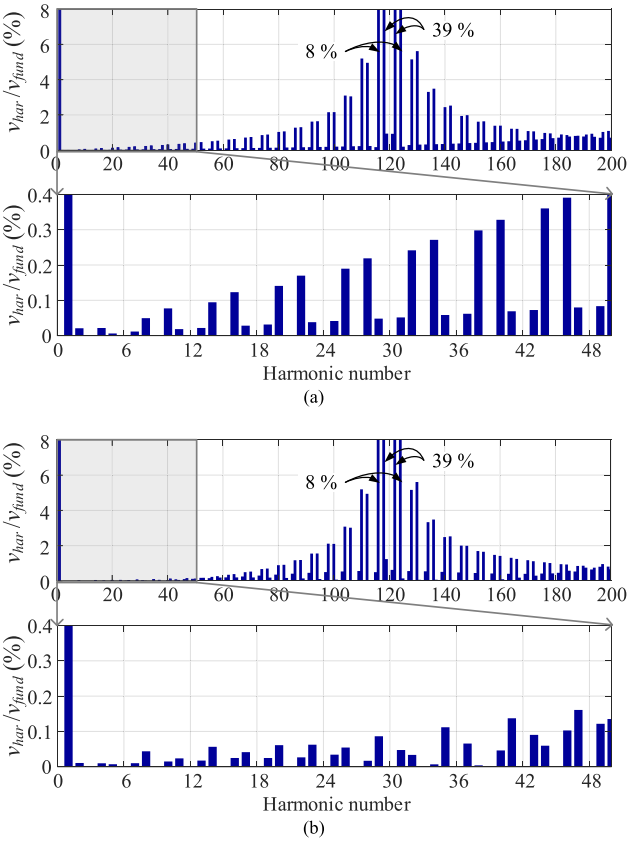

FIGURE 6. Harmonic spectra of v_{as} near f_{res} when MI = 0.9, f_{sw} = 7.2 kHz (a) α_{peak} = 0.00 (b) α_{peak} = −0.04.

Fig. 5 shows the conceptual relationship between the ratio of the feedforward voltage, α_{peak}, and the magnitude of harmonic currents represented by THD$_i$. Here, THD$_i$ is the total harmonic distortion of i_{grid}, and α_{opt} represents the optimal α_{peak} to minimize the harmonic distortion at v_{sn}^* edge. The correlation between THD$_i$ and α_{peak} varies depending on the operating conditions such as the filter admittance and the harmonic spectra of PWM. Thus, it is difficult to find an analytical solution for α_{opt} in real-time due to heavy computational burden.

The harmonic spectra of PWM are the function of MI and f_{sw}, which are influenced by disturbances such as a converter nonlinearity [27], [28], and a sensor accu-

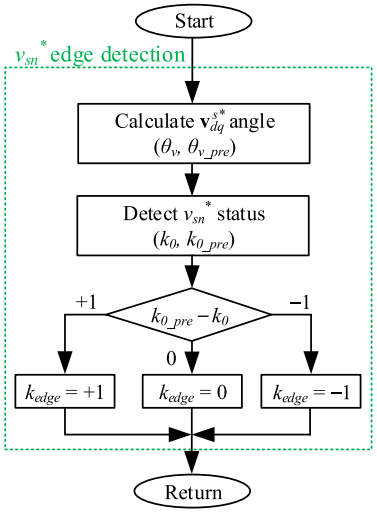

FIGURE 7. Flowchart of the proposed v_{sn}^* edge detection algorithm.

racy [29]. In addition, the filter characteristics are affected by the manufacturing tolerance and grid impedance variation. Thus, a searching algorithm would be a practical solution to find α_{opt} in real-time. As a result, the proposed method combines the searching algorithm instead of the premade LUT.

Fig. 6 shows the harmonic spectra of v_{as} when MI and f_{sw} are set to 0.9 and 7.2 kHz, respectively. The low-order harmonics up to 50-th are zoomed in to distinguish v_{har} components near f_{res}. There are v_{har} components near f_{res} owing to the widespread sideband harmonics of DPWM as shown in Fig. 6(a). It can be suppressed by changing α_{peak} while maintaining DPWM. Fig. 6(b) reveals that low-order harmonics are minimized by setting α_{peak} to -0.04, close to α_{opt}. In this case, low-order harmonics owing to DPWM are reduced by almost one-third by adding the feedforward voltage at the edge of v_{sn}^*.

Active damping algorithms, e.g., filter capacitor current- or voltage- feedback-based algorithms [6]–[8], are insufficient to suppress the resonance incurred by DPWM because the damping performance is limited by a sampling noise and digital delay. These algorithms reduce the current harmonics after v_{sn}^* edge have passed by adding the virtual damping resistors. It cannot eliminate a root cause of the *LCL* resonance, i.e., v_{har} near f_{res}, which triggers the harmonic oscillation at each v_{sn}^* edge. However, it can suppress the harmonics provoked by other causes such as grid harmonics and other converters. Thus, the active damping algorithms can be utilized in conjunction with the proposed method to enhance the system stability under a weak grid condition.

B. IMPLEMENTATION OF PROPOSED METHOD

To realize the proposed method, the edge of offset voltage, v_{sn}^* edge, should be detected in advance and the feedforward voltage, $\alpha_{peak} \cdot \mathbf{v}_{dq}^{s*}$, added at each edge of the offset voltage.

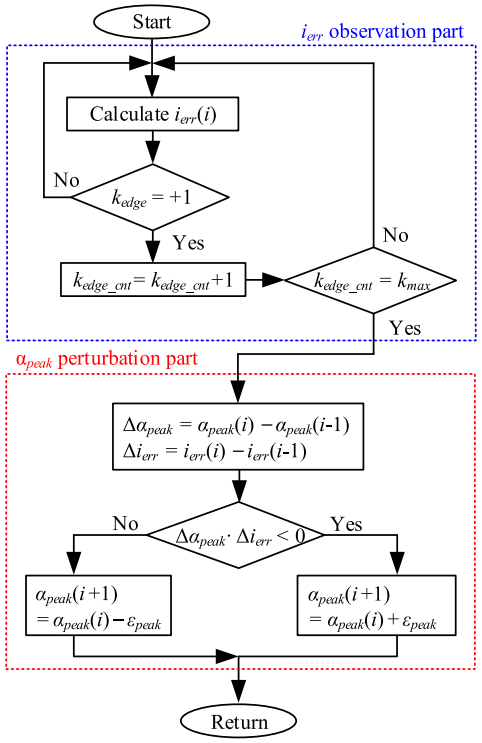

FIGURE 8. Flowchart of the proposed α_{peak} P&O algorithm.

Moreover, the optimal α_{peak}, defined as α_{opt}, is searched in real-time to minimize the resonance incurred by DPWM. Thus, v_{sn}^* edge detection and α_{opt} searching algorithms should be processed at each calculation point.

Fig. 7 shows the flowchart of the proposed v_{sn}^* edge detection algorithm. First, the voltage reference angles at present and the next operating point, θ_v and θ_{v_pre}, are calculated by an arctangent function as shown below, respectively.

$$\theta_v = \text{atan2}(v_{qs}^{s*}, v_{ds}^{s*}), \tag{7}$$

$$\theta_{v\_pre} = \theta_v + \omega_{grid} T_{samp}, \tag{8}$$

where $\text{atan2}(v_{qs}^{s*}, v_{qs}^{s*})$ returns the four-quadrant arctangent of $\mathbf{v}_{dq}^{s*}$ in the range of $[-\pi, \pi]$.

Here, θ_{v_pre} is predicted under the assumption of steady-state condition. On the basis of θ_v and θ_{v_pre}, each status of $v_{sn}^*[n]$ and $v_{sn}^*[n+1]$, equivalent to k_0 and k_{0_pre}, is decided. When $k_0 = 0$; $v_{sn}^* = v_{sn,pos}^*$, and when $k_0 = 1$; $v_{sn}^* = v_{sn,neg}^*$ as defined in (6). Then, positive and negative edges of v_{sn}^* are distinguished by the difference of k_{0_pre} and k_0, k_{edge}, as follows:

$$k_{edge} = k_{0\_pre} - k_0. \tag{9}$$

Consequently, k_{edge} is utilized to detect the edge of v_{sn}^*. $k_{edge} = +1$ means a positive v_{sn}^* edge, whereas $k_{edge} = -1$ means a negative v_{sn}^* edge.

α_{opt} searching algorithm is based on the P&O algorithm, also referred to as a hill-climbing method [30], [31]. It is

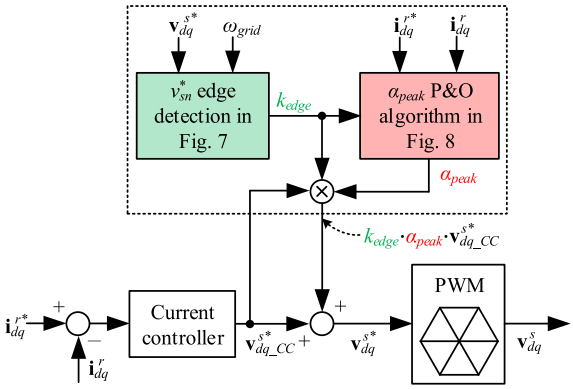

FIGURE 9. Flowchart of the proposed α_{peak} P&O algorithm.

widely utilized for a maximum power point tracking (MPPT) algorithm in photovoltaic applications due to ease of implementation. The basic principle is to perturb α_{peak} and observe a current error, i_{err}, where i_{err} is measured twice and compared to track down α_{opt}.

Fig. 8 shows the flowchart of the proposed α_{peak} P&O algorithm. First, i_{err} was extracted until the number of v_{sn}^{*} edge is sufficient to minimize the effects of other disturbances in i_{err} observation part. i_{err} is simply extracted from the current error terms in the current controller at the steady-state condition, i.e., the error between current references and sensed currents. Otherwise, a current observer could predict the converter current without the effects of PWM harmonics [8]. i_{err} is calculated from the sum of the squared current error, where the current error is the difference between actual and predicted currents. i_{err} is accumulated until the number of k_{edge}, defined as k_{edge_cnt}, is equal to k_{max}. The duration of $i_{err}(i)$ calculation is $120^{\circ}\cdot k_{\max}$.

The direction of α_{peak} is then determined by comparing a measured i_{err} in α_{peak} perturbation part. The principle of α_{peak} perturbation part is as follows: If measured i_{err}, $i_{err}(i)$, is less than i_{err} measured at one sample before, $i_{err}(i-1)$, α_{peak} keeps the present moving direction, i.e., the direction of $\Delta\alpha_{peak} \equiv \alpha_{peak}(i)$ - $\alpha_{peak}(i-1)$. Otherwise, α_{peak} is changed to the opposite direction of $\Delta\alpha_{peak}$. It can be shortly implemented by comparing $\Delta\alpha_{peak}$ with Δi_{err} as follows:

$$\alpha_{peak}(i+1) = \begin{cases} \alpha_{peak}(i) - \varepsilon_{peak}, & (\Delta\alpha_{peak}\cdot\Delta i_{err} \geq 0) \\ \alpha_{peak}(i) + \varepsilon_{peak}. & (\Delta\alpha_{peak}\cdot\Delta i_{err} < 0), \end{cases} \tag{10}$$

where ε_{peak} is a perturbation step size of α_{peak}.

As a result, α_{peak} is updated and directly applied at the next v_{sn}^{*} edge.

Fig. 9 shows the overall control block diagram of the proposed method. First, k_{edge} is extracted by the v_{sn}^{*} edge detection algorithm. Then, α_{peak} is calculated based on the P&O algorithm. k_{edge} and α_{peak} are utilized to modify the output voltages of the current controller, $\mathbf{v}_{dq\_CC}^{s*}$. Finally, d-q voltage references, $\mathbf{v}_{dq}^{s*}$, are revised as follows after the proposed algorithms are applied.

$$\mathbf{v}_{dq}^{s*} = (1 + k_{edge}\alpha_{peak})\mathbf{v}_{dq\_CC}^{s*}. \tag{11}$$

$\mathbf{v}_{dq}^{s*}$ is limited within a voltage hexagon at a stationary reference frame, which is a physical limit of PWM. If $\mathbf{v}_{dq}^{s*}$ is out of the hexagon boundary, then the voltage should be adjusted at the boundary of the hexagon. This means that the range of α_{peak} is naturally set within the dc-link voltage.

C. GAIN SETTING IN PROPOSED METHOD

The tuning factors of the proposed method are k_{max} and ε_{peak}. Disturbances such as converter nonlinearity and grid harmonics influence the current error, i_{err}. They provoke undesirable fluctuations of α_{peak}. Thus, k_{max} can be increased to make the P&O algorithm more robust to the disturbances. However, the dynamic response gets sluggish as k_{max} becomes larger. To minimize the effects of a current unbalance in the three-phase system, k_{max} is set in multiples of three, i.e., $k_{max} = 3n$. In this case, α_{peak} is updated at an interval of $360^{\circ}\cdot n$.

Likewise, small ε_{peak} minimizes the oscillation of α_{peak}, enhancing the steady-state performance owing to its small perturbation. However, small ε_{peak} slows down the transient response under abrupt changes of the operating condition such as current reference and grid voltage variations. Thus, k_{max} and ε_{peak} should be adjusted considering both dynamic responses in the transients and oscillatory responses in the steady states. Otherwise, a dynamic step size can be applied to improve the performances of the proposed method further.

The proposed method can be applied for whole MI ranges where the range of α_{peak} is limited owing to its voltage margin as aforementioned. However, this is not a concern because the oscillation caused by DPWM decreases as MI increases. In other words, the effects of v_{sn}^{*} jumps are reduced under high MI operation, which lessens the *LCL* resonance. In any case, α_{peak} is converged to α_{opt} by the proposed P&O algorithm within the physical voltage limit.

IV. SIMULATION RESULTS

In the simulation, the performances can be evaluated under ideal conditions without the effects of noise and disturbance. The grid-connected converter with *LCL* filter in Fig. 1 was simulated in MATLAB/Simulink with PLECS. System parameters were set as Table. I, and a grid inductance, defined as L_{grid}, was 0.05 pu (=0.8 mH). In this case, f_{res} was located at 2.03 kHz, near 34$^{\text{th}}$ harmonics. The gains of the proposed method, k_{max} and ε_{peak}, were set to 3 and 0.0005, respectively.

Fig. 10 shows the waveforms and harmonic spectra of a-phase grid current, $i_{grid,a}$, at the rated current and unity power factor conditions, i.e., $P^{*} = 5$ kW and $Q^{*} = 0$ kW,

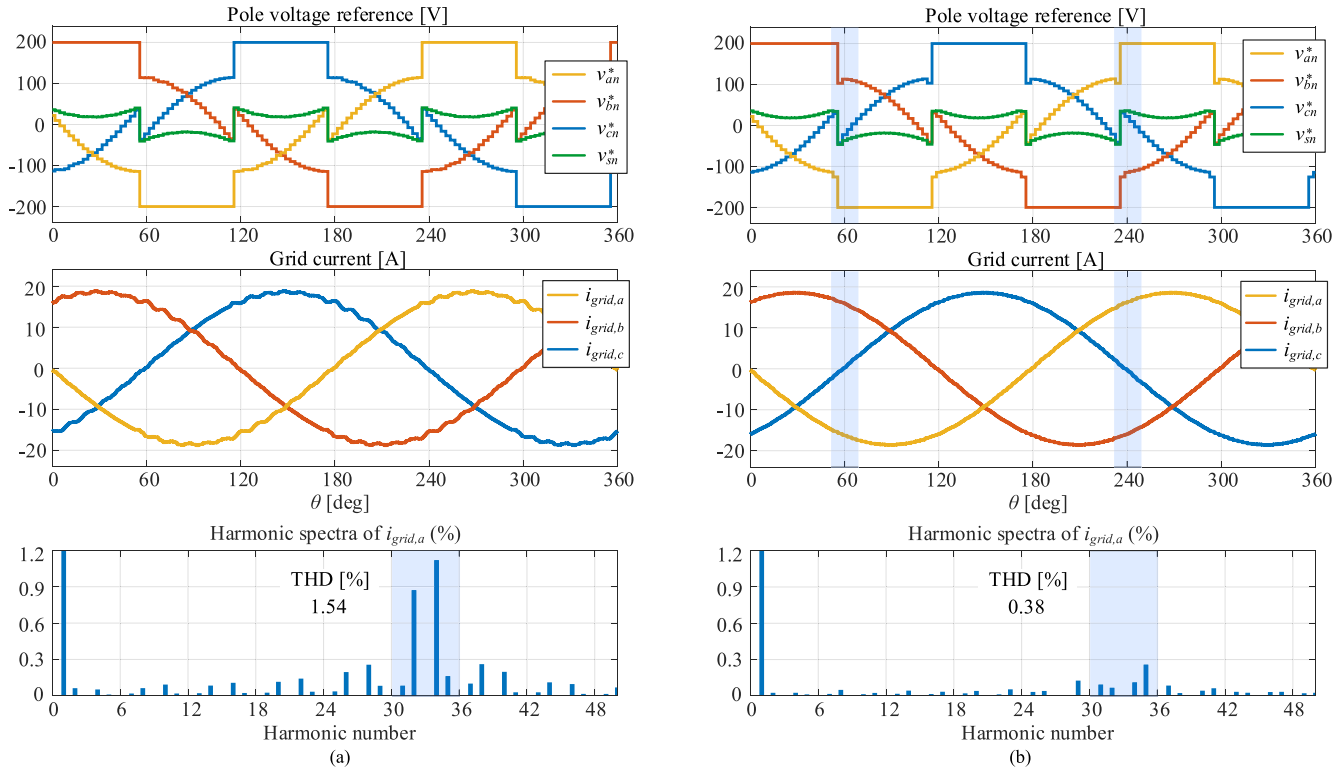

FIGURE 10. Simulation 1: Waveforms and harmonic spectra of $i_{grid,a}$ when V_{dc} = 400 V under DPWM (a) without the proposed method. (b) with the proposed method.

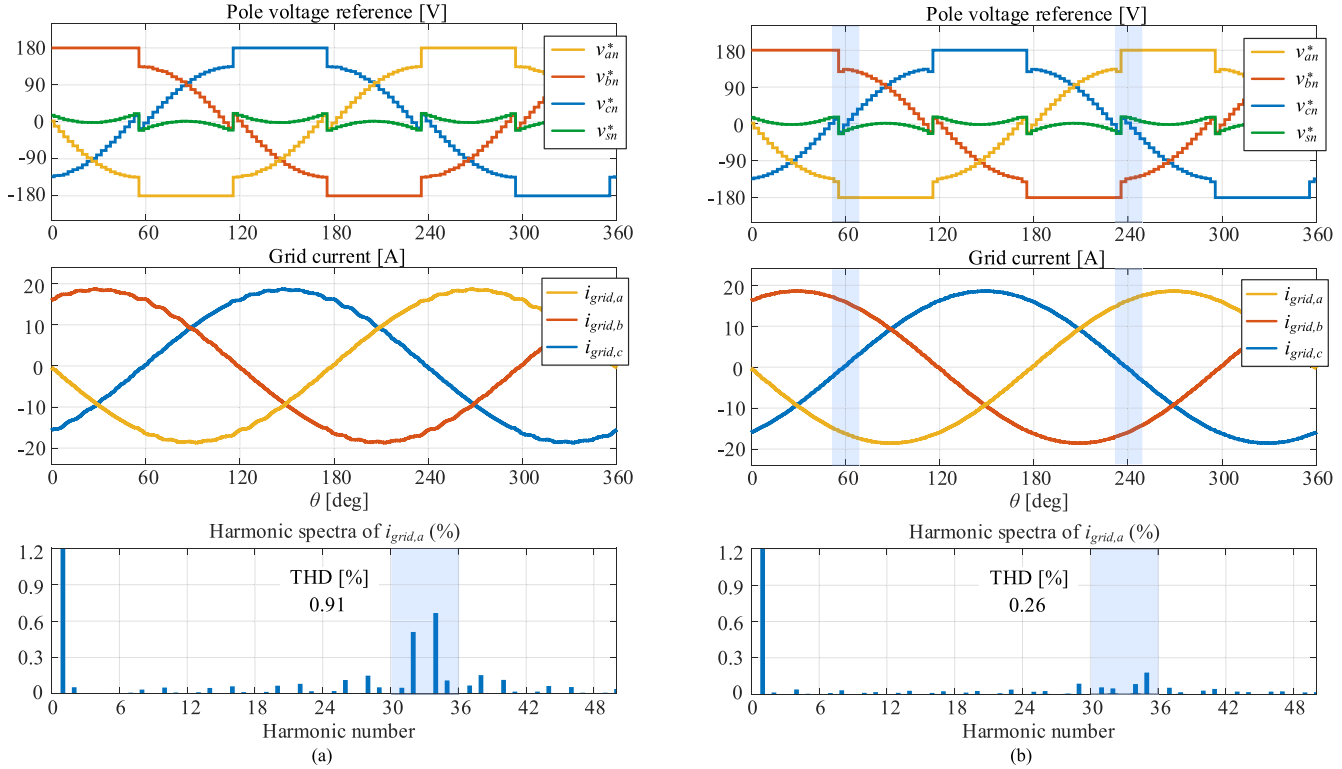

FIGURE 11. Simulation 2: Waveforms and harmonic spectra of $i_{grid,a}$ when V_{dc} = 360 V under DPWM (a) without the proposed method. (b) with the proposed method.

where the dc-link voltage, V_{dc}, was set to 400 V. Fig 9(a) shows that the resonance occurs when DPWM is applied. Current oscillations are provoked when $\mathbf{v}^*_{abcn}$ is abruptly changed, i.e., at v^*_{sn} edges. The current harmonics exceeds the grid regulation near f_{res} band, i.e., 0.3 % of the rated current in the case of IEEE 519. After applying

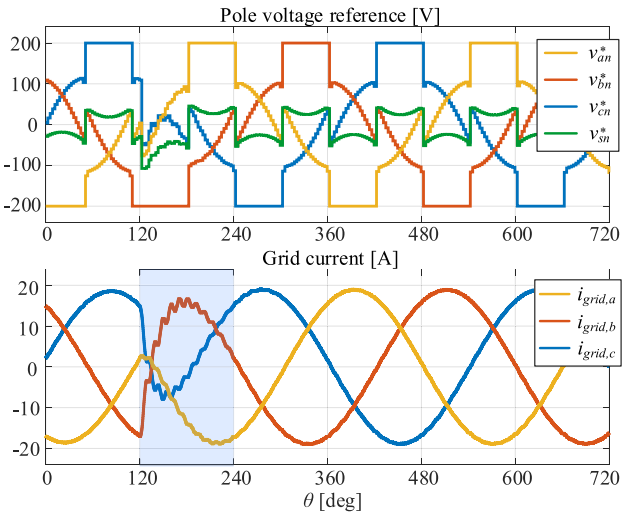

FIGURE 12. Simulation 3: Voltage and current waveforms under P^* variations.

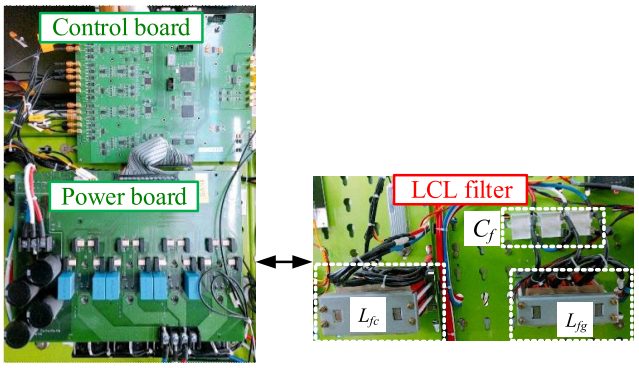

FIGURE 13. Experimental setup: 5 kW converter with *LCL* filter.

the proposed method, harmonics near f_{res} are remarkably decreased as shown in Fig. 10(b), satisfying the regulation while still maintaining DPWM. It means that the effective f_{sw} can be reduced by adopting DPWM with the proposed method.

Fig. 11 shows the simulation results when P^*, Q^* and V_{dc} were set to 5 kW, 0 kW, and 360 V, respectively. The dc-link voltage decreased by 10 % when compared to the case of Fig. 10, reducing the effects of v_{sn}^* jumps at v_{sn}^* edges. As shown in Fig. 11(a), the current harmonics near f_{res} exceed the grid regulation when DPWM is applied even under the reduced dc-link voltage, i.e., high MI operation. However, the current oscillations are decreased and satisfy the regulation by applying the proposed method as shown in Fig. 11(b).

Fig. 12 shows the current and voltage waveforms under P^* transients from +5 kW to −5 kW when the proposed method was applied. The proposed method can rapidly suppress the current oscillations during P^* variations where the resonance effects are remarkably reduced within a half cycle. It means that α_{peak} set by the P&O algorithm is quite effective even under transient conditions because MI is not significantly changed in the grid-connected converter. Moreover,

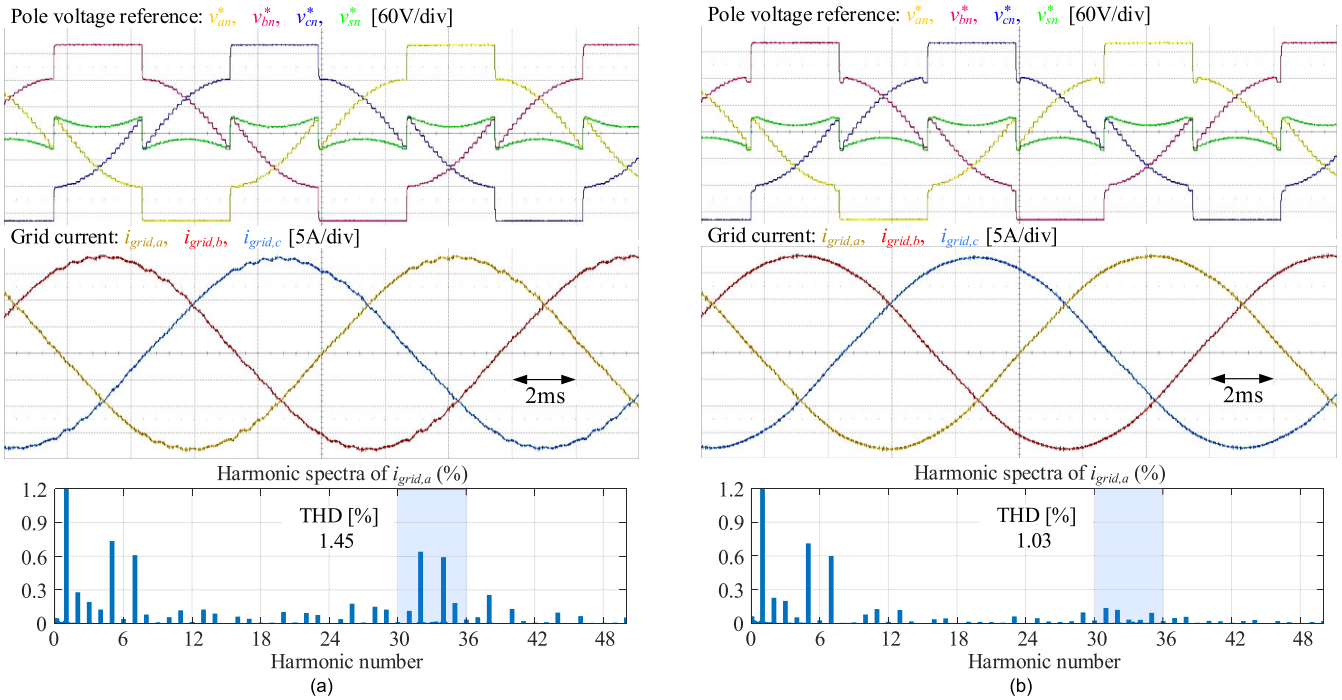

FIGURE 14. Experiment 1: Waveforms and harmonic spectra of $i_{grid,a}$ when V_{dc} = 400 V under DPWM (a) without the proposed method. (b) with the proposed method.

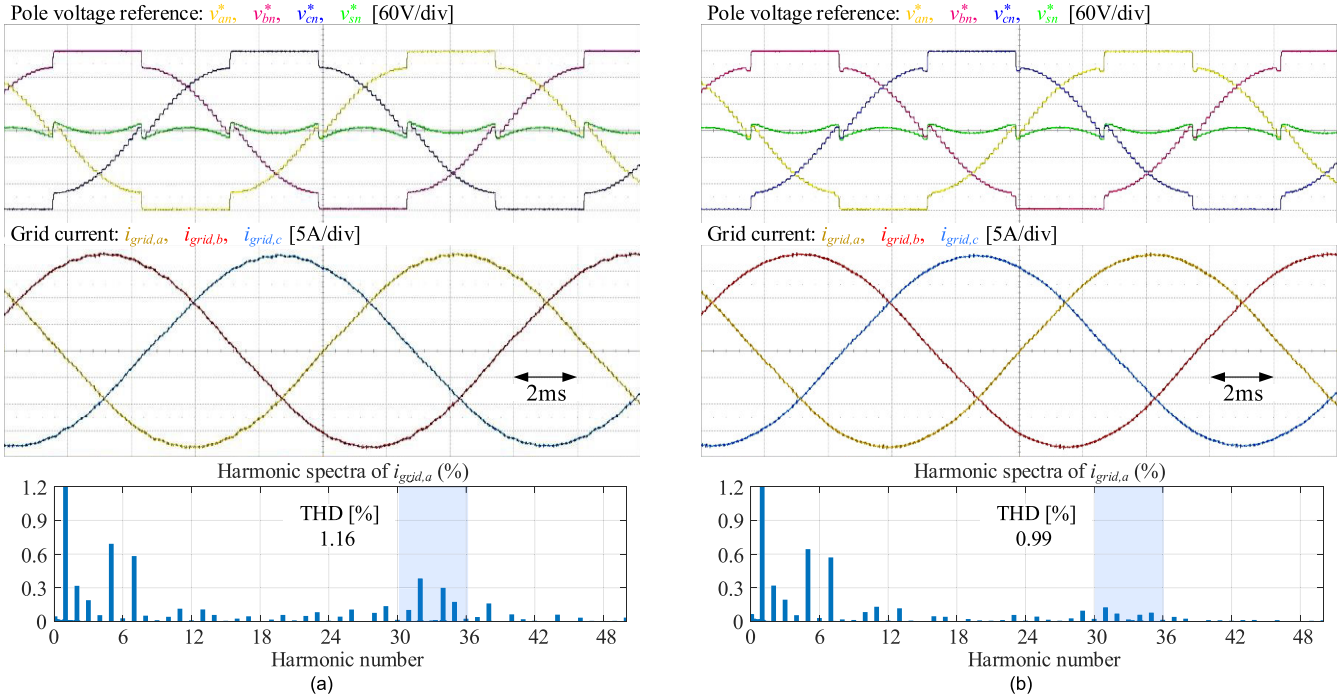

FIGURE 15. Experiment 2: Waveforms and harmonic spectra of $i_{grid,a}$ when $V_{dc} = 360$ V under DPWM (a) without the proposed method. (b) with the proposed method.

the current reference varies within a slew rate limit in the actual system. Thus, the proposed method could be a practical solution when DPWM is applied.

V. EXPERIMENTAL RESULTS

The proposed and conventional methods were conducted in a 5-kW converter system with *LCL* filter as shown in Fig. 13, where the system configurations are identical with the circuit diagram in Fig. 1. All control algorithms were implemented in a digital signal processor (DSP), TMS320F28335. System parameters and controller gains of the experiment were identical to those of the simulation. The dead time was set to 2 μs, and V_{dc} was changed by a dc power supply. In addition, the three-phase grid was emulated by a programmable ac power source.

Fig. 14 shows the experimental results during the steady-state operation, the same condition as those in Fig. 10. In contrast to the simulation results, low-order harmonics such as 5th and 7th are provoked by the converter nonlinearity. In Fig. 14(a), where DPWM is applied, there are harmonics near f_{res} due to the transition of v_{sn}^*. Without the proposed method, the harmonic distortion occurs at the edge of v_{sn}^*. It shows that the harmonic regulation cannot be achieved under v_{sn}^* jumps as shown in the harmonic spectra of $i_{grid,a}$. Thanks to the proposed method, the harmonic oscillations are significantly suppressed by shifting $\mathbf{v}_{abcn}^*$ at the edge of v_{sn}^* as shown in Fig. 14(b).

Fig. 15 shows the experimental results under the same condition as those in Fig. 11. Similar to the case of Fig. 14(a),

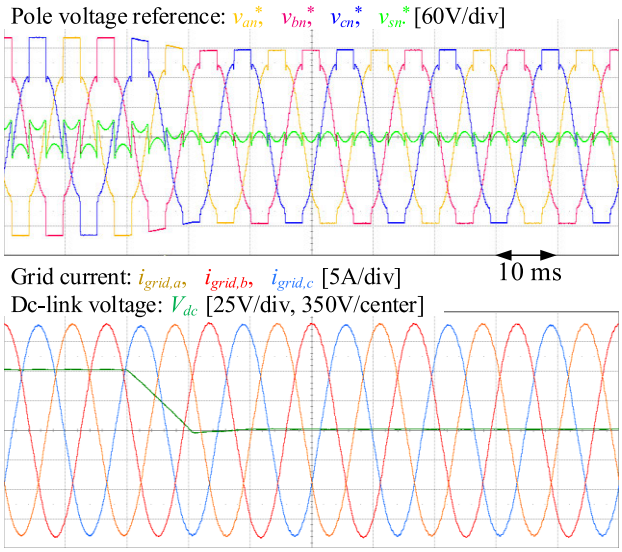

FIGURE 16. Experiment 3: Voltage and current waveforms under V_{dc} transients.

the harmonic distortion occurs at each v_{sn}^* edge by DPWM as shown in Fig. 15(a). The current harmonics near f_{res} are slightly decreased by internal resistances of the *LCL* filter compared with those in the simulation. However, the internal resistances are not sufficient to satisfy the harmonic regulation. After applying the proposed method, harmonic oscillation incurred by DPWM is significantly reduced as shown in Fig. 15(b). It satisfies the harmonic regulation by applying

the proposed method without adding the damping resistor or increasing the switching frequency.

Fig. 16 shows the performance under V_{dc} transients from 400 V to 350 V. It shows that the proposed method can suppress *LCL* resonance even under rapid V_{dc} variations, i.e., MI variations. α_{peak} is slowly converged to α_{opt} under MI variations by applying the P&O algorithm. However, the variation of MI is restricted within certain ranges for the grid-connected converter. In addition, V_{dc} is slowly changed in practical applications. Thus, the P&O algorithm can be an effective solution to search α_{opt} in real-time where α_{opt} varies slightly depending on the operating conditions.

VI. CONCLUSION

This paper analyzes the resonance problem incurred by DPWM for the grid-connected converter with *LCL* filter. In this paper, the resonance problem is dealt with the frequency and time domain analysis. The root cause of *LCL* resonance is interpreted as abrupt changes of the offset voltage. Thus, the voltage references near the edge of offset voltage is modified to minimize the current oscillation while preserving the merits of DPWM scheme. In the proposed method, the pole voltage references at the v_{sn}^* edge are moved closer to the optimal point. It becomes possible to implement the v_{sn}^* edge detection and α_{opt} searching algorithms. The performance of the proposed method has been verified with various simulation and experimental results. The current oscillation at v_{sn}^* edges is conspicuously reduced through the proposed method, minimizing the effective switching frequency of PWM converter under the satisfaction of the grid harmonics regulation.

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