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A Self-Regulating Method for IGBT Turn-Off Peak Voltage Control With Turn-Off Characteristics Improvement

YATAO LING, (Graduate Student Member, IEEE), ZHENGMING ZHAO, (Fellow, IEEE), AND BOCHEN SHI, (Graduate Student Member, IEEE)
Department of Electrical Engineering, Tsinghua University, Beijing 100084, China

Corresponding author: Yatao Ling (1546517440@qq.com)

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ABSTRACT In hard-switching applications, insulated gate bipolar transistors (IGBTs) always suffer from harmful turn-off peak voltages. To switch the devices safely, it is a common practice to use large enough drive resistances in conventional gate drives (CGD). This, however, slows down the turn-off transients and increases switching losses. Many other measures have been proposed in the literature to limit the peak voltage but they cannot apply direct or accurate control, making the voltage margin of IGBT in use still large. In this article, a novel self-regulating peak voltage control (SRPVC) method based on active gate drive (AGD) is proposed. The SRPVC method is the first developed and reported method that can control the peak voltage in a direct and accurate way regardless of commutation conditions. The SRPVC has high simplicity. By applying independent control on turn-off di/dt, the SRPVC can produce desired voltage spikes with small drive resistance under different switching conditions. Hence, the SRPVC can reduce the turn-off delays and losses to the utmost without increasing peak voltages. The control ability, accuracy and switching characteristics improvement with SRPVC are validated experimentally on an Infineon IGBT module FF300R12ME4. The experimental results show that under identical peak voltage, the SRPVC can realize up to 53% turn-off delay and 28% loss reduction under various load currents compared with CGD.

INDEX TERMS IGBT, turn-off peak voltage, active gate drive, control accuracy, turn-off characteristics improvement.

I. INTRODUCTION

Due to the rapid hard switching, IGBT can produce large turn-off peak voltage. The control of the peak voltage, denoted as v_{PK}, is critical for safe operating of converters as high overvoltage is destructive. Regulating v_{PK} is also beneficial for the maximum utilization of power-processing capacity for IGBTs as analyzed in reference [1]. Thus, this article is intended to develop a method for the accurate control of v_{PK} together with optimizations of other switching characteristics, e.g., turn-off delays and losses.

The existing methods to suppress the high transient voltage in hard switching can be classified into two categories.

The first category modifies the power stage, including improving the laminated bus bar structure for lower stray inductance [2]–[4], and adding auxiliary snubber circuits to help suppress the switching stresses [5], [6]. However, the drawback of the former technique lies in its limited effect because laminated bus bar usually cannot be reduced too low considering design complexity and manufacturing costs, and the drawback of the later one is that added snubber circuit itself can experience high stresses and some losses.

The second group simply relies on the gate driver [7]–[15]. Introducing no changes in power circuits, these methods for v_{CE} control can overcome the aforementioned shortcomings of the first group. This article focuses on methods in the second group.

In the conventional gate drive (CGD) method, increasing the drive resistance can attain target v_{PK} value at the largest load current, which, unfortunately, can slow down the switching and cause extra turn-off delays and losses. To attain better tradeoff between the v_{PK}, turn-off delays and losses with CGD, numerous active gate drive methods (AGDs) for v_{PK} suppression have been proposed [7]–[15] and are analyzed below.

Before giving the review, the expression for v_{PK} is shown as (1), where V_{bus} is the bus voltage, L_S is the total stray inductance in commutation path and $||\mathrm{d}i_C/\mathrm{d}t||$ is absolute

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value of the falling rate of IGBT current i_C.

$$v_{PK} = V_{bus} + L_S \left\| di_C/dt \right\| \quad (1)$$

Nearly all existing AGD methods focus on the regulating of $||di/dt||$ to control v_{PK}. K. Miyazaki *et al.* propose a novel integrated circuit (IC) driver, which has numerous drive strengths and this IC driver is verified to be able to reduce v_{PK} [7]. However, it relies on massive offline experiments and iterations to optimize the switching behavior. Hence, it has little flexibility when switching conditions including load current I_L, V_{bus}, L_S, IGBT model etc. vary. With feedback circuits, some drivers can control v_{PK} more accurately, either by applying predetermined drive resistances and currents in concerned di/dt stage [8]–[10], or by directly sampling and controlling the turn-off di/dt [11]–[13]. Unfortunately, with no direct v_{PK} sensing, these drivers still cannot attain target v_{PK} under changing switching conditions.

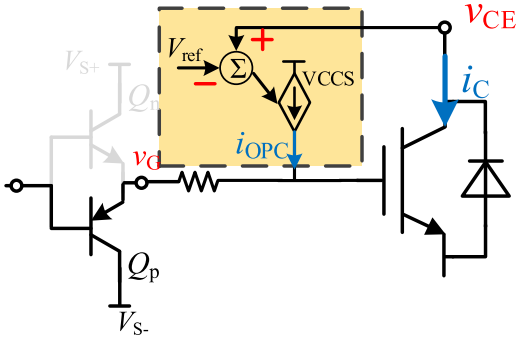

FIGURE 1. Schematic diagram of the control on turn-off v_{PK} by the active driver proposed in reference [14], [15].

Different from the above drive methods that control v_{PK} via regulating di/dt, the active driver developed in references [14], [15] applies control to v_{PK} only when v_{PK} exceeds a reference value. Fig. 1 gives the schematic diagram of its control on v_{PK}. From Fig. 1, it can be seen that when v_{PK} is above its reference value V_{ref}, the VCCS (voltage controlled current source) will be activated and extra gate current, i_{OPC} is injected to the gate to slow down i_C falling. The expression of i_{OPC} is given in (2), where α is the amplification factor of VCCS. Apparently, with direct sensing of v_{PK}, this driver can better adapt to the varying switching conditions. However, when i_C falls rapidly, i_{OPC} will exist and even have large magnitudes. Thus, according to (2), it can be safely concluded that the suppressed v_{PK} is still above its reference value V_{ref}. This inaccuracy of v_{PK} control requires careful design of the voltage margin of bus voltage.

$$i_{OPC} = \alpha \cdot (v_{CE} - V_{ref}) \quad (2)$$

Based on the analysis above, existing drivers are unable to adapt to different switching conditions for target v_{pk}, denoted as V_{ref}. Besides, these active drivers fail to control v_{PK} with high accuracy. Both the shortcomings weaken the practical value of v_{PK} control.

To solve this problem, a self-regulating peak voltage control (SRPVC) method is proposed, described and verified in detail in this article and the SRPVC is the first reported method to achieve direct and accurate v_{PK} control. With a proportional-integral (PI) regulator, this AGD based method, can helps the peak voltage automatically approach its reference value, regardless of the load current, L_S or device model, i.e. in a self-regulating manner. Hence, SRPVC can adapt to different switching conditions and achieve accurate control of v_{PK}. Consequently, the turn-off delay and turn-off loss can be optimized without risking the device safety.

In this article, operation principle, hardware configuration, PI factors tuning and control accuracy of SRPVC are described and analyzed in theory. Afterwards, the control accuracy, control effects and switching characteristics improvement with SRPVC are experimentally validated.

II. THEORETICAL DESCRIPTIONS AND ANALYSIS OF THE SRPVC METHOD

This section first gives brief descriptions of the operating principles and the theoretical analysis, explanations for the advantages of SRPVC over CGD method regarding the detailed switching performance.

A. OPERATING PRINCIPLE OF THE SRPVC METHOD

The SRPVC is a voltage-source driver which uses fixed drive resistances. The basic idea that how the SRPVC regulates the peak voltage, v_{PK} is to adjust and change drive voltages v_G in turn-off i_C falling stage. As a digital driver, the SRPVC has an on-board field programmable gate array (FPGA) to apply self-regulating switching control. The detailed operating principle is introduced below.

As shown in Fig. 2, the typical hard-switching turn-off process is divided into four stages here, i.e., delay, dv/dt, di/dt and off stages. In Fig. 2, v_G, i_C, v_{CE} are drive voltage, current and voltage of IGBT respectively. The delay stage starts when the driver receives the off commands and ends

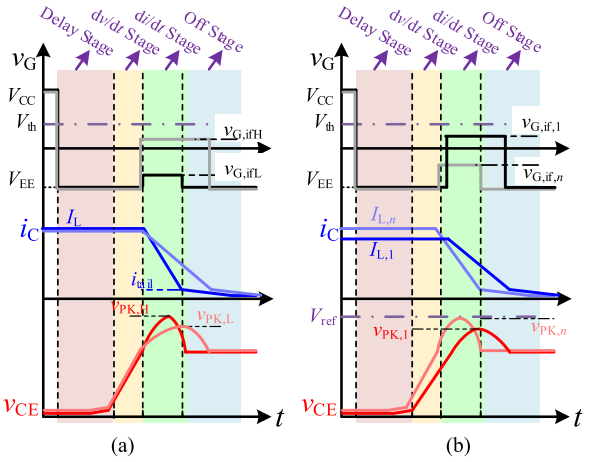

FIGURE 2. Theoretical turn-off waveforms of (a) independent regulating of turn-off peak voltages with SRPVC. (b) process of the self-regulating control for peak voltages with SRPVC.

when $v_{CE} = 10\%V_{bus}$. The v_{CE} rising stage spans from when $v_{CE} = 10\%V_{bus}$ to when $v_{CE} = V_{bus}$, marking the onset of i_C falling. The i_C falling stage lasts until i_C falls to tail current, i_{tail}.

The i_C falling rate in (1) can be expresses as (3), where g_m, V_{th}, R_{goff}, C_{ies} are respectively trans-conductance, threshold voltage drive resistance and input capacitance of IGBT, $v_{G,if}$ is the drive voltage in the i_C falling stage.

$$\left\| di_C/dt \right\| = \left\| \frac{g_m\left(i_C/g_m + V_{th} - v_{G,if}\right)}{R_{goff}C_{ies}} \right\| \tag{3}$$

By (1), (3), the SRPVC regulates v_{PK} by adjusting $v_{G,if}$ as shown in Fig. 2. As shown in Fig. 2(a), with simple feedback circuit, the SRPVC method can identify the i_C falling stage and then apply high drive voltage $v_{G,ifH}$ or low $v_{G,ifL}$ to attain low $v_{PK,L}$ or high $v_{PK,H}$. In the meantime, the delay and v_{CE} rising stages are both accelerated by applying the minimum drive voltage $v_G = V_{EE}$, yielding the smallest delays and losses.

In this way, the SRPVC can control v_{PK} without sacrificing the switching delay and losses.

In practical applications, as analyzed above, the accuracy and adaption of v_{PK} control under different switching conditions (I_L, V_{bus}, L_S, IGBT model, etc) are crucial. Fig. 2(b) shows the operating principle of SRPVC in practical uses. With the switching conditions unknown, the SRPVC is designed to apply a large drive voltage $v_{G,if,1}$ in the initial cycle as in Fig. 2(b). This can bring a low and safe initial v_{PK}, denoted as $v_{PK,1}$ in Fig. 2(b). Thereafter, the SRPVC method directly senses the actual v_{PK} in each switching cycle and compares the sensed values with the reference V_{ref}. Their difference which is in digital and decimal value, is processed by a PI regulator in the on-board FPGA to produce the $v_{G,if}$ for the next cycle. This regulating process is always active, making the SRPVC adaptive to changed switching conditions. As shown in Fig. 2(b), in the n_{th} cycle, the load current rises from $I_{L,1}$ to $I_{L,n}$ and the SRPVC has automatically controlled the $v_{G,if}$ to a lower $v_{G,n}$ so to achieve $v_{PK,n}$ value close to V_{ref}.

Fig. 3 gives the block diagram of the self-regulating control process. In the n_{th} cycle, peak voltage $v_{PK,n}$ is sampled and digitalized by a peak detector and an analog-to-digital converter (ADC). $N_{PK,n}$ and $N_{PK,ref}$ are digital values of sensed v_{PK} and target v_{PK} and the expressions are given as (4) and (5) respectively. In (4) and (5), k_{PK} is the whole gain of the sensing circuit and it is deduced in Section III.

$$N_{PK,n} = v_{PK,n}k_{PK} \tag{4}$$

$$N_{PK,ref} = V_{ref}k_{PK} \tag{5}$$

As the analysis of Fig. 2(b), the difference of digital values $N_{PK,n}$ and $N_{PK,ref}$ are calculated and amplified by a PI regulator implemented in FPGA. This calculation just takes time in the sub-microsecond range. Also, this calculation takes up only small resources in FPGA. Hence, this PI calculation can be accomplished by a low cost FPGA. Finally, the calculated drive voltage $v_{G,if}$ in n_{th} cycle is applied to IGBT in the next switching cycle after a delay. With this cycle-to-cycle operating manner, the peak voltage v_{PK} can be controlled directly and accurately.

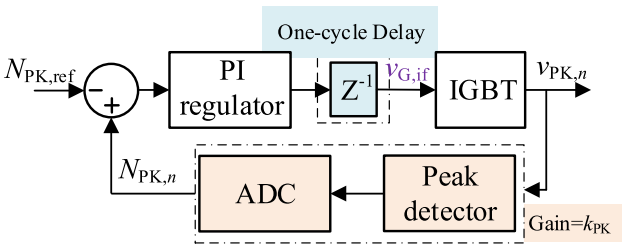

FIGURE 3. Block diagram of v_{PK} self-regulating control with the SRPVC.

B. TEORETICAL COMPARISON WITH CGD METHOD

To explain the advantages of SRPVC more clearly, this part gives the comparison between the SRPVC and CGD method based on their operating principles. The comparison of turn-off transient between both drivers is illustrated in Fig. 4.

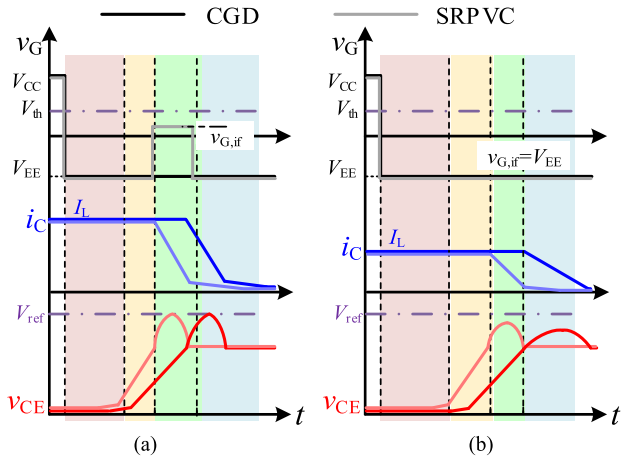

FIGURE 4. Theoretical turn-off behavior between the CGD and SRPVC methods where SRPVC uses a smaller R_{goff} than CGD. (a) under high load current. (b) under low load current.

Since the maximum v_{PK} commonly occurs at the largest load current I_L, to limit v_{PK} below the reference value V_{ref}, CGD method needs to use a relatively large R_{goff} so that $v_{PK} = V_{ref}$ at this large I_L. As analyzed in Fig. 2, the SRPVC, however, can apply large $v_{G,if}$ to reduce v_{PK}. Hence, with smaller R_{goff}, the SRPVC can still attain identical v_{PK} to CGD method. Hence, at high I_L, as shown in Fig. 4(a), the SRPVC applies $v_{G,if}$ larger than V_{EE} to achieve the same v_{PK} reference value, V_{ref} as CGD. Since SRPVC uses a smaller R_{goff} and applies the same $v_G = V_{EE}$ in other turn-off stages, the SRPVC method has lower delays and losses than CGD.

Fig. 4(b) compares the turn-off behavior with both drivers under low I_L. When I_L is lower, for both drivers, typically the delays will be larger, and $||dv/dt||$ will be lower. However,

with smaller R_{goff}, the SRPVC will always have higher $||dv/dt||$, lower delays and losses in comparison with CGD.

With CGD, the $||di/dt||$ and hence peak voltage v_{PK} will be reduced at low I_L. Nonetheless, it can be seen from Fig. 4(a) that actually, the SRPVC method is able to apply lower $v_{G,if}$ to attain v_{PK} higher than V_{ref} under high I_L. Hence, under smaller I_L, with self-regulating control, SRPVC can still realize $v_{PK} = V_{ref}$. However, under small enough I_L, with the self-regulating control, even when the SRPVC method finally applies the smallest drive voltage $v_{G,if} = V_{EE}$, the peak voltage, v_{PK} will still be below V_{ref}. This is the case shown in Fig. 4(b), where the SRPVC method applies constant drive voltage $v_G = V_{EE}$ in the whole turn-off transient and except a smaller drive resistance, the SRPVC method works just like CGD method.

All these theoretical comparisons between the SRPVC and CGD methods will be validated experimentally in Section IV.

C. CONCLUSION

In summary, this section shows the operating principle of the proposed SRPVC. The SRPVC method is the first developed and proposed method that features theoretical capabilities of direct and accurate peak voltage v_{PK} sensing and control.

To show the superior turn-off performance of the SRPVC method, it is compared with CGD method in theory under different load currents. This comparison is in essence convincing and clear. This comparison lays a solid foundation for the experiments later shown in this article.

It should be noted that since the SRPVC method regulates the peak voltage in a cycle-to-cycle manner, the load currents had better not change too much in adjacent switching cycles. This is because, for example, when v_{PK} reaches V_{ref} in the n_{th} cycle, the drive voltage $v_{G,if}$ in the $n + 1_{th}$ cycle may stay the same as that in the n_{th} cycle. In this case, if the load current in the $n + 1_{th}$ cycle is significantly larger than in the n_{th} cycle, $v_{PK,n+1}$ may exceed $v_{PK,n} = V_{ref}$ much. Therefore, when applying the SRPVC in ac-dc or dc-ac converters whose switching frequencies are rather low, attention must be paid to the possible significant load current changes from cycle to cycle.

It is pointed out here that based on the analysis in Part A, the SRPVC method requires several crucial circuits for the v_{PK} sensing and control. These circuits will be introduced in Section III.

III. HARDWARE IMPLEMENTATION OF THE PROPOSED SRPVC METHOD

This section introduces three crucial circuit implementations in SRPVC method for the self-regulating control of v_{PK}.

A. DRIVE VOLTAGE CIRCUIT

By preceding analysis in Section II, the SRPVC method relies on the drive voltage adjustment to achieve v_{PK} control. With (1), (3), the number of available v_{PK}s is decided by the available number of drive voltages that can be provided by the SRPVC method.

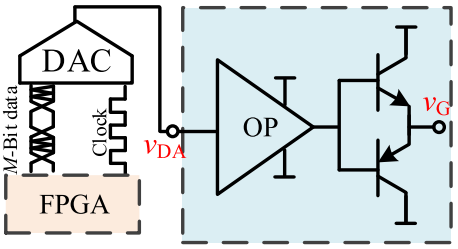

FIGURE 5. Circuit diagram of the multi-level drive voltage circuit with high resolution.

Apparently, an ideal drive voltage circuit should be able to produce numerous and stepless drive levels. Hence, a concise, multi-level drive voltage circuit with high resolution is used as in Fig. 5.

The on-board FPGA feeds parallel M-Bit binary numbers (denoted as CODE) that are corresponding to the desired v_G to a high-speed DAC. The output voltage of the DAC, v_{DA} is in the range of 0V and 1V, and amplified by an op amp and push-pull, v_{DA} finally turns into the desire v_G, which is in the range of V_{EE} and V_{CC}.

v_G is related to CODE by (6), where k_1 and V_{bias} are respectively the factor and bias voltage determined by the detailed configuration. Since CODE is in the range of 0 and 2^M-1, the step of available v_G, Δv_G is given as (7). When a 10-Bit DAC is chosen, Δv_G will be smaller than (V_{CC}-V_{EE})/1000, which shows high resolution.

The DAC CODE for $v_G = v_x$ will be denoted as CODE(v_x).

$$v_G = k_1 \frac{\text{CODE}}{2^M - 1} - V_{bias} \tag{6}$$

$$\Delta v_G = \frac{V_{CC} - V_{EE}}{2^M} \tag{7}$$

B. IDENTIFICATION CIRCUIT FOR THE TURN-OFF CURRENT FALLING STAGE

From the preceding analysis of Fig. 2 and Fig. 4, to maintain low turn-off delay and losses when controlling v_{PK}, the SRPVC method should identify the i_C falling stage correctly.

The way SRPVC identifies the i_C falling stage is shown in Fig. 6. There is an inherent parasitic inductance L_E between the auxiliary and power emitter of IGBT module, and thus

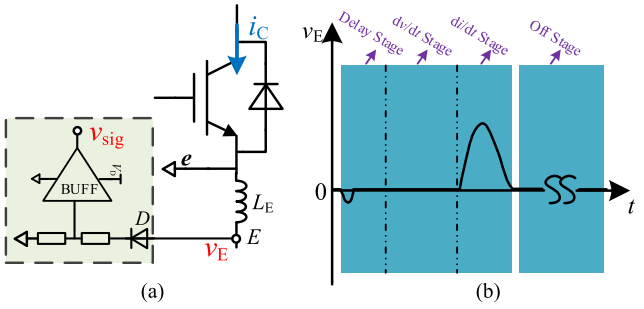

FIGURE 6. (a) Feedback circuit for the identification of i_C falling stage. (b) Diagram of the voltage at power emitter, v_E.

the voltage v_E at power emitter E in Fig. 6(a) is given as (8). By (8), the diagram for v_E in turn-off transients can be depicted as Fig. 6(b). It can be seen from Fig. 6(b) that, only within di/dt stage, is v_E positive. With this feature, as shown in Fig. 6(a), a diode D, a R divider and a buffer can be used for the identification of i_C falling stage. That is, when the

$$v_E = -L_E \frac{di_C}{dt} \tag{8}$$

buffer outputs 1, IGBT has entered di/dt stage. Afterwards, when the buffer outputs 0, IGBT has left the di/dt stage and entered the off stage.

C. SENSING AND DIGITIZATION CIRCUIT OF PEAK VOLTAEG VPK

According to the theoretical analysis in Section II, the direct sensing of v_{PK} is the foundation of the v_{PK} self-regulating control with the SRPVC method. Hence, here gives the descriptions of the v_{PK} sensing circuit, i.e., the whole feedback path in Fig. 3.

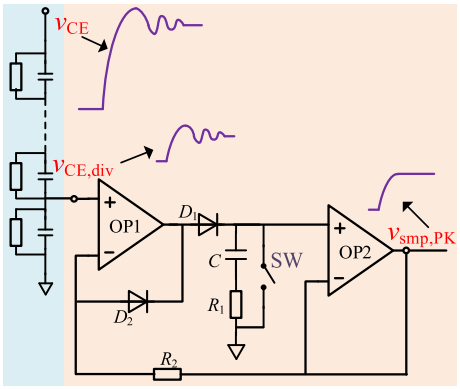

FIGURE 7. Schematic of the v_{PK} analog sensing circuit.

Fig. 7 shows the circuit for attaining the v_{PK} in a scaled down and analog form. The real v_{CE} is first proportioned by a RC divide, yielding $v_{CE,div}$ and the scaling factor is denoted as k_V. $v_{CE,div}$ is fed to the following circuit that contains two amps for the high sensing accuracy. This following circuit is able to hold and output the maximum value of $v_{CE,div}$, i.e., $v_{smp,PK} = v^*_{PK} k_V$. Closing the analog switch SW in this circuit can reset its output. The shapes of key voltages in the sensing circuit are also given in Fig. 7.

$$v_{smp,PK} = v_{PK} k_V \tag{9}$$

This analog variable, $v_{smp,PK}$ ($= v^*_{PK} k_V$), is further converted to digital quantities for FPGA calculations via an ADC as shown in Fig. 3. The conversion ratio of this ADC is denoted as k_{ADC}. Then digital values of sensed v_{PK} at the n_{th} cycle, denoted as $N_{PK,n}$ in (4), equals $v^*_{smp,PK} k_{ADC}$. Combining (4), (9), the total scaling factor between v_{PK} and its digital values, k_{PK} can be deduced as (10).

$$k_{PK} = k_V k_{ADC} \tag{10}$$

D. SUMMARY

This section describes three crucial circuits in detail for the operating of SRPVC method. Among them, the error of the whole v_{PK} sensing circuit, which includes the analog part shown in Fig. 7 and the ADC part, has direct impact on the control accuracy of v_{PK}. Hence, the evaluation the whole sensing error from v_{PK} to digital values is necessary and will be dealt with in the next section.

IV. EXPERIMENTAL VERIFICATIONS OF THE SRPVC METHOD

In this section, experimental verifications of the SRPVC method are performed. The verifications will include the evaluation of drive voltage circuit response speed, the whole error of v_{PK} sensing circuit, the proportional-integral factors tuning, the v_{PK} control with the SRPVC method under different load currents and the corresponding turn-off characteristics in comparison with CGD method.

A. SRPVC AND TEST PLATFORM PRAMETERS

Fig. 8 marks the crucial parts that are related to the v_{PK} control in the developed SRPVC PCB board. TABLE 1 lists the critical parameters in the designed test platform. Since this is cycle-to-cycle control, a general-purpose ADC can be used for digitalization.

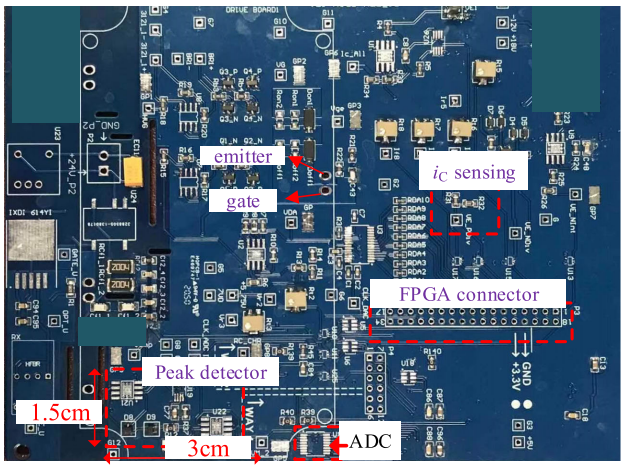

FIGURE 8. Photograph of the developed SRPVC PCB board.

B. RESPONSE SPEED OF THE DRIVE VOLTAGE CIRCUIT

The response speed of the drive voltage circuit in Fig. 5 is critical for the control of i_C falling speed and v_{PK}. Only when the circuit alters drive voltage quickly enough after receiving the updated DAC CODE, can the control takes effect. Fig. 9 gives the tested response speed in turn-off transient. It can be seen that under the large 10V v_G step, the delay is no more than 10ns, which is acceptable for this IGBT.

C. EVALUATION OF THE WHOLE SENSING ERROR FOR PEAK VOLTAGE VPK

This part evaluates the whole sensing error for peak voltage v_{PK} and its effects on the control accuracy of v_{PK}.

TABLE 1. Parameters for the SRPVC test platform.

Name	Parameters
IGBT	FF300R12ME4
Push-pull BJTs	ZXTN07045EFF/ZXTP07040DFF
v_{CE} Measurement	P5100A, 2500V/500MHz
Analog Sensing Circuit	Scaling factor k_V=1/220
ADC	Conversion ratio k_{ADC}=51

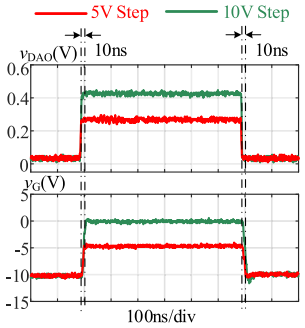

FIGURE 9. Tested response speed of the drive voltage circuit in turn-off transient.

There always exist sensing errors in the analog value $v_{smp,PK}$ in Fig. 7 and in the subsequent digitalization. Here, the whole sensing error from v_{PK} to digital values N_{PK} is denoted as N_e. Accordingly, taking N_e into account, the block diagram of v_{PK} control is as Fig. 10.

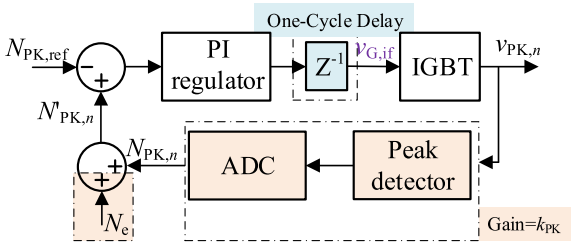

FIGURE 10. Block diagram of v_{PK} self-regulating control with error N_e taken into account.

From Fig. 10, the v_{PK} control error, $v_{PK,e}$ that is caused by sensing error can be deduced as (11). Equation (11) reveals the proportional relationship between $v_{PK,e}$ and N_e. In (11), the total gain k_{PK} is 51/220, as calculated by (10) and the k_V, k_{ADC} values in TABLE 1.

$$v_{PK,e} = \left\| N_e / k_{PK} \right\| \tag{11}$$

To show the high control accuracy of SRPVC, namely low $v_{PK,e}$, N_e is tested extensively in Fig. 11 by experiments. Fig. 11(a) gives the experimental waveforms of the v_{pk} sensing under 600V/300A. It can be seen that the output of the analog sensing circuit in Fig. 7, i.e., $v_{smp,PK}$ is 4.11V. This value is close to the maximum value 4.109V of $v_{CE,div}$.

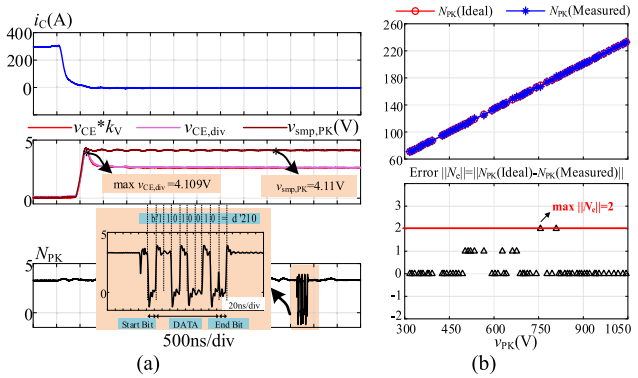

FIGURE 11. (a) Key waveforms for the sensing of v_{PK} under 600V/300A. (b) Ideal and measured N_{PK} results under various v_{PK}.

Hence, the analog sensing circuit in Fig. 7 has high accuracy. Then, N_{PK} in Fig. 11(a) represents the digital values fed to FPGA. Ideally, without sensing error, the 4.109V should correspond to 210 decimal values. In Fig. 11(a), the measured N_{PK} is 210. Therefore, Fig. 11(a) shows no sensing errors.

More tests under various v_{PK} are performed to assess the sensing error N_e in Fig. 11(b), where N_{PK}(Ideal) are the ideal N_{PK} without sensing errors and N_{PK}(Measured) are the actual N_{PK} received by the on-board FPGA with sensing errors. It can be seen that majority of v_{PK} have no sensing errors and only several v_{PK} have errors with absolute values of 1 or 2. Based on (11), the maximum control error $v_{PK,e}$ can thus be determined to be 8.6V, which is acceptable and can be compensated easily.

D. PROPORTIONAL-INTEGRAL FACTORS TUNING

The proposed SRPVC method uses a single proportional-integral regulator for the automatic and self-regulating control of v_{PK}. Hence, the tuning of PI factors needs discussing here.

The PI factors refer to proportional factor k_P and integral factor k_I. The tuning of PI factors in this article is divided into two steps. Firstly, under the condition of stable system response, it is always desired that k_P, k_I be as large as possible. This is because that larger PI factors can help shorten the settling process. Thus, the first step in k_P, k_I tuning is to calculate their upper limit in theory. Thereafter, the second step is to test PI factors down from the upper limit and find the large factors with stable response.

Here gives the calculation method for the upper limit of PI factors. As described in Part A, Section II, a large $v_{G,if}$ should be applied in the first switching cycle for a low and safe $v_{PK,1}$. Denoted as $v_{G,if,1}$, this initial large drive voltage has DAC CODE($v_{G,if,1}$). $v_{G,if,1}$ yields the first peak voltage $v_{PK,1}$, whose sensed decimal value is $N_{PK,1} = v_{PK,1}k_{PK}$ given by (5). Accordingly, the decimal value of v_{PK} reference value V_{ref} is as $N_{PK,ref} = V_{ref}k_{PK}$. Hence, the error in the first cycle, $e_{PK,1}$ and the DAC CODE for the second cycle, CODE($v_{G,if,2}$) can be obtained as (12), (13). To ensure the normal operation of v_{PK} self-regulating control,

CODE($v_{G,if,2}$) should be within its allowable range. Since $v_{PK,1}$ is low, the first error $e_{PK,1}$ is negative, CODE($v_{G,if,2}$) must be no less than the allowed smallest value, which is CODE(V_{EE}) here. Therefore, combining (12), (13), the upper limit for PI factors is given as (14).

$$e_{PK,1} = N_{PK,1} - N_{PK,ref} \tag{12}$$

$$\text{CODE}\left(v_{G,if,2}\right) = \text{CODE}\left(v_{G,if,1}\right) + k_P e_{PK,1} + k_I e_{PK,1} \tag{13}$$

$$k_P + k_I \leq \frac{\text{CODE}\left(v_{G,if,1}\right) - \text{CODE}\left(V_{EE}\right)}{N_{PK,ref} - N_{PK,1}} \tag{14}$$

Take the k_P, k_I tuning of v_{PK} control at 200A/600V as an example.

Firstly, the upper limit of PI factors is calculated. The reference peak voltage V_{ref} is 820V and $N_{PK,ref}$ is 190. The large initial v_G applied in turn-off di/dt stage, $v_{G,if,1}$ is 0V here which corresponds to the DAC CODE(0V). Calculated by (6), CODE(0V) is 400 in decimal value. This first $v_{G,if,1}$ yields a measured $v_{PK,1} = 770$V, whose sensed decimal value is $N_{PK,1} = 179$ by (4). CODE(V_{EE}) is assumed to be 0. Hence, by (14), the upper limit for PI factors is calculated to be 36.

Secondly, experiments with k_P, k_I down from this limit are performed to find the suitable factors. Fig. 12(a) shows the experimental waveforms with $k_P = 16$, $k_I = 20$ and the PI factors just meet the upper limit. It can be seen in Fig. 12(a) that, the $v_{G,if,2}$ falls from $v_{G,if,1} = 0$V to V_{EE}. This results a v_{PK} exceeding V_{ref} by a significant amplitude of 35V. In Fig. 12(b), k_P, k_I are lowered and they are 5, 6 respectively. From the waveforms in Fig. 12(b), $v_{G,if,2}$ falls a bit and $v_{PK,2}$ just equals V_{ref}. By Fig. 12, $k_P = 5$, $k_I = 6$ are suitable PI factors, which can bring stable and fast response.

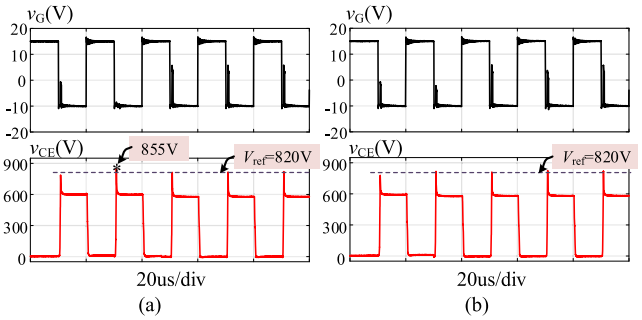

FIGURE 12. Tuning of PI factors by experimental results with factors down from the calculated upper limit. (a) $k_P = 16$, $k_I = 20$. (b) $k_P = 5$, $k_I = 6$.

In summary, this part gives a PI tuning method for v_{PK} self-regulating control. This method helps find the suitable k_P, k_I with convenience. The analysis and calculations are all experimentally validated.

E. PEAK VOLTAGE REULTS UNDER 600V/300A WITH THE SRPVC AND CGD METHODS

Fig. 13 shows the multi-cycle experimental results of v_{PK} control with $R_{goff} = 4\Omega$ for both the CGD and SRPVC methods. V_{bus} is 600V and reference value for v_{PK} is $V_{ref} = 900$V.

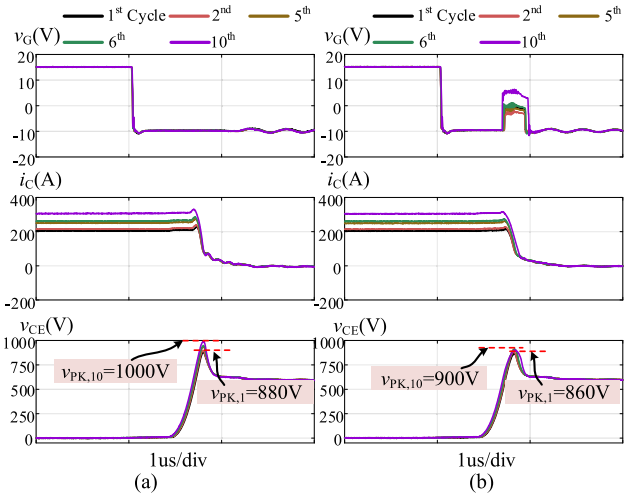

FIGURE 13. Turn-off waveforms comparison under 600V/300A with $R_{goff} = 4\ \Omega$ at first, second, fifth, sixth and tenth cycles for both (a) the CGD method (b) the SRPVC method.

In Fig. 13(a), the initial v_{PK} is 880V. In the following cycles, the load current rises, so is v_{PK}. At the 10th cycle, when $I_L = 300$A, rated value for the IGBT module, v_{PK} has risen to 1000V.

Fig. 13(b) shows the control results with the SRPVC method. As analyzed in Part A, Section II, since the switching conditions are unknown, SRPVC applies a large drive voltage, here around 0V in the initial cycle to attain a safe v_{PK}, i.e., $v_{PK,ini} = 860$V, smaller than that in Fig. 13(a). Since this v_{PK} is lower than V_{ref}, the SRPVC method reduces $v_{G,if}$ in the 2nd cycle to increase v_{PK}. In the subsequent cycles, with I_L rising, to achieve $v_{PK} = V_{ref}$, the SRPVC method increases $v_{G,if}$ gradually to control v_{PK}. In the last cycle, $v_{G,if}$ has risen to +4V and v_{PK} is controlled to 900V.

Experimental results in Fig. 13 can prove the self-regulating control abilities with the SRPVC.

F. TURN-OFF CHARACTERISTICS IMPROVEMENT WITH THE SRPVC UNDER ALL LOAD CURRENRTS

In Fig. 13(b), as analyzed in Section II, under the SRPVC method, v_G in delay and dv/dt stages can be maintained at V_{EE} whatever I_L is, helping reduce delays and losses. This part compares the turn-off characteristics of SRPVC and CGD. The comparison criterion is to achieve $v_{PK} = V_{ref}$ for both drivers under the highest load current (i.e., IGBT rated current) and then compares their characteristics at various currents.

In this part, V_{bus} and V_{ref} are 600V and 900V respectively, the same as Part E. After experimental tests, 8.5Ω is found to be the smallest R_{goff} for CGD to achieve $v_{PK} = V_{ref}$ under the highest current. From Fig. 13(b), the SRPVC method can attain $v_{PK} = V_{ref}$ with $R_{goff} = 4\Omega$.

Fig. 14 shows the experimental turn-off waveforms of CGD and SRPVC methods under different load currents. From Fig. 14, it can be seen that with $R_{goff} = 8.5\Omega$, CGD realizes $v_{PK} = V_{ref}$ under 300A current. Also, with

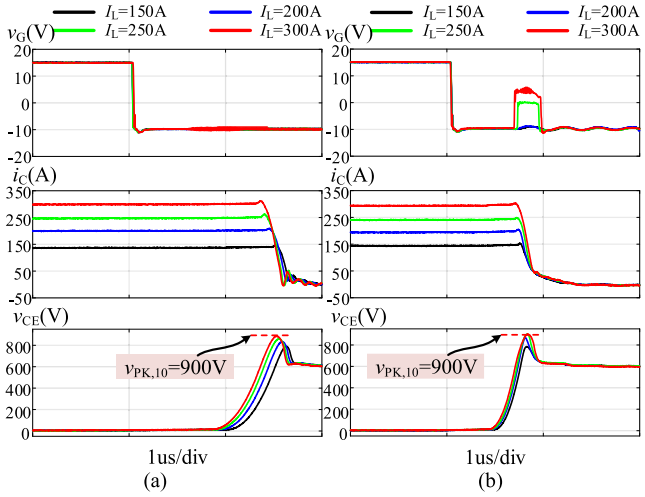

FIGURE 14. Turn-off waveforms comparison under different load currents at first, second, fifth, sixth and tenth cycles for both (a) the CGD method with R_{goff} = 8.5 Ω (b) the SRPVC method R_{goff} = 4 Ω.

R_{goff} = 4Ω, the SRPVC realizes v_{PK} = V_{ref} under 300A current. Fig. 14(a) shows that with CGD, apparently, both v_{PK}, $||dv_{CE}/dt||$ will fall and turn-off delay will rise obviously when load current reduction. In Fig. 14(b), it can be seen that when load current is 300A and 250A, $v_{G,if,10}$ is controlled to high value with the SRPVC method. This means that v_{PK} are both controlled to V_{ref} under 300A and 250A load currents. However, when load current is 200A or lower, it can be seen that $v_{G,if}$ is controlled to V_{EE}, which means that under this low current, v_{PK} will always be below V_{ref}, even with the lowest $v_{G,if}$ applied.

In Fig. 14(b), the SRPVC method also shows the trends of lower v_{PK}, lower $||dv_{CE}/dt||$, higher turn-off delay with the reduction of load currents. However, with a smaller drive resistance R_{goff} and the same v_G = V_{EE} in turn-off delay and dv/dt stages as the CGD method, the SRPVC method can produce achieve smaller delays and losses, which can be seen from Fig. 14(a) and (b).

To gain a clearer comparison of both drive methods, the turn-off characteristics of both drivers in Fig. 14 are Fig. 15 summarizes in Fig. 15. The turn-off characteristics include v_{PK}, turn-off delays and turn-off losses. Note that there are more load currents being covered in Fig. 15.

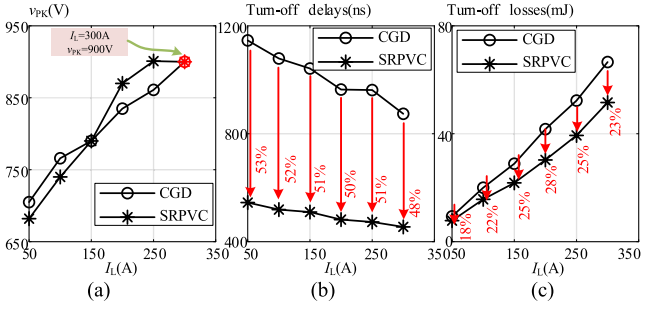

FIGURE 15. Summarized turn-off characteristics in Fig. 14 with v_{PK} = V_{ref} at 300A rated current for both the CGD and SRPVC methods. (a) Turn-off peak voltage v_{PK}. (b) Turn-off delays. (c) Turn-off losses.

From Fig. 15(a), both drivers realize v_{PK} = V_{ref} under the rated 300A I_L. Under 250A load current, v_{PK} with CGD falls by 50V. The SRPVC, however, as indicated by the analysis of Fig. 14, can still realize v_{PK} = V_{ref}. At 200A and below, since the I_L is small enough, the SRPVC method can not achieve v_{PK} = V_{ref} either even when it applies the lowest $v_{G,if}$ = V_{EE} as CGD. Note that when I_L is lower than 150A, even with this smaller R_{goff}, the SRPVC v_{PK} can fall below CGD. This is due to the non-monotone dependence of i_C falling speed on the drive resistance and this dependence is inherent in trench-gate field-stop IGBTs. It is pointed out here that, as shown in Fig. 15(a), under I_L >150A, the SRPVC method brings larger v_{PK} than CGD method. This is acceptable since they are all no larger than V_{ref} = 900V which is the reference value for turn-off peak voltages here.

Consistent with the analysis in Part B, Section II, with self-regulating control of v_{PK} and smaller R_{goff}, the SRPVC method can not only achieve v_{PK} = V_{ref} to ensure safe switching, but can reduce turn-off delays and losses significantly. As shown in Fig. 15(b), Fig. 15(c), the SRPVC method achieves up to 53% reduction in turn-off delays and 28% reduction in turn-off losses respectively compared with the CGD method.

V. CONCLUSION

This article presents a gate driver based method for direct and accurate control of turn-off peak voltage v_{PK}. By sensing and controlling the peak voltages directly, the SRPVC method can well adapt to different switching conditions.

The presented hardware configuration features high simplicity and cost effectiveness.

The SRPVC PI factor tuning method, the sensing and control accuracy for v_{PK} are all discussed by theoretical analysis and are experimentally verified.

This SRPVC method is the first developed and reported method that can control v_{PK} in a self-regulating manner. By applying a large initial drive voltage in turn-off di/dt stage, and applies self-regulating control afterwards, the SRPVC method can realized the safe v_{PK} control with high accuracy even under unknown switching conditions. This control can overcome the two shortcomings described in Introduction.

Also, this control capability not only allows the SRPVC to switch the devices safely with unknown switching conditions, but also to reduce the turn-off delays and losses significantly, which is validated experimentally. All this makes the SRPVC attractive for practical engineering applications.

In addition, as analyzed in Part C, Section II, attention should be paid to the applications of the SRPVC method. When applying the SRPVC in ac-dc or dc-ac converters whose switching frequencies are rather low, the load current may change significantly in adjacent switching cycles and hence, attention must be paid to the possible occurrence of v_{PK} exceeding V_{ref}.

In the future work, the SRPVC method will be applied to SiC power semiconductors.

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YATAO LING (Graduate Student Member, IEEE) received the B.S. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2014. He is currently pursuing the Ph.D. degree in electrical engineering with the Department of Electrical Engineering, Tsinghua University, Beijing, China.

His current research interests include gate drive technologies for IGBT and silicon carbide devices, and control techniques for PWM converters.

ZHENGMING ZHAO (Fellow, IEEE) received the B.S. and M.S. degrees in electrical engineering from Hunan University, Changsha, China, in 1982 and 1985, respectively, and the Ph.D. degree from Tsinghua University, Beijing, China, in 1991.

From 1994 to 1996, he was a Postdoctoral Fellow with The Ohio State University, Columbus, OH, USA, and a Visiting Scholar with the University of California Irvine, Irvine, CA, USA. He is currently a Professor with the Department of Electrical Engineering, Tsinghua University. His current research interests include high-power conversion, power electronics and motor control, and solar energy applications.

BOCHEN SHI (Graduate Student Member, IEEE) was born in Dalian, China, in 1995. He received the B.S. degree from the Department of Electrical Engineering, Tsinghua University, Beijing, China, in 2017, where he is currently pursuing the Ph.D. degree in electrical engineering.

His research interests include modeling of power semiconductor devices and simulation approach for power electronics systems.