IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received July 12, 2021, accepted July 29, 2021, date of publication August 30, 2021, date of current version September 14, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3109155

Digital Instrument for Time Measurements: Small, Portable, High–Performance, Fully Programmable

NICOLA CORNA, (Member, IEEE), FABIO GARZETTI, (Member, IEEE), NICOLA LUSARDI, (Member, IEEE), AND ANGELO GERACI, (Senior Member, IEEE)
Politecnico di Milano, 20133 Milano, Italy

Corresponding author: Nicola Corna (nicola.corna@polimi.it)

ABSTRACT We present a small, portable, plug–and–play time measurement instrument entirely based on Field Programmable Gate Array (FPGA). Its performance is state–of–the–art in terms of the most recent Application–Specific Integrated Circuit (ASIC) solutions of Time–to–Digital Converters (TDCs), and all operating features are fully–programmable. The instrument offers an excellent cost–performance and is suitable for detector test and time correlation measurement applications. More generally, the instrument is very well suited for fast–prototyping of systems where time measures are involved, at low cost and design effort. All the features of the instrument can be easily accessed through either the Graphical User Interface (GUI) or directly from the software Application Programming Interface (API).

INDEX TERMS TDC, FPGA, fast–prototyping, detector test, correlation measures.

I. INTRODUCTION

Time measurements, that is identification of the position of events over time with respect to an absolute reference or the duration of time intervals, are increasingly used in the scientific and industrial field to obtain information, even if not homogeneous with time [1]–[5]. A classic example of this is the measurement of the distance to a target obtained from the time of flight of a signal to reach and return from the target (Time-Of-Flight, TOF measurements) at the base of next generation mobility systems [6]–[10].

In general, time measurements can provide both direct information, for example the duration of the interval between two events, and indirect information, that is deduced from the time measurement. The obvious measure of a distance from the time of flight of a signal that propagates at a known and finite speed through that distance belongs to this second category. It is impossible to give a complete view of possible applications, therefore we just focus on some significant examples of the diversity of time measurements used in different sectors. First, laser rangefinders are used to monitor or measure distances or object lengths in several fields, from geodesy to sports, from 3-D object recognition to forestry,

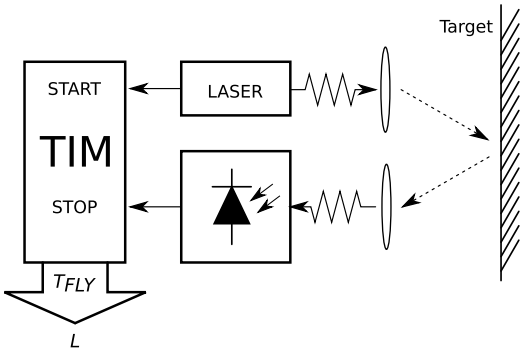


FIGURE 1. Block diagram of laser a rangefinder. The distance L is calculated from the physically measured time of flight T_{FLY}, which is the time interval between the departure (START) and arrival (STOP) of the laser pulse. The module Time Interval Measure (TIM) calculates the interval duration.

just to name a few. These instruments provide positional information even over long distances up to several kilometers. The most common form of laser rangefinder operates on the time of flight principle by sending a laser pulse on a narrow beam towards the target and measuring the time taken by the pulse to be reflected off and returned to the generation point (Figure 1) [11].

Further, in physics and physical chemistry, time–resolved spectroscopy investigates mechanistic and kinetic details of

The associate editor coordinating the review of this manuscript and approving it for publication was Liang-Bi Chen.

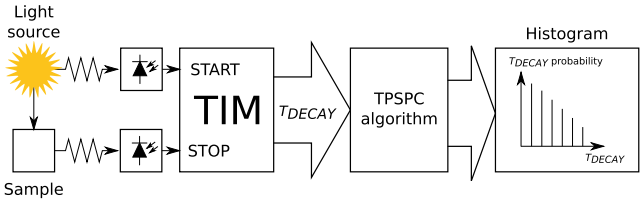


FIGURE 2. Block diagram of a TSCPC measurement setup. As single photon sensitive detector, a Photomultiplier Tube (PMT), Micro Channel Plate (MCP), a Single Photon Avalanche Diode (SPAD) or Hybrid PMT can be used. The STOP events are photons emitted by the decay fluorescence, while START event can be either a fraction of the laser light source or a virtual signal if the periodic laser emission is synchronized with the time measure system (TIM).

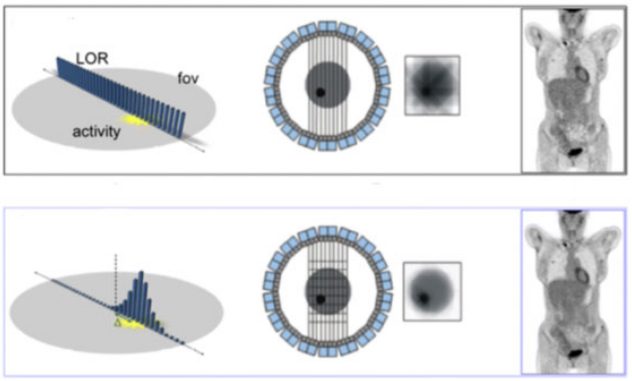


FIGURE 3. Comparison of PET images without measure of the time of arrival of photons to detectors (top) and with these measures performed (bottom). The information of time of arrival translates in a very significantly improved definition of the constructed image.

chemical processes in materials or chemical compounds by means of spectroscopic techniques. Most often, processes are studied after the illumination of a material occurs, but in principle the technique can be applied to any process leading to a change in the properties of a material. By means of pulsed lasers, it is possible to study processes that occur on time scales as short as 10^{-16} s. In particular, time–resolved fluorescence spectroscopy is an extension of fluorescence spectroscopy. Here, the fluorescence of a sample is monitored as a function of time after excitation by a flash of light to record the time decay profile of the signal and, from it, deduce the properties of the material. The time resolution can be obtained in a number of ways, depending on the needed sensitivity and time resolution, (e.g. the Time Correlated Single Photon Counting, TCSPC [12], can achieve resolutions in the range of picoseconds and lower). With periodic excitation, the TCSPC technique extends the data collection over multiple cycles of excitation and emission. In this way, one can reconstruct the fluorescence decay profile from the multitude of single photon events collected over many cycles. The method is based on the repetitive, precisely timed recording of single photons of a fluorescence signal [13, 14]. The reference for the timing is the corresponding excitation pulse. Provided that the probability of recording more than one photon per cycle is kept negligible, the histogram of photon arrivals per time bin represents the time decay (TDECAY) one would have obtained from a ''single shot'' time – resolved recording. A schematic view of the TSCPC operation is depicted in Figure 2.

Many applications need more time measurements performed in parallel. This is, for instance, the case of investigating the temporal correlation between a common trigger event (one START) and the corresponding generated events (multiple STOPs). This mechanism is the basis of one of the most advanced medical imaging tools, the Positron Emission Tomography (PET) [15, 16]. The PET imaging systems construct 3–D medical images by detecting radiation emitted when radioactively substances (tracers) are injected into a patient and are absorbed by tissues with higher levels of activity/metabolism (e.g. active tumors) than the rest of the body. After injection of the tracer compound, the patient is placed within the field of view of a cluster of detectors arranged around the area of the body under examination. The radionuclide decays emitting positrons, which subsequently annihilate on contact with electrons after traveling a short distance (∼1mm) within the body. Each annihilation produces two 511 keV photons (gamma ray range) traveling in opposite direction along the so-called line of response (LOR), and these photons are detected. In first generation PET systems, the read-out electronics of the detectors was able to associate events occurring within a certain time window (time of flight, TOF), and consider them provided by the same annihilation event. Through tomographic elaboration, the lines of corresponding events allowed the construction of images showing the tracer distribution throughout the body of the patient. This is a breakthrough with respect to Computed Tomography (CT), nuclear magnetic resonance (NMR) and X-ray and ultrasound imaging, since provides functional information of tissues and organs. Last generation PET systems add the precise measurement of the time of arrival of the two corresponding photons into the TOF window allowing the localization of the annihilation along the line of response. This corresponds to a dramatic improvement of the constructed image, as in Figure 3.

Traditionally, time measurements are accomplished by means of Time-to-Amplitude Converter (TAC) circuits. The TAC is a mixed–signal circuit that converts the information of interval extent into a voltage level by integrating a voltage ramp on a capacitor for the interval's duration: the final voltage amplitude on the capacitor is proportional to the time interval's duration. Although the TAC approach is the most promising in term of precision, linearity, and resolution, three main drawbacks afflict this technique making it not equipped to handle modern applications [12]. First, the trade-off between resolution and Full-Scale Range (FSR), due to the ramp slope, second the necessity in several modern applications of measuring time events in cascade (''multi-hit'' mode) that is inconceivable with the reset procedure between consecutive measurements of the TAC capacitor and third the design overhead due to the complexity of its mixed-signal structure [13].

The solution to overcome these limits is the Time-to-Digital Converter (TDC) circuit [12]. The TDC uses a fully

digital approach to perform time measurement. In literature a great number of TDC architectures exist [14], the highest performing of which use asynchronous digital structures to quantise the time interval by means of the propagation delay of logic gates. Almost all TDC circuits can be implemented in Application–Specific Integrated Circuit (ASIC) devices (consider for instance ACAM TDCs [15], [16]). One breakthrough is moving the whole TDC into configurable integrated devices based on programmable logic (PL) such as Field Programmable Gate Array (FPGA) [17], [18] and System–on–Chip (SoC) devices [19], greatly improving the system's overall performance and versatility. The variability of systems's operating features, together with the pressing demand forfast–prototyping at low Non–Recursive Engineering (NRE) costs, pushed research towards all–programmable TDCs [20]. The design of high–performance FPGA–based TDCs forces forsaking of traditional synchronous digital design moving to asynchronous architectures processing up to Tera samples per seconds, entering the field of what is known as Terahertz electronics.

We present a consolidated fully FPGA based TDC instrument with state–of–the–art performance of ASIC solutions, with complete programmability of the operating features [21]. The instrument is small, portable, low–price and plug–and–play. It has two channels (START and STOP) plus one input (SYNC) for laser synchronization for instance. The main features are resolution (LSB) of 250 fs over an FSR of some seconds, single shot precision below 10 ps r.m.s. at an acquisition rate of up to 100 Msps, dead–time of less than 5 ns, and differential and integral non–linearity (DNL, INL) below 85 fs and 5.6 ps respectively. Input events coming from detectors (e.g., CDL, SiPM, SPAD, PMT, etc.) are converted into digital pulses by means of a constant fraction discriminator or programmable threshold comparator that are fully processed by the TDC on FPGA [22]–[25].

The instrument killer applications are the test of detectors and the measure of correlation by means of the sync channel. In general, the combination of ease of use with high–performance also makes it an ideal instrument for exploring new ideas and variants of systems containing time measurements quickly and with limited effort. By way of example, Figure 4 shows an application of the instrument in a setup for coincidence measurements.

The claim the proposed design achieves the state-of the-art of both small size and high performance is difficult to support by comparison with existing solutions. In fact, at our knowledge, there are no instruments maximizing both these features contemporary at the same level.

At the state of the art, we can identify two significant similar instruments and consider these as a source of comparison. These are the PicoHarp 300 and the TimeHarp 260 by PicoQuant.

Table 1 allows an at-a-glance comparison of the main characteristics of the different systems. Only the proposed design is reconfigurable, being the only one based on an FPGA device and not an ASIC. A substantial difference is given by the maximum sustainable rate: being able to perform all the processing in FPGA, the proposed system offers a much higher rate without requiring time tagging like the other two solutions. The PicoHarp 300 reaches a precision r.m.s. of the single channel more than 30% but with twenty times greater dead time. The TimeHarp 260 allows to halve the dead time compared to the proposed project but at the expense of the worsening of the r.m.s. of the single channel by more than an order of magnitude.

There are other two-channel instruments with excellent measuring precision, for instance the two-channel time meters of the SPC series by Becker & Hickl. However, these are specific for measurement applications of the time interval defined by the START and STOP signals. Conversely, the systems considered and compared are general purpose, as they measure and assign a timestamp to the START signal and a timestamp to the STOP signal with respect to a reference.

II. THEORETICAL BACKGROUND

Nowadays, an increasing number of time–based experiments [4], [7], [8], [22], [26], [27], require TDCs with higher and higher performance, in terms of resolution [17], [18], precision [28], linearity [18], [29], measuring rate [30], Full-Scale Range (FSR) [21], [31]–[33] and number of channels [34], [35].

In this scenario, two kinds of TDC hardware solutions are available.

In the first solution, the TDC system consists of a standalone TDC in ASIC connected to a digital logic that manages and transmits the measurements to a PC or an embedded monitor system. The ASIC can be mixed–signal or pure–digital [36], which provides more channels at higher measure rate but lower precision respect to the mixed–signal one [37].

The second available solution has the TDC system fully embedded in a configurable device, which can be an FPGA or an SoC. First of all, there are all the benefits associated with the programmability of the host device, from total versatility of the implementable architecture to the absence of significant NRE costs, which make this solution the main way for prototyping or creating systems in small–scale production. To be sure, the ASIC solution traditionally performed better than programmable logic implementations. But if this gap was significant in the past, today it can be said to be negligible if not non–existent for most applications [7].

The proposed instrument belongs to the second category and is state-of-the-art as regards configurability and performance-cost ratio.

In modern applications, one of the main merits in favour of high–performance TDCs is certainly their resolution, which is now required to be in the order of ps, which corresponds to clock frequencies of hundreds of GHz. This is obviously not possible in an FPGA device, which requires the use of architectural choices that involve using the device in asynchronous mode. The most promising solutions are based on the Tapped Delay–Line (TDL) implemented using the carry chain logic

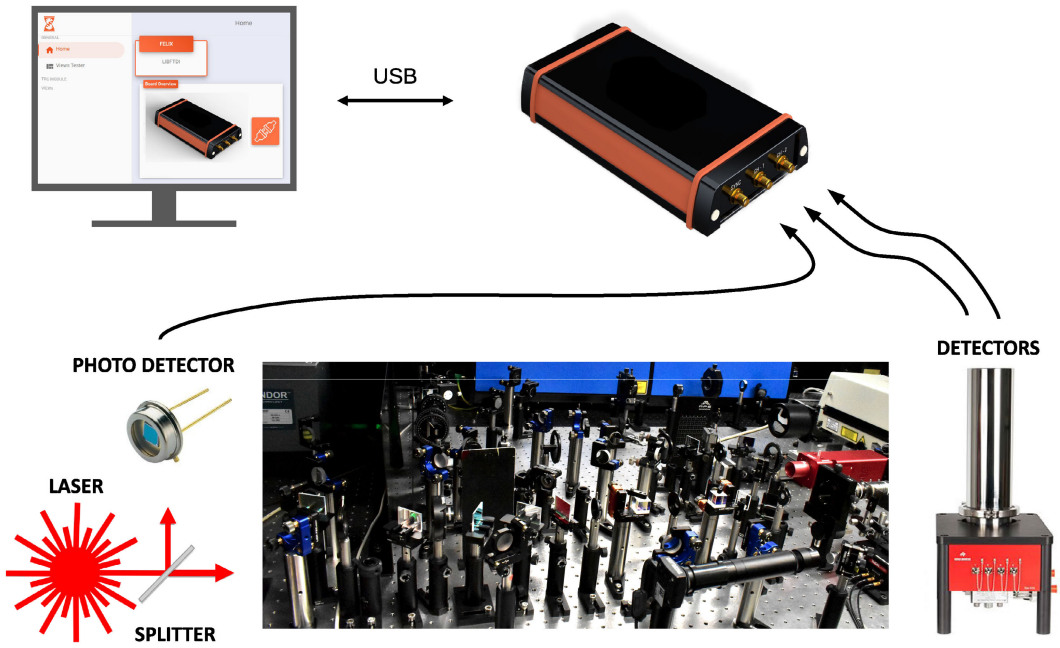


FIGURE 4. Graphical representation of the instrument in a setup for coincidence measurements. The beam coming from a laser source through a splitter is sent in parallel to the SYNC input of the presented instrument through a photo-detector and to the setup on which to perform the measure for checking the coincidence between the two possible emissions resulting from excitation. Two detectors catch these emissions and have their respective outputs connected to the inputs of the instrument, which calculates the timestamps of the laser source (cause) and of the detector outputs (effects). The instrument performs the processing of interest, in this case the check of the coincidence between detected events corresponding to the same laser pulse. However, other investigations could be possible, for instance the calculation of the statistical frequency between causes and effects on a histogram. The role of the PC is exclusively to display the results of the processing.

TABLE 1. Synoptic view comparing the main features of the proposed design and two similar systems at the state of the art. Legend of measure units: ns = 10^{-9} sec; ps = 10^{-12} sec; fs = 10^{-15} sec; Msps stands for Millions of samples per second.

Feature	Proposed design	PicoHarp 300	TimeHarp 260
Technology	FPGA	ASIC	ASIC
Reconfigurability	Yes	No	No
Number of channels	2	2	2
Full–Scale Range	Extendable via software	Extendable via software	Extendable via software
Maximum measurement rate	100 Msps (no time tagging)	10 Msps	40 Msps
Minimum dead time	5 ns	95 ns	25–2 ns
Channel precision	12 ps r.m.s.	8,5 ps r.m.s.	14-180 ps r.m.s.
Plug&play	Yes	No	No

available in the FPGA fabric [38]. In this case, the resolution is a function of the propagation delay associated with the taps that make up the TDL [39]. The resulting TDC is referred as a TDL–TDC.

The TDL consists of a chain of D flip-flops and in parallel a chain of buffers (belonging to the device's carry–chain resource), each with known propagation time t_p [20]. The TDL converts an interval limited by two time markers into a number [40]. With reference to Fig. 5, the starting marker (for instance a logic transition 0 to 1) serially propagates along the sequence of buffers, whose outputs are inputs of the flip–flops. The flip–flops clock is the line in which the marker ending the interval (for instance again a logic transition 0 to 1) occurs. In this way, the flip–flop chain simultaneously captures the output status of all buffers, returning a sequence of 1s of length proportional to the duration of the time interval being measured as output [41]. Since N is the number of buffers, the resolution (LSB) and the maximum FSR are

$$LSB = t_p \tag{1}$$

$$FSR = N \cdot t_p \tag{2}$$

In the conventional synchronous use of the FPGA device, the propagation delay of the buffers that make up the carry propagation chain in the sum operations is not a parameter whose value needs control. So the buffers have similar delays but absolutely not equal to each other and also the layout of the chain of these buffers helps to make them different. This has a negative impact on resolutions and linearity. To solve the problem, interpolation [38], [42]–[44] and calibration [45], [46] are mandatory. The interpolation compensates for the poor native resolution, and calibration guarantees the linearity. Wide FSR is nowadays a primary requirement for several

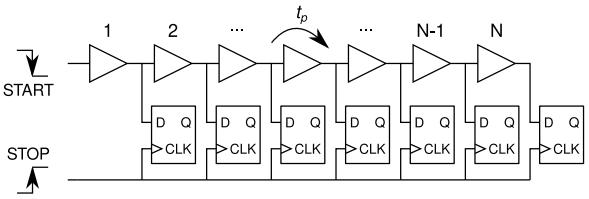


FIGURE 5. TDL-TDC structure where the markers defining the interval being measured are named START and STOP. The length of the interval is read as a sequence of 1s at the outputs Q of the flip-flops.

core applications of TDCs (such as 3D imaging and time–of–flight measures as LIDAR systems [8], [47], [48]). But, since high–resolution forces low LSB and the number of buffers is structurally limited in the device, the FSR according with (1) and (2) cannot be directly extended as much as you would like. The issue of its extension can be solved by implementing the Nutt interpolation [49] that makes it possible to extend the FSR up to several seconds.

In the wake of this theoretical outline, the instrument presented was made with main features recapped in Table 2.

TABLE 2. Presented instrument's main features. Legend of measure units: ns = 10^{-9} sec; ps = 10^{-12} sec; fs = 10^{-15} sec; Msps stands for Millions of samples per second.

Feature	Value
Hardware Full–Scale Range	614.4ns
Resolution (LSB)	37 fs
Maximum Measurement Rate	100 Msps
Minimum Dead–Time	5 ns
Precision	<12.5ps r.m.s.
Absolute DNL	<380 fs
Absolute INL	<16 ps

III. THE INSTRUMENT

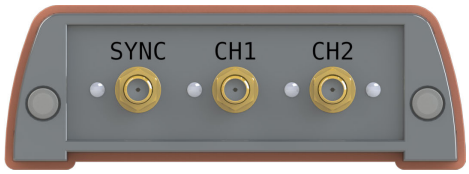
The instrument, a picture of which is shown in Figures 6a and 6b, consists of a hardware substrate based on an FPGA device (Figure 7) that hosts the firmware implementing the TDL–TDC, in line with what is described in Section II, and software for interfacing with the external environment, consisting of a PC for example.

The instrument's connection gates are CH1, CH2, SYNC channels (Figure 6a) and a USB port with a communication and power supply function (Figure 6b).

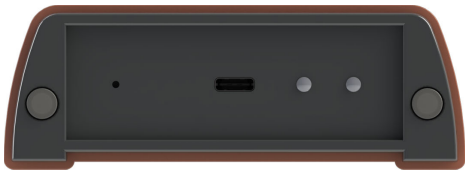
Inside, the FPGA device is a 28 nm Xilinx Artix-7 on which, in addition to the main core that implements the TDL–TDC, ancillary processing modules are placed, organized in the form of IP–Cores. The software consists of plug–ins, one for each kind of processing done by the firmware. In this way, the user can customize the instrument with maximum flexibility adding their own IP–Cores and the related software plug–ins. Figure 8 shows a synoptic diagram of the instrument's architecture, highlighting the hardware, firmware and software parts with the relative connections.

A. HARDWARE

The hardware consists of a 200 mm x 100 mm Printed Circuit Board (PCB) partitioned into three regions, analog, digital, and power region (Figure 9). Note how the analog front-end



(a) Front panel.



(b) Back panel.

FIGURE 6. Picture of the instrument.

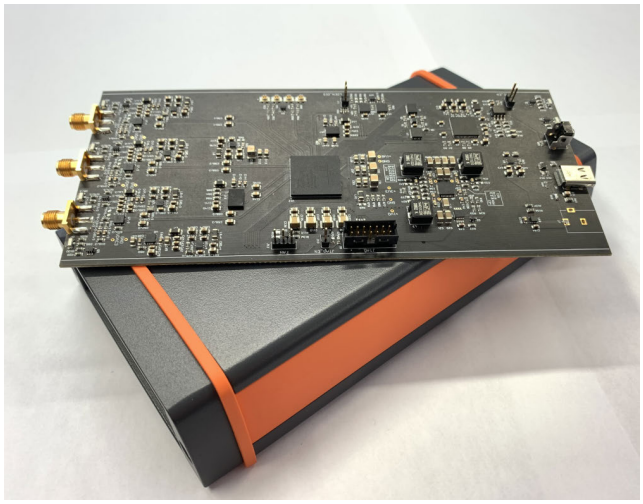


FIGURE 7. Instrument hardware substrate.

and the FPGA device are on the same board, avoiding the use of connectors between the analog and digital sections.

1) ANALOG SECTION

On entering the instrument via the input channel gates, the first section you encounter is the analog front-end. CH1, CH2 and SYNC are each DC coupled with the input of a comparator (Analog Devices AD8465 [50]) whose threshold is regulated by a Digital–to–Analog Converter (DAC) (Analog Devices AD5694R [50]). The threshold voltage level can be set in the range 0–2.5 V in 4096 steps of 0.61 mV by means an I2C bus driven by the FPGA [18], [24]. This stage acts as a threshold discriminator converting the analog input pulses (0–3.3V) into Low Voltage Differential Signals (LVDS) with a timing jitter of less than 7 ps r.m.s. Since it is located on the same board as the digital region, great attention has been paid to signal integrity from the comparators to the FPGA by acting on the signal transmission method and on the layout of the lines (Figure 10) [51]–[54].

The analog region also hosts a high–performance oscillator (Texas Instruments LMK61E2BBA-SIAT [55]) used for clocking the synchronous parts of the TDC.

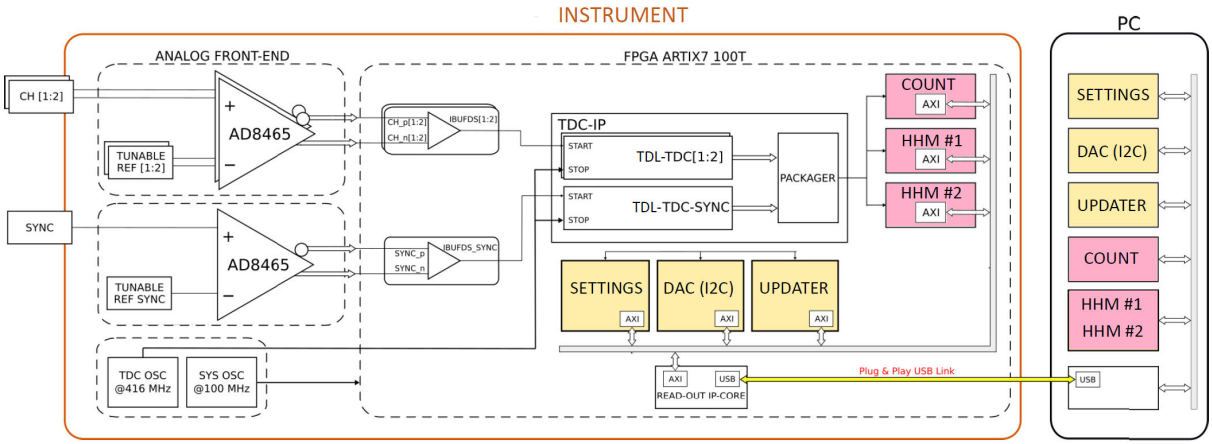


FIGURE 8. Schematic description of the architecture that constitutes the instrument in the hardware, firmware and software components. The parts, both firmware and software, that the user can freely program to best adapt the instrument to his operational needs are highlighted in yellow.

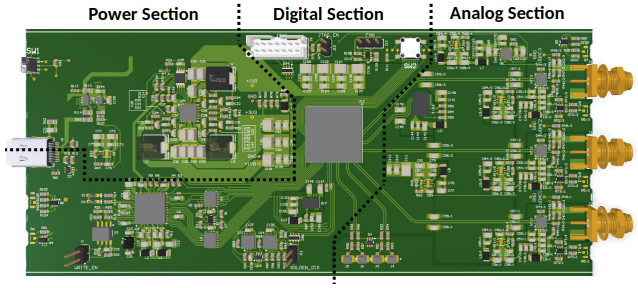


FIGURE 9. Layout of the PCB pointing out analog, digital and power regions.

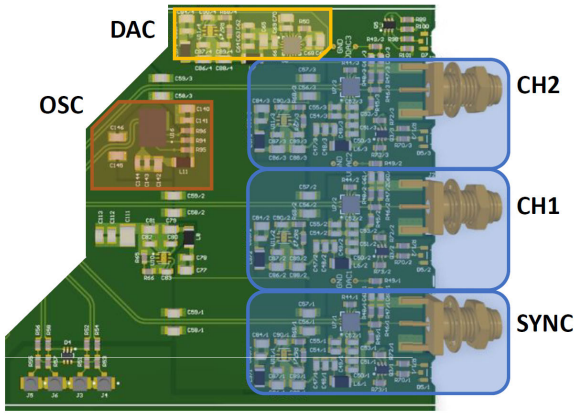


FIGURE 10. Isolation layout detail.

Besides giving the system compactness and high–performance, the single PCB introduces great challenges of signal integrity. In fact, if a solid reference plane for the connection lines from the analog stage to FPGA guarantees less interference due to cross-talk, it also eliminates the separation of ground planes, that ensures proper isolation between the analog and digital parts. Without introducing other layers to remedy the problem, a solution which, as is well known,

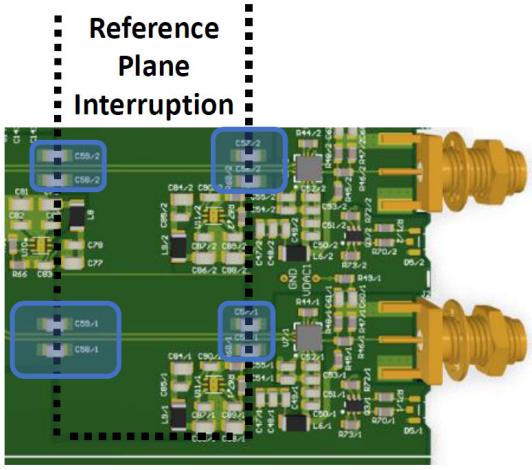


FIGURE 11. Layout detail of the reference plane stitching capacitors.

is partial in any case, we have opted for partitioning the reference in different planes for analog and digital parts, but connecting them in proximity to the crossing lines that pass from one to the other with stitching capacitors [51]–[54], [56], to guarantee an adequate return path for signal currents circulating on the differential pairs (Figure 11).

Obviously, maximum attention was also given to observing all the rules for optimizing signal integrity in differential transmission [56].

2) DIGITAL SECTION

The digital region is the most dense in terms of devices, of which the main are the FPGA as the processing core, the FT2232 [57] that is in charge of connecting the FPGA to the outside via USB 2.0 at 40 MB/s, and a QSPI FLASH memory S25FL064L [58] that stores the firmware's bitstream. Proper decoupling techniques are implemented to minimize the ground bounce noise generation due to the switching activity of the digital devices.

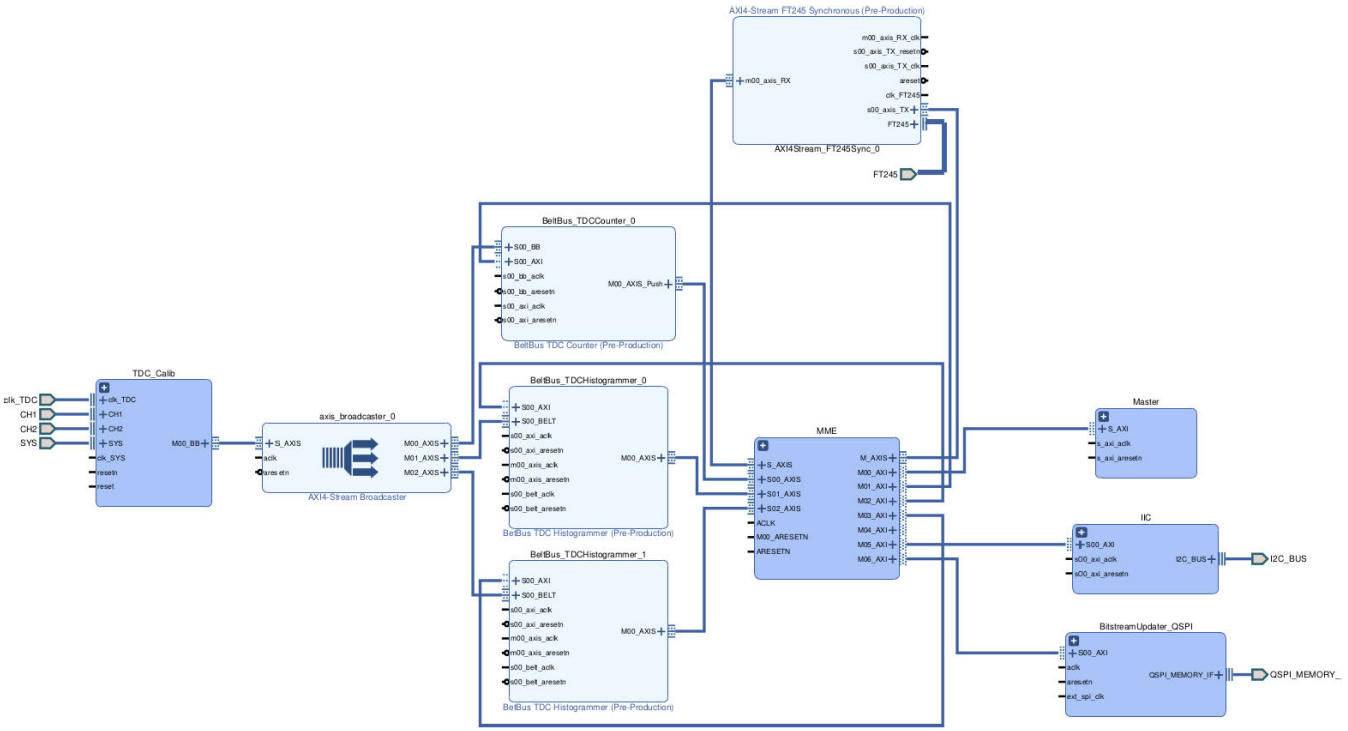


FIGURE 12. Block design of the firmware (clocks and resets are left unconnected to make the picture clearer).

3) POWER SECTION

The power section hosts the DC/DC converters and the LDOs powering the instrument's components. The power comes from the USB gate that provides 5V with a maximum power budget of 2.5W due to the 500 mA maximum current available in the USB 2.0 protocol [59]. To minimise the power noise, the analog section and the bank of the FPGA used for TDC inputs are powered by means of low noise LDOs.

B. FIRMWARE

The firmware hosted in the FPGA is realised in the Xilinx's Vivado 2020.2 suite [60] and it is organized as a collection of IP–Cores. Figure 12 shows the block design of the whole firmware portion, according to the synoptic visual of the system in Figure 8.

The firmware is composed of several cores, 7 of which are the main ones, i.e. the TDC, the Memory Management Engine, the FT245–Sync, the Hardware Histogram Maker (HHM), the count–meter, the I2C master, and the bit-stream updater.

The firmware makes it possible to generate 2 histograms of the timestamps in real–time up to 100 Msps simultaneously.

1) FT245–SYNC CORE

The FT245–Sync is the IP–Core that connects the FPGA to the FT2232 device, which converts the USB 2.0 standard into an 8–bit data–wide bidirectional synchronous bus (FT245 protocol). The core converts this FT245 into two different Advanced eXtensible Interface 4 Streams (AXIS) [61], one in input and one in output, compatible with the FPGA architecture.

2) TIME–TO–DIGITAL CONVERTER CORE

The TDC has the 3 independent channels CH1, CH2 and SYNC. Each channel converts the incoming external event into a 24–bit timestamp (with LSB of 37 fs) following the AXIS standard. Furthermore, to reduce routing complexity, these 24–bit AXIS channels are merged in a single 32–bit wide one (Figure 13). The 8 additional bits are used to insert the channel number and to flag an incoming overflow. This AXIS stream is sent in broadcast to all the cores that perform timestamp processing.

3) MEMORY MANAGEMENT ENGINE CORE

The Memory Management Engine IP–Core (MME) converts the input and output AXIS coming from the FT245–Sync into many ''address oriented'' Advanced eXtensible Interfaces 4 (AXI4) [62]. In this manner each core hosted in the firmware has its own dedicated address space, and can communicate to the outside using an AXI4 interface. The AXI4 cores are connected to the MME by means of an AXI4 and AXIS interconnect provided by Xilinx.

4) COUNT–METER CORE

The count–meter is connected by means of AXIS to the TDC output and to the MME via AXI4. It is in charge of measuring the rate of the concurrency in each channel.

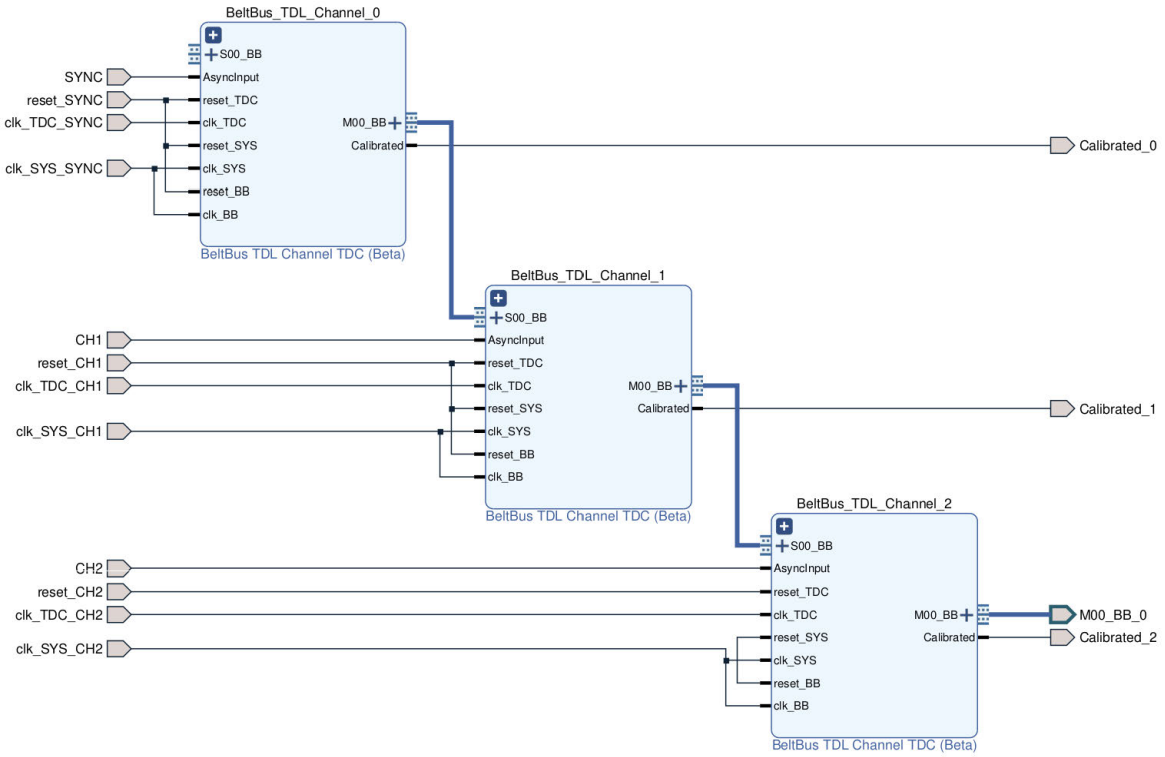


FIGURE 13. Graphical representation of the TDC IP–Core.

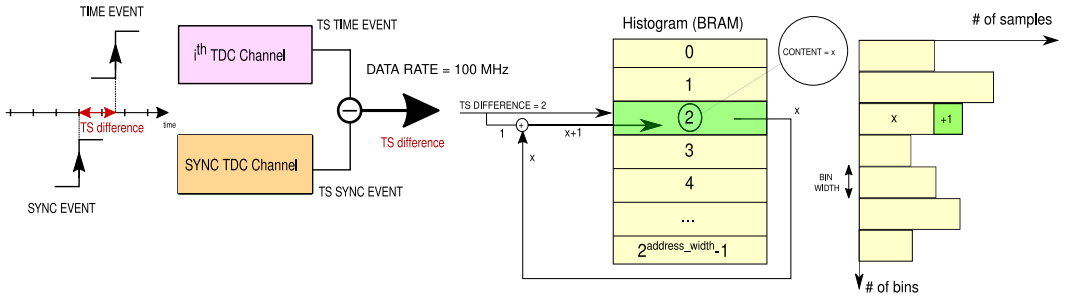


FIGURE 14. Scheme of structure and operation of the HHM core.

5) HARDWARE HISTOGRAM MAKER CORE

The Hardware Histogram Maker (HHM) is connected by means of AXIS to the TDC output and to the MME via AXI4. It generates the histogram of the programmable difference of the timestamps coming from two different channels (e.g. CH1-SYNC, CH2-SYNC, CH1-CH2, etc.). In the firmware, a couple of HHM cores are present, allowing the generation of two histograms in parallel and in real-time up to 100 Msps. Histograms are stored in BRAM, as can be seen in the diagram in Figure 14.

The user can program the HHM for adjusting the bin–width down to the minimum value that corresponds to the TDC's LSB, i.e. 37 fs, and the full-scale dynamic range (FSR) up to 10.3s.

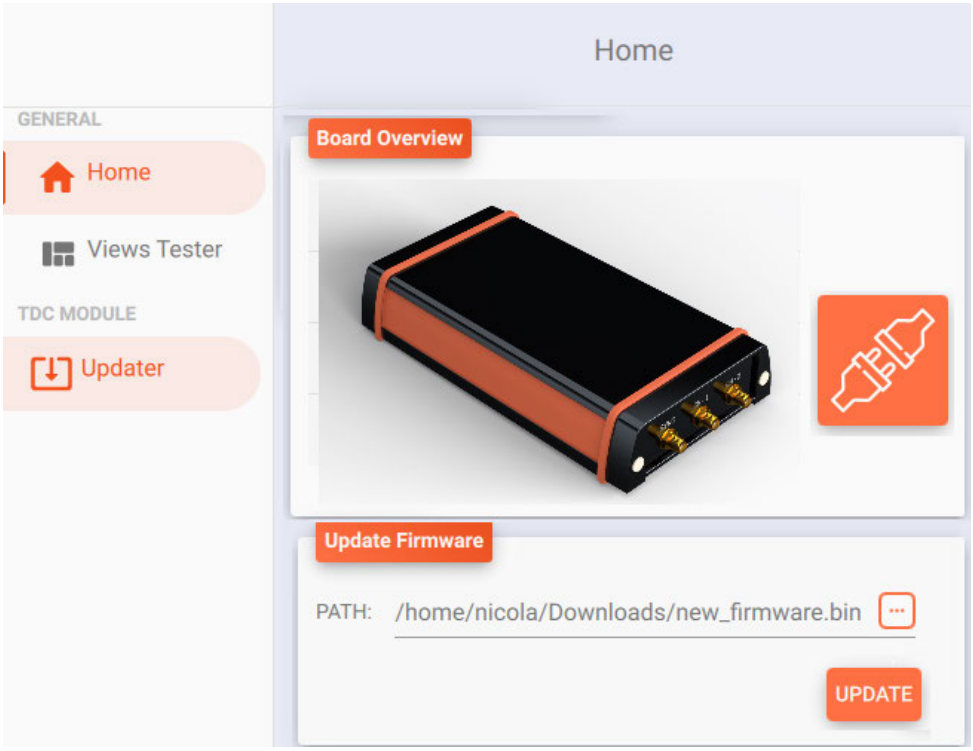
6) I2C MASTER CORE

The I2C Master manages the I2C bus configuring the DACs that set the threshold for input discriminators (Paragraph III-A, Analog section description).

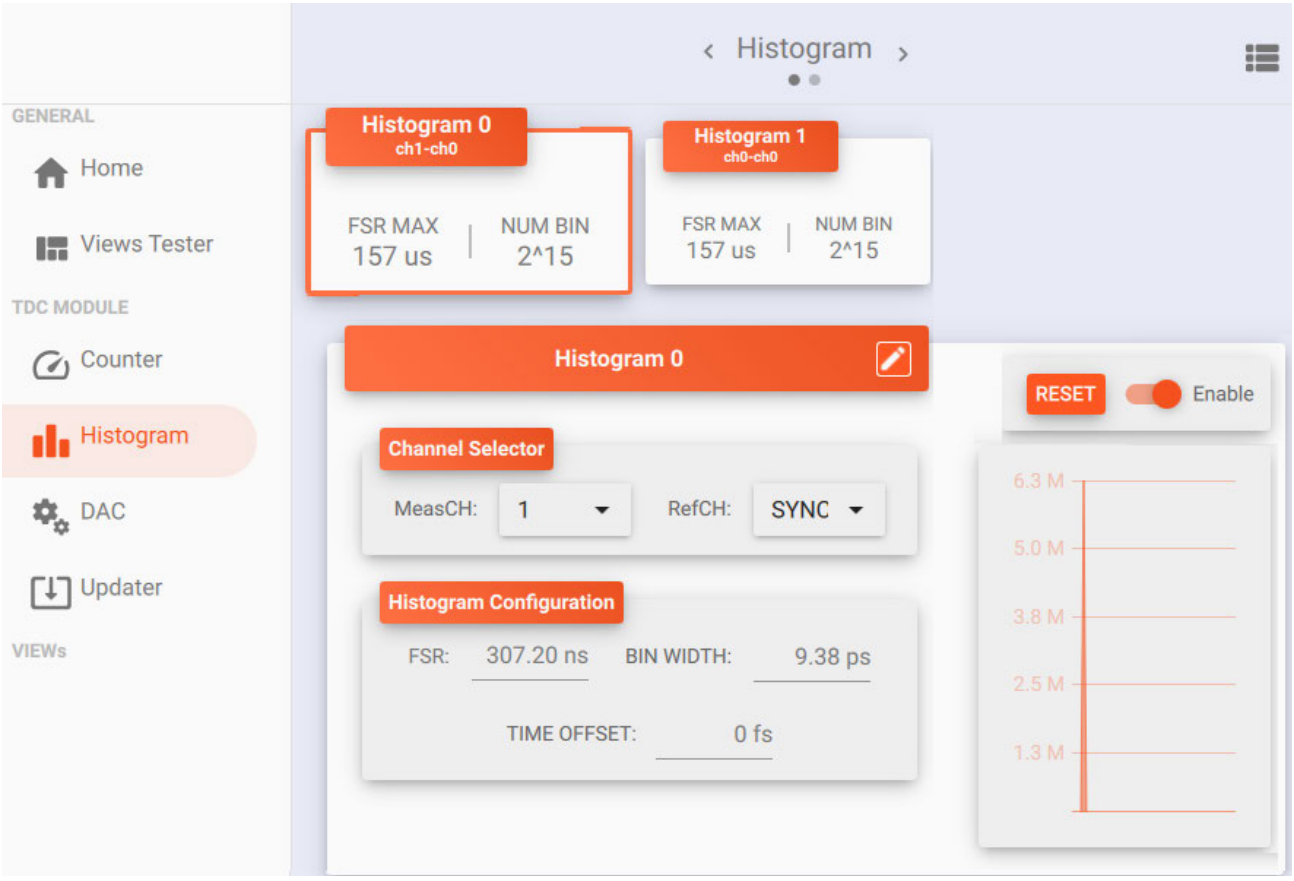
7) BITSTREAM UPDATER CORE

The bit-stream of the FPGA is hosted in an external QSPI memory (Paragraph III-A, Digital section description) and, at power on, it is loaded in the FPGA. The bit-stream updater allows the user to change the bit-stream stored in the QSPI for update orany need for modification in general.

In order to prevent any fatal corruption of the system, during the update phase, a portion of the FLASH memory

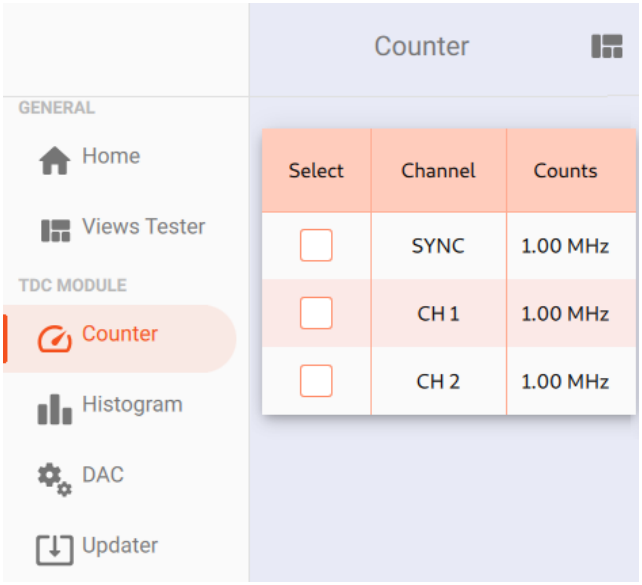


(a) Home and Bitstream updater.

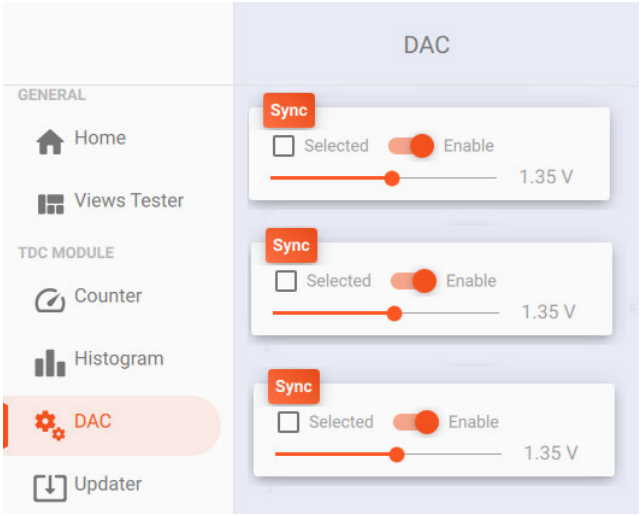


(b) Hardware Histogram Maker.

FIGURE 15. Screenshots of the GUI software in different operating steps.



(a) Counter–Meter.



(b) DAC Settings.

FIGURE 16. Screenshots of the GUI software in different operating steps.

is reserved as read-only memory (ROM) and hosts recovery firmware.

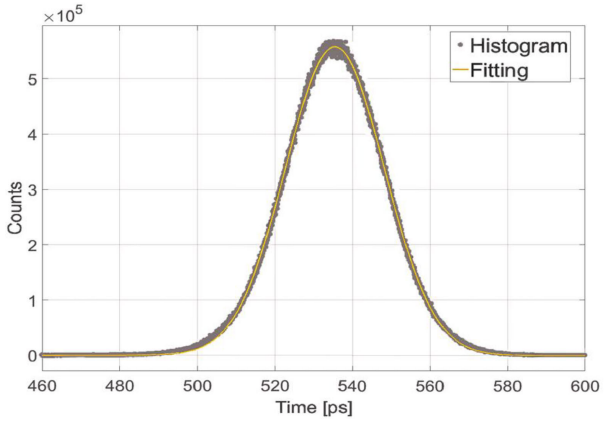
C. SOFTWARE

The software is designed in the image of the firmware following the plug-in philosophy. In fact, each core implemented has its own software plug-in that allows it to be managed, and the results of the processing carried out to be visible. Each plug-in consists of two parts, the back end and the front end.

The back end is the data access layer written in C++ to maximise system performance, in terms of both data processing and transfer. The back end of each module has all the classes and functions required for timestamp processing.

The front-end, i.e. the presentation layer, is written in Qt and implements the GUI (Graphical User Interface). It is not an essential part of the software, since it can be replaced if, for instance, the user wants to drive the instrument using the console or Python bindings.

Figures 15 and 16 show some GUI screenshots of the instrument.



(a) Data fitting in MATLAB.

(b) Screenshot from the GUI software.

FIGURE 17. Gaussian distribution of measurements of the same time interval. The histogram bin is set to 4.68 ps.

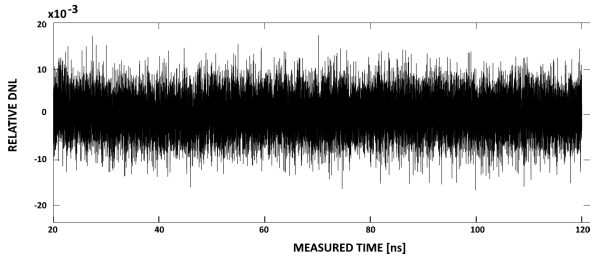


FIGURE 18. Relative DNL curve (the histogram bin is set to 4.68 ps) between two of the instrument's channels.

IV. EXPERIMENTAL TESTS

The instrument has been engineered and tested, validating all its functions, with tests both in the laboratory and in specific application environments.

TABLE 3. Absolute and relative resources usage expressed in terms of look-up tables (LUTs), flip-flops (FFs), and block random access memory (BRAM).

IP-Core	LUT	FF	BRAM
TDC	8497	12649	4.5
MME	4720	4185	14.5
FT245–Sync	319	627	1
Count–Meter	258	564	0
HHM	954	1202	40
I2C Master	1085	658	0
Bitstrean Updater	1460	1363	0
Ancillary IPs	2413	417	3

(a) Absolute resources usage.

IP-Core	LUT%	FF%	BRAM%
TDC	13.4	10	3
MME	7.5	3.3	9.7
FT245–Sync	0.5	0.5	0.7
Count–Meter	0.4	564	0
HHM	1.5	0.4	27
I2C Master	1.7	0.5	0
Bitstrean Updater	2.3	1.1	0
Ancillary IPs	3.8	0.33	2

(b) Relative resources usage.

A. PRECISION TEST

The precision test consists of calculating the standard deviation of the distribution obtained considering multiple measurements of the same time interval. This test returned very good results, showing a Gaussian distribution of the measurements with Full Width Half Maximum (FWHM) equal to 22.1 ps, that means standard deviation of 9.4 ps r.m.s. ($\sigma \approx \frac{FWHM}{2.355}$). The result was found to be consistent for all combination pairs of the three channels. Figure 17 shows the plot of one of the Gaussian distributions measured.

B. LINEARITY TEST

The linearity can be investigated by taking a statistically significant number of measurements of the time intervals of randomly distributed extent and looking at deviations from the expected uniform distribution of the measurements. Deviations are qualitative and quantitative indicators of the non-linearity of the instrument. This is referred to as the code-density test [63]. In this way, the differential (DNL) and integral (INL) non-linearity curves were calculated. Due to the symmetry of the PCB and of the firmware, the DNL and INL curves computed between each couple of channels have same characteristics. For this reason only a couple of DNL and INL plots are shown in Figures 18 and 19.

The DNL is computed by means of a code–density test binned at 4.68 ps between two uncorrelated events. We can observe a relative (referred to 4.68 ps) DNL in the range of $[-1.6\% \div +1.8\%]$ that means an absolute value in the range of $[-75fs \div +85fs]$.

For further verification of the correct functioning of the system, the relative INL curve was calculated (considering the same bin–width of 4.68 ps) by integrating the relative DNL curve. The result is shown in Figure 19. This relative INL error represents the distortion in linearity not compensated for by the calibration mechanism implemented. As you can see the relative (refereed to 4.68 ps) INL is in the range of $[-0.5\% \div +1.2\%]$ that means absolute error in the range of $[-2.3ps \div +5.6ps]$.

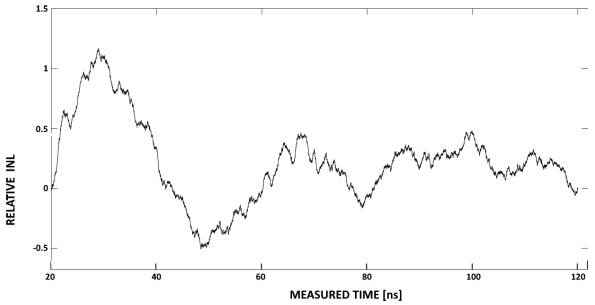


FIGURE 19. Relative INL curve (the histogram bin is set to 4.68 ps) between two of the instrument's channels.

C. RESOURCES USAGE

Table 3 shows the absolute and relative resources usage of the Artix–7 100T FPGA device (XC7A100T) that counts 63400 LUTs, 126800 FFs, and 150 BRAM.

As you can see, the default firmware reserves 19706 LUTs (31.08%), 24665 FFs (19.5%) and 103 BRAMs (69%), while the remaining resources of 43694 LUTs (68.91%), 102135 FFs (80.5%) and 47 BRAMs (31%) are free and available for the user to instantiate custom cores. Furthermore, if more resources are required, it is possible to reduce the dimension of the HHMs or even remove both the HHMs and the count–meter. In this way, the user–available resources go up to 45860 LUTs (72.33%), 105103 FFs (82.9%) and 127 BRAMs (84.7%).

V. CONCLUSION

A fully engineered and tested instrument is proposed for measuring time intervals using the TDC technique.

Its main features are being small, portable, high–performance and fully programmable. It has three independent channels able to signal timestamps with a resolution of 35 fs and precision below 12 ps r.m.s. at an acquisition rate of up to 100 Msps with a dead–time of less than 5 ns for each channel.

Fine interpolation and calibration procedures are implemented providing differential and integral non–Linearity (DNL, INL) lower than 85 fs and 5.6 ps respectively.

The core of the instrument is a Tapped Delay–Line TDC implemented as an IP–Core in a Xilinx Artix 7 100T FPGA device.

The software associated with the instrument is designed in the image of the firmware following the plug-in philosophy.

In addition to the programmability of the instrument's intrinsic functionalities, the user has the possibility of eventually inserting theirs own procedures in the processing flow as cores to be implemented on the FPGA device.

ACKNOWLEDGMENT

The authors thank Dr. Christophe Galland for his precious collaboration in the experimental evaluation of the instrument.

REFERENCES

[1] M. Cardinali *et al.*, "Frontend electronics for high-precision single photo-electron timing using FPGA-TDCs," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 766, pp. 231–234, Dec. 2014. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0168900214004847

[2] K. Akiba *et al.*, "The Timepix Telescope for high performance particle tracking," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 723, pp. 47–54, Sep. 2013. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0168900213004816

[3] W. Becker, *Advanced Time-Correlated Single Photon Counting Techniques*. Berlin, Germany: Springer, 2005.

[4] R. J. Cotter, "Time-of-flight mass spectrometry for the structural analysis of biological molecules," *Anal. Chem.*, vol. 64, no. 21, pp. 1027A–1039A, Nov. 1992.

[5] D. V. O. D. Phillips, *Time-Correlated Single Photon Counting*. London, U.K.: Academic, 1984.

[6] J. Wu, "An FPGA wave union TDC for time-of-flight applications," in *Proc. IEEE NSS/MIC*, Orlando, FL, USA, Nov. 2009, pp. 299–304.

[7] E. Venialgo, N. Lusardi, F. Garzetti, A. Geraci, S. E. Brunner, D. R. Schaart, and E. Charbon, "Toward a full-flexible and fast-prototyping TOF-PET block detector based on TDC-on-FPGA," *IEEE Trans. Radiat. Plasma Med. Sci.*, vol. 3, no. 5, pp. 538–548, Sep. 2019.

[8] R. Lussana, F. Villa, A. D. Mora, D. Contini, A. Tosi, and F. Zappa, "Enhanced single-photon time-of-flight 3D ranging," *Opt. Exp.*, vol. 23, no. 19, pp. 24962–24973, Sep. 2015. [Online]. Available: http://www.opticsexpress.org/abstract.cfm?URI=oe-23-19-24962

[9] N. Lusardi, A. Geraci, R. B. M. Gourgues, J. W. N. Los, and G. Bulgarini, "Array of superconducting nanowire single photon detectors resolving the number of photons in a weak optical pulse," in *Proc. IEEE Nucl. Sci. Symp., Med. Imag. Conf. Room-Temp. Semiconductor Detect. Workshop (NSS/MIC/RTSD)*, Oct. 2016, pp. 1–4.

[10] F. Garzetti, N. Lusardi, A. Geraci, E. Dobovicnik, G. Cautero, C. Dri, R. Sergo, and L. Stebel, "Fully FPGA-based and all-reconfigurable TDC for 3D (X, y, t) cross delay-line detectors," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Nov. 2018, pp. 1–3.

[11] J. Nissinen, I. Nissinen, and J. Kostamovaara, "Integrated receiver including both receiver channel and TDC for a pulsed time-of-flight laser rangefinder with cm-level accuracy," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1486–1497, May 2009.

[12] D. Vyhlidal and M. Cech, "Time-to-digital converter with 2.1-ps RMS single-shot precision and subpicosecond long-term and temperature stability," *IEEE Trans. Instrum. Meas.*, vol. 65, no. 2, pp. 328–335, Feb. 2016.

[13] S. H. Hall and H. L. Heck, *Advanced Signal Integrity for High-Speed Digital Designs*. Hoboken, NJ, USA: Wiley, 2009.

[14] R. Machado, J. Cabral, and F. S. Alves, "Recent developments and challenges in FPGA-based time-to-digital converters," *IEEE Trans. Instrum. Meas.*, vol. 68, no. 11, pp. 4205–4221, Nov. 2019.

[15] Z.-h. Ma and M. Li, "Research on pulse hand-held laser rangefinder based TDC-GP2," in *Proc. 2nd Int. Conf. Comput. Eng. Technol.*, Apr. 2010, pp. V6-670–V6-672.

[16] L. Stebel, M. Malvestuto, V. Capogrosso, P. Sigalotti, B. Ressel, F. Bondino, E. Magnano, G. Cautero, and F. Parmigiani, "Time-resolved soft X-ray absorption setup using multi-bunch operation modes at synchrotrons," *Rev. Sci. Instrum.*, vol. 82, no. 12, Dec. 2011, Art. no. 123109.

[17] N. Lusardi, F. Garzetti, and A. Geraci, "Fully programmable system for multi-channel experiments targeting to time measurement at high performance," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Oct. 2017, pp. 1–5.

[18] F. Garzetti, N. Lusardi, and A. Geraci, "All-digital fully-configurable instrument for multi-channel time measurements at high performance," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Nov. 2018, pp. 1–5.

[19] N. Corna, F. Garzetti, N. Lusardi, and A. Geraci, "Complete system-on-chip linux-based platform for measurement and generation of time domain signals," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Oct. 2019, pp. 1–3.

[20] F. Caponio, A. Abba, N. Lusardi, and A. Geraci, "A high-precision wave union TDC implementation in FPGA," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Nov. 2013, pp. 1–4.

[21] N. Lusardi, F. Garzetti, A. Geraci, J. Marjanovic, and M. Gustin, "Multi-channel time-to-digital converter for MTCA.4 standard in FPGA," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Oct. 2017, pp. 1–4.

[22] F. Garzetti, S. Salgaro, E. Venialgo, N. Lusardi, N. Corna, A. Geraci, and E. Charbon, "Plug-and-play TOF-PET module readout based on TDC-on-FPGA and gigabit optical fiber network," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Oct. 2019, pp. 1–4.

[23] N. Lusardi, F. Garzetti, A. Geraci, G. Cautero, C. Dri, P. Pittana, R. Sergo, and L. Stebel, "Development of fully FPGA-based 3D (X, Y, t) detection systems using multi-channel tapped-delay-line time-to-digital converter with cross delay-line detectors," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Oct. 2017, pp. 1–4.

[24] N. Lusardi, F. Garzetti, and A. Geraci, "Digital instrument with configurable hardware and firmware for multi-channel time measures," *Rev. Sci. Instrum.*, vol. 90, no. 5, May 2019, Art. no. 055113, doi: 10.1063/1.5028131.

[25] N. Lusardi, F. Garzetti, N. Corna, R. D. Marco, and A. Geraci, "Very high-performance 24-channels time-to-digital converter in Xilinx 20-nm kintex UltraScale FPGA," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Oct. 2019, pp. 1–4.

[26] P. O'Keeffe, P. Bolognesi, M. Coreno, A. Moise, R. Richter, G. Cautero, L. Stebel, R. Sergo, L. Pravica, Y. Ovcharenko, and L. Avaldi, "A photoelectron velocity map imaging spectrometer for experiments combining synchrotron and laser radiations," *Rev. Sci. Instrum.*, vol. 82, no. 3, Mar. 2011, Art. no. 033109.

[27] N. Lusardi, J. W. N. Los, R. B. M. Gourgues, G. Bulgarini, and A. Geraci, "Photon counting with photon number resolution through superconducting nanowires coupled to a multi-channel TDC in FPGA," *Rev. Sci. Instrum.*, vol. 88, no. 3, Mar. 2017, Art. no. 035003, doi: 10.1063/1.4977594.

[28] X. Qin, L. Wang, D. Liu, Y. Zhao, X. Rong, and J. Du, "A 1.15-ps bin size and 3.5-ps single-shot precision time-to-digital converter with on-board offset correction in an FPGA," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 12, pp. 2951–2957, Dec. 2017.

[29] H. Chen and D. D.-U. Li, "Multichannel, low nonlinearity time-to-digital converters based on 20 and 28 nm FPGAs," *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 3265–3274, Apr. 2019.

[30] X. Qin, W. Zhang, L. Wang, Y. Zhao, Y. Tong, X. Rong, and J. Du, "An FPGA-based hardware platform for the control of spin-based quantum systems," *IEEE Trans. Instrum. Meas.*, vol. 69, no. 4, pp. 1127–1139, Apr. 2020.

[31] N. Lusardi, F. Garzetti, M. A. Cibin, R. Sury, and A. Geraci, "Hardware and software co-design of a system-on-chip for real-time bidirectional transfer and processing of data from a time-to-digital converter," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Oct. 2017, pp. 1–6.

[32] N. Corna, F. Garzetti, N. Lusardi, and A. Geraci, "System-on-chip linux-based platform for high-performance time-to-digital conversion," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Nov. 2018, pp. 1–4.

[33] N. Lusardi, A. Geraci, J. Marjanovic, and M. Gustin, "High-resolution TDL-TDC system for MTCA.4 standard," in *Proc. IEEE Nucl. Sci. Symp., Med. Imag. Conf. Room-Temp. Semiconductor Detect. Workshop (NSS/MIC/RTSD)*, Oct. 2016, pp. 1–4.

[34] C. Liu and Y. Wang, "A 128-channel, 710 M samples/second, and less than 10 ps RMS resolution time-to-digital converter implemented in a Kintex-7 FPGA," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 3, pp. 773–783, Jun. 2015.

[35] S. Mandai and E. Charbon, "A 128-channel, 9ps column-parallel two-stage TDC based on time difference amplification for time-resolved imaging," in *Proc. ESSCIRC (ESSCIRC)*, Sep. 2011, pp. 119–122.

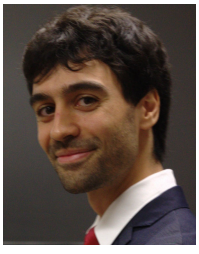
[36] F. Yuan, *CMOS Time-Mode Circuits and Systems*, B. Raton, Ed. Boca Raton, FL, USA: CRC Press, 2016.

[37] A. Kirichenko, S. Sarwana, D. Gupta, I. Rochwarger, and O. Mukhanov, "Multi-channel time digitizing systems," *IEEE Trans. Appl. Supercond.*, vol. 13, no. 2, pp. 454–458, Jun. 2003.

[38] N. Lusardi, F. Garzetti, and A. Geraci, "The role of sub-interpolation for delay-line time-to-digital converters in FPGA devices," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 916, pp. 204–214, Feb. 2019. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0168900218317479

[39] N. Lusardi, A. Abba, F. Caponio, and A. Geraci, "Quantization noise in non-homogeneous calibration table of a TCD implemented in FPGA," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Nov. 2014, pp. 1–5.

[40] Z. Jaworski, "Verilog HDL model based thermometer-to-binary encoder with bubble error correction," in *Proc. MIXDES 23rd Int. Conf. Mixed Design Integr. Circuits Syst.*, Jun. 2016, pp. 249–254.
[41] J. Y. Won and J. S. Lee, "Time-to-digital converter using a tuned-delay line evaluated in 28-, 40-, and 45-nm FPGAs," *IEEE Trans. Instrum. Meas.*, vol. 65, no. 7, pp. 1678–1689, Jul. 2016.
[42] E. Bayer, P. Zipf, and M. Traxler, "A multichannel high-resolution (<5 ps RMS between two channels) time-to-digital converter (TDC) implemented in a field programmable gate array (FPGA)," in *Proc. IEEE Nucl. Sci. Symp. Conf. Rec.*, Oct. 2011, pp. 876–879.
[43] N. Lusardi and A. Geraci, "Comparison of interpolation techniques for TDCs implementation in FPGA," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Oct. 2015, pp. 1–2.
[44] J. Wu and Z. Shi, "The 10-ps wave union TDC: Improving FPGA TDC resolution beyond its cell delay," in *Proc. IEEE Nucl. Sci. Symp. Conf. Rec. (NSS)*, Oct. 2008, pp. 3440–3446.
[45] W. Pan, G. Gong, H. Li, and J. Li, "A 20-ps temperature compensated time-to-digital converter (TDC) implemented in FPGA," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Oct. 2013, pp. 1–6.
[46] K.-J. Choi and D.-W. Jee, "Design and calibration techniques for a multichannel FPGA-based time-to-digital converter in an object positioning system," *IEEE Trans. Instrum. Meas.*, vol. 70, pp. 1–9, 2021.
[47] D. Li, M. Liu, R. Ma, and Z. Zhu, "An 8-ch LIDAR receiver based on TDC with multi-interval detection and real-time *in situ* calibration," *IEEE Trans. Instrum. Meas.*, vol. 69, no. 7, pp. 5081–5090, Jul. 2020.
[48] N. Lusardi, F. Garzetti, N. Corna, A. Reale, A. Geraci, E. Dobovicnik, G. Cautero, C. Dri, R. Sergo, and L. Stebel, "Advanced system in FPGA for 3D (X, Y, t) imaging with cross delay-lines," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Oct. 2019, pp. 1–4.
[49] R. Nutt, "Digital time intervalometer," *Rev. Sci. Instrum.*, vol. 39, no. 9, pp. 1342–1345, Sep. 1968, doi: 10.1063/1.1683667.
[50] *Analog Devices*. Accessed: Jul. 8, 2021. [Online]. Available: https://www.analog.com/
[51] S. H. Hall and H. L. Heck, *Advanced Signal Integrity for High-Speed Digital Designs*. Hoboken, NJ, USA: Wiley, 2009, p. 432.
[52] S. H. Hall and H. L. Heck, *Advanced Signal Integrity for High-Speed Digital Designs*. Hoboken, NJ, USA: Wiley, 2009, p. 300
[53] S. H. Hall and H. L. Heck, *Advanced Signal Integrity for High-Speed Digital Designs*. Hoboken, NJ, USA: Wiley, 2009, p. 422
[54] S. H. Hall and H. L. Heck, *Advanced Signal Integrity for High-Speed Digital Designs*. Hoboken, NJ, USA: Wiley, 2009, p. 302
[55] *Texas Instruments*. Accessed: Jul. 8, 2021. [Online]. Available: https://www.ti.com/
[56] H. Johnson, H. W. Johnson, and M. Graham, *High-Speed Signal Propagation: Advanced Black Magic*. Upper Saddle River, NJ, USA: Prentice-Hall, 2003.
[57] *FTDI*. Accessed: Jul. 8, 2021. [Online]. Available: https://www.ftdichip.com/
[58] *Cypress*. Accessed: Jul. 8, 2021. [Online]. Available: https://www.cypress.com/
[59] *USB*. Accessed: Jul. 8, 2021. [Online]. Available: https://www.usb.org/
[60] *Xilinx*. Accessed: Jul. 8, 2021. [Online]. Available: https://www.xilinx.com/
[61] *AMBA AXI Stream*. Accessed: Jul. 8, 2021. [Online]. Available: https://developer.arm.com/documentation/ihi0051/a
[62] *AMBA AXI*. Accessed: Jul. 8, 2021. [Online]. Available: https://developer.arm.com/documentation/ihi0022/e/
[63] R. Pelka, J. Kalisz, and R. Szplet, "Nonlinearity correction of the integrated time-to-digital converter with direct coding," *IEEE Trans. Instrum. Meas.*, vol. 46, no. 2, pp. 449–453, Apr. 1997.



NICOLA CORNA (Member, IEEE) was born in 1992. He received the bachelor's and master's degrees in electronics engineering from the Politecnico di Milano, in 2015 and 2018, respectively, where he is currently pursuing the Ph.D. degree with DEIB, with a focus on development of systems on FPGA and SoC reconfigurable devices, particularly time-domain devices. He has always been interested in free software. He is the author and a developer of various open-source projects.

FABIO GARZETTI (Member, IEEE) received the bachelor's and master's degrees in electronic engineering from the Politecnico di Milano. He developed his thesis work at the Digital Electronics Laboratory, DEIB, on a topic regarding innovative solutions for calibration and triggering of asynchronous signals for time-to-digital converters (TDCs) in field programmable gate arrays (FPGA). In DEIB, he applied for the award of a temporary research fellowship within the framework of the research programme "Design of modules for readout and processing of sampled data based on FPGA architectures," supported by CAEN ELS.

NICOLA LUSARDI (Member, IEEE) was born in Piacenza, in November 1990. He received the Ph.D. degree, in 2018.

He developed his thesis work at the Digital Electronics Laboratory, DEIB, on a topic regarding high-resolution time-to-digital converters (TDCs) in field programmable gate arrays (FPGA). He is currently a Temporary Researcher at DEIB. He is a Professor of electronics at the Politecnico di Milano and an Associate Member of the Italian National Nuclear Physics Institute (INFN). His research line and knowledge as a Digital Designer have been acknowledged by public and private research centers. Since 2014, he has been collaborating with CERN in the LHCb experiment, CAEN S.p.A. (Viareggio, Lucca), CAELels S.r.l. (Basovizza, Trieste), the Elettra Sincrotrone Trieste S.C.p.A. (Basovizza, Trieste), Single Quantum B.V. (Delft, The Netherlands), the Technology University of Delft, École Polytechnique Fédérale de Lausanne, and Rete Ferroviaria Italiana. He is a Co-Founder of TEDIEL S.r.l., an Italian start-up and spin-off of the Politecnico di Milano.

ANGELO GERACI (Senior Member, IEEE) received the M.Sc. degree *(cum laude)* in electrical engineering and the Ph.D. degree *(cum laude)* in electronics and communication engineering from the Politecnico di Milano, in 1993 and 1996, respectively. Since 2004, he has been an Associate Professor with the Department of Electronics, Information and Bioengineering (DEIB), Politecnico di Milano, where he is currently a Lecturer for the "Sistemi Elettronici Digitali" and "Digital Electronic Systems Design" courses with the School of Industrial and Information Engineering. He holds courses for the Ph.D. program in information technology. Since 1995, he has been a Scientific Collaborator of the Italian National Nuclear Physics Institute (INFN). He is a member of the Management Board and a Deputy Coordinator of the Ph.D. School of Information Engineering, Politecnico di Milano. He is an Auditor of projects on behalf of the Italian MIUR. He has been the Advocate and a Manager of several sponsored joint research projects between the Politecnico di Milano and private/public companies. He is the author and the coauthor of more than 320 publications on refereed international congress proceedings and journals. His research interests include digital electronics based on microcontrollers, DSP, and FPGA devices, specifically in the areas of radiation detection, medical imaging, energy storage for automotive electric systems, and HPC applications. In 2003, he was elevated to the grade of a Senior Member of the IEEE Nuclear and Plasma Society. He received the IEEE TRANSACTIONS Prize Paper Award by the IEEE Power Electronic Society, in 2004. He is a Referee for several international journals, including IEEE TRANSACTIONS ON NUCLEAR SCIENCE and *Review of Scientific Instruments*.