IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received August 11, 2021, accepted August 22, 2021, date of publication August 27, 2021, date of current version September 15, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3108596

A Low Noise Power Amplifier MMIC to Mitigate Co-Site Interference in 5G Front End Modules

NEHA BAJPAI[1], (Member, IEEE), AHTISHAM PAMPORI[1], (Member, IEEE), PARAMITA MAITY[2], MANISH SHAH[2], AMITAVA DAS[2], AND YOGESH SINGH CHAUHAN[1], (Fellow, IEEE)

[1]Department of Electrical Engineering, Indian Institute of Technology Kanpur, Kanpur 208016, India
[2]Tagore Technology Inc., Arlington Heights, IL 60006, USA

Corresponding author: Neha Bajpai (bajpai@iitk.ac.in)

The work was funded in part by the Indo-U.S. Science and Technology Forum/US-India Science and Technology Endowment Fund IUSSTF/USISTEF/9th call/EC-059/2018/2019-20, Swarna Jayanti Fellowship under Grant DST/SJF/ETA-02/2017-18 and in part by the Fund for Improvement of ST Infrastructure (FIST) Scheme of the Department of Science and Technology under Grant SR/FST/ETII-072/2016.

ABSTRACT This paper presents a comparative performance analysis of a single-stage GaAs Low-Noise Power Amplifier (LNPA) fabricated in a **0.25** μ**m** pHEMT process to mitigate co-site interference across multiple frequencies in the L- and S-bands. We compare five different designs from 1.2 to 3.8 GHz, each offering a minimum bandwidth of 300 MHz. Designed bandwidth is sufficient to cover several popular 5G NR FR1 channels as well as suitable for carrier aggregation in the LTE bands. An Output 1-dB compression point (OP_{1dB}) of 27.5 dBm, noise figure (NF) below 1 dB and an Output 3rd-order Intercept Point (OIP3) up to 40 dBm is achieved. Adjacent Channel Leakage Ratio (ACLR) measurements are performed at 2.5 GHz with a Peak to Average Power Ratio (PAPR) of 11.8 dB. We achieve an ACLR of −25 dBc at 25 dBm of output power for a 20 MHz, 16-QAM modulation signal, while the corresponding power added efficiency & Drain-efficiency (DE) are, on average, more than 47% & 50% respectively. An integrated Electro-Static-Discharge (ESD) limiter is also incorporated, which can tolerate up to 350 V Human Body Model (HBM) and 125 V Charged Device Model (CDM) without failure. The design occupies a footprint of only **0.325 mm**^{2}.

INDEX TERMS Electrostatic discharge, Gallium Arsenide, low noise amplifier, monolithic microwave integrated circuit (MMIC), noise figure, power amplifier, pseudomorphic-high electron mobility transistor (pHEMT), radiofrequency amplifier.

I. INTRODUCTION

5th Generation New Radio (5G NR) wireless systems are state-of-the-art networks deploying smaller cells with an ability to connect significantly more devices simultaneously than a 4G cell. The applications of this technology range all the way from connected smart city appliances and robotics to autonomous and networked automobiles [1]. The 3rd Generation Partnership Project (3GPP) has classified 5G into two different spectra, FR1 (sub-6 GHz) and FR2 (above 24 GHz) [2]. Modern cellular wireless network devices and subsystems are expected to provide concurrent access to users, necessitating the use of multiple telecommunication protocols and carrier aggregation (CA) techniques across multiple frequency bands. The 5G small cell, being significantly smaller than its predecessors, is expected to have crowded and closely located receivers and transmitters operating simultaneously. Such a setup requires RF system designers to pay more attention to the generation and rejection of signals and noise in communication systems. The collocated (co-site) transmitter raises the system noise floor, which makes diminished dynamic range for the receiver operating in an adjacent channel in the presence of the transmitter's interfering signals [3].

Typical sources of interference include self-interference due to collocation of transmitters and receivers (known as co-site interference), jammers, broadband noise, spectral splatter, naturally occurring space weather, rusty bolt effects or any of the numerous other sources [3]. RF interference is very crucial in the military communication systems [4], especially in Command and Control (C2) platforms, ship-board, and submarine and fighter plane communications, which require multiple RF communications channels to ensure communication over long distances. Quite often these critical communication requirements are not met, as in the case of an aircraft, or a 5G transceiver, due to transmitter and receiver

The associate editor coordinating the review of this manuscript and approving it for publication was Tae Wook Kim.

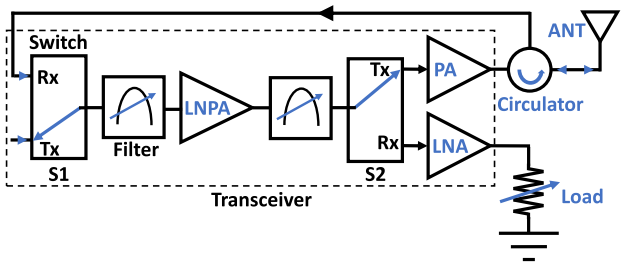


FIGURE 1. Block diagram of a co-site transceiver.

site separation being restricted. This severely degrades communication range primarily due to self-generated or co-site interference.

Co-site interference in the 5G FR1 band is more pronounced compared to the 5G FR2 band due to the coexistence of Long-Term Evolution (LTE) bands [5]. Simulation results for a LTE sub-band of 2.1 GHz indicate that LTE frequency-division duplexing (FDD) downlink is expected to cause harmful interference to 5G NR FDD downlink in the same band. In the case of co-station, an additional 1.16 dB ACIR (Adjacent Channel Interference Ratio) is required for proper communication [5].

The impact of RF interference can lead to receiver front-end overload or receiver desensitization. The former is the most severe source of RF co-site interference and occurs when a co-located transmitter on a nearby band starts saturating the receiver front-end. This interference causes all kinds of problems with the receiver system and can be addressed using a first stage RF filter in the design. However, receiver manufacturers leave out the first stage RF filter in the design, since its band insertion loss adds directly to the total system noise figure. This makes the receiver to have a low noise figure on paper but very susceptible to out-of-band RF interference. The absence of a RF filter installed prior to the first stage LNA also makes the system prone to wide band noise [3]. The latter happens when a nearby transmitter overloads the receiver in-band – curtailing its sensitivity to actual signals of interest.

To address broadband demands and high data rates in 5G communication, active phased-array systems are increasing. An active phased-array system consists of multiple stages of a Front-End Module (FEM). In a typical FEM, several stages of power amplifiers (PAs) and low-noise amplifiers (LNAs) are used to meet the system requirements. The two main blocks of FEMs, LNA and PA, have noise and high power (as linear as possible) as the most crucial parameters, respectively. Instead of using multi-stage LNAs and PAs separately, we can design an amplifier which delivers both low noise and high linearity moderately, with a common driver as the first stage of FEM. In this case, for a robust co-site communication, the use of a co-site LNPA is recommended, though it has not been explored much in the literature. In [6], a two-stage LNPA in Ka-band using $0.15\mu m$ GaAs pHEMT technology with 14.92 dBm of output power and 2.88 dB of noise figure is presented. In [7], a commercial ultra-broadband LNPA in E-band with 30 GHz of bandwidth, 16 dBm of output power, and 6 dB of noise figure using GaAs HEMT is shown. A new, tunable, RF FEM using a tunable inter-stage filter in between the two LNPAs is shown in [8], making a single chain tunable RF FEM for cellular terminals feasible.

A new approach to reduce the co-site interference generated in collocated transceivers using an LNPA in an RF FEM is shown in Fig. 1. In this block diagram for signal transmission switches, S1 and S2 connect the Tx node to the LNPA and then to the PA via filters. Eventually, the antenna transmits an incoming signal in the channel of interest. Similarly, for signal reception, incoming signal from the antenna is connected directly to the Rx node of switch S1, connecting it to the LNPA via the filter. Finally, switch S2 connects the LNPA output to the input of LNA, and eventually to the load. A circulator between the PA and the antenna helps in isolating transmitting and receiving signals.

Using an LNPA, as the first stage of a transmitter chain, reduces the overall noise generated during transmission. This leads to reduced noise introduction to adjacent receiving channels and aids in reducing co-site interference. Having a reduced receiver noise floor leads to a higher dynamic range of the transceiver system. The use of LNPAs significantly reduces circuit footprints which leads to a compact transceiver design [6]. Reduced transceiver footprints are of significant importance, particularly for use in an antenna array with a multitude of antenna elements – a key feature of 5G transmission systems [9]. Applications of LNPAs span a wide range from harmonic feedback loop oscillators [10], to RF frontends [8], to active backscatter tags [11].

In this work, we have designed and fabricated a cost-effective co-site LNPA using GaAs to reduce these interference problems. Gallium Arsenide (GaAs) is a well-established technology for the implementation of high-frequency Power Amplifiers (PAs) [12]. Our design of a co-site LNPA for 5G applications is based on a standard 0.25-μm GaAs pHEMT technology – with a cutoff frequency (f_T) of 70 GHz and a maximum transconductance (g_m) of 800 mS/mm. We discuss the device and assembly board technology used for the LNPA design in Section. II, the measured results in Section. III and then conclude in Section. IV.

II. INTEGRATED ESD-LIMITER LNPA CIRCUIT DESIGN

A. DEVICE TECHNOLOGY AND ASSEMBLY BOARD DESIGN

The designed MMIC is based on a standard 0.25-μm GaAs pHEMT technology, fabricated on a 6-inch, 100-μm thick wafer. Some key electrical characteristics of this process are summarized in Table. 1. The LNPA MMIC is dielectrically coated and housed in a standard 16L-QFN 3 × 3 surface-mount package, which is fully RoHS compliant to ensure good die protection against mechanical constraints and humidity.

To take the estimate of the package pads and bond wires into account, we used the QFN package template in ADS®

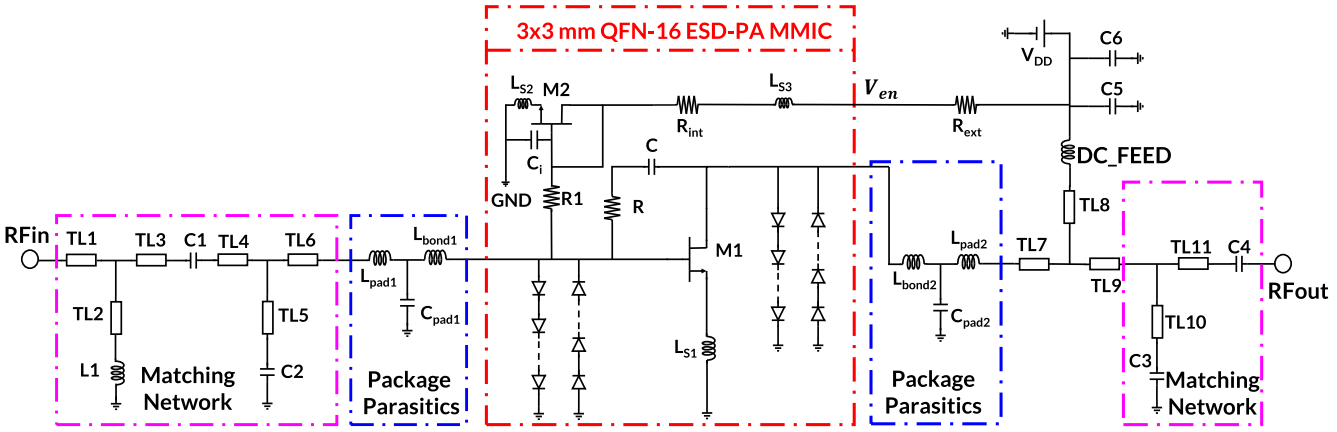


FIGURE 2. ESD-limiter-LNPA schematic for the 1.7 – 2.0 GHz sub-band.

which uses both Keysight Momentum (for 2D structures) and FEM (for 3D structures) in the package.

We employ a motherboard based on the Rogers RO4350B substrate, with the dielectric exhibiting a relative permittivity of 3.66. The board is 508 μm thick, with a 1oz top and bottom copper cladding. The corresponding 50 Ω transmission line has a strip width of around 1.05 mm. To achieve a reliable RF performance on the motherboard, a grid of plated vias with a diameter of less than 380 μm and a spacing of less than 700 μm is fabricated. The schematic of the design is shown in Fig. 2 and the photograph of the corresponding packaged LNPA mounted on a motherboard is shown in Fig. 3.

TABLE 1. Summary of the 6-inch 0.25μm e-pHEMT process.

Parameter	Typical Value
Breakdown voltage V_{dg}	16 V
Saturation current $I_{d,max}$	500 mA/mm
Pinch-off voltage V_{t0}	0.3 V
Cut-off frequency f_t	70 GHz

B. MMIC DESIGN

In this paper we are presenting design of a LNPA with 27.5 dBm of output power. The process flow involved in the design of an LNPA can be sub-divided into following steps:

1) DEVICE SELECTION

To design an LNPA, selection of the device size plays a vital role. Based on the Watt/mm rating for our device technology, a device with a periphery of 2.7 mm is chosen to deliver output power close to the desired output power. A comparison of the minimum noise figure (NF_{min}) for the chosen device periphery of 2.7 mm with different permutations of width and number of fingers is done as shown in Fig. 4. For this comparison, we performed an S-parameter analysis of the matched device at 1.8 GHz with a DC bias of $V_{DD} = 5\ V$ and $I_{ddq} = 140\ mA$ for any one combination of W and F. Since the matching network comprises of lossless passive elements only, NF_{min} is independent of matching network. We then recorded the values of NF_{min} for various combinations of

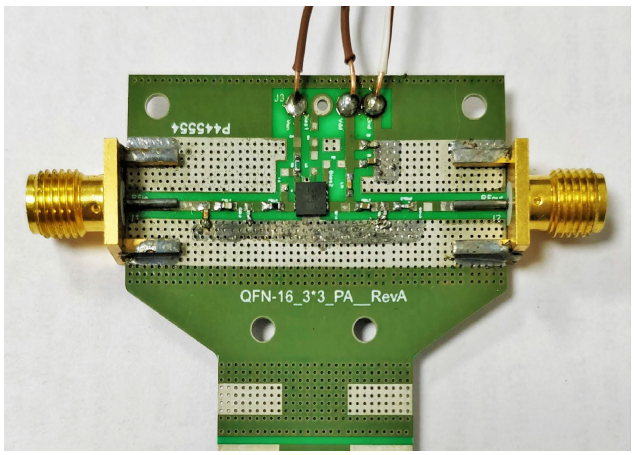


FIGURE 3. 16L-QFN 3 × 3 packaged LNPA assembled on a Rogers RO4350B board.

W and F, while keeping the matching network unchanged. To obtain the exact behaviour of the device, we used an ideal DC choke to bias the device instead of current mirror (CM) bias. Among the various combinations of widths and fingers, a device with a smaller width per finger was observed to have the best noise performance. This is because the device with a smaller width per finger offers a smaller gate resistance compared to a device having a larger width per finger, while keeping the device size constant. Therefore, to optimize the noise performance in our design, we select a 2.7 mm device with a smaller width per finger and use it in a common source (CS) configuration.

2) BIAS POINT SELECTION AND DESIGN STABILITY

After selecting the right combination of device width and number of fingers for minimum NF, the dc bias current is chosen based on the compromise made among minimum noise figure (NF_{min}), output power (P_{out}) and power added efficiency (PAE). NFmin is a function of bias current density as shown in Fig. 5. For this figure, we used the same set of conditions as in Fig. 4, except that a CM bias was used at the gate side instead of an ideal DC choke. First, we select a

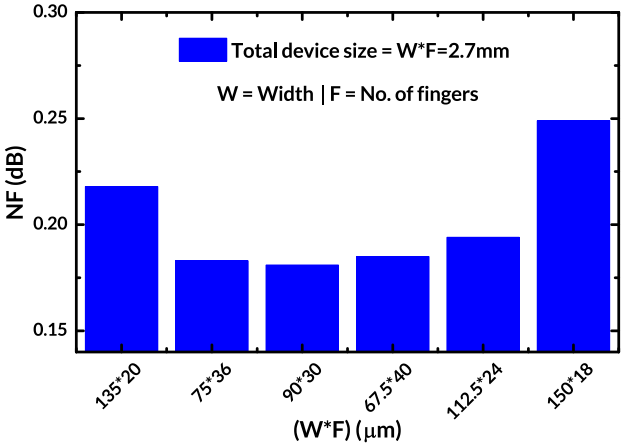


FIGURE 4. Noise figure variation using different widths and fingers for a device periphery of 2.7mm.

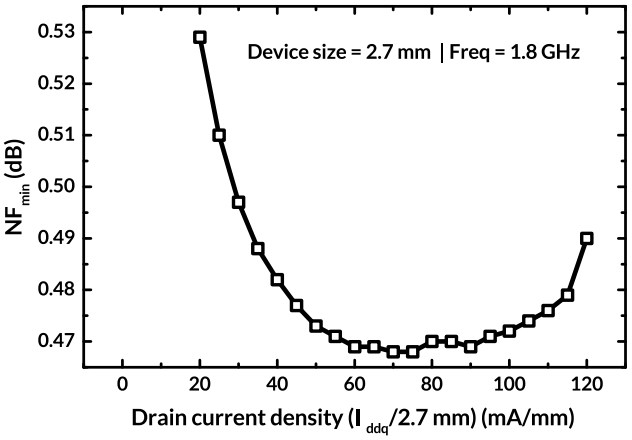


FIGURE 5. Dependence of NF_{min} on the drain bias current density, for 2.7 *mm* device only, $V_{DD} = 5$ *V* and variable gate bias at 1.8 *GHz* of frequency.

current density based on the lowest possible NF_{min} for the device size selected. In our case, this number came out to be 60mA/mm. Next, we calculate the value of bias current required to provide output power of 27.5 dBm using the equations presented in [13]. The required fundamental current (I_{f1}) for a given drain bias, V_{DD} and required P_{out} is given by:

$$I_{f1} = \frac{2 * P_{out}}{(V_{DD} - V_{knee})} \tag{1}$$

For our design, $V_{DD} = 5\ V$, $V_{knee} = 1\ V$ and $P_{out} = 0.562\ W$. Substituting these values in (1) gives us $I_{f1} = 281\ mA$.

A conduction angle (θ_c) of 218° (equivalent to θ of 109° in [13]) is chosen which results in a theoretical efficiency (η) of 70.6% for $V_{knee} = 0$V. With $V_{knee} = 1$V (obtained from the DC analysis), as in our design, and keeping the conduction angle unchanged, we get $\eta = 56.5\%$. Using these values for bias-current calculations [13], we arrive at $I_{dc-bias} = 130.2\ mA$ which has been rounded off to 140 *mA* in our design.

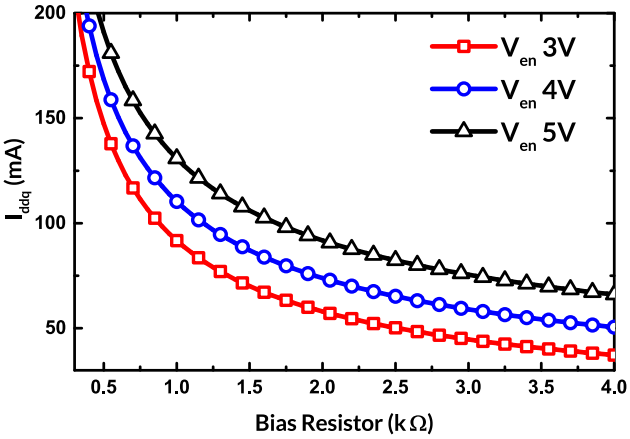


FIGURE 6. Dependence of the drain bias current, I_{ddq}, on the external bias resistor, R_{ext}, for different gate bias conditions.

A bias current of 140 *mA* gives a current density of $140\ mA/2.7mm = 51.9mA/mm$, which is smaller than the current density required for smallest possible NFmin. We settle for a compromise of 0.01 dB in NFmin for an output power of 27.5 dBm and finally choose a 140 *mA* bias current for our design.

A current mirror (CM), is used to avoid the need for two power supplies as shown in Fig. 2. The gate current for the M1 device is restricted to a few micro-amperes, allowing the design to realize low noise figure. To compensate for any process variation in the bias network, an external bias resistance, R_{ext} is used. It serves a dual purpose by allowing the designer to vary the bias conditions externally using the lookup chart shown in Fig. 6.

The LNPA MMIC, including the bias network, occupies a chip area of 0.325 mm^2. Stability is ensured from DC to 20 GHz using RC feedback, source inductances and optimized matching networks. The RC feedback network also helps to reduce the matching circuit's Q factor, avoiding unwanted resonances caused by the microstrip lines, the parasitic inductance of the via holes, and the MIM capacitor (C_i in Fig. 2). All closely laid transmission lines have been simulated using Keysight Momentum® to quantify coupling effects.

3) MATCHING NETWORK DESIGN

Having modeled the parasitics and fixed a bias point for the design, we move on to designing the matching networks. In an LNPA, the low noise figure is mainly decided by the input match, whereas P_{out} and PAE are decided by the output matching network. The preferred loading conditions vary over frequency, as shown in Figs. 7(a) and 7(b). The load impedance offering the best P_{out} and PAE shift in an anti-clockwise direction as shown by the magenta and green traces in Fig. 7(b) respectively. For the input matching network design, a compromise between NF and P_{out}/PAE is made. As observed in Fig. 7(a), PAE and P_{out} contours are overlapping in source pull simulations. The contours of

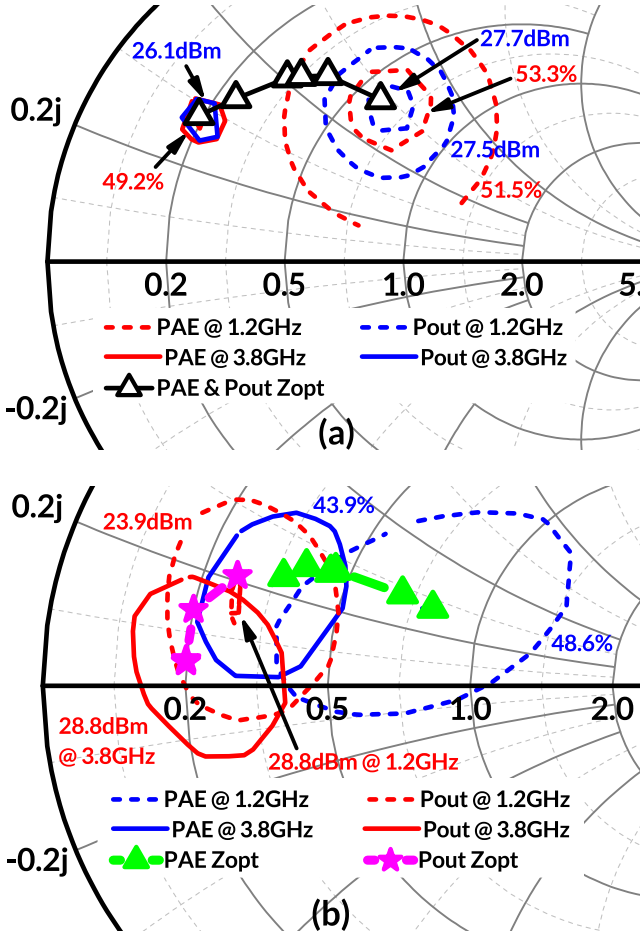


FIGURE 7. One-tone (a) source-pull and (b) load-pull simulations showing constant output power contours (Red) and constant PAE contours (Blue) for a constant input power level of 18.5 dBm. Lines with symbols indicate the trajectory of the optimum P_{out} and PAE with frequency while looking into the device. The simulations were performed with the models for the packaged parasitics in place. $V_{DD} = 5\ V$, $I_{dc-bias} = 140\ mA$, Frequency = 1.2 – 3.8 GHz. Normalized with a 50Ω impedance.

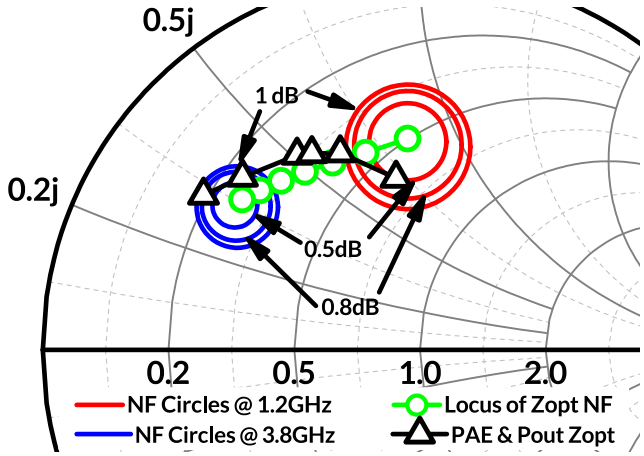


FIGURE 8. Noise figure circles showing contour of NF_{min} with frequency from 1.2 – 3.8 GHz, for $V_{DD} = 5\ V$, $I_{dc-bias} = 140\ mA$ while looking into the device.

minimum noise figure are plotted in Fig. 8. It can be seen from Fig. 8, that the locus of optimum impedance for NF_{min} and P_{out}/PAE from source-pull (SP) are in close proximity

TABLE 2. Extracted values of components for the 1.7 – 2.0 GHz sub-band.

Component	Value	Components	Values
L1	4.7 nH	C1	1.2 pF
L_{bond1}	0.8 nH, $Q = 50$	C2	1.5 pF
L_{bond2}	0.96 nH, $Q = 50$	C3	0.5 pF
L_{pad1}, L_{pad2}	0.05 nH, $Q = 50$	C4	4.3 pF
L_{S1}	0.12 nH	C5	27 pF
L_{S2}	0.12 nH	C6	100 nF
L_{S3}	0.9 nH	$C_{pad1,pad2}$	100 fF, $Q = 100$
DC feed	18 nH	M1	$2.7\ mm$
R_{ext}	1.1 KΩ	M2	$0.1\ mm$

to each other. Therefore, input matching network is designed prioritizing the NF_{min}, while the compromise for P_{out}/PAE is made at the input side. In contrast, the output PAE contours deviate from those for P_{out}, indicating that compromises between efficiency and power are inevitable for the output matching network design. At the output side we prioritize the P_{out}.

To compare the best performance across the entire frequency band based on above design criterion, we design matching networks for five sub-bands [14]: (a) 1.2 GHz – 1.6 GHz, (b) 1.7 GHz – 2.0 GHz, (c) 2.3 GHz – 2.7 GHz, and (d) 2.7 – 3.2 GHz (e) 3.3 GHz – 3.8 GHz.

Finally, some on board optimization is done to accommodate the unexpected variations like unwanted parasitics. All component parameters are targeted to achieve low noise and high output power simultaneously while keeping non-linearities at bay. Component values obtained after optimization are listed in Table. 2 for the 1.7 – 2.0 GHz sub-band. The matching network designed for this sub-band is shown in Fig. 2. Similar matching networks, based on 3-element π- and T-networks, are designed for other sub-bands.

C. ELECTROSTATIC DISCHARGE (ESD) PROTECTION

GaAs based devices are significantly prone to ESD damage than Si based devices [15], [16]. For a GaAs based LNPA to be robust, the design has to be resilient to ESD damage while maintaining compactness. Additionally, when multiple systems operating at neighboring frequencies and collocated, there is an increasing ESD problem. A key challenge faced in designing an ESD network is to have a low insertion loss to minimize loading the RF path. Traditionally, ESD protection is deployed using diodes in the signal path to increase impedance for the ESD signal [16], using input/output short-circuit stubs [17], or using L-C resonance structures [18], which not only occupy a large area in case of MMICs, but also induce high insertion loss, especially at high frequencies. We implement ESD protection at the input and output stage of the LNPA using a single stage of anti-parallel diode arrays (fabricated using the 0.25-μm GaAs technology), one for a positive zap and another for a negative zap [16], as shown in Fig. 9(a). The number of diodes required at the input and output chains is a direct function of the LNPA saturated power and gain. A simple relation dictating the number of diodes,

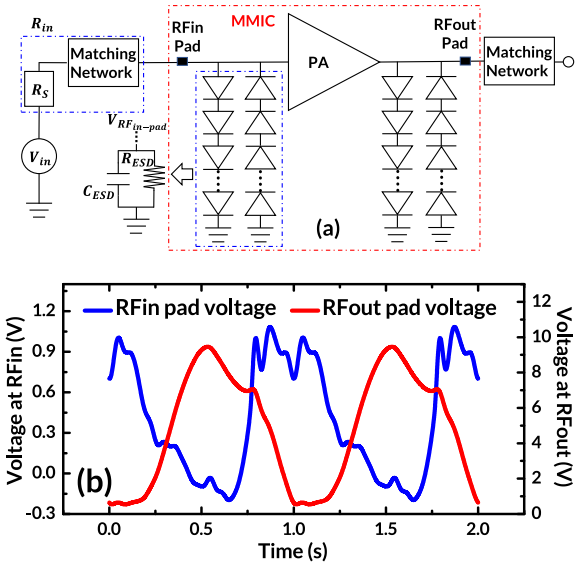


FIGURE 9. (a) Schematic of the LNPA with the ESD protection circuits and an equivalent network for the input-side ESD diodes (b) Voltage swings at RFin and RFout pads of LNPA MMIC at 20 dBm of input power.

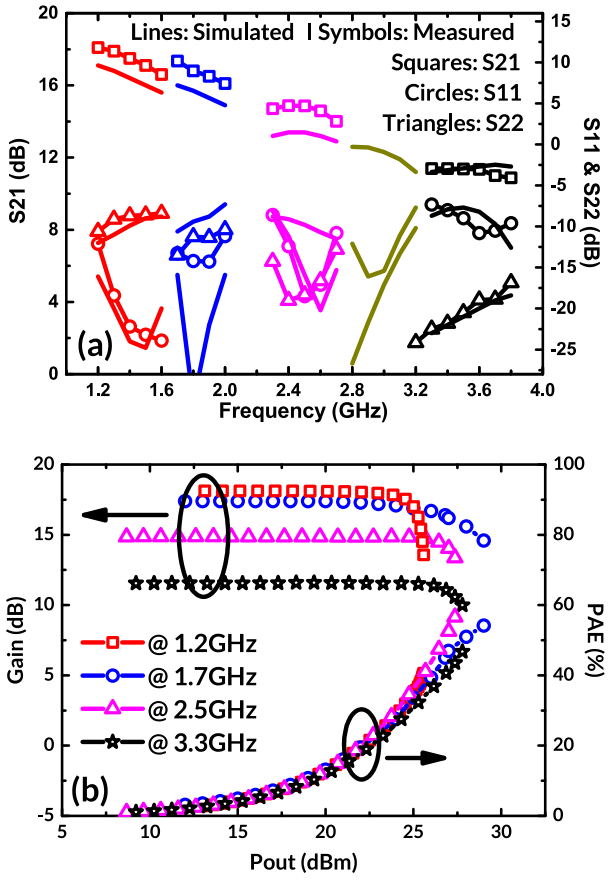


FIGURE 10. On-board (a) Measured and simulated S-parameters for the five sub-bands (b) Gain and PAE vs. output power (CW) for the LNPA at $V_{DD} = 5\ V$ and $I_{DD} = 140\ mA$.

N_{D-ESD}, required is given as:

$$N_{D-ESD} = \frac{V_{RF-peak}}{V_{t-ESD}} \tag{2}$$

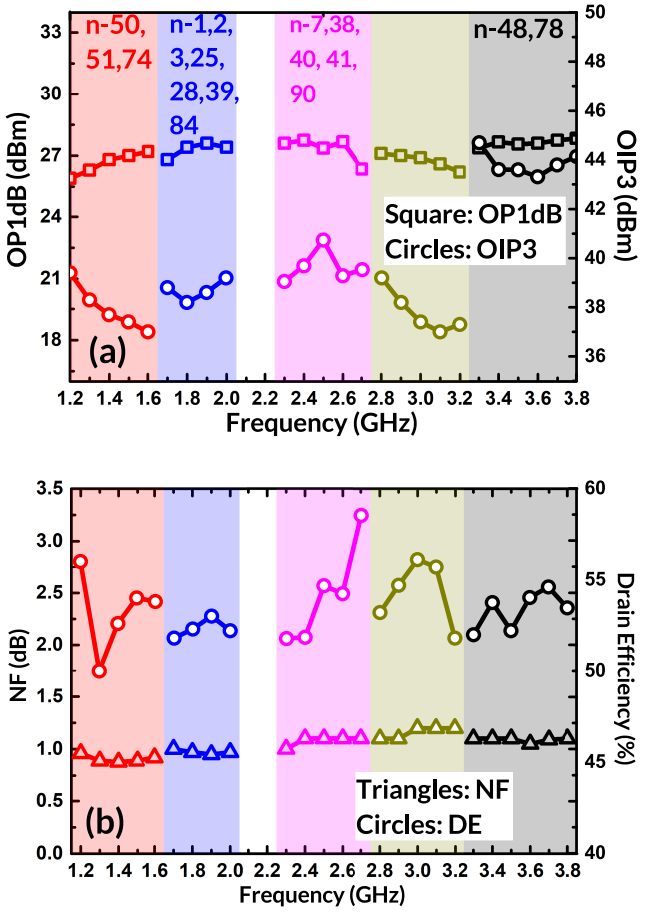


FIGURE 11. Measured results of (a) OP_{1dB} and OIP3 (b) NF and DE for the ESD-limited-LNPA in all four sub-bands from 1.2 to 3.8 GHz. Each color represents one of the frequency bands. The numbers in (a) represent the 5G NR FR1 channels in that particular sub-band.

where $V_{RF-peak}$ is the peak output voltage at an RF power level around 8 dBm above the input 1-dB compression point (IP_{1dB}) superimposed on DC, as shown in Fig. 9(b) and V_{t-ESD} is the knee voltage of the ESD diode. The LNPA's RF input pad has 5 anti-parallel diodes, whereas the output pad has 16 and 3 anti-parallel ESD-diodes for positive and negative zaps respectively, as shown in Fig. 9(a). The drain is biased at 5 V, which clamps the drain voltage waves at 5 V, thus requiring only 3 diodes for the negative zap as compared to the 16 diodes for a positive zap. At the small-signal level, the equivalent circuit of the ESD diode can be approximated by a capacitor C_{ESD} in parallel with a resistor R_{ESD}, behaving as a LPF which decreases the MMIC's bandwidth and increases its noise figure.

As shown in Fig. 9(a), the voltage transfer function from the source to the input of the MMIC after passing through the ESD protection circuit is:

$$\frac{V_{RFin-pad}}{V_{in}} = \frac{R_{ESD}}{R_{ESD} + R_{in}} \frac{1}{1 + sC_{ESD}(R_{ESD}||R_{in})} \tag{3}$$

where, R_{in} is the source impedance, R_{ESD} and C_{ESD} are the equivalent shunt resistance and capacitance of the input ESD protection circuit respectively. The larger the parasitic

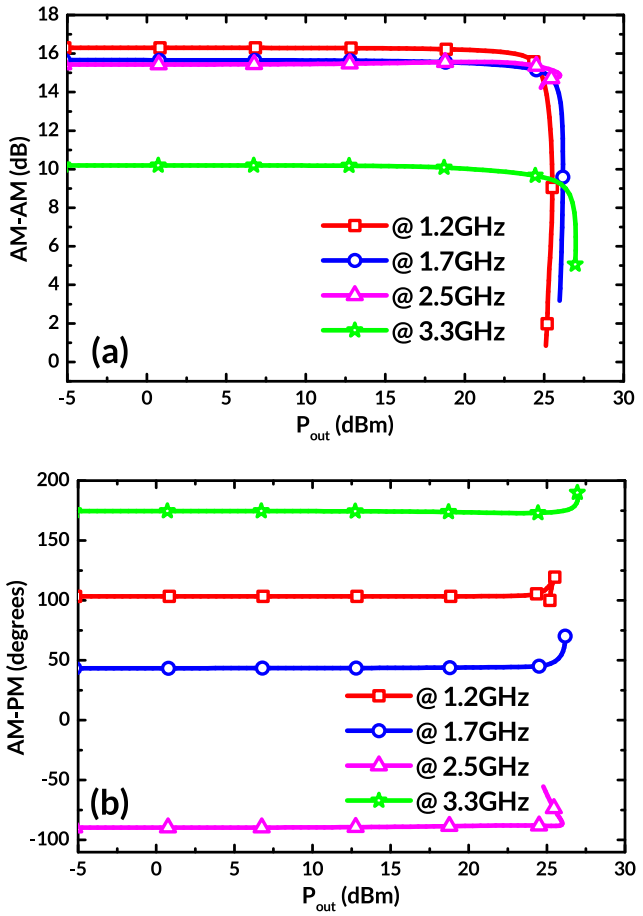


FIGURE 12. (a) AM/AM and (b) AM/PM distortion characteristics, from HB simulations of a circuit-level model.

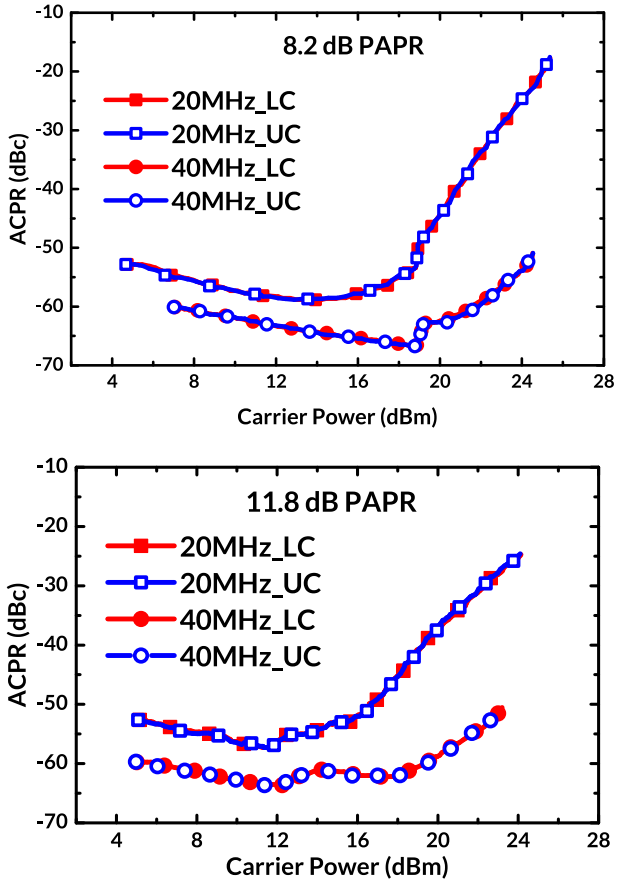


FIGURE 13. Measured results of ACPR for (a) 8.2 dB of PAPR (b) 11.8 dB of PAPR, at 2.5GHz for 20MHz and 40MHz channel spacing using 16QAM modulated signal.

capacitance (C_{ESD}), smaller is the passband frequency of the equivalent LPF. The NF also increases due to the parasitic shunt resistance of the ESD diodes; below the roll-off frequency, the NF is $(1 + R_{in}/R_{ESD})$, and it increases by ∼0.2 dB with a decrease in R_{ESD} by ∼ 500 Ω [19]. The design objective is to absorb the parasitic capacitance in the matching network to mitigate losses. The designed ESD structure can tolerate up to 350 V-HBM and 125 V-CDM without damage. For complete protection of the MMIC, high current shunt diodes have been added on each DC biasing pad.

III. RESULTS AND DISCUSSIONS

A. LNPA MEASURED PERFORMANCE

The LNPA S-Parameters have been measured using a Keysight PNA-X N5244A at a bias condition of $(V_{DD}, I_{DD}) = (5\ V, 140\ mA)$, and compared with the simulated results in Fig. 10(a). The measured linear gain (S_{21}) averages around 16.5 dB, while the input and output reflection S-Parameters stay at or below −10 dB for all four sub-bands. The measured gain is higher than the simulated gain because the actual value of down bond wire inductance L_{S1} obtained is smaller compared to the value estimated by Keysight Momentum®. Fig. 10(b) shows the gain and PAE variation with increasing output power. The design is able to operate at ∼50% PAE around OP_{1dB}.

The measured large signal metrics of the design are presented in Fig. 11(a) along with noise and efficiency in Fig. 11(b) for all the four designed sub-bands. We obtain an OP_{1dB} of around 27.5 dBm, almost constant across all sub-bands. Some of the popular 5G NR FR1 channels in these bands have been pointed out in Fig. 11(a). The noise figure for the PCB mounted LNPA MMIC is measured using a Keysight N8975B Noise Figure Analyzer (NFA). The NF, at room temperature, stays below 1.2 dB for all four sub-bands, as seen in Fig. 11(b). The measured drain efficiency (DE) averages around 54% as shown in Fig. 11(b), DE at 1.2 GHz and 2.7 GHz is higher than the average DE because at these points output impedance obtained is closer to optimum PAE compared to OP_{1dB}. A sub-1.2 dB NF and a mean OIP3 of 38 dBm make this design a good LNA and a linear PA respectively.

This enhanced linearity is further evident in the AM/AM and AM/PM distortion characteristics as shown in Fig. 12. The designs offer an AM-AM distortion of −2 to −6.5 dB and an AM-PM distortion of 5 to 15 degrees at the 1-dB compression points as shown in Fig. 12(a) and Fig. 12(b) respectively.

TABLE 3. Performance comparison for the 1.7 – 2.0 GHz sub-band with other PA and LNA designs in the literature.

Parameters	[21]	[22]	[23]	[24]	[25]	[26]	[27]	[28]	This work
Process	GaAs HBT	CMOS 180nm	GaAs-HBT 200nm	GaAs 150nm	CMOS 180nm	GaN 250nm	GaAs 250nm	CMOS 130nm	GaAs 250nm
Frequency (GHz)	1.8–2.17	2.4	1.7–2.05	2–6.5	2	2–4	1.95	2.1	1.7–2.0
V_{DD} (V)	5	3.6	3.3	5	1.8	10	5	1.3	5
Gain (dB)	31	21.4	34.6–35.8	21	16	22	20	19.2	17
NF (dB)	–	–	–	–	2	2	0.5	2.4	1.07
OP_{1dB} (dBm)	27.5	17.8	28	30	–	–	–	–	27.5
IIP_3 (dBm)	–	–	–	–	3	7	15	8.6	22
PAE_{max} (%)	30	28	40-55	31.4–51.5	–	–	–	–	47
Die size (mm×mm)	3.5×4.5	0.61×0.51	0.95×0.9	3.7×2.6	–	4.4×2.1	1.2×1.7	–	0.325 mm^2
ESD Protection	No	Yes	No	No	Yes	No	No	No	Yes
Topology	2-stage CS	1-stage Cascode	3-stage	2-stage	1-stage Cascode	2-stage CS	1-stage Cascode	1-stage CS	1-stage CS
FOM ($x10^6$)	23.7	–	244.8	–	2.8	0.46	16.8	60.7	10.5–PA 11.5–LNA

The PA achieves an average output power of 27.5 dBm, with IMD3 and IMD5 levels under −18 dBc. The fabricated LNPA has also been evaluated with two LTE 16-Quadrature Amplitude Modulation (QAM) signals exhibiting PAPRs of 8.2 dB and 11.8 dB respectively, at a carrier frequency of 2.5 GHz and offset channel bandwidths of 20 MHz and 40 MHz for each input PAPR. Fig. 13(a) and Fig. 13(b) present the ACLR characteristics versus output power with 8.2 dB and 11.8 dB PAPR respectively for two different offset channel bandwidths of 20 MHz and 40 MHz from carrier. From Fig. 13(b), the lower channel (LC) and upper channel (UC) ACPRs at the output power of 25 dBm are −25/−50 dBc, achieved at frequency offsets of 20/40 MHz respectively. The LNPA can be operated at back-off power levels to improve the ACLR, resulting in lower efficiencies. However, with pre-distortion techniques in place, the LNPA can be utilized up to its saturation point while still maintaining good linearity, thereby significantly increasing its non-linear performances.

B. PROCESS VARIATION AND COMPARISON WITH EXISTING DESIGNS

In order to account for the impact of process variability on the LNPA performance, Monte Carlo simulations for S_{21} are carried out considering a variability in the lengths and widths of the MMIC resistors and capacitors as well as the transistor width. The simulations yielded a mean value of 14.9 dB and a standard deviation of 0.49 dB for S_{21} at 1.9 GHz with a 10% Gaussian process variation, offering a process yield of 99% – indicating that the design exhibits excellent robustness to process variation as shown in Fig. 14.

Table. 3 compares the performance of our design in the 1.7 – 2.0 GHz sub-band with published results across device technologies in the literature. The proposed single-stage LNPA is able to closely match the performance of multi-stage circuit designs across the literature in a significantly small footprint.

When compared with contemporary PAs ([21]–[24]), as in Table. 3, our design offers an excellent single stage performance in a compact footprint with in-built ESD protection. With a PAE of 47%, the design is significantly power efficient as compared to contemporary designs, while offering the same output power levels. Being a single-stage design, the gain achieved is slightly lower.

It is difficult to come up a Figure of Merit (FoM) for an LNPA which can do an honest comparison with both LNAs and PAs simultaneously. To quantify the performance of our LNPA with the state of art LNAs and PAs, we used a modified version of ITRS LNA-FOM [20] that has all the design parameters of LNA and PA, which is defined as.

$$FoM = \frac{G_V|_{lin} f_c|_{GHz} IIP3|_{mW} OP1dB|_{mW} PAE|_{lin}}{(NF-1)|_{lin} P_{DC}|_{mW}} \quad (4)$$

where $G_V|_{lin}$ is the amplifier voltage gain in linear scale, f_c is the centre frequency (GHz) of operation, $IIP_3|_{mW}$ is the 3rd order Input Intercept Point (W), $OP1dB|_{mW}$ is the power at 1dB gain compression point (mW), $PAE|_{lin}$ is the power added efficiency in linear scale, $(NF-1)|_{lin}$ is the noise

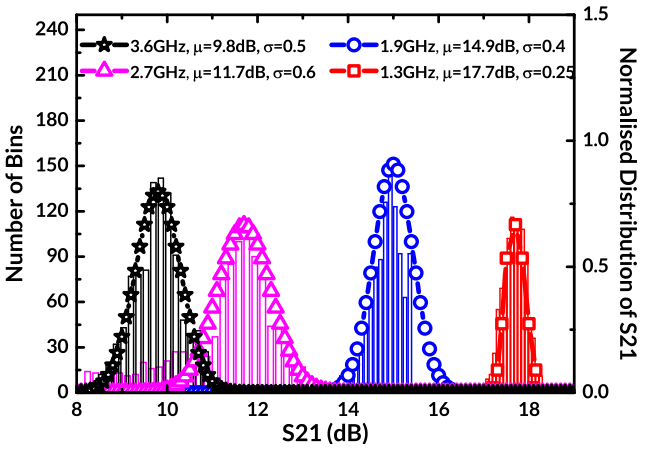


FIGURE 14. Monte-Carlo simulation results for S_{21} variation at four different frequencies considering a 10% Gaussian process variation and 1000 iterations.

figure in linear scale and $P_{DC}|_{mW}$ is the DC power consumed by the amplifier (mW). To calculate FOM we exclude $OP1dB|_{mW}$ and $PAE|_{lin}$ for LNAs whereas for PAs we exclude $IIP_3|_{mW}$ and $(NF-1)|_{lin}$ from equation 4. As seen in Table. 3, the designed LNPA fares well against recent LNA designs ([25]–[28]) across various device technologies in the literature, with a FoM of 11.5×10^6. Being a LNPA, it offers one of the highest IIP3 and OP_{1dB} while maintaining a low NF of 1.07 dB, offering a better performance than contemporary designs in the same band. It is worth mentioning here that the proposed design delivers this performance with the ESD protection circuit incorporated - which is absent in most of the recent designs compared here.

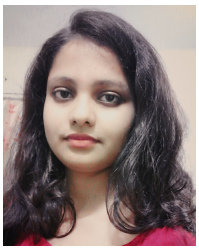
IV. CONCLUSION

Production-ready, compact and linear ESD-limited-Low Noise Power Amplifier MMIC designs were presented in four sub-bands between 1.2 and 3.8 GHz for co-site interference applications. The LNPA offered excellent noise characteristics with a noise figure below 1.2 dB across the entire design space along with higher linearity and integrated ESD protection. Monte-Carlo simulations were performed to ensure minimal performance drop due to variability. The large-signal characteristics offered by our single-stage LNPA were comparable to multi-stage amplifiers in the literature.

REFERENCES

[1] D. Choudhury, "5G wireless and millimeter wave technology evolution: An overview," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2015, pp. 1–4, doi: 10.1109/MWSYM.2015.7167093.
[2] *5G; NR; User Equipment (UE) Conformance Specification; Radio Transmission and Reception; Part 2: Range 2 Standalone*, document 3GPP TS 138 521-2, TS 38.101-1, Version 15.3.0, 15.2.0, Release 15, 2018, pp. 1–72.
[3] *Pole/Zero Catalog—Integrated Cosite Equipment (ICE)*, Microw. Products Group, Dover Corp.
[4] G. W. Travis and H. F. Lenzing, "Shipboard HF interference: Problems and mitigation," in *Proc. IEEE Mil. Commun. Conf.*, vol. 1, Oct. 1989, pp. 106–110, doi: 10.1109/MILCOM.1989.103907.
[5] N. An, C. Wang, and W. Wang, "Interference coexistence of 5G NR and LTE system based on 2.1 GHz," in *Proc. 12th Int. Conf. Commun. Softw. Netw. (ICCSN)*, Jun. 2020, pp. 90–94, doi: 10.1109/ICCSN49894.2020.9139105.
[6] C. Tsao, Y. Tsao, T. Lin, T. Huang, and H. Hsu, "Compact low-noise power amplifier design and implementation for millimetre wave frequencies," *IET Circuits, Devices Syst.*, vol. 14, no. 7, pp. 1026–1031, Oct. 2020, doi: 10.1049/iet-cds.2020.0274.
[7] AFB-E27HP-01, "60 to 90 GHz E-band low-noise power amplifier," Ducommun Incorporated, Santa Ana, CA, USA, 2017, vol. 87, pp. 149–200. [Online]. Available: https://www.ducommun.com/pdf/RF datasheets/RF2-0617AFB-E27HP-01 Datasheet.pdf
[8] H. Obiya, S. Hitomi, T. Wada, H. Hayafuji, Y. Kusumoto, M. Koshino, M. Kawashima, and N. Nakajima, "A study on low Rx-band noise power amplifier for reconfigurable RF front-end circuit," in *IEEE MTT-S Int. Microw. Symp. Dig.* Piscataway, NJ, USA: Institute of Electrical and Electronics Engineers, May 2015, pp. 1–3, doi: 10.1109/MWSYM.2015.7166919.
[9] W. Hong, K.-H. Baek, Y. Lee, Y. Kim, and S.-T. Ko, "Study and prototyping of practically large-scale mmWave antenna systems for 5G cellular devices," *IEEE Commun. Mag.*, vol. 52, no. 9, pp. 63–69, Sep. 2014, doi: 10.1109/MCOM.2014.6894454.
[10] A. Mohsen, "Harmonic feedback multi-oscillator for 5G application," Dept. Elect. Electron. Eng., Université de Bordeaux, Bordeaux, France, 2018. [Online]. Available: https://tel.archives-ouvertes.fr/tel-02410778
[11] J. Prades, A. Ghiotto, T. Taris, N. Regimbal, J.-M. Pham, V. Dupuy, and E. Kerherve, "A microwave switchable low-noise power amplifier for an active backscatter tag," *Microw. Opt. Technol. Lett.*, vol. 56, no. 5, pp. 1251–1255, May 2014, doi: 10.1002/mop.28310.
[12] V. Camarchia, R. Quaglia, A. Piacibello, D. P. Nguyen, H. Wang, and A. V. Pham, "A review of technologies and design techniques of millimeter-wave power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 2957–2983, Jul. 2020, doi: 10.1109/TMTT.2020.2989792.
[13] M. K. Kazimierczuk, *RF Power Amplifiers*. Hoboken, NJ, USA: Wiley, 2014. [Online]. Available: https://www.wiley.com/en-us/RF+Power+Amplifiers%2C+2nd+Edition-p-9781118844342, doi: 10.1002/9781118844373.
[14] D. E. Dawson, "Closed-form solutions for the design of optimum matching networks," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 1, pp. 121–129, Jan. 2009, doi: 10.1109/TMTT.2008.2009041.
[15] K. Bock, "ESD issues in compound semiconductor high-frequency devices and circuits," *Microelectron. Rel.*, vol. 38, no. 11, pp. 1781–1793, Nov. 1998, doi: 10.1016/S0026-2714(98)00181-4.
[16] Y. Ma and G. P. Li, "ESD protection design considerations for InGaP/GaAs HBT RF power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 1, pp. 221–227, Jan. 2005, doi: 10.1109/TMTT.2004.839307.
[17] A. Bessemoulin, S. J. Mahon, J. T. Harvey, and D. Richardson, "GaAs PHEMT power amplifier MMIC with integrated ESD protection for full SMD 38-GHz radio chipset," in *Tech. Dig. IEEE Compound Semiconductor Integr. Circuit Symp. (CSIC)*, Oct. 2007, pp. 84–87, doi: 10.1109/CSICS07.2007.24.
[18] S. Galal and B. Razavi, "40-Gb/s amplifier and ESD protection circuit in 0.18-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2389–2396, Dec. 2004, doi: 10.1109/JSSC.2004.835639.
[19] M. Sun, Y. Lu, and Y. Huai, "Low capacitance ESD protection circuits for GaAs RF ICs," *J. Electrostatics*, vol. 65, no. 3, pp. 189–199, Mar. 2007, doi: 10.1016/j.elstat.2006.07.016.
[20] *2001 ITRS System Drivers*, ITRS, London, U.K., 2001.
[21] W. Ma, B. Lin, S. Male, M. Peter, W. Andreas, and M. Tobias, "Wide-band & high efficiency small cell PA characterized by dual band DPD for LTE carrier aggregation application," in *Proc. Eur. Microw. Week*, Sep. 2015, pp. 254–257, doi: 10.1109/EuMIC.2015.7345117.
[22] C.-Y. Lin and G.-Y. Li, "ESD protection design for open-drain power amplifier in CMOS technology," *IEEE Trans. Device Mater. Rel.*, vol. 19, no. 4, pp. 782–790, Dec. 2019, doi: 10.1109/TDMR.2019.2951939.
[23] U. R. Jagadheswaran, H. Ramiah, P. I. Mak, and R. P. Martins, "A 2-μm InGaP/GaAs class-J power amplifier for multi-band LTE achieving 35.8-dB gain, 40.5% to 55.8% PAE and 28-dBm linear output power," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 1, pp. 200–209, Jan. 2016, doi: 10.1109/TMTT.2015.2498150.
[24] X. Ding and L. Zhang, "A high-efficiency GaAs MMIC power amplifier for multi-standard system," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 1, pp. 55–57, Jan. 2016, doi: 10.1109/LMWC.2015.2505615.
[25] A. Çağlar and M. B. Yelten, "Design of cryogenic LNAs for high linearity in space applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 12, pp. 4619–4627, Dec. 2019, doi: 10.1109/TCSI.2019.2936506.

[26] Z. O. Provost, L. Caillé, M. Camiade, M. Olivier, D. Leclerc, C. Tolant, and M. Stanislawiak, "High robustness S-band GaN based LNA," in *Proc. 14th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Sep. 2019, pp. 243–246, doi: 10.23919/EuMIC.2019.8909569.
[27] J. Yao, X. Sun, and B. Lin, "1.5–2.7 GHz ultra low noise bypass LNA," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2014, pp. 1–3, doi: 10.1109/MWSYM.2014.6848521.
[28] G. Guitton, T. Taris, M. De Souza, and A. A. Mariano, "Design of CMOS LNA with the inversion coefficient," in *Proc. 16th IEEE Int. New Circuits Syst. Conf. (NEWCAS)*, Jun. 2018, pp. 182–186, doi: 10.1109/NEWCAS.2018.8585633.



NEHA BAJPAI (Member, IEEE) was born in Lucknow, India. She received the bachelor's degree in electronics engineering from Aligarh Muslim University, Aligarh, in 2017. She is currently pursuing the Ph.D. degree in electrical engineering with the Indian Institute of Technology Kanpur. Her research interests include RF circuit design, RF device characterization, and wide band gap semiconductors device modeling.

AHTISHAM PAMPORI (Member, IEEE) received the bachelor's degree in electronics and communications engineering from NIT Srinagar. He is currently pursuing the Ph.D. degree with the Indian Institute of Technology Kanpur (IIT Kanpur), working on the characterization and modeling of GaN HEMT RF devices. His research interests include modeling and characterization of GaN HEMTs and their applications in RF systems. He was a recipient of the prestigious Prime Minister's Research Fellowship (PMRF).

PARAMITA MAITY received the bachelor's degree in electronics and communication engineering from WBUT, in 2008, and the master's degree in VLSI design from IIEST, in 2010. She worked as a Research Scientist and then as a Senior Research Scientist with the Society for Applied Microwave Electronics Engineering and Research, Ministry of Electronics and Information Technology, Government of India, under the Circuit and System Division. During the same, she has designed various RF and mm-wave subsystems, such as LNA, PA, BPF, Coupler, Magic Tee, PLL, and Mixer. She also worked in system integration and testing of various mm-wave front-end transceiver module. She is currently working as a RF Engineer with the GaAs MMIC Design Group, Tagore Technology, where she is responsible for' developing a wide-band GaAs MMIC product line.

MANISH SHAH received the bachelor's degree (Hons.) in electrical engineering from the University of Illinois at Chicago, and the master's degree in electrical engineering from the National Technological University. He is currently a Co-Founder of Tagore Technology and the VP of engineering responsible for the overall engineering and product development activities. He brings over 20 years' experience in semiconductor industry ranging from design and development of RF-Mixed Signal IC, 2G, 3G, and 4G cellular transceivers' architecture and system, and cellular radio design. He has extensive experience in leading design teams at Fujitsu, Motorola, and Freescale. He has pushed design boundaries in all his endeavors in numerous research and development, and design projects. He has ten issued patents and many more pending.

AMITAVA DAS received the bachelor's degree in EE from Jadavpur University, the M.S. degree in EE from the University of Akron, and the Ph.D. degree in electrical engineering from Purdue University. He was an Associate Professor with the Indian Institute of Technology Bombay. He worked as the Director at Maxlinear and Freescale. He held senior engineering roles at Motorola and Freescale developing 2.5G/3G RF IC circuits and modules which shipped in large volumes in cellular phones. He is one of the founders of Tagore, in 2011, the CEO, and a Board Member.

YOGESH SINGH CHAUHAN (Fellow, IEEE) is currently a Professor with the Indian Institute of Technology Kanpur, India. He is the developer of several industry standard models: ASM-GaN-HEMT model, BSIM-BULK (formerly BSIM6), BSIM-CMG, BSIM-IMG, and BSIM4 and BSIM-SOI models. His research group is involved in developing compact models for GaN transistors, FinFET, Nanosheet/Gate-All-Around FETs, FDSOI transistors, Negative Capacitance FETs and 2D FETs. He has published more than 250 articles in international journals and conferences. His research interests include characterization, modeling, and simulation of semiconductor devices. He is a member of the Indian National Young Academy of Science (INYAS). He received the Ramanujan Fellowship, in 2012, the IBM Faculty Award, in 2013, the P. K. Kelkar Fellowship, in 2015, the CNR Rao Faculty Award, the Humboldt Fellowship, and the Swarnajayanti Fellowship, in 2018. He has served in the Technical Program Committee of the IEEE International Electron Devices Meeting (IEDM), the IEEE International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), the IEEE European Solid-State Device Research Conference (ESSDERC), the IEEE Electron Devices Technology and Manufacturing (EDTM), and the IEEE International Conference on VLSI Design and International Conference on Embedded Systems. He is the Chair of the IEEE-EDS Compact Modeling Technical Committee. He is the Founding Chairperson of the IEEE Electron Devices Society U.P. Chapter. He is an Editor of IEEE TRANSACTIONS ON ELECTRON DEVICES. He is a Distinguished Lecturer of the IEEE Electron Devices Society.