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Reconfigurable Scan Architecture for High Diagnostic Resolution

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ABSTRACT Scan chain diagnosis is essential to solving yield-reduction problem caused by the miniaturization of manufacturing process. The accurate diagnosis of scan chain faults that frequently occur in the initial process is vital for rapidly improving yield. Moreover, the importance of scan chain diagnosis with a high resolution for the multiple faults is increasing because multiple faults occur in the early stages of the process, further increasing the cost of physical failure analysis. Although multiple faults can be diagnosed with existing methods, a high diagnostic resolution is difficult to achieve in the early stages of the process (where many faults occur) due to the rapid increase in the number of diagnosed fault candidates as the number of actual faults in the circuit increases. In this paper, a novel reconfigurable scan architecture that reconfigures the diagnosis paths and a test algorithm that uses this scan architecture are proposed to reduce the number of diagnosed fault candidates in the scan chain diagnosis with multiple circuit faults. Experimental results indicate that the proposed method achieves the higher diagnostic resolution for multiple faults than conventional methods. In addition, the proposed method reduces the routing overhead by scan partitioning.

INDEX TERMS Design for testability, hardware-based scan chain diagnosis, flush test, multiple faults.

I. INTRODUCTION

For obtaining high test coverage, scan tests that improve the controllability and testability of sequential circuits are essential for modern design. Furthermore, fault locations can be diagnosed by analyzing scan test results, leading to an immediate improvement in the yield by improving the processes for those sites. However, a scan architecture that penetrates all flip-flops in a circuit is distributed throughout the circuit [1], so as many as 50% of the chip failures occur because of the faults in the scan architecture [2]. Many of the defects in the initial process can be analyzed through fault analysis in the scan chain, but further analysis of defects across all logic is possible only if the faults appearing in the scan chain are removed. Therefore, enhancing scan chain diagnosis is crucial for improving the initial yield.

Scan chain diagnosis methods are classified into three categories: tester-based [3]–[7], software-based [8]–[18], [31], [32] and hardware-based diagnosis [19]–[25], [27]–[30].

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Tester-based diagnosis uses testers such as laser provers or current meters to observe defective responses. However, it involves a significant amount of time to analyze the results and the risk of sample destruction. Software-based diagnosis is an algorithmic method that identifies the range of fault candidate locations without circuit modification based on test pattern generation and scan test response. It is popular because it does not require the additional hardware overhead; thus, many algorithmic methods have been proposed.

However, they have two limitations. First, the diagnostic resolution of scan cells, which is inversely proportional to the number of diagnosed fault candidates per actual number of faults in the circuit, depends on the positional relationship between the launched scan cells and the captured scan cells or the complexity of the related logic in the scan architecture. It results in some scan cells with the low diagnostic resolution. Second, the reliability of diagnosis cannot be guaranteed in the presence of a fault in the combinational logic because it inevitably involves a capture operation that passes through the combinational logic area.

Therefore, a hardware-based diagnosis improves the resolution of scan chain diagnosis most significantly, even with the associated hardware overhead. It can achieve superior diagnostic performance compared with algorithm-only diagnostic methods by adding hardware. In contrast to software-based diagnosis algorithms that provide a wide range of the diagnosed fault candidates even for a single fault, hardware-based diagnosis methods succeed in finding precisely one fault location for a single fault irrespective of the circuit structure.

Most of the hardware-based diagnosis methods studied thus far focus on stuck-at fault diagnosis, targeting a single fault. However, defects that are likely to cause the faults in multiple scan cells occur frequently in the early stages of the process. Various types of defects occur as the manufacturing processes are miniaturized. Therefore, it is essential to perform an accurate diagnosis not only for a single stuck-at fault but also for the various fault models.

In this paper, a novel reconfigurable scan architecture that reconfigures the diagnosis paths and a test algorithm that uses this architecture are proposed. They can diagnose not only a single stuck-at fault but also the transition-delay faults and the multiple faults. In contrast to a conventional scan architecture, the proposed reconfigurable scan architecture divides the entire scan area into several partitions, enables the exchange of diagnosis paths between the adjacent scan chains, and executes the test using the proposed scan architecture. The experimental results indicate that it accurately diagnoses various failure conditions even for multiple faults with mixed stuck-at and transition-delay faults. In addition, the proposed method reduces the routing overhead by scan partitioning.

The rest of this paper is organized as follows. Section II details previous studies related to the hardware-based diagnosis and the motivation for the proposed method. In Section III, the proposed reconfigurable scan architecture is detailed. The diagnosis method using the proposed scan architecture is explained in Section IV. The experimental results of the proposed scan architecture are presented in Section V. Finally, Section VI concludes this paper.

II. PREVIOUS STUDIES

Multiple studies have been conducted to maximize the diagnostic resolution of scan chain diagnosis [19]–[25], [27]–[30]. These comprise two categories: diagnosis of a single fault in a single chain and diagnosis of the multiple faults in the entire circuit. This section introduces these studies related to hardware-based diagnosis. Then, the motivation for the proposed reconfigurable scan architecture is presented, together with the limitations of the previous studies.

A. DIAGNOSIS OF A SINGLE FAULT

Some studies [19]–[21], [23], [24] were conducted to diagnose a single stuck-at fault in a scan chain. Hardware-based diagnosis methods achieve very high diagnostic resolutions when compared with software-based diagnosis methods that produce a low diagnostic resolution for even a single fault. These methods perform fault diagnosis using additional hardware in different ways, and the exact location of the candidate for a single fault in a single chain can be obtained. Significant hardware overhead of 12 transistors per cell was required in the early stages [19]. However, this was gradually reduced to achieve the same level of diagnostic resolution with only four transistors per cell [23]. It is possible to diagnose a single fault in a single chain with the maximum resolution even with a small hardware overhead of four transistors per cell. However, the diagnosis is limited to a single stuck-at fault.

Some studies [22], [25] on the diagnosis of a single fault in a single chain are still limited but enable the diagnosis of both stuck-at and transition-delay faults. Similarly, significant hardware overhead was required in the early stages of research [22] but was gradually decreased. The latest study [25] is a follow-up of another study [24] that diagnosed only a stuck-at fault. However, the latest study [25] enables the diagnosis of both stuck-at and transition-delay faults with only two transistors per cell. Although it uses the minimal hardware overhead, there is a reduction in the diagnostic resolution, and it is still limited to the diagnosis of a single fault in a single chain.

B. DIAGNOSIS OF MULTIPLE FAULTS

Many studies have been conducted on the diagnosis of a single fault in a single chain. Although the multiple faults may exist in a chain at the initial process stage, these methods only diagnose a single dominant fault closest to the scan-in or the scan-out ports, irrespective of the number of actual faults. Accordingly, studies have been conducted on methods to diagnose not only a single fault in a single chain but also multiple faults in the entire circuit [27]–[30]. The methods proposed in these studies are based on the flush tests of scan paths that can diagnose both stuck-at and transition-delay faults.

A previous study [27] proposed a diagnostic method using a double tree scan (DTS) architecture designed for a low-power scan test [26]. Faults are diagnosed on the DTS architecture using the flush tests through the several branching scan paths. The architecture diagnoses not only a single fault in a chain but also the multiple faults. However, it yields a poor diagnostic accuracy when the multiple faults are diagnosed because it adopts the law of parsimony (i.e., a method of adopting the smallest number of suspects to explain a particular faulty response). Consequently, a situation can occur in which the faulty cell is diagnosed as a normal cell, and the normal cell is diagnosed as a faulty cell.

A two-dimensional scan architecture was proposed [28] to diagnose the multiple faults without accuracy loss that enables scan shifting in the horizontal and vertical directions using one multiplexer per cell. It diagnoses the faults with a horizontal and vertical flush tests and performs an additional diagonal flush tests to diagnose the multiple faults. The faults can be diagnosed without a loss in accuracy even for the multiple faults, but the diagnostic resolution

gradually decreases significantly as the number of circuit faults increases. In addition, [28] requires the high routing overhead for the construction of the 2-dimensional scan architecture since it connects every cell crom the uppermost scan chain to the lowermost scan chain.

The number of additional ports required for the application of [28] to the circuit with a scan chain length, L_{sc}, and the number of scan chains, N_{sc}, is $2(L_{sc} - N_{sc})$, which increases as the scan chain length increases without the optimization of the square-shaped scan structure. An N-way scan architecture using one N:1 multiplexer per cell was proposed [28] to further improve the diagnostic resolution for the multiple faults. It guarantees the maximum resolution for up to N circuit faults. However, it requires excessive hardware overhead that is prohibitive.

Afterward, [29] was conducted to reduce the excessive number of additional ports in [28], [29] connects the additional vertical scan-in and out ports created for input/output of the test patterns in the vertical direction of [28]. In contrast to [28], where horizontal, vertical, and diagonal flush tests were performed separately using the vertical scan-in, out ports, [29] performs the flush tests by combining the horizontal and vertical tests and the horizontal and diagonal tests. The pattern loaded in the horizontal direction is used for the vertical and diagonal tests. Consequently, the fault diagnosis for the multiple faults is possible with a very small number of additional ports. However, due to the drastically reduced number of available test points, the diagnostic resolution of [29] is significantly lower than that of [28].

In [30], a reversible scan architecture that enables the reverse shifting from right to left as well as the forward shifting from left to right was proposed. As same as the other methods for diagnosing the multiple faults, one multiplexer per cell is used, and the shifting direction is determined according to the multiplexer control signal. Through this, the fault locations at both ends of each scan chain can be diagnosed by shifing in the flush pattern in one direction of each scan chain, and then shifting out it in the reverse direction as it was entered. However, it is no longer possible to analyze between the two diagnosed fault locations, so the diagnostic resolution decreases as the length of scan chain increases.

In this paper, a novel reconfigurable scan architecture and an associated test algorithm are proposed that enable an accurate high-resolution diagnosis even with a large number of faults in the entire circuit. Through the flush tests using numerous diagnosis paths obtained from the proposed reconfigurable scan architecture, a high-resolution diagnosis is possible for a large number of circuit faults. In addition, the proposed method reduces the routing overhead by scan partitioning.

In contrast to [28] and [29], which connect each scan flip-flop (SFF) from the SFF directly above through an additional path, the proposed scan architecture acquires the various diagnosis paths through an additional diagonal path connection between SFFs (Figure 1) and an optimized path control

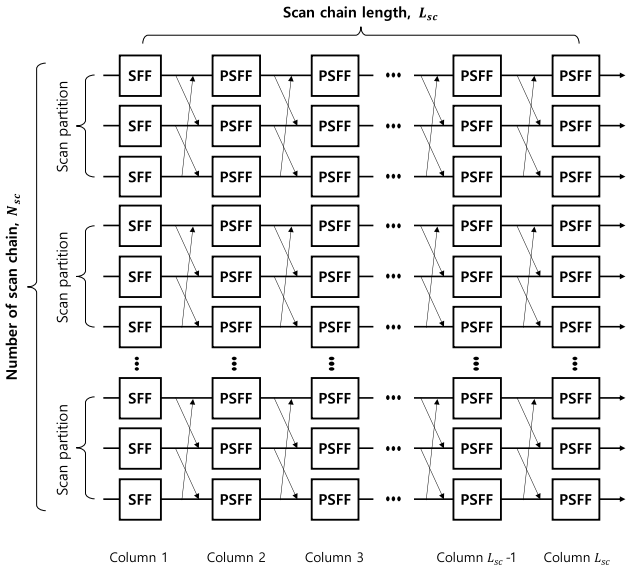


FIGURE 1. Schematic of the proposed reconfigurable scan architecture.

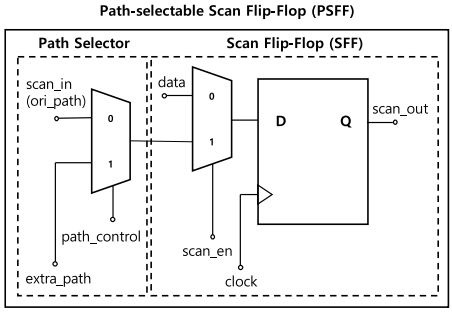


FIGURE 2. Path-selective scan flip-flop (PSFF) for the proposed reconfigurable scan architecture.

signals arrangement. The details of the proposed reconfigurable scan architecture are introduced in Sections III and IV.

III. PROPOSED RECONFIGURABLE SCAN ARCHITECTURE

A. RECONFIGURABLE SCAN ARCHITECTURE SCHEME

The schematic of the proposed reconfigurable scan architecture is presented in Figure 1. In contrast to the conventional scan architecture, the proposed scan architecture, consisting of a path-selective scan flip-flop (PSFF, Figure 2), enables shifting to the various reconfigured diagnosis paths and diagnosing the fault location with the flush tests through the corresponding diagnosis paths. These diagnosis path reconfigurations are performed in units of the scan partitions, as shown in Figure 1. An example of the diagnosis path reconfiguration within each scan partition is illustrated in Figure 3. The number of diagnosed fault candidates are gradually decreases by performing the flush tests through the various diagnosis paths in the scan partition.

In addition to the SFF, a conventional scan cell architecture, a 2:1 multiplexer is added in front of a scan-in pin of all SFFs in each PSFF to choose a scan path between the original scan path and an additional scan path. If the control signal of the added multiplexer is 0, the PSFF activates as a normal

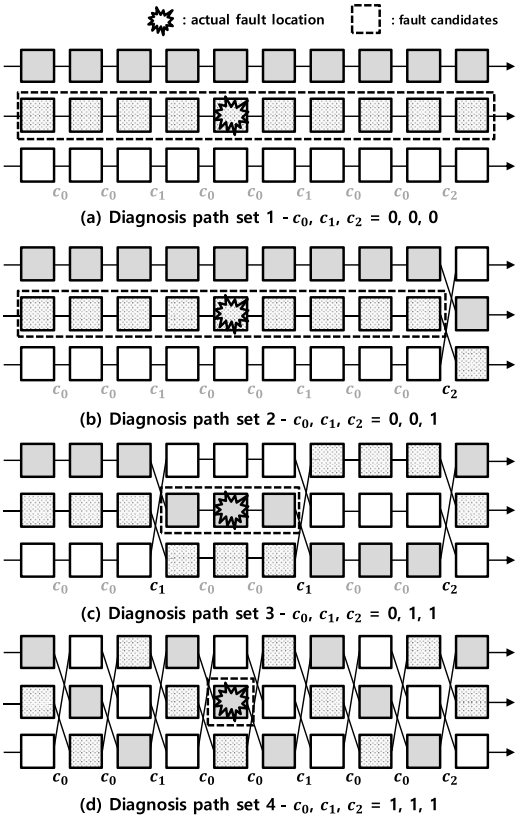


FIGURE 3. Example of a single fault diagnosis in a single scan partition of the proposed scan architecture ($L_{sc} = 10, N_{sp} = 3$).

scan cell. However, if the control signal is 1, it receives a scan-shifting signal from an additional scan path, which is an adjacent scan chain; thus, the scan path alternation occurs.

The scan chains in each scan partition of Figure 1 are connected from the scan chain immediately above through the additional path, and the uppermost scan chain is connected from the lowermost scan chain. Because the additional multiplexers are connected to the scan-in pin of the scan cell and are independent of the data pin for the capture operation, the proposed architecture does not affect the functional operation.

Several control signals are used to control the input paths of the multiplexers. All the multiplexers in the same column in Figure 1 use the same control signal. Accordingly, simultaneous path alternations are performed in each column unit. Various diagnosis paths can be obtained by turning on only a fraction of the control signals as shown in Figure 3. In Figure 3, $c_i (i = 0, 1, 2)$ represents the control signals connected to each column, and c_i with the black color indicated below Figure 3 (a), (b), (c), and (d) indicates that the corresponding control signal is turned on. Each control signal c_i is connected from the external input ports as a global signal like the scan enable signal in the scan test. Therefore, in all the scan partitions, the c_is with same i are always activated at the same time. For column 1, which is the first column, the scan path reconfiguration in front of the column is meaningless. Therefore, scan cells in column 1 are not replaced by PSFFs but remain as normal SFFs.

B. MULTIPLEXER CONTROL SIGNAL ROUTING ALGORITHM

Figure 3 illustrates that the number of fault candidates gradually decreases in each scan partition by performing the flush tests through the various obtained diagnosis paths. Each diagnosis path is reconfigured according to the combination of c_is, the control signals of PSFFs. As mentioned in Section III-A, all the PSFFs in the same column use the same control signal. Therefore, the control signals are first mapped for each column according to the algorithm to be described in this section. Then, the diagnosis path sets as shown in Figure 3 are constructed according to the combination of c_is. The control signal c_i connected to each column is indicated at the bottom of Figure 3(a)-(d), and c_i with the black color means that the corresponding control signal is turned on.

In each diagnosis path set of Figure 3, let the diagnosis path starting from the top scan-in port be diagnosis path 1, and the diagnosis paths starting from the scan-in ports below are diagnosis paths 2 and 3, sequentially. First, as a result of the flush test in Figure 3(a), diagnosis path 2 becomes the faulty path, and all the cells in the path become the fault candidates. Then, in Figure 3(b), only diagnosis path 2 is the faulty diagnosis path. Diagnosis path 1 becomes a fault-free path, which excludes one fault candidate within the path. The remaining fault candidates are the intersection of the faulty diagnosis paths in Figure 3(a) and (b). The flush tests are performed in the same way in Figure 3(c) and (d), and the final diagnosed fault candidate is the intersection point of all the diagnosis paths determined as the faulty diagnosis paths in each test.

The intersection points of each diagnosis path must be matched to each scan cell in the circuit one-to-one to achieve maximum diagnostic resolution. Otherwise, multiple locations can be diagnosed as the fault candidates even for a single fault. The multiplexer control signal connection algorithm in Figure 4 is the most effective method to create the one-to-one relationship between the intersection points of the diagnosis paths and the scan cells in the proposed reconfigurable scan architecture with the minimum number of control signals. It enables the path optimization for the high-resolution diagnosis in the proposed scan architecture.

The number of multiplexer control signals, N_{mc}, of the proposed reconfigurable scan architecture is defined as follows:

$$N_{mc} = \left\lfloor \log_{N_{sp}} (L_{sc} - 1) \right\rfloor + 1, \tag{1}$$

where L_{sc} is the scan chain length, and N_{sp} is the number of scan chains in each scan partition. All the multiplexers of the PSFFs arranged in the same column (Figure 1) are connected to the same control signals, as previously mentioned. And the control signal connection for the multiplexers in each column follows the pseudo algorithm in Figure 4.

Algorithm I: Multiplexer Control-Signal Connection Algorithm

L_{sc} is the length of scan chain
N_{sp} is the number of scan chains in each scan partition
$N_{mc} = \left\lfloor \log_{N_{sp}}(L_{sc} - 1) \right\rfloor + 1$
for $i = 1$ to $L_{sc} - 1$ **do**
  for $j = (N_{mc} - 1)$ to 0 **do**
    if i mod ${N_{sp}}^{j} = 0$ **begin**
      Connect all the multiplexers of the PSFFs in the $(i+1)^{th}$ column to the control-signal, c_j, if no control signal is connected yet .
      break
    end
  end for
end for

FIGURE 4. Multiplexer control-signal connection algorithm for the diagnosis path reconfiguration.

Assume that scan path alternation occurs behind each scan cell for a scan chain of length L_{sc} in Figure 1; the scan path change can occur behind $L_{sc} - 1$ columns, for all but the last ${L_{sc}}^{th}$ column. The PSFFs responsible for path alteration behind each i^{th} column are located in the $i + 1^{th}$ column. Therefore, in the algorithm in Figure 4, the control signal connection for the multiplexers in the $i + 1^{th}$ column is performed for all i^{th} columns (i from 1 to $L_{sc} - 1$).

A total of N_{mc} control signals are connected to the multiplexers of each $i + 1^{th}$ column, as depicted in Figure 3. The control signal, c_j (j from 0 to $N_{mc} - 1$), is connected first in descending order of the value of j. Each c_j is mapped to the multiplexers that are responsible for path alternation behind the multiple columns of N_{sp}^{j}. For the example of $L_{sc} = 10$ and $N_{sp} = 3$ (Figure 3), c_2 is connected behind the ninth column, which is the second power of 3, c_1 is connected behind the columns that are multiples of 3, and c_0 is connected behind the columns that are multiples of 1.

Accordingly, the control signals of all inserted multiplexers can be mapped, and N_{mc} is the number of additional ports required for the proposed reconfigurable scan architecture for input of the control signals. These N_{mc} additional ports can be reduced through sharing with test point input ports if a sufficient number of test points are inserted to improve the test coverage of the circuit. This is because both the test point input signals and the control signals have no effect on the circuit when the values are 0, and only operate when the values are 1. Therefore, it is possible with a simple structural modification by adding one input signal port to distinguish between test mode and diagnosis mode. The test algorithm using the connected control signals are described in Section IV.

C. SELECTION OF THE SCAN PARTITION SIZE

Fault diagnosis is performed separately for each scan partition, as depicted in Figure 1 in the proposed reconfigurable scan architecture. When N_{sp} gradually decreases from the same number of scan chains, N_{sc}, two effects occur.

First, the number of multiplexer control signals, N_{mc}, generated from Eq. (1) increases as N_{sp} decreases with fixed L_{sc}. If only a single fault exists in a scan partition, the exact fault location can be diagnosed with only some of the diagnosis paths obtained from combination of the control signals (Figure 3). However, if there are multiple faults in the scan partition, a diagnosis using a larger number of diagnosis paths is required to improve the diagnostic resolution. The number of control signals can be increased to increase the number of diagnosis paths by reducing N_{sp} for a fixed L_{sc}. Through this, it is possible to increase the number of diagnosis paths available for diagnosis in the scan partition.

Next, scan partitioning divides the faults in the entire circuit into several scan partitions. When diagnosing the multiple faults in a scan chain, the resolution of fault diagnosis inevitably decreases as the number of faults in the scan chain increases. Faults concentrated in one area can also affect the entire circuit and reduce the diagnostic resolution of the fault diagnosis. However, if the diagnosis is performed for each partition by scan partitioning—even if the diagnostic resolution of the partition where the faults are concentrated decreases—the influence of the corresponding concentrated faults on other partitions can be eliminated. Therefore, the diagnostic resolution may be improved.

Under the same N_{sc} condition, the effect of scan partitioning is further increased as the number of scan partitions increases as N_{sp} decreases. Therefore, an improvement in diagnostic resolution can be expected if the size of each scan partition is reducted, although the test time increases as the number of diagnosis paths to be used for the entire diagnosis process increases.

D. SCAN PARTITIONING FOR PLACE AND ROUTING

It is difficult to arrange the scan cells in a complete grid structure as depicted in Figure 3 after place and route (PNR). Each scan chain may not be placed precisely parallel, and each scan cell in the scan chain may not be arranged horizontally in sequence. However, it is possible to arrange the scan chains vertically in order through the PNR based on the scan chain arrangement in the tool (Figure 5). In this case, for N_{sp}, which is the number of the scan chains in the scan partition, it may be difficult to connect all the i^{th} scan cells vertically in N_{sp} scan chains through the additional paths as N_{sp} increases, because the irregularity between horizontal positions of N_{sp} scan cells in the scan partition increases. The routing complexity for the connection of the additional paths increases as N_{sp} increases.

However, the diagnostic resolution of the proposed scan architecture is improved as N_{sp} decreases, so only a small number of scan chains are grouped into a scan partition to ensure high diagnostic resolution. Therefore, the routing complexity for the connection of the additional paths can be reduced using a small N_{sp} for high diagnosis resolution, although the number of tests increases as N_{sp} decreases.

Moreover, the routing complexity of the proposed scan architecture is much lower than [28] or [29], which require the vertical scan paths that penetrate all the scan chains to diagnose the multiple faults. Although a routing issue can occur for the connection of the additional path because the scan chains are not parallel, routing complexity can be

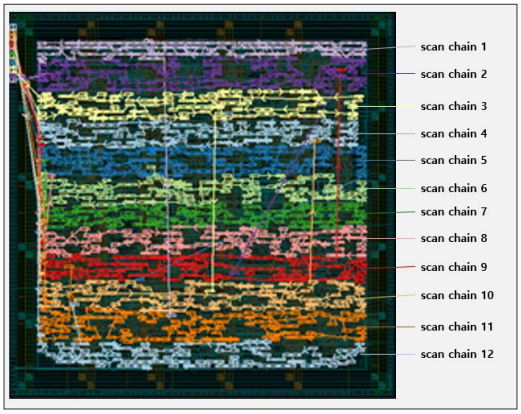


FIGURE 5. Place and routing result based on the scan chain arrangement ($N_{SC} = 12$).

minimized by reducing N_{sp} of the proposed scan architecture and proceeding with PNR based on the scan chain arrangement.

IV. DIAGNOSIS METHOD USING THE PROPOSED RECONFIGURABLE SCAN ARCHITECTURE

A. TEST FLOW FOR DIAGNOSIS USING RECONFIGURABLE SCAN ARCHITECTURE

The test flow for a diagnosis using the proposed reconfigurable scan architecture is performed through the flush tests with the various acquired diagnosis paths. It is possible to diagnose both stuck-at and transition-delay faults because the diagnosis process is based on the flush test, and the test is divided into two stages. Depending on the distribution of the faults in the entire circuit, the diagnosis can be terminated early at the first stage to reduce the test time with maximum diagnostic resolution. The early termination of this diagnosis is possible only under certain conditions; if the condition is not satisfied, the second stage is conducted to improve the diagnostic resolution.

The number of signal combinations that can be generated for N_{mc} multiplexer control signals is $2^{N_{mc}}$. It becomes the total number of diagnosis path sets available for the tests. In the first stage, only some of the $2^{N_{mc}}$ diagnosis path sets are used for the flush tests according to the test algorithm (Figure 6) introduced in Section IV-B. During this process, the fault candidates are initially reduced. If the number of faults in each of the scan partitions is only one or zero (because the number of faults in the entire circuit is small and the faults are evenly distributed), the correct and unique fault location is diagnosed, and the test is terminated early. It is possible to determine whether to terminate early based on the number of diagnosed fault candidates for each scan partition.

If there are two or more faults in a single scan partition, the flush tests at the first stage can still be used to diagnose them. However, for diagnosing multiple faults, non-faulty cells can also be diagnosed as fault candidates, which may lead to low diagnostic resolution. Therefore, when more than two fault candidates are diagnosed in a single scan partition, the second-stage test algorithm for fault candidate reduction

Algorithm II: First-Stage Flush Test Algorithm using Only Basic Diagnosis Paths

L_{sc} is the length of scan chain
N_{sp} is the number of scan chains in each scan partition
$N_{mc} = \lfloor \log_{N_{sp}}(L_{sc} - 1) \rfloor + 1$
for i = 0 to N_{mc} **do**
  Turn off every control signal, c_j which satisfy $0 \le j < N_{mc}$.
  Turn on every control signal, c_j which satisfy $N_{mc} - i \le j < N_{mc}$.
  Execute flush pattern test through current scan path.
  Narrow down faulty cell candidates according to newly flush pattern test result.
end for

FIGURE 6. First-stage flush test algorithm using only the basic diagnosis paths.

Algorithm III: Second-Stage Flush Test Algorithm using Remaining Diagnosis Paths

L_{sc} is the length of scan chain
N_{sp} is the number of scan chains in each scan partition
$N_{mc} = \lfloor \log_{N_{sp}}(L_{sc} - 1) \rfloor + 1$
for i = 0 to $2^{N_{mc}} - 1$ **do**
  if $i == (2^k - 1)$ is not satisfied for any integer k **then** // select remaining diagnosis paths
    $temp = i$
    for $j = N_{mc} - 1$ to 0 **do** // binary conversion for control signals
      if $temp \ge 2^j$ **then**
        multiplexer control signal, $c_{N_{mc}-1-j} = 1$
        $temp = temp - 2^j$
      else
        multiplexer control signal, $c_{N_{mc}-1-j} = 0$
    end for
    Execute flush test through current diagnosis path formed by control signals.
    Narrow down faulty cell candidates according to new flush -pattern test result.
end for

FIGURE 7. Second-stage flush test algorithm using the remaining diagnosis paths.

(Figure 7) is applied after the first stage to improve the diagnostic resolution.

B. FIRST-STAGE FLUSH TEST USING BASIC DIAGNOSIS PATHS ONLY

After the multiplexer control signal is connected according to the algorithm presented in Section III-B, the circuit faults can be diagnosed in the scan partition units according to the algorithm (Figure 6). It uses the characteristics of the flush test to check for the presence of the fault in a diagnosis path where the flush test is conducted. In the first stage, flush tests are performed using only some of the $2^{N_{mc}}$ diagnosis path sets that can be generated from the combination of multiplexer control signals in the proposed scan architecture. A total of $N_{mc} + 1$ diagnosis path sets are used, which is the minimum number of diagnosis path sets required to match the intersection of each diagnosis path with each scan cell one-to-one.

For all values of j in the range 0 to $N_{mc} - 1$, the flush test is started with all control signals, c_j, off. During this process, the first flush test is executed, and all scan cells in the diagnosis path containing more than one fault are first diagnosed as fault candidates. After the first test, signals c_j are individually turned on in descending order of j, and the flush tests are performed through the reconfigured diagnosis path sets. The diagnosis paths are reconfigured as the multiplexer control signals are individually turned on.

The flush test results through these reconfigured diagnosis path sets enable scan cells in the diagnosis paths identified as fault-free paths to be removed from the fault candidates. The flush tests using these diagnosis paths decreases the number

of diagnosed fault candidates, and the intersection of all the faulty diagnosis paths represents the final fault candidates. Both stuck-at and transition-delay faults can be diagnosed using the flush test.

Figure 3 illustrates an example of the diagnosis performed using the algorithm in Figure 6 for a circuit with $L_{sc} = 10$ and $N_{sc} = 3$. Assuming that there is a single stuck-at fault or a transition-delay fault in the fifth cell of the second chain, a flush test is first performed on the diagnosis path set (a) where all multiplexer control signals are zero, confirming that the fault is in the second diagnosis path. Accordingly, all the scan cells in the second diagnosis path first become fault candidates.

Next, c_2, c_1, and c_0 are turned on individually, and flush tests are performed on the reconfigured diagnosis paths. During this process, scan cells in the reconfigured fault-free diagnosis paths are gradually excluded from the fault candidates. This process iteratively narrows down the fault candidate range using the intersection of the candidate range determined by the flush test for each path. It is possible to diagnose the unique fault candidate accurately for both the stuck-at and the transition-delay faults in the presence of a single fault.

Consequently, it is possible to obtain the maximum diagnostic resolution for a single fault, irrespective of the fault location. However, when there are multiple circuit faults, the resolution decreases depending on the fault location, as depicted in Figure 8(a). In the example, eight fault candidates are diagnosed for three faults after the flush test on all the diagnosis paths. There are 2.666 candidates per a fault; thus, the resolution is reduced considerably compared with the case of a single fault. This value may vary depending on the fault location in the scan partition, since the intersections of faulty diagnosis paths are generated differently depending on the location of the faults. Additional test processes that can maximize the diagnostic resolution for these multiple faults are described in the next section.

C. SECOND-STAGE FLUSH TEST USING FULL DIAGNOSIS PATHS

If the number of faults in each scan partition is one or zero, the exact location of the fault can be found even with a flush test that uses only basic diagnosis paths (Figure 3) because the intersection of each path and each scan cell has a one-to-one relationship. Only when there are two or more faults in each scan partition is the number of fault candidates per scan partition diagnosed as two or more. Consequently, if the number of diagnosed fault candidates is two, two fault locations have been accurately identified. Even in this case, no further tests are required to improve the resolution.

If the number of fault candidates for each partition is diagnosed as two or fewer, the diagnosis in the corresponding partition is complete. Therefore, if fewer than two fault candidates are diagnosed in all partitions, the test is terminated early without proceeding to the second stage. Otherwise, the second-stage test is performed using all the remaining

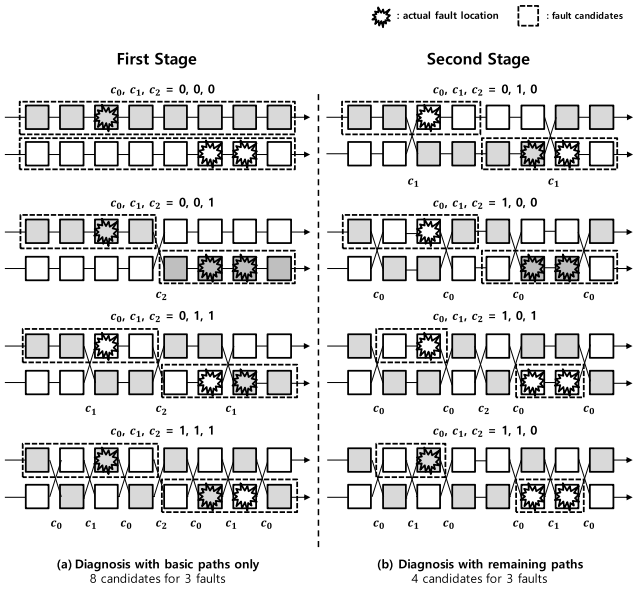


FIGURE 8. Example of the multiple faults diagnosis in a single scan partition of the proposed scan architecture ($L_{sc} = 8, N_{sp} = 2, N_f = 3$).

diagnosis paths not used in the first-stage test to improve the diagnostic resolution. The diagnosis paths in the second stage test are formed according to the algorithm in Figure 7.

The total number of diagnosis path sets that can be generated from N_{mc} multiplexer control signals is $2^{N_{mc}}$, a number including the $N_{mc} + 1$ basic diagnosis paths used in the first-stage test. As described in Section IV-B, the diagnosis paths in the first stage are formed by turning on each control signal, c_j, sequentially. In this case, if the control signal, c_j, used in the diagnosis path composition during each flush test is considered a single-digit number in binary and listed in ascending order of j from left to right, the following rules emerge. If the constructed binary number is converted to a decimal number, there is an integer, k, for which the corresponding converted value matches $2^k - 1$. Based on this characteristic, only the remaining diagnosis paths used in the second-stage test can be selected to exclude the signal combination that satisfies the condition in the algorithm (Figure 7).

Figure 8 illustrates an example of the diagnosis of three faults in the scan partition with $L_{sc} = 8$ and $N_{sp} = 2$; (a) indicates the first-stage test using basic diagnosis paths, and (b) indicates the second-stage test using all remaining diagnosis paths. When converting the 3-bit binary numbers $\{c_0, c_1, c_2\}$ in Figure 8(a) into decimal numbers, they become 0, 1, 3, and 7, which all correspond to the characteristics of the basic paths described earlier.

Subsequently, the remaining paths in Figure 8(b) are used as diagnosis paths in the second stage. Because additional diagnosis paths are used, the number of fault candidates previously diagnosed as eight for the three faults is reduced to four. Accordingly, flush tests can be performed by reconfiguring various diagnosis paths with a combination of arranged multiplexer control signals, and diagnosis can be performed in units of the scan partitions.

The number of flush tests using all the diagnosis paths, N_{test}, of the proposed reconfigurable scan architecture is defined as follows:

$$N_{test} = 2^{N_{mc}} = 2^{\left\lfloor \log_{N_{sp}}(L_{sc}-1) \right\rfloor + 1}, \quad (2)$$

where L_{sc} is the scan chain length, and N_{sp} is the number of scan chains in each scan partition. If N_{sp} is reduced, more diagnosis paths are obtained for the fixed L_{sc} condition, and the number of scan partitions increases, increasing diagnostic resolution. Therefore, when considering diagnostic resolution only, the design with the highest performance is $N_{sp} = 2$. However, if a quick test is required, the trade-off between the diagnostic resolution and the test time can be adjusted by increasing N_{sp}.

D. FLUSH PATTERN MODIFICATION FOR DIAGNOSTIC ACCURACY IMPROVEMENT

The fault locations are diagnosed in the proposed scan architecture using the flush tests to the diagnosis paths. The diagnosis paths are reconfigured using the signal inserted through the path control pin of Figure 2. If the diagnosis paths are not configured as intended during the flush tests due to the stuck-at fault in the path control pin, the diagnosis results of the proposed scan architecture become unreliable. Therefore, it is necessary to filter out the circuits prior to fault diagnosis that cannot be accurately tested due to the faults in the path control pin.

With the following flush pattern modification method, it is possible to filter out the circuits with problems in diagnosis path reconfiguration due to the stuck-at faults in the path control pin. Because the fault locations are diagnosed in the proposed scan architecture using the flush tests in which the diagnosis paths are fixed for sufficiently long clock cycles, the transition delay faults in the path control pin has no effect. Therefore, the transition delay faults in the path control pin is not considered.

The concept of the flush pattern modification for diagnostic accuracy improvement is simple. The flush pattern used in the flush test usually assumes the form of repeating "0011," which can also be made by repeating "1001," "1100," and "0110." Given this characteristic, if the scan partition consists of four or fewer scan chains, different flush pattern combinations can be shifted in for each scan chain, equivalent to labeling each scan chain.

Figure 9 illustrates an example of the scan partition consisting of three scan chains, where "0011," "1001," and "1100" flush patterns are inserted into each scan chain. After performing the flush test using these modified flush patterns through diagnosis paths, the flush test results are classified into three categories: the normal response (which is the same as the inserted flush pattern), the fail response affected by the faulty scan cell, and the fail response affected by the faulty multiplexer control signal pin. The fail response affected by the faulty scan cell marked "FFFF" in Figure 9 can be distinguished from the faulty multiplexer affected fail response

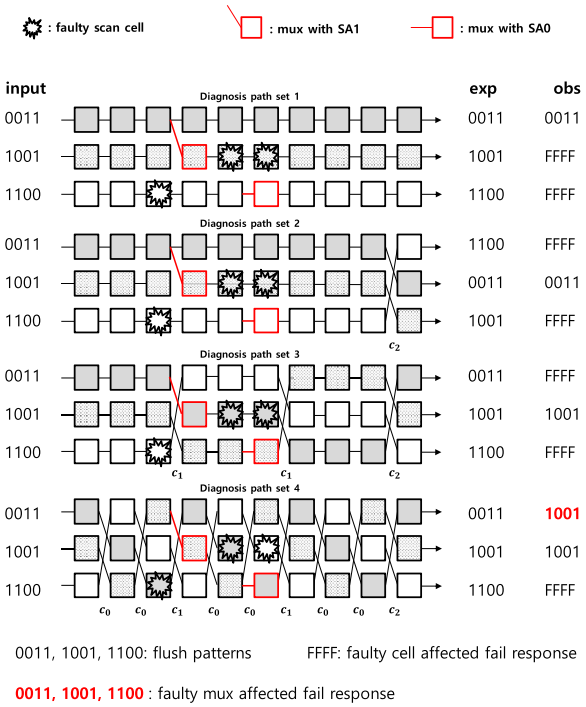


FIGURE 9. Example of the multiple faults diagnosis in a single scan partition of the proposed scan architecture ($L_{sc} = 8, N_{sp} = 2, N_f = 3$).

because the ratios of 0 to 1 differ, such as "0000," "1111," "0111," and "0001".

Excluding these fail responses affected by the faulty cells, the observed test responses are compared with the expected responses. If the test response differs from the expected response, it means that the path selection is not properly performed at some point in the scan architecture. In this case, because the accuracy of the diagnosis result in the scan partition may be lower, the diagnosis result of the corresponding scan partition is ignored. Depending on the location and the number of faults, some path selector faults are not filtered out in this way, but a significant number of faults can be filtered to improve diagnostic accuracy.

For the scan partition consisting of four or more scan chains, the same test can also be performed using a longer flush pattern, such as "000111." By simply modifying the flush pattern accordingly, it is possible to prevent a loss in the diagnostic accuracy due to the faults occurring in additional hardware without adding test costs. Because the additional multiplexers are used only for the scan chain diagnosis, it is possible to improve the yield using only the diagnosis results from the filtered circuits determined to have no fault in the multiplexer.

E. FAULT MODELING

Except for the multiplexer control signal pin covered in Section IV-D, there are a total of 4 possible fault locations in the PSFF as shown in Figure 10. In the examples of 9 PSFFs in Figure 10, a possible fault locations in the PSFF and the paths which may be affected by the faults are indicated based

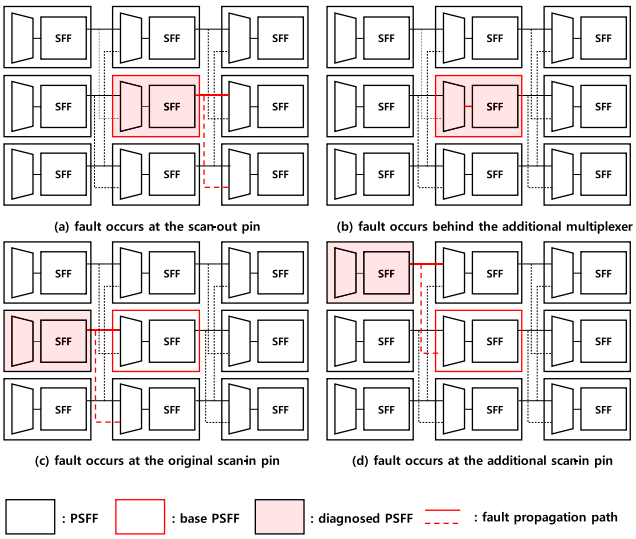


FIGURE 10. Example of the available fault locations in PSFF except for the multiplexer control signal pin.

on the central PSFF. First, in the cases of Figure 10 (a) and (b), the same effect as the fault propagation from the central PSFF's scan-out pin appears, so the central PSFF is diagnosed as the fault location. And Figure 10 (c) and (d) are cases where the fault occurs in the input pins of the multiplexer added in the PSFF. In these cases, the same effect as the propagation from the fault in the front PSFF connected to the corresponding pin occur, and the corresponding PSFF is diagnosed as the fault location. In this way, the fault can be accurately diagnosed regardless of coupling by assuming that the fault exists in the scan-out pin of each scan cell during fault modeling.

V. EXPERIMENTAL RESULTS

This section presents the experimental results of scan chain fault diagnosis using the proposed reconfigurable scan architecture. A performance comparison with existing methods for diagnosing a single fault in the circuit is presented in Section V-A. In addition to the existing hardware-based diagnosis methods, the experiments described in Section V-A were conducted to compare the software-based diagnosis method using a commercial tool, Synopsys TetraMAX. The experiments were conducted on ISCAS'89 and ITC'99 benchmark circuits synthesized with Synopsis Design Compiler. The TSMC 32-nm cell library was used for the synthesis. In Section V-B, the diagnostic resolution of the proposed scan architecture in the presence of multiple faults is compared with [28]–[30], which can diagnose the multiple faults without accuracy loss.

In contrast to software-based diagnosis methods, the hardware-based diagnosis methods, [28]–[30], and the proposed method do not require capture operations. Only the two elements that constitute the scan architecture, the scan chain length and the number of scan chains, affect the diagnostic performance of these methods. Therefore, the experiments were performed by changing the number of scan chains for a fixed number of scan cells in the various test circuits to compare the diagnostic resolution according to these two variables. After a certain number of faults were inserted at random locations in the circuit, the number of diagnosed fault candidates was measured, and the number of average fault candidates was calculated over 1,000 iterations.

A comparison of the test time required in this process is presented in Section V-C. Then, in contrast to Section V-B, where only rough comparisons were made for the additional ports count in each method, detailed comparisons of additional ports count under various conditions are provided in Section V-D. Finally, Section V-E compares the area and the routing overhead of each method in detail for ISCAS'89 and ITC'99 benchmark circuits.

A. PERFORMANCE COMPARISON FOR A SINGLE FAULT DIAGNOSIS

Table 1 presents the diagnostic performance when a single stuck-at fault or a single transition-delay fault is inserted and diagnosed for the ISCAS'89 and ITC'99 benchmark circuits. Experiments were performed by varying the number of inserted scan chains for each circuit. After diagnosis using the proposed and existing methods, comparisons were made in terms of various indicators: the minimum, maximum, and average number of candidates for an inserted fault (min), (max), (avg), number of added transistors per single scan cell (N_{TR}/N_{SFF}), and the number of additional ports (extra I/O). Circuit and N_{SFF} at the top of the tables represent the name of the circuit used in the experiment and the number of SFFs in the circuit, respectively.

First, for software-based diagnosis, it was possible to diagnose only one fault candidate for some fault locations (Table 1). In some cases, however, several fault candidates were identified even when there was only a single stuck-at fault. For b19, up to 300 fault candidates were identified for a single fault. The average number of fault candidates was considerably smaller than the maximum number of candidates. However, if the faults were present in the position with the maximum number of candidates, physical failure analysis that investigates the diagnosed fault candidate locations after diagnosis becomes a significant challenge.

The methods in [23], [25], and [28]–[30], and the proposed hardware-based diagnosis method result in additional hardware. However, both the stuck-at fault and transition-delay fault have a maximum of one or two fault candidates for a single fault, indicating high diagnostic resolution regardless of the fault location. For [23], only the diagnosis of stuck-at faults is possible. Among the existing methods, [23] and [25] require a small number of transistors per cell, but only the diagnosis of a single fault is possible.

The method in [28]–[30], and the proposed method exhibit a higher N_{TR}/N_{SFF} than that in [23] and [25]; thus, they incur higher hardware overhead, however, multiple faults can be diagnosed as described in Section V-B. In diagnosing a single fault, [28]–[30], and the proposed method also exhibit the maximum diagnostic resolution. The diagnostic resolution

TABLE 1. Performance comparison on the benchmark circuits for a single fault.

*: stuck-at fault diagnosis only
**: $N_{sp} = 2$ condition(maximum I/O)

circuit	N_{SFF}	N_{sc}	software-based diagnosis			[23]*			[25]			[28]			[29]			[30]			[proposed]**		
			min	max	avg	max	N_{TR}/N_{SFF}	extra I/O	max	N_{TR}/N_{SFF}	extra I/O	max	N_{TR}/N_{SFF}	extra I/O	max	N_{TR}/N_{SFF}	extra I/O	max	N_{TR}/N_{SFF}	extra I/O	max	N_{TR}/N_{SFF}	extra I/O
s9234	228	2	1	21	3.944	1	4.000	2	2	2.000	1	1	6.053	225	1	6.000	1	1	6.000	1	1	5.947	7
		5	1	10	1.625	1	4.000	2	2	2.000	1	1	6.130	83	1	6.000	1	1	6.000	1	1	5.870	6
		10	1	6	1.450	1	4.000	2	2	2.000	1	1	6..261	27	1	6.000	1	1	6.000	1	1	5.739	5
s13207	336	2	1	15	2.286	1	4.000	2	2	2.000	1	1	6.036	333	1	6.000	1	1	6.000	1	1	5.964	8
		5	1	15	2.229	1	4.000	2	2	2.000	1	1	6.088	127	1	6.000	1	1	6.000	1	1	5.912	7
		10	1	15	2.140	1	4.000	2	2	2.000	1	1	6.176	49	1	6.000	1	1	6.000	1	1	5.824	6
s15850	597	2	1	16	2.070	1	4.000	2	2	2.000	1	1	6.020	595	1	6.000	1	1	6.000	1	1	5.980	9
		5	1	16	1.749	1	4.000	2	2	2.000	1	1	6.050	231	1	6.000	1	1	6.000	1	1	5.950	7
		10	1	16	1.715	1	4.000	2	2	2.000	1	1	6.100	101	1	6.000	1	1	6.000	1	1	5.900	6
s38417	1636	2	1	31	3.376	1	4.000	2	2	2.000	1	1	6.007	1633	1	6.000	1	1	6.000	1	1	5.993	10
		5	1	31	3.226	1	4.000	2	2	2.000	1	1	6.018	647	1	6.000	1	1	6.000	1	1	5.982	9
		10	1	31	3.059	1	4.000	2	2	2.000	1	1	6.037	309	1	6.000	1	1	6.000	1	1	5.963	8
s38584	1452	2	1	18	1.631	1	4.000	2	2	2.000	1	1	6.008	1449	1	6.000	1	1	6.000	1	1	5.992	10
		5	1	16	1.563	1	4.000	2	2	2.000	1	1	6.021	573	1	6.000	1	1	6.000	1	1	5.979	9
		10	1	19	1.422	1	4.000	2	2	2.000	1	1	6.041	273	1	6.000	1	1	6.000	1	1	5.959	8
b18	3276	2	1	300	117.218	1	4.000	2	2	2.000	1	1	6.003	3272	1	6.000	1	1	6.000	1	1	5.996	11
		5	1	237	89.329	1	4.000	2	2	2.000	1	1	6.009	1302	1	6.000	1	1	6.000	1	1	5.990	10
		10	1	234	53.089	1	4.000	2	2	2.000	1	1	6.018	636	1	6.000	1	1	6.000	1	1	5.981	9
b19	6564	2	1	300	150.278	1	4.000	2	2	2.000	1	1	6.003	6560	1	6.000	1	1	6.000	1	1	5.998	12
		5	1	300	111.166	1	4.000	2	2	2.000	1	1	6.009	2616	1	6.000	1	1	6.000	1	1	5.995	11
		10	1	237	79.451	1	4.000	2	2	2.000	1	1	6.018	1294	1	6.000	1	1	6.000	1	1	5.990	10

of the proposed method for a single fault is independent of N_{sp} because of the one-to-one relationship described in Section IV-B. The proposed method requires a significantly smaller number of additional ports than the method in [28], even for the $N_{sp} = 2$ condition that requires the maximum extra I/O. The extra I/O in [28] increase significantly as the scan chain length increases. However, [29], which significantly reduces the extra I/O of [28] using the circular method, requires only a single additional port. And [30] also requires only a single extra I/O. A detailed comparison of the additional ports count under various conditions is presented in Section V-D.

B. DIAGNOSTIC RESOLUTION COMPARISON FOR THE MULTIPLE FAULTS DIAGNOSIS

Table 2 presents a comparison of the diagnosis resolution for the multiple faults with the proposed and existing methods. The experiments were conducted by changing the number of scan chains, N_{sc}, for circuits with a fixed number of scan cells, N_{SFF}, at 720, 1,440, and 2,160 and inserting the faults in random locations. N_f represents the total number of faults inserted in the circuit. The execution of the experiments for the proposed method was divided into the following conditions: N_{sp}, the numbers of scan chains in each scan partition, which were 4, 3, and 2, respectively (Table 2 and Figure 11). Graphs in Figure 11 illustrate the average number of diagnosed fault candidates per actual faults after diagnosis in each experimental condition.

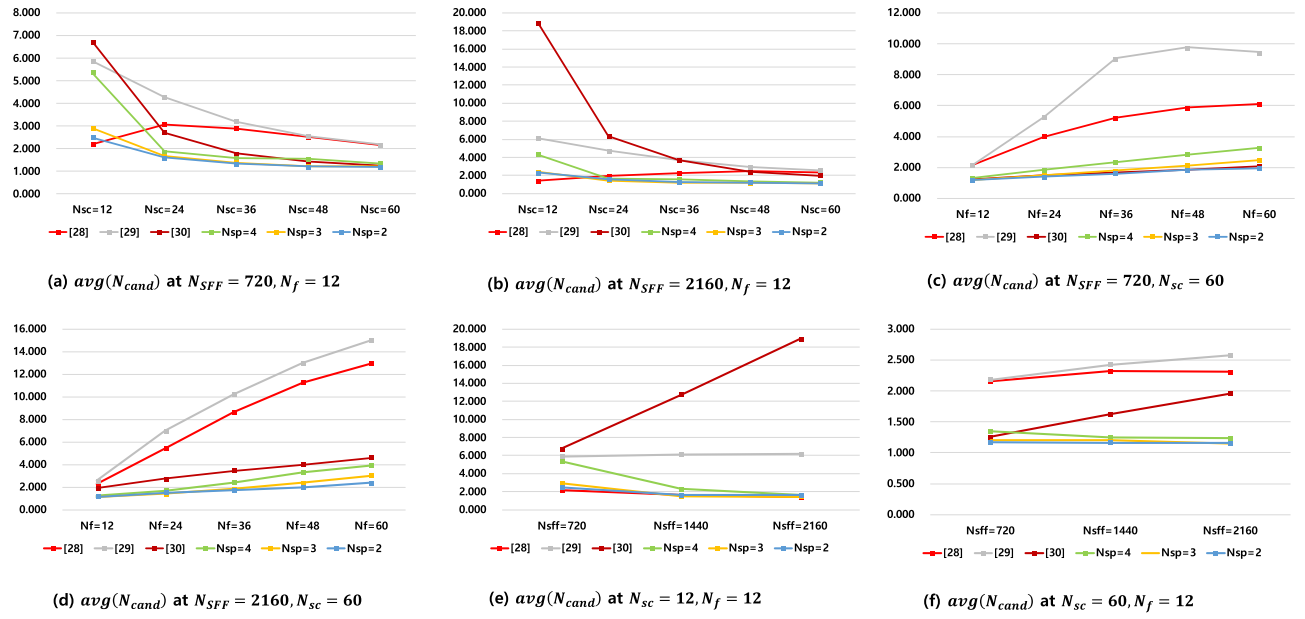
First, the experimental results depicted in Figure 11 (a) and (b) confirm that the diagnosis resolution of the proposed method increases as the number of scan chains, N_{sc}, increases and the number of scan chains in each scan partition, N_{sp}, decreases. These results confirm the improvement in the diagnostic resolution from scan partitioning. When $N_{sc} = 12$, where scan partitioning is insufficiently performed due to the small number of scan chains in the circuit, the diagnostic resolution of the propose method is no higher than that of [28]. However, the diagnostic resolution of the proposed method increases as the number of scan chains increases. This relationship is advantageous in a multi-scan test environment where multiple scan chains are inserted to reduce the test time. The proposed scheme designed with $N_{sp} = 2$ under the condition of $N_{SFF} = 2160$, $N_{sc} = 60$ in Figure 11 (b) demonstrates 81.56%, 84.05%, and 45.66% reductions in fault candidates for 60 faults compared with [28], [29], and [30], respectively.

Because of structural characteristics, when N_{SFF} is constant, the diagnostic resolution of [28] decreases as N_{sc} increases until the number of scan chains equals the scan chain length and then increases again (Table 2 and Figure 11). And [29] has a structure in which the test points in [28] are significantly reduced to reduce excessive extra I/O, so the diagnostic resolution is inevitably lower than that of [28], as confirmed by Table 2 and Figure 11. And in the case of [30], since only the faults at both ends of each scan chain can be diagnosed, all the cells between the two fault locations become the fault candidates after diagnosis. Therefore, the diagnostic resolution of [30] decreases as L_{sc} increases according to the increase in N_{SFF} or decrease in N_{sc}.

Figure 11 (c) and (d) depict the experimental results when the number of scan chains is fixed and only the number of faults increases. In [28]–[30] and the proposed method,

TABLE 2. Number of the diagnosed fault candidates per single fault.

N_{SFF}	N_{sc}	L_{sc}	N_f	[28]			[29]			[30]			Proposed								
													$N_{sp}=4$			$N_{sp}=3$			$N_{sp}=2$		
				min	max	avg	min	max	avg	min	max	avg	min	max	avg	min	max	avg	min	max	avg
720	12	60	12	1.167	5.167	2.198	2.417	10.000	5.887	1.083	15.250	6.754	1.333	20.917	5.371	1.000	16.250	2.909	1.000	21.000	2.488
			36	3.278	7.972	5.212	6.111	20.000	15.030	5.250	12.722	8.918	7.056	20.000	14.917	6.778	20.000	12.474	3.861	15.444	8.831
			60	4.383	7.900	6.088	6.600	12.000	11.812	5.783	9.800	7.726	8.150	12.000	11.587	7.900	12.000	11.282	6.033	12.000	10.299
	36	20	12	1.333	5.500	2.887	1.417	6.167	3.186	1.000	4.750	1.787	1.000	4.583	1.578	1.000	6.167	1.379	1.000	7.250	1.326
			36	4.750	12.389	7.779	5.250	18.333	8.907	1.417	4.694	2.775	1.833	5.944	3.532	1.417	5.694	3.015	1.056	6.028	2.249
			60	5.950	10.850	8.269	6.650	12.000	9.894	2.150	4.283	3.225	2.900	7.167	4.982	2.933	6.667	4.541	1.417	6.000	3.166
	60	12	12	1.083	5.000	2.154	1.167	4.917	2.183	1.000	2.417	1.258	1.000	3.083	1.342	1.000	3.750	1.207	1.000	4.667	1.173
			36	3.333	7.389	5.220	3.389	15.000	9.064	1.111	2.556	1.695	1.194	4.083	2.365	1.028	3.056	1.810	1.000	3.889	1.594
			60	4.367	8.067	6.101	4.767	11.600	9.451	1.400	2.667	2.083	1.983	4.467	3.271	1.550	3.783	2.473	1.117	3.783	1.964
1440	12	120	12	1.000	3.333	1.624	2.667	10.000	6.140	1.250	34.500	12.730	1.000	30.417	3.783	1.000	30.750	2.361	1.000	40.250	2.678
			36	2.528	5.528	3.733	6.444	40.000	26.741	8.694	26.000	17.206	10.833	36.667	23.767	6.667	32.083	18.246	4.167	30.111	12.837
			60	3.700	6.717	5.110	7.517	24.000	23.072	10.067	19.417	15.147	14.767	24.000	22.372	12.383	24.000	21.256	11.500	24.000	18.380
	36	40	12	1.333	4.917	2.679	1.833	6.000	3.515	1.000	10.000	2.635	1.000	6.417	1.453	1.000	10.750	1.274	1.000	7.833	1.386
			36	5.583	13.917	9.234	7.444	18.000	12.360	2.417	7.778	4.841	1.972	9.472	4.477	1.111	8.861	2.905	1.056	9.472	2.354
			60	8.150	16.450	12.072	10.533	20.400	14.658	3.950	8.183	5.795	4.567	11.967	7.892	2.717	10.167	5.438	1.483	9.300	3.910
	60	24	12	1.250	4.333	2.319	1.417	4.500	2.427	1.000	6.000	1.626	1.000	4.333	1.251	1.000	3.417	1.201	1.000	5.167	1.161
			36	4.611	12.583	7.682	4.556	24.000	8.547	1.222	4.528	2.573	1.222	5.306	2.244	1.028	5.667	2.164	1.000	5.972	1.682
			60	7.067	13.833	10.401	7.650	22.000	12.096	2.117	4.417	3.435	1.933	6.100	3.533	1.833	6.267	3.197	1.150	4.933	2.308
2160	12	180	12	1.000	2.667	1.410	2.250	11.000	6.153	1.250	48.917	18.903	1.000	45.250	4.311	1.000	45.250	2.396	1.000	31.583	2.314
			36	2.056	4.639	2.985	7.250	60.000	37.542	14.444	37.250	25.812	16.389	55.000	34.535	10.000	50.000	26.278	3.472	32.944	13.594
			60	3.100	5.550	4.174	8.250	36.000	34.618	16.550	28.450	22.502	23.683	36.000	33.399	19.200	36.000	31.402	13.450	36.000	24.393
	36	60	12	1.167	4.083	2.297	1.833	6.083	3.705	1.000	12.500	3.676	1.000	11.833	1.590	1.000	7.250	1.231	1.000	10.917	1.288
			36	5.556	14.111	8.655	8.861	21.250	13.926	2.806	12.333	6.859	2.417	16.194	6.006	1.222	10.833	3.380	1.056	11.417	2.814
			60	8.983	17.467	12.911	12.517	23.650	17.827	5.033	12.433	8.393	6.350	19.283	11.172	2.600	15.000	7.224	1.700	12.883	4.761
	60	36	12	1.250	4.167	2.308	1.250	4.083	2.576	1.000	5.917	1.958	1.000	6.000	1.236	1.000	4.583	1.153	1.000	6.833	1.158
			36	5.389	13.667	8.634	6.306	15.444	10.205	1.250	6.194	3.471	1.111	7.028	2.417	1.000	5.444	1.866	1.000	8.833	1.754
			60	9.250	18.400	12.984	10.250	21.350	14.989	2.600	6.317	4.610	2.133	7.717	4.239	1.433	5.850	3.022	1.083	6.700	2.391



(a) $avg(N_{cand})$ at $N_{SFF}=720, N_f=12$

(b) $avg(N_{cand})$ at $N_{SFF}=2160, N_f=12$

(c) $avg(N_{cand})$ at $N_{SFF}=720, N_{sc}=60$

(d) $avg(N_{cand})$ at $N_{SFF}=2160, N_{sc}=60$

(e) $avg(N_{cand})$ at $N_{sc}=12, N_f=12$

(f) $avg(N_{cand})$ at $N_{sc}=60, N_f=12$

FIGURE 11. Diagnostic resolution comparison of the multiple faults.

the number of diagnosed fault candidates per faults increases as the number of faults increases. However, the rate of increase in the proposed method is substantially lower, indicating high diagnostic resolution performance, especially under the $N_{sp}=2$ condition, when the number of scan chains in each scan partition is small. The diagnostic resolution of [30] is relatively high under the condition with $N_{SFF}=720$ as shown in Figure 11 (c), but as mentioned in the previous paragraph, the diagnostic resolution of [30] decreases when L_{sc} increases as the circuit size increases under the same

TABLE 3. Comparison of the test time and the additional ports count.

N_{SFF}	N_{sc}	L_{sc}	[28]		[29]		[30]		Proposed					
									$N_{sp}=4$		$N_{sp}=3$		$N_{sp}=2$	
			N_{test}	extra I/O	N_{test}	extra I/O	N_{test}	extra I/O	N_{test}	extra I/O	N_{test}	extra I/O	N_{test}	extra I/O
720	12	60	4	97	6	1	6	1	8	3	16	4	64	6
	24	30	4	13	6	1	6	1	8	3	16	4	32	5
	36	20	4	1	6	1	6	1	8	3	8	3	32	5
	48	15	4	1	6	1	6	1	4	2	8	3	16	4
	60	12	4	1	6	1	6	1	4	2	8	3	16	4
1440	12	120	4	217	6	1	6	1	16	4	32	5	128	7
	24	60	4	73	6	1	6	1	8	3	16	4	64	6
	36	40	4	9	6	1	6	1	8	3	16	4	64	6
	48	30	4	1	6	1	6	1	8	3	16	4	32	5
	60	24	4	1	6	1	6	1	8	3	8	3	32	5
2160	12	180	4	337	6	1	6	1	16	4	32	5	256	8
	24	90	4	133	6	1	6	1	16	4	32	5	128	7
	36	60	4	49	6	1	6	1	8	3	16	4	64	6
	48	45	4	7	6	1	6	1	8	3	16	4	64	6
	60	36	4	1	6	1	6	1	8	3	16	4	64	6

conditions as shown in Figure 11 (d). And in Figure 11 (c), the diagnostic resolution of [29] when $N_f = 60$ may seem to be higher than when $N_f = 48$. However, this phenomenon occurs because all the cells are diagnosed as fault candidates due to reaching the diagnostic limit. The number of diagnosed fault candidates cannot exceed the total number of cells.

Figure 11 (e) and (f) show the experimental results for the case where L_{sc} increases as N_{SFF} increases with fixed N_{sc}. As shown in Figure (e) and (f), [28], [29] and the proposed method have relatively small changes in diagnostic resolution according for L_{sc} changes due to their structures. However, the diagnostic resolution of [30] decreases significantly when L_{sc} increases as N_{SFF} increases with fixed N_{sc}, as shown in Figure 11 (e) and (f). The average number of diagnosed faults per actual faults of [30] is 18.903 in the case of $N_{SFF} = 2160$, $N_{sc} = 12$ and $N_f = 12$ in Figure 11 (f), where $L_{sc} = 180$. Therefore, [30] is difficult to obtain high diagnostic resolution in large circuits.

Although the experimental results for only some N_f conditions are depicted in Table 2 and Figure 11, the proposed scan architecture illustrates higher diagnostic resolution for all N_f conditions than [28] and [29] except for $N_{sc} = 12$—for which the number of the scan partitions is not sufficiently secured because the total number of the scan chains is too small. Although the diagnostic resolution decreases as N_f increases, this is the same for all the diagnostic methods.

C. TEST TIME COMPARISON

N_{test} in Table 3 represents the number of flush tests used for diagnosis in [28]–[30], and the proposed method. For [28], four flush tests were always conducted in the horizontal, vertical, and two diagonal directions. For [29], two more flush tests are required than in [28] to shift out the test responses. In [30], the test is conducted using 4 patterns for stuck-at fault and 2 patterns for transition-delay fault. In the proposed scan architecture, $2^{\lfloor \log_{N_{sp}}(L_{sc}-1) \rfloor + 1}$ flush tests were performed according to Eq. (2) of Section IV-C, independent of the number of circuit faults. When N_{SFF} is fixed, the number of tests decreases as N_{sc} increases, and the number of tests increases as the diagnostic paths diversifies as N_{sp} decreases. This trend is confirmed in Table 3.

The experimental results for the diagnostic resolution described in Section V-B confirm that the diagnostic resolution of the proposed architecture improves as N_{sc} increases and N_{sp} decreases. For N_{test}, the number of tests increases as N_{sp} decreases. Consequently, there is a trade-off between the diagnostic resolution and the test time according to N_{sp}. When inserting as many scan chains as possible to reduce shifting time during scan testing and maximize diagnostic performance, the trade-off between test time and diagnostic resolution can be adjusted by selecting N_{sp} by predicting the number of tests according to Eq. (2).

Although the diagnostic resolution is lower than when N_{sp} is small (e.g., 2 or 3), if N_{sp} increases, as with $N_{SFF} = 720$, $N_{sc} = 60$, and $N_{sp} = 4$ in Table 3, a diagnosis with a similar number of tests as in [28] is possible. Even in this case, the diagnostic resolution of the proposed method is higher than [28]; the number of fault candidates for 60 faults decreases by 46.385% as shown in Table 2. If N_{sp} decreases under the same conditions, N_{test} increases and the diagnostic resolution improves further. When observing only diagnostic resolution, the $N_{sp} = 2$ design is optimal, although its relatively long test time is a limitation. In this case, the trade-off between the diagnostic resolution and the test time can be adjusted by increasing N_{sp}.

D. ADDITIONAL PORTS COUNT COMPARISON

The extra I/O in Table 3 illustrates the number of additional test ports used for diagnosis in [28]–[30], and the proposed method. The scenario in [28] requires $2 \times L_{sc}$ vertical scan-in/out ports to form the vertical scan paths and one path control signal. However, in this method, if the number of general scan-in/out ports is sufficient to reduce the pin counts, the corresponding ports can be shared as the vertical scan-in/out ports. Accordingly, when the number of scan chains is greater than the scan chain length, only one control signal is required, as with $N_{SFF} = 720$ and $N_{sc} = 36$ in Table 3.

Accordingly, in [28], if a large number of scan chains are secured compared with the circuit size, diagnosis with a small number of additional ports is possible; otherwise, a very large number of additional ports are required. In contrast, the proposed method uses $N_{mc} = \lfloor \log_{N_{sp}}(L_{sc}-1) \rfloor + 1$ additional ports according to Eq. (1). Because N_{mc} increases logarithmically with L_{sc}, a relatively small number of additional ports can be used even in a situation where L_{sc} is large.

The number of additional ports required to use more diverse diagnostic paths increases as N_{sp} decreases. As in N_{test} in Section V-C, additional I/O also incur a trade-off with the diagnostic resolution according to N_{sp}. If the number of scan chains does not exceed the scan chain length, diagnosis

TABLE 4. Comparison on the total area.

circuit	N_{SFF}	N_{sc}	basic scan	[28]		[29]		[30]		Proposed					
										$N_{sp}=4$		$N_{sp}=3$		$N_{sp}=2$	
			total area	total area	Δ(%)	total area	Δ(%)	total area	Δ(%)	total area	Δ(%)	total area	Δ(%)	total area	Δ(%)
s9234	228	12	2943.08	3704.04	25.86	3700.13	25.72	3702.30	25.80	3638.20	23.62	3630.90	23.37	3622.02	23.07
s13207	669	12	10348.60	13411.47	29.60	13403.66	29.52	13404.01	29.52	13331.06	28.82	13322.18	28.73	13306.01	28.58
s15850	597	12	10636.73	13368.52	25.68	13361.55	25.62	13361.72	25.62	13289.14	24.94	13281.84	24.87	13264.09	24.70
s38417	1636	12	31642.16	40152.19	26.89	40129.01	26.82	40134.77	26.84	40018.66	26.47	40006.74	26.43	39965.75	26.31
s38584	1452	12	31363.21	38118.73	21.54	38081.84	21.42	38100.73	21.48	37996.88	21.15	37982.34	21.10	37953.27	21.01
b18	3276	12	154670.91	174692.87	12.94	174637.73	12.90	174640.50	12.91	174475.50	12.80	174452.70	12.78	174388.43	12.74
b19	6564	12	318369.52	362744.49	13.93	362622.42	13.89	362624.32	13.90	362423.33	13.83	362393.96	13.82	362287.18	13.79

TABLE 5. Comparison on the routing length.

circuit	N_{SFF}	N_{sc}	basic scan	[28]		[29]		[30]		Proposed					
										$N_{sp}=4$		$N_{sp}=3$		$N_{sp}=2$	
			routing length	routing length	Δ(%)	routing length	Δ(%)	routing length	Δ(%)	routing length	Δ(%)	routing length	Δ(%)	routing length	Δ(%)
s9234	228	12	1747.97	6356.24	263.63	6305.20	260.71	5119.72	192.89	6106.42	249.34	6003.67	243.46	5549.14	217.46
s13207	669	12	9285.33	31807.70	242.55	29984.94	222.92	21673.48	133.41	28328.56	205.08	26957.38	190.32	25331.81	172.81
s15850	597	12	8832.01	28045.48	217.54	27785.10	214.59	20456.29	131.61	26185.20	196.48	24826.79	181.10	25304.80	186.51
s38417	1636	12	39438.29	93788.34	137.81	88963.32	125.57	59080.73	49.80	85595.73	117.03	77623.88	96.82	72726.04	84.40
s38584	1452	12	40162.87	82601.43	105.66	82573.66	105.59	58905.17	46.66	77755.55	93.60	71563.16	78.18	67996.36	69.30
b18	3276	12	285186.01	521603.53	82.89	527281.94	84.89	323837.22	13.55	508970.5	78.46	492693.01	72.76	452761.12	58.75
b19	6564	12	571919.25	1191781.62	108.38	1163711.38	103.47	636331.94	11.26	1149267.75	100.94	1050879.75	83.74	957454.94	67.41

with the proposed method is possible with a significantly smaller number of additional ports compared with [28].

Next, [29] requires only one extra I/O, which is much less than the number of extra I/O required for the proposed method. However, [29] has a structure in which the vertical scan-in and out ports of [28] are connected to reduce the excessive extra I/O, and shows the poor diagnostic resolution as shown in Figure 11. The extra I/O required in the proposed method decreases as N_{sp} increases. In the case of $N_{SFF} = 720$, $N_{sc} = 60$, and $N_{sp} = 4$, only two extra I/O are required in the proposed method, as shown in Table 3. And as shown in Figure 11 (c), the proposed method still maintains the higher diagnostic resolution than [29] even for this case. [30] also requires only one extra I/O and shows the high diagnostic resolution when L_{sc} is small. However, as shown in Figure 11 (e) and (f), the diagnostic resolution of [30] is greatly reduced as L_{sc} increases, making it difficult to apply to large circuits.

E. AREA & ROUTING OVERHEAD COMPARISON

Tables 4 and 5 shows the total area and the routing length after PNR for ISCAS89' and ITC'99 benchmark circuits of [28]–[30] and the proposed method. For the experiments on the $N_{sp} = 4, 3, 2$ conditions of the proposed method, the experiments were carried out under $N_{sc} = 12$ condition. The "basic scan" in each table means the scan architecture that has not been modified for the scan chain diagnosis, and $\Delta(\%)$ represents the ratio of the additional overhead compared to the basic scan architecture of each method.

For the diagnosis of scan chain faults, all of [28]–[30] and the proposed method require one multiplexer per cell. In the proposed method, additional multiplexers are not required for the SFFs of the first column in the overall scan architecture, so there is an advantage in terms of the total cell area compared to [28]–[30], as shown in Table 4. In addition to this, in terms of the routing length, the routing overhead of the proposed method is much less than that of [28] and [29], which connect every cell from the uppermost scan chain to the lowermost scan chain. In the proposed scan architecture, the routing overhead decreases as N_{sp} decreases according to the scan partitioning, as shown in Table 5. However, it shows a higher routing overhead compared with [30], in which only the additional routing in one scan chain occurs without connection with an adjacent scan chain. But the area and the routing overhead of the proposed method tends to decrease as the circuit size increases.

VI. CONCLUSION

Scan chain diagnosis is essential for the rapid improvement of yield in the early stages of the manufacturing process. Often, there are many faults in the scan chains before the process is stabilized; thus, a diagnostic method for multiple faults is required. This paper presents a novel reconfigurable scan architecture and a diagnosis method for using this architecture to diagnose such multiple faults in the scan chains. The proposed method achieves a high diagnostic resolution in a multi-fault environment as the number of scan chains inserted in the circuit increases. In addition, the proposed method reduces the routing overhead required to apply the structure through scan partitioning.

The experimental results identify the difference in diagnostic resolutions between the proposed and conventional methods as the number of faults in the same circuit environment increases. The proposed method achieves a high diagnostic resolution for multiple stuck-at faults, transition-delay faults,

and a combination of both fault types. The improvement in the diagnostic resolution is maximized when applying the proposed method and optimizing the circuit by increasing the number of scan chains and reducing the scan chain length for a circuit of the same size regardless of the fault type.

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