IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received July 30, 2021, accepted August 24, 2021, date of publication August 26, 2021, date of current version September 3, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3108232

Electrical Stability of p-Channel Feedback Field-Effect Transistors Under Bias Stresses

JAEMIN SON, KYOUNGAH CHO, AND SANGSIG KIM
Department of Electrical Engineering, Korea University, Seongbuk-gu, Seoul 02841, Republic of Korea

Corresponding author: Sangsig Kim (sangsig@korea.ac.kr)

This work was supported by the Brain Korea 21 Plus Project of 2021 through the NRF funded by the Ministry of Science, ICT and Future Planning, and in part by Korea University and Samsung Electronics Company Ltd., under Grant IO201223-08257-01.

ABSTRACT In this study, we examined electrical stability of the p-channel feedback field-effect transistors (FBFETs) under negative bias stress (NBS) and positive bias stress (PBS). The intact FBFETs have a subthreshold swing (*SS*) of 0.12 mV/dec, an on-current of $\sim 10^{-4}$ A, and a threshold voltage (V_{TH}) of –0.76 V. There is a negligible change in the on-current and *SS* when the FBFETs are stressed by a gate-bias voltage corresponding to an electric field of 5.4 MV/cm across the gate oxide. On the other hand, as the duration of the stress increases to 1000 s, the V_{TH} shifts to –0.89 V and –0.67 V for NBS and PBS, respectively. The V_{TH} was recovered to over 83% at a recovery bias voltage of ±5 V. The electrical stabilities of FBFETs under NBS and PBS are discussed in this study.

INDEX TERMS Field-effect transistor, positive feedback loop, reliability, bias stress, recovery.

I. INTRODUCTION

Feedback field-effect transistors (FBFETs) have recently emerged as promising devices for next-generation electronics owing to their unique characteristics that allow their application in memory and switching devices [1]–[6]. FBFETs having p^+-n-p-n^+ structures are operated by positive feedback (FB) loops that are the reciprocal interaction between potential barriers and charge carriers. When a potential barrier formed in the p-doped region is lowered by the accumulation of holes, electrons in the n^+ source are accumulated in the n-doped region. Consequently, electrons flow toward the p^+ drain, and the accumulation of electrons prompts the injection of holes. More recently, their neuronal oscillation and spiking behaviors have opened their potential applications in neuron devices [7], [8]. In order to use FBFETs in next-generation electronics, it is essential to examine their reliabilities under various conditions, including temperature and gate-bias stresses. To date, studies on the reliabilities have been conducted using simulation models to determine the dependence of their electrical properties on temperature [9]–[11]. Nevertheless, there has not been any research reported on their electrical stability under gate-bias stresses.

Considering the trend of the scaling down of the gate dielectric thickness in FETs, gate-bias stresses are one of the crucial issues affecting the electrical stability because the electric field across the gate oxide (E_{OX}) increases as the thickness of the gate dielectric decreases [12], [13]. In particular, the electrical properties of p-channel FETs are significantly damaged under negative gate bias stress (NBS) [14], [15]. Therefore, in this study, we investigate the electrical stabilities of p-channel FBFETs under positive gate bias stress (PBS) and NBS with a gate-bias voltage corresponding to a 5.4 MV/cm of E_{OX}. Furthermore, we examined recovery characteristics of the FBFETs treated with NBS and PBS in terms of the threshold voltage (V_{TH}).

The associate editor coordinating the review of this manuscript and approving it for publication was Anisul Haque.

II. EXPERIMENTAL

Figure 1 shows a schematic of the p-channel FBFET on a silicon-on-insulator wafer with 340 nm-thick Si layer. The n-type well was formed by implantation of P^+ ions (a dose of 3×10^{13} cm^{-2} and an energy of 60 keV) and annealing at 1100 °C for 30 min. A 22-nm thick silicon dioxide (SiO_2) gate dielectric was thermally grown at 850 °C, and a poly silicon gate was formed on top of the channel using low-temperature chemical vapor deposition and photolithography. Prior to the ion implantation process of the p-type dopants, sidewall spacers were formed to make the gated region with a length of 2.5 μm by suppressing the lateral diffusion of the dopants. The sidewall spacers were made of tetraethyl orthosilicate with a length of approximately 200 nm, and the p-type non-gated region was formed by implantation of BF_2^+

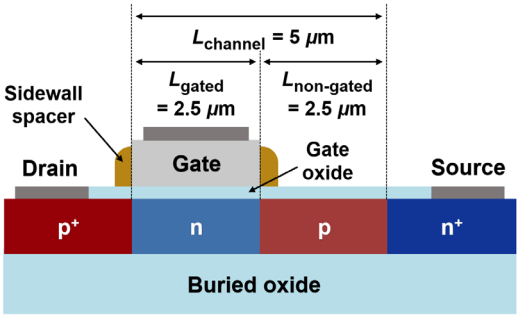

FIGURE 1. A schematic of the p-channel FBFET.

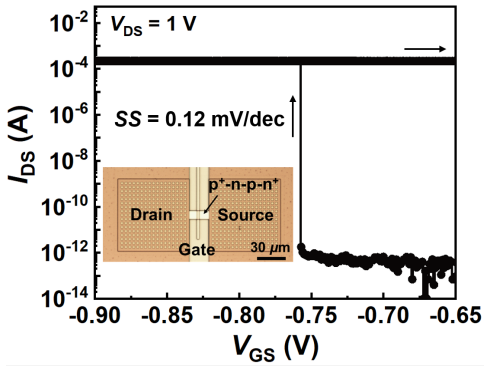

FIGURE 2. Represent transfer curve of the p-channel FBFET and the optical image (inset).

ions (a dose of 6×10^{13} cm^{-2} and an energy of 40 keV). The p^+ drain and n^+ source regions were formed by implantation of BF_2^+ and P^+ ions at a dose of 3×10^{15} cm^{-2} at ion energies of 30 keV (for BF_2^+) and 100 keV (for P^+), respectively. Thereafter, the annealing process was carried out at 1000 °C for 30 min and subsequently at 1050 °C for 30 s using a rapid thermal annealing system to activate the implanted dopants. Finally, the drain, source, and gate electrodes were made of Ti/TiN/Al/TiN metal alloy using sputtering and photolithography.

In this study, gate-bias stresses of –12 V and +12 V were applied in case of NBS and PBS, respectively, and the electrical properties were measured at room temperature with an Agilent HP4155C semiconductor parameter analyzer in the dark.

III. RESULTS AND DISCUSSION

Figure 2 exhibits the optical image and representative transfer curve of a p-channel FBFET at a V_{DS} of 1 V. As V_{GS} is swept from −0.65 V, the I_{DS} increases abruptly at $V_{GS} = -0.76$ V that is defined to be V_{TH}; the abrupt increase in the current is called the latch-up phenomenon. The 'OFF' ('ON') state of the FBFET are determined before (after) the latch-up phenomenon is generated. Owing to the positive FB mechanism, the FBFET exhibits an extremely low subthreshold swing (*SS*, 0.12 mV/dec), a high on-current ($\sim 10^{-4}$ A), and a low off-current ($\sim 10^{-13}$ A). Herein, the V_{TH} was extracted using the transconductance change method, the *SS* was extracted from the equation of $dV_{GS}/d\log(|I_{DS}|)$, and the on-current was measured at $V_{GS} = 0.9$ V. Moreover, the open window in the transfer curve shows the presence of bistable states which is prerequisite condition to act as a memory device.

For the p-channel FBFETs under NBS and PBS, the transfer curves and V_{TH} shifts are plotted in Fig. 3 as a function of the stress time. As the NBS time increases to 1000 s, the V_{TH} negatively shifts from –0.76 to –0.89 V ($\Delta V_{TH} =$ 0.13 V), as shown in Figs. 3(a) and (b). On the other hand, as the PBS time increases to 1000 s, the V_{TH} positively shifts from –0.76 to –0.67 V ($\Delta V_{TH} = 0.09$ V), as shown in Figs. 3(c) and (d). The V_{TH} shift results from interface traps between the channel and the gate dielectric layer, and these interface traps are identified as oxide traps associated with oxygen vacancies on the surfaces of the SiO_2 gate dielectric [16]. The oxide traps become positively charged by hole trapping or neutralized by electron trapping through the oxide electric field [17]. According to previous studies on the electrical characteristics of p-channel FETs under gate-bias stresses [18], [19], the negative shift of V_{TH} under NBS is attributed to interface traps (positive oxide traps) acting as donor-like defects, and the positive V_{TH} in PBS is ascribed to interface traps (neutralized oxide traps) acting as acceptor-like defects. For the p-channel FBFETs, the shift in V_{TH} under the gate bias stresses is consistent with that for other p-channel FETs. Nevertheless, considering that other p-channel FETs are highly vulnerable to NBS [20]–[22], the electrical characteristics of p-channel FBFETs are relatively reliable even under NBS. In addition, the degradation mechanisms of the FBFETs and conventional FETs are different since these FETs have their different operation mechanisms although the shift of V_{TH} of the FBFETs under PBS and NBS is consistent with that of conventional FETs. For the FBFETs, the interface traps generated under NBS and PBS do not hinder the generation of the positive FB loop that enables them to operate. Contrary to the V_{TH}, the change in the on-current and *SS* is subtle, even though gate-bias stress is applied on the FBFETs for 1000 s (see supplementary information). In terms of the *SS* and on-current, the electrical stability of the p-channel FBFETs under PBS and NBS is superior to those of conventional FETs because the FBFETs operated by interplay between the potential barriers and charge carriers are relatively immune to the interface traps generated by PBS and NBS, compared to conventional FETs. Once the positive FB loop is generated, the *SS* and on/off current are nearly identical. Moreover, the electrical stability of the n-channel FBFETs is expected to be similar to that of the p-channel FBFETs. The n-channel FBFETs are operated by the positive FB loop as well.

Figure 4 represents the recovery in the V_{TH} of the p-channel FBFETs that had already suffered from NBS and PBS. The recovery rate increased when a recovery bias voltage was applied to the FBFETs, irrespective of the stress bias conditions; the recovery rate dramatically increased within seconds and was maintained after approximately 200 s. The recovery

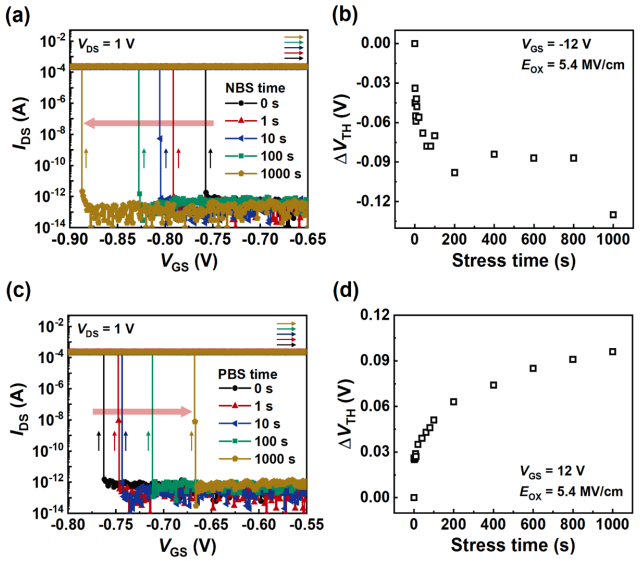

FIGURE 3. Transfer curves and threshold voltage (V_{TH}) shifts under (a-b) NBS and (c-d) PBS.

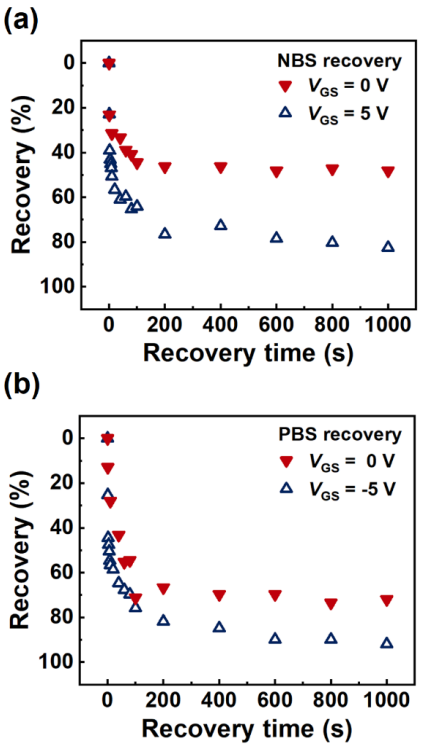

FIGURE 4. The percentage scale of the normalized V_{TH} recovery rates for (a) NBS and (b) PBS.

rate in the V_{TH} reaches up to 83% (92%) when a recovery bias voltage of +5 V (–5 V) was applied to the FBFETs stressed by NBS (PBS). This indicates that the recovery bias contributes to compensating the defect traps. Full recovery in the shift of V_{TH} was not observed in any event, which was due to permanent irrecoverable defect components [23]. On the other hand, after 1000 s the V_{TH} is naturally recovered without a recovery bias at room temperature, up to 48% and 71% for the FBFETs stressed by NBS and PBS, respectively. In terms of the V_{TH}, the resilience of the FBFETs is superior to that of other FETs that are not retained at a maximum of 30% at room temperature. The self-recovery of V_{TH} enables the p-channel FBFETs to be more profitable than other p-channel FETs.

IV. CONCLUSION

In this study, we examined electrical characteristics of the p-channel FBFETs under NBS and PBS to confirm the electrical stability of the FBFETs. The change in the on-current and *SS* of the FBFETs is negligible even under gate-bias stresses corresponding to a 5.4 MV/cm of E_{OX} for 1000 s. On the other hand, the V_{TH} shifts to –0.89 and –0.67 V for NBS and PBS, respectively, as the stress time increased to 1000 s. The V_{TH} was recovered to over 83% when a recovery bias voltage of ±5 V was applied. The reliability of the FBFETs was confirmed from their electrical stabilities under NBS and PBS.

REFERENCES

[1] S. Cristoloveanu, K. H. Lee, H. Park, and M. S. Parihar, "The concept of electrostatic doping and related devices," *Solid-State Electron.*, vol. 155, pp. 32–43, May 2019.
[2] H. Kang, J. Cho, Y. Kim, D. Lim, S. Woo, K. Cho, and S. Kim, "Non-volatile and volatile memory characteristics of a silicon nanowire feedback field-effect transistor with a nitride charge-storage layer," *IEEE Trans. Electron Devices*, vol. 66, no. 8, pp. 3342–3348, Aug. 2019.
[3] A. Z. Badwan, Q. Li, and D. E. Ioannou, "On the nature of the memory mechanism of gated-thyristor dynamic-RAM cells," *IEEE J. Electron Devices Soc.*, vol. 3, no. 6, pp. 468–471, Nov. 2015.
[4] D. Lim, J. Son, K. Cho, and S. Kim, "Quasi-nonvolatile silicon memory device," *Adv. Mater. Technol.*, vol. 5, no. 12, Nov. 2020, Art. no. 2000915.
[5] S. Cristoloveanu *et al.*, "A review of the Z2-FET 1T-DRAM memory: Operation mechanisms and key parameters," *Solid. State. Electron.*, vol. 143, pp. 10–19, May 2018.
[6] J. Cho, D. Lim, S. Woo, K. Cho, and S. Kim, "Static random access memory characteristics of single-gated feedback field-effect transistors," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 413–419, Jan. 2019.
[7] Y.-S. Park, S. Woo, D. Lim, K. Cho, and S. Kim, "Integrate-and-fire neuron circuit without external bias voltages," *Frontiers Neurosci.*, vol. 15, p. 309, Mar. 2021.
[8] D. Lim, K. Cho, and S. Kim, "Single silicon neuron device enabling neuronal oscillation and stochastic dynamics," *IEEE Electron Device Lett.*, vol. 42, no. 5, pp. 649–652, May 2021.
[9] K. Park, M.-W. Kwon, M.-H. Baek, S. Hwang, T. Jang, T. Kim, and B.-G. Park, "Analysis of minority carrier lifetime dependence on dual gate feedback field effect transistor," *J. Nanosci. Nanotechnol.*, vol. 19, no. 10, pp. 6767–6770, Oct. 2019.
[10] M. Kim, Y. Kim, D. Lim, S. Woo, K. Cho, and S. Kim, "Steep switching characteristics of single-gated feedback field-effect transistors," *Nanotechnology*, vol. 28, no. 5, Dec. 2016, Art. no. 055205.
[11] J. Park and C. Shin, "Study of random dopant fluctuation in PNPN feedback FET," *Semicond. Sci. Technol.*, vol. 35, no. 3, Feb. 2020, Art. no. 035019.
[12] C. Peng, Z. Lei, R. Gao, Z. Zhang, Y. Chen, Y. En, and Y. Huang, "Investigation of negative bias temperature instability effect in partially depleted SOI pMOSFET," *IEEE Access*, vol. 8, pp. 99037–99046, May 2020.
[13] S. Navarro, C. Navarro, C. Marquez, N. Salazar, P. Galy, S. Cristoloveanu, and F. Gamiz, "Reliability study of thin-oxide zero-ionization, zero-swing FET 1T-DRAM memory cell," *IEEE Electron Device Lett.*, vol. 40, no. 7, pp. 1084–1087, Jul. 2019.
[14] K.-H. Bae, M. G. Shin, S.-H. Hwang, H.-S. Jeong, D.-H. Kim, and H.-I. Kwon, "Electrical performance and stability improvement of p-channel SnO thin-film transistors using atomic-layer-deposited Al_2O_3 capping layer," *IEEE Access*, vol. 8, pp. 222410–222416, Dec. 2020.

[15] G. W. Yang, S. G. Seo, S. Choi, D. H. Kim, and S. H. Jin, "Unscrambling for subgap density-of-states in multilayered MoS_2 field effect transistors under DC bias stress via optical charge-pumping capacitance-voltage spectroscopy," *IEEE Access*, vol. 9, pp. 73090–73102, May 2021.
[16] D. S. Ang, "Observation of suppressed interface state relaxation under positive gate biasing of the ultrathin oxynitride gate p-MOSFET subjected to negative-bias temperature stressing," *IEEE Electron Device Lett.*, vol. 27, no. 5, pp. 412–415, May 2006.
[17] S.-K. Kwon, S.-H. Oh, H.-S. Song, S.-Y. Kim, G.-W. Lee, and H.-D. Lee, "Identification of interface states and shallow and deep hole traps under NBTI stress using fast, normal, and charge-pumping measurement techniques," *J. Semicond. Technol. Sci.*, vol. 18, no. 2, pp. 160–166, Apr. 2018.
[18] B. Bhuvana, C. Thomas Soren, E. Mary, G. Kalyani, and G. Naman, "Mitigating the impact of NBTI and PBTI degradation," *Global J. Technol. Optim.*, vol. 7, no. 2, p. 195, May 2016.
[19] D. K. Schroder, "Negative bias temperature instability: What do we understand?" *Microelectron. Rel.*, vol. 47, no. 6, pp. 841–852, Jun. 2007.
[20] H.-Y. Tu, T.-M. Tsai, C.-C. Wu, Y.-C. Tsao, M.-C. Tai, T.-C. Chang, Y.-L. Tsai, S.-P. Huang, Y.-Z. Zheng, Y.-X. Wang, and H.-C. Chen, "Analysis of negative bias temperature instability degradation in p-type low-temperature polycrystalline silicon thin-film transistors of different grain sizes," *IEEE Electron Device Lett.*, vol. 40, no. 11, pp. 1768–1771, Nov. 2019.
[21] W. Mizubayashi, T. Mori, K. Fukuda, Y. Ishikawa, Y. Morita, S. Migita, H. Ota, Y. Liu, S. O'uchi, J. Tsukada, H. Yamauchi, T. Matsukawa, M. Masahara, and K. Endo, "Bias temperature instability in tunnel field-effect transistors," *Jpn. J. Appl. Phys.*, vol. 56, no. 4S, Mar. 2017, Art. no. 04CA04.
[22] M.-G. Shin, K.-H. Bae, H.-S. Jeong, D.-H. Kim, H.-S. Cha, and H.-I. Kwon, "Effects of capping layers with different metals on electrical performance and stability of p-channel SnO thin-film transistors," *Micromachines*, vol. 11, no. 10, p. 917, Sep. 2020.
[23] T. Grasser, T. Aichinger, G. Pobegen, H. Reisinger, P.-J. Wagner, J. Franco, M. Nelhiebel, and B. Kaczer, "The 'permanent' component of NBTI: Composition and annealing," in *Proc. Int. Rel. Phys. Symp. (IRPS)*, Monterey, CA, USA, 2011, pp. 605–613.

JAEMIN SON is currently pursuing the Ph.D. degree with the Nanotronics Laboratory, Korea University, under the supervision of Prof. Sangsig Kim. His research interests include logic-in-memory and memory devices.

KYOUNGAH CHO received the Ph.D. degree from The University of Tokyo, in 2000. She has been a Research Professor with the Department of Electrical Engineering, Korea University, since 2002. Her research interests include logic-in-memory, thermoelectric devices, energy storage devices, and flexible/stretchable electronics.

SANGSIG KIM received the Ph.D. degree from Columbia University, in 1996. He was a Postdoctoral Researcher with the University of Illinois at Urbana–Champaign, from 1996 to 1999. He has been a Professor with the Department of Electrical Engineering, Korea University, since 1999. His research interests include logic-in-memory, memory devices, energy devices including thermoelectric devices and micro supercapacitors, and flexible/stretchable electronics.