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Integrate-and-Fire Neuron Circuit With Synaptic Off-Current Blocking Operation

SEUNGHWAN SONG, BOSUNG JEON, (Student Member, IEEE), SUNGMIN HWANG, (Student Member, IEEE), MYUNG-HYUN BAEK, (Student Member, IEEE), JONG-HO LEE, (Fellow, IEEE), AND BYUNG-GOOK PARK, (Fellow, IEEE)

Department of Electrical and Computer Engineering, Seoul National University, Seoul 08826, South Korea
Inter-University Semiconductor Research Center, Seoul National University, Seoul 08826, South Korea

Corresponding author: Byung-Gook Park (bgpark@snu.ac.kr)

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ABSTRACT In this study, we propose an analog CMOS integrate-and-fire (I & F) neuron circuit with a synaptic off-state current blocking operation. The proposed circuit prevents unintended potential changes in the membrane capacitor owing to the off-state current of synaptic devices, thereby preventing a decrease in the accuracy of the spiking neural network (SNN) inference system. Compared to the conventional I & F neuron circuit, the basic I & F and synaptic off-current blocking operations of the proposed I & F neuron circuit were confirmed in a circuit-level simulation. Furthermore, to verify the effect of the proposed circuit on the neural network, a multi-layer SNN simulation was performed, and the accuracy of the inference system was compared for the conventional and proposed I & F neuron circuits. The simulation and analysis results demonstrate the robustness of the I & F neuron circuit to the drop in accuracy of inference systems due to off-state currents in synaptic devices.

INDEX TERMS Neuromorphic system, CMOS-based integrate-and-fire (I&F) neuron circuit, spiking neural networks (SNNs), synaptic off-state current blocking operation, TCAD simulation, SPICE simulation, SNN high-level simulation.

I. INTRODUCTION

Recently, various attempts have been made on neuromorphic computing systems to emulate biological brain behavior in terms of energy consumption and parallel processing [1]–[4]. Although conventional computers based on the von Neumann architecture sufficiently perform the functionality of artificial neural networks (ANNs), their sequential processing exponentially increases the energy consumption required to process parallel operations on data. Compared to the von Neumann architecture, a neuromorphic computing system based on a spiking neural network (SNN) is suitable for complex data processing such as pattern recognition [5], [6], image denoising [7], and speech recognition [8] owing to the energy efficiency and parallel processing capability of SNNs. To make SNNs more biologically plausible, learning algorithms for SNNs that correspond to the error backpropagation (BP) of non-spiking ANNs are under investigation [9]–[11]. Moreover, SNNs can also be implemented using the pre-trained weights of the ideal ANN because the output activations of the non-spiking ANN and SNN firing rates are equivalent [12], [13]. Thus, without its own learning rule, SNNs exhibit a good performance in inference. Hardware-based neurons have been implemented in the form of electrical circuits emulating the characteristics of the integrate-and-fire (I & F) model [14]–[28]. The I & F neuron circuit accumulates the weighted sum current of the synapses, and creates an action potential instantaneously after the membrane potential (V_{mem}) exceeds the threshold of the circuit. The firing rate of the I & F neuron circuit and the common output activation function of the non-spiking ANN, rectified linear unit, perform the same function when there is no extra current component of the synapse. However, synaptic devices made of field effect transistors (FETs) or memristors have off-state current (i.e., off-current) components even when no input spike is applied [29]–[31], which may vary depending on the synaptic weights. Once the synaptic off-current exists, it flows continuously into the neuron circuit, causing a

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change in V_{mem}. This change is not intended by the network; therefore, the firing rate of the I & F neuron circuit can be increased or decreased compared to the correct activation rate of the non-spiking ANN. Consequently, the performance of the inference system is adversely affected. The distortion of V_{mem} becomes more severe as the idle time of the neuron increases. One of the greatest advantages of SNNs over non-spiking ANNs is energy efficiency; therefore, to minimize the energy consumption of SNNs, the pulse interval of the input data can be maximized within the range to meet the application requirements. Therefore, energy-efficient SNNs cannot ignore the idle time of the neuron circuit. Recent studies on silicon neuron circuits [16], [17], [22], [24], [28] and non-silicon materials [18]–[20] exhibit extremely low energy consumption, but their firing rate can still be affected by the synaptic off-current, which is an external off-current component of the neuron circuit.

To prevent the distortion of V_{mem} by the synaptic off-current, several solutions proposed in previous studies can be employed. First, various types of leaky I & F neuron circuits can be proposed to manage V_{mem} at the circuit level [24], [26]. The leak conductance in the leaky I & F neuron circuit successfully blocks the constant off-current generated in the network from constantly changing V_{mem} during idle time. However, reported synaptic devices often have off-currents that are weight-dependent [29]–[31], and the leaky I & F neuron circuit may not be sufficient to block the off-current from the synaptic array comprising these synaptic devices. In addition, the synaptic off-current sum flowing to the neuron circuit varies with the number of synaptic devices in a source line, which is determined by the number of presynaptic neurons in the network. Consequently, the leaky I & F neuron circuit has its limitations in multi-layer SNNs in terms of blocking the synaptic off-current, even if the off-current in each synaptic device is not weight-dependent. Second, synaptic devices and arrays have often been restricted so that no synaptic off-current flows in the idle state [32], [33]. This type of solution can eliminate synaptic off-currents flowing from the synaptic device to the I & F neuron circuits. However, the selection range of synaptic devices and arrays is narrow. Therefore, there is a strong need for a method that can block the change in membrane potential due to synaptic off-current at the circuit level. We propose a novel method to minimize the effect of the synaptic off-current on SNN inference systems, irrespective of the device or array type.

In this study, we propose an analog CMOS I & F neuron circuit that actively controls the current of the synaptic array. First, the electrical characteristics of the proposed circuit were compared with those of a conventional circuit using an analog circuit simulation by *Silvaco SMARTSPICE* (ver. 4.32.4.R). An in-depth analysis of the energy consumption of the proposed circuit was performed. Second, a dual-gate FET-type synaptic device was simulated to estimate the off-current distribution of a real synaptic array. Device simulations were performed using a computer-aided design (TCAD) simulation. Finally, the proposed circuit was validated by comparing the results of high-level SNN simulations for two types of modified National Institute of Standards and Technology (MNIST) image recognition using a system simulation in *MATLAB R2019b*.

II. CIRCUIT DESIGN AND SIMULATION

A. CONVENTIONAL I & F NEURON CIRCUIT

Fig. 1 shows a conventional CMOS I & F neuron circuit based on the circuit proposed in our previous study [21]. The circuit consists of an integration part and a spike generation part to perform the I & F functions. Synaptic devices separated by excitatory and inhibitory arrays were connected in parallel with the circuit. Spikes generated in the presynaptic neurons are transferred as a current with a weighted value through synapses, and the integration part receives this current. The integration part determines the direction in which the input synaptic current acts on the membrane capacitor and changes V_{mem} as per the change in the accumulated charge

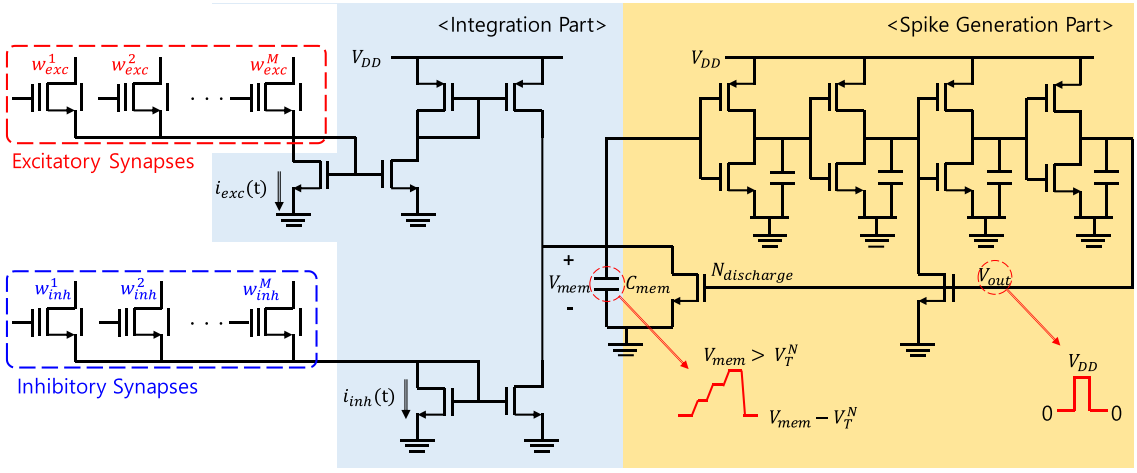

FIGURE 1. Schematic of the conventional I & F neuron circuit.

of the membrane capacitor. When V_{mem} exceeds the neuron threshold (V_T^N), that is, the threshold voltage of the cascaded inverters at the spike generation part, a V_{out} voltage of V_{DD} is immediately formed, and this voltage is subsequently reset to zero by the $N_{discharge}$ transistor. Additionally, the overflow retaining concept is applied to the circuit to prevent the discarding of residual charges that contribute to the formation of the membrane voltage above V_T^N. Only the value of V_{mem} is reduced by V_T^N during spike generation by selecting an appropriately sized $N_{discharge}$ transistor.

However, conventional I & F neuron circuits are vulnerable to off-currents continuously occurring in the synaptic array because the integration part passes the input synaptic current to the membrane capacitor without any control. To analyze the effect of the synaptic off-current on the neuron circuit, we can model the analog relationship between the current and V_{mem} based on previous work [34]. The V_{mem} of the conventional I & F neuron circuit at time t can be expressed as:

$$V_{mem}(t) = V_{mem}\left(t_{pre}^{-}\right) - V_T^N \delta(t_{pre}) + C_{mem}^{-1} \int_{t_{pre}}^{t} \left(i_{exc}(t) - i_{inh}(t)\right) dt \quad (1)$$

where C_{mem}, t_{pre}, t_{pre}^{-}, $i_{exc}(t)$, and $i_{inh}(t)$ are the membrane capacitance, latest time of fire, time immediately before t_{pre}, excitatory synaptic current sum, and inhibitory synaptic current sum, respectively. In the conventional I & F neuron circuit, the current component ($i_{exc}(t) - i_{inh}(t)$) in Eq. (1) can be expressed as the sum of the weighted sum currents and the synaptic off-current sum (i_{offsum}) as follows:

$$i_{exc}(t) - i_{inh}(t) = \sum_{j=1}^{M} \{(w_{exc}^j - w_{inh}^j)\delta_j(t) + \left(1 - \delta_j(t)\right) i_{offsum}\} \quad (2)$$

where M, w_{exc}^j, and w_{inh}^j are the number of neurons in the presynaptic layer (i.e., pre-layer), and the excitatory and inhibitory weights of the synapse connected between the j-th neuron in the pre-layer and the current neuron, respectively. The spike voltage of the j-th neuron in the pre-layer can be represented as an impulse $\delta_j(t)$ with a value of one only when there is a spike; otherwise, it is zero. In addition, i_{offsum} of Eq. (2) can also be expressed by dividing it into excitatory and inhibitory parts, as follows:

$$i_{offsum} = \sum_{j=1}^{M} \{i_{off,exc}^j - i_{off,inh}^j\} \quad (3)$$

where $i_{off,exc}^j$ and $i_{off,inh}^j$ represent the excitatory and inhibitory synaptic off-currents connected between the j-th neuron in the pre-layer and the current neuron, respectively. Equations (1) to (3) show that the charge of the synaptic off-current continuously changes V_{mem} in the absence of spikes in the pre-layer neurons. The currents from the excitatory and inhibitory synapses contribute in opposite directions to the formation of V_{mem}; thus, the membrane capacitor can be charged or discharged in the idle state even if the magnitudes of the synaptic off-currents in the two directions are only slightly different.

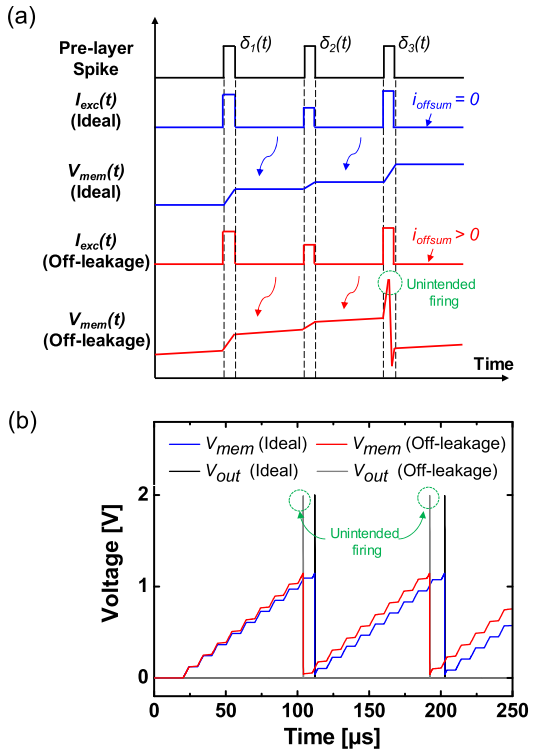

FIGURE 2. Effect of synaptic off-current on the membrane potential shown in (a) timing diagram and (b) output characteristics of a conventional CMOS I & F circuit.

The timing diagram in Fig. 2(a) shows the effect of the synaptic off-current on V_{mem} in a conventional I & F neuron circuit. In the "ideal" case where no synaptic off-current component exists in the array, only the charge from the weighted synaptic current is transferred from the pre-layer, as intended. However, in the case of "off-leakage" where the charge from the off-current of the synaptic device constantly accumulates in the membrane capacitor, the network can cause unintended firing of neurons. Therefore, an SNN inference system organized without a synaptic off-current control methodology can cause a fundamental distortion of the transmitted information. The simulation results of the conventional neuron circuit in Fig. 2(b) show that this phenomenon can occur at an actual circuit level. Charges from the pre-layer spikes will not accumulate correctly in C_{mem}, except when two synaptic off-current components of $i_{exc}(t)$ and $i_{inh}(t)$ are equal. Consequently, the amount of information transmitted using conventional neuron circuits can always be greater or less than intended.

B. PROPOSED I & F NEURON CIRCUIT

To minimize the effect of synaptic off-currents on the membrane capacitor, we propose a CMOS I & F neuron circuit that performs the synaptic off-current blocking operation, as shown in Fig. 3. In the proposed neuron circuit, two pass

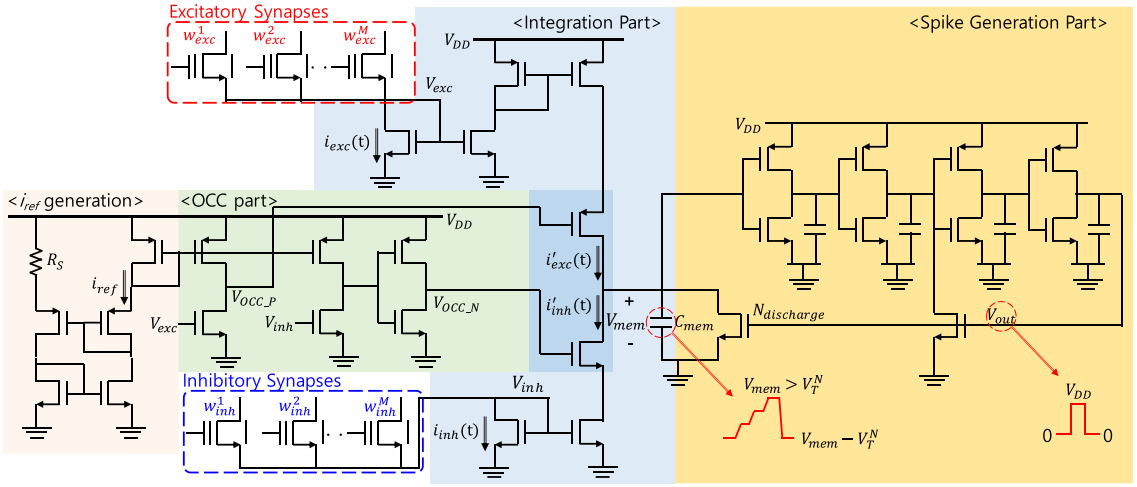

FIGURE 3. Schematic of the proposed I & F neuron circuit.

transistors that enable special integration are added to the circuit. Each gate voltage of the pass transistor is controlled by the voltages V_{OCC_P} and V_{OCC_N} determined by the logic of the off-current cancelation (OCC) part. The reference current (i_{ref}) was generated using a cascade current mirror circuit, and the i_{ref} amplitude was modulated by the series resistor R_S. Subsequently, i_{ref} is copied to the pull-up stage of the OCC decision logic of each neuron circuit and compared with the copied pull-down current of the excitatory and inhibitory current sum of synapses. By comparing the two currents, the OCC part determines the voltages V_{OCC_P} and V_{OCC_N}. When the sum of the excitatory current exceeds i_{ref}, V_{OCC_P} becomes V_{DD} from 0 V, allowing the sum of the excitatory current to flow. Similarly, when the inhibitory current sum exceeds i_{ref}, V_{OCC_N} becomes 0 V from V_{DD}, allowing the inhibitory current to sum to flow. Thus, the proposed circuit can determine whether to separate the membrane capacitor from the synaptic array. By choosing an appropriate i_{ref} between i_{offsum} and the minimum weighted current of the unit synapse, the current components of the proposed circuit, $i'_{exc}(t)$ and $i'_{int}(t)$, can exclude the synaptic off-current component from $i_{exc}(t)$ and $i_{inh}(t)$, which is expressed as:

$$i'_{exc}(t) = \sum_{j=1}^{M} \{w^j_{exc}\delta_j(t)\}, \tag{4}$$

$$i'_{int}(t) = \sum_{j=1}^{M} \{w^j_{inh}\delta_j(t)\}. \tag{5}$$

Note that $i'_{exc}(t)$ and $i'_{int}(t)$ are generated by two pass transistors in the integration part, and the gate voltages of the two pass transistors are independently determined by each OCC decision logic. In other words, the OCC decision logic does not compare $(i_{exc}(t) - i_{inh}(t))$ directly with i_{ref} because the integration part cannot exclude the synaptic off-current when only one of $i_{exc}(t)$ and $i_{inh}(t)$ is below i_{ref}. By controlling the synaptic current flow independently in the integration part, the proposed circuit can transfer the weighted sum current to the membrane capacitor without being affected by the current component on the opposite side. Finally, the V_{mem} of the proposed I & F neuron circuit at time t can be expressed as:

$$V_{mem}(t) = V_{mem}\left(t^-_{pre}\right) - V_T^N\delta(t_{pre}) + C^{-1}_{mem}\int_{t_{pre}}^{t}\{\sum_{j=1}^{M}(w^j_{exc} - w^j_{inh})\delta_j(t)\}dt \tag{6}$$

As shown in Eq. (6), it is expected that the SNN inference system without V_{mem} distortion can be implemented using the proposed I & F neuron circuit. Although not yet studied, non-CMOS devices previously used in neuron circuits, such as MTJ-based devices [18], [19] and resistive RAMs [20], could be used to perform the same operation as the OCC part of the proposed circuit. However, these devices should adjust the threshold voltage of each device to change i_{ref}. Conversely, the proposed CMOS neuron circuit has the flexibility to change i_{ref} simply by adjusting the common gate bias from the i_{ref} generation circuit owing to the CMOS comparator characteristic driven by two different gate biases.

Fig. 4 shows the simulation results to confirm the performance of the proposed I & F neuron circuits. Operating waveforms of the proposed circuit in Fig. 4(a) shows that i_{ref} of 80.3 nA is generated corresponding to R_S, and the OCC part clearly performs the current blocking operation that controls V_{OCC_P} and V_{OCC_N}. Using the range of R_S from 0.3 MΩ to 2.5 MΩ, an i_{ref} can be generated in the range of 500 nA to 40 nA, as shown in Fig. 4(b), and any input current less than i_{ref} is blocked by two pass transistors controlled by OCC part. Fig. 4(c) shows the charge transfer ratio according to the pulse widths of $i_{exc}(t)$ and $i_{inh}(t)$. If the pulse width of the weighted sum current is less than the switching time of the OCC part, the integration part cannot transmit part of the input synaptic current; therefore, the charge transferred to the membrane capacitor can be discarded permanently. For the simulation, the amplitudes of $i_{exc}(t)$ and $i_{inh}(t)$ were 0.5 μA, and we confirmed a charge transfer ratio of over 98.5% with a pulse width of $i_{exc}(t)$ and $i_{inh}(t)$ longer

than 200 ns. This result indicates that the SNN inference system using the proposed circuit can operate without data loss, even when a sub-μs level of input pulse interval is applied to the network. Fig. 4(d) shows the comparisons between the OCC part and neuron circuits [16], [17], [22]–[24], [28] in terms of the neuron spiking rate and energy consumption per spike. Because only the OCC part performs the synaptic off-current blocking operation via its comparison logic, it can be independently combined with other I & F neuron circuits. The energy consumption of silicon neurons is important as it mimics the biological behavior of neurons. In other words, the energy consumption of the OCC part per spike should be relatively lower than that of the entire I & F neuron circuit. The energy consumption of the i_{ref} generation circuit was not considered because several OCC parts can operate using the gate voltage of an i_{ref} generation circuit. For the OCC part simulation, we used the following parameters: V_{DD} of 2 V, i_{ref} of 0.1 μA, weighted current of 0.5 μA, and channel widths of 0.15 and 0.3 μm for NMOS and PMOS, respectively. A channel length of 0.1 μm was used for both NMOS and PMOS devices. As shown in Fig. 4(d), the OCC part consumes 0.076 pJ of energy per spike for a spiking rate of the neuron of up to 1×10^7 spikes/sec. This result validates the OCC part to have a reasonable energy consumption to combine it with several I & F neuron circuits examined earlier. Quantitative comparisons of the energy consumption per spike are presented in Table. 1. In the low-spiking-rate region, the energy consumption per spike in the OCC part

TABLE 1. Energy consumption comparison between the OCC part and previous neuron circuits.

Ref.	Circuit type (Technology)	Approximate spiking rate [spikes/sec]	Neuron energy per spike [pJ]	OCC part energy per spike [pJ]
[16]	FBFET+CMOS (n/a)	1.08×10^5	6.54	0.076
[17]	FDSOI (22 nm)	1000	0.85	0.090
[22]	SOI + Schmitt trigger (0.4 μm)	1×10^6	159	0.076
[23]	CMOS (0.35 μm)	1×10^6	8.5~9	0.076
[24]	PDSOI (0.1 μm)	8×10^6	35	0.076
[28]	FDSOI (22 nm)	65	0.99	0.296

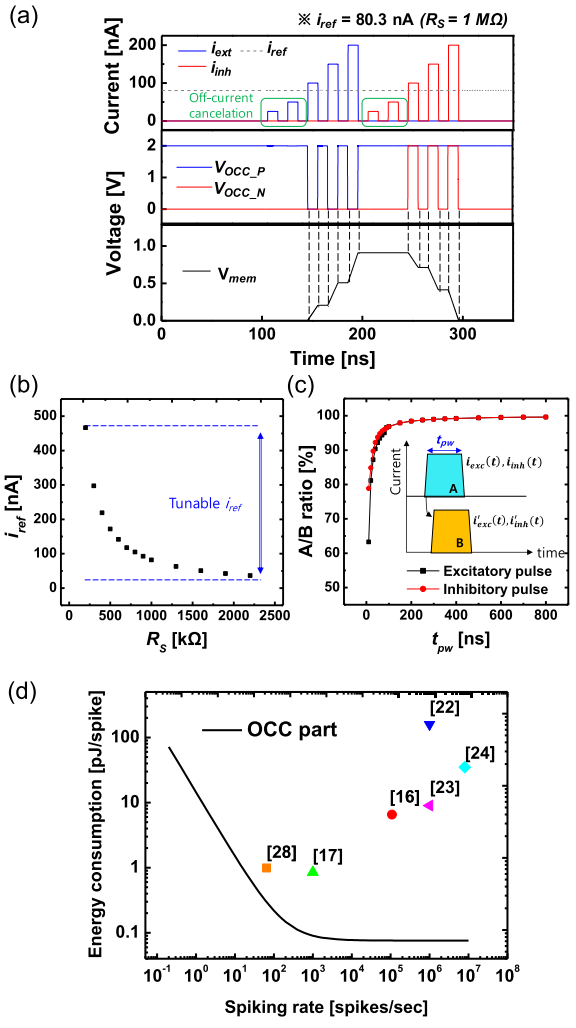

FIGURE 4. Simulation results of the proposed neuron circuit. (a) Transient response of current blocking operation. (b) Change of i_{ref} according to the series resistor R_S. (c) Charge transfer ratio according to the width of the input spiking current. (d) Energy consumption per spike of the OCC part and other neuron circuits according to the spiking rate.

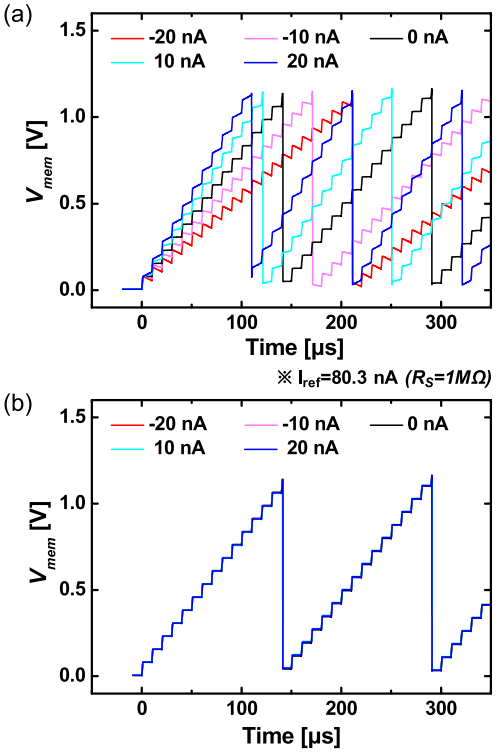

FIGURE 5. Variation in V_{mem} according to the input spike pulse with different values of i_{offsum}. (a) Conventional I & F neuron circuit. (b) Proposed I & F neuron circuit.

increases because the energy consumption in the OCC part is dominated by leakage components in the idle time; hence, the OCC part exhibits a better energy efficiency in the accelerated spiking-rate region, where the total energy consumption is dominated by dynamic power. Several architectures of the SNN accelerator are under investigation to show better energy efficiency compared to the standard ANN accelerators, which have exhibited similar or better performance in terms of energy efficiency [35], [36]. Therefore, SNN accelerators that adopt the OCC part can be energy efficient with synaptic off-current blocking operations. This result indicates that the proposed circuit exhibiting low energy consumption can be used for energy-constrained SNN system applications such as mobile phones and robotics.

Fig. 5 shows the V_{mem} change in the conventional and proposed neuron circuits when the input current of the neuron is a continuous current spike with various i_{offsum} amplitudes. Because the conventional circuit transfers synaptic off-current charges without any control, V_{mem} is continuously charged or discharged, except when i_{offsum} is 0, as shown in Fig. 5(a). Meanwhile, the proposed circuit maintains V_{mem} regardless of i_{offsum} by actively controlling the pass gates of the integration part to cancel the input current below i_{ref}, as shown in Fig. 5(b). Fig. 5(a) and (b) show that, without separate control, the synaptic off-current charge accumulated in the membrane capacitor can degrade the accuracy of the SNN inference system by changing the firing rate of the I & F neuron circuits.

III. DEVICE STRUCTURE AND MEASUREMENT

If the off-current of the real synaptic device varies with the weight stored in each synaptic device, then i_{offsum} is a non-fixed value because i_{offsum} is directly determined by summing all off-currents of each synaptic device, as shown in Eq. (3). This effect of i_{offsum} on the I & F neuron circuit is expected to be different between the two types of I & F neuron circuits, as the conventional circuit steadily accumulates i_{offsum} in the membrane capacitor, while the proposed circuit actively blocks i_{offsum} below i_{ref}, as shown in Fig. 5. The FET-type synaptic device could be an example of this comparison because its off-current characteristics depend on the density of the trapped charge in the storage layer. The FET-type synaptic devices reported in our previous studies modulated the synaptic weight by changing the density of the trapped charge [29], [32], [37]. Consequently, the off-current of the FET-type device was determined with respect to the synaptic weight. To confirm the relationship between the off-current and the synaptic weight of a real synaptic device, we fabricated and measured a dual-gate FET-type synaptic device based on our previous work [37].

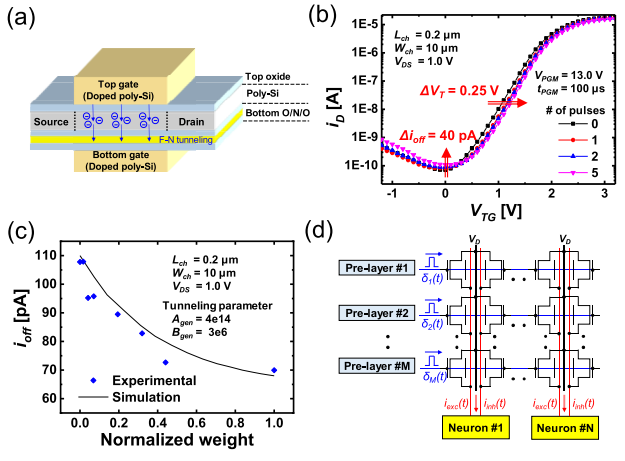

FIGURE 6. (a) 3-D schematic view of dual-gate synaptic device. (b) $I_D - V_{TG}$ curves measured in the fabricated synaptic device with different values of V_T. (c) Simulated and measured i_{off} with normalized weights. (d) The AND-type M × N synaptic array consisting of dual-gate synaptic devices.

Fig. 6(a) shows a schematic of the proposed device. First, doped n^+ polysilicon was deposited as a bottom gate on a buried oxide with a thickness of 400 nm. Subsequently, a bottom gate insulator consisting of oxide/nitride/oxide (O/N/O) gate dielectrics was formed on the bottom gate layer, and the thicknesses of each O/N/O layer were 8, 7, and 3 nm, respectively. For the body of the device, amorphous silicon with a thickness of 20 nm was deposited on the bottom layer insulator and then annealed at 600° for 24 h. A top gate oxide with a thickness of 3 nm was deposited as a top-gate insulator. To form the top gate, n^+ polysilicon was deposited and patterned with channel lengths and widths of 200 nm and 10 μm, respectively. Finally, the source and drain regions were doped by ion implantation with 3×10^{15} cm^{-2} of As^+ ions using the top gate as a mask layer.

In this device, electrons are injected from the top gate into the nitride layer, based on Fouler-Nordheim tunneling. The number of trapped electrons in the nitride layer can be modulated by changing the time of the programming pulse or changing the bottom gate voltage, thereby adjusting the trapped charge, and the threshold voltage of the device (V_T^D) performs the function of the synaptic weight of each device. Fig. 6(b) shows the transfer characteristics of the device, which presents the drain current (i_D) versus the top gate-read voltage (V_{TG}) when the drain-to-source voltage (V_{DS}) is 1 V. The top-gate V_T^D is increased by applying a programming pulse to the bottom gate voltage (V_{BG}), and the total adjustable range of V_T^D is 0.25 V. As V_T^D increases, the off-current of the fabricated device (i_{off}) increases owing to the gate-induced drain leakage (GIDL) effect that varies with V_T^D. In other words, the effective field that produces the same amount of GIDL effect in the body-drain junction is dependent on the nitride trapped charge. Fig. 6(c) shows the simulated and measured i_{off} when V_{TG} is 0 V with normalized weights. All of the physical parameters were calibrated in the simulation to implement $I_D - V_{TG}$ curves with respect to V_T^D, as shown in Fig. 6(b). Bandgap narrowing and Shockley-Read-Hall recombination models were used in the simulation. In addition, career density, mobility, and transport properties were evaluated using the Fermi, Lombardi, and hydrodynamic models, respectively. In addition, the quantum

potential model of the careers was used in the density gradient equation. The results in Fig. 6(c) indicate that the synaptic weight and i_{off} are inversely related; in other words, i_{off} is proportional to V_T. The simulated and measured i_{off} ranges for the total weight of the proposed device were 70 pA to 110 pA. Moreover, using the results in Fig. 6(c), the synaptic weight can be directly converted into i_{off}, and this i_{off} can be used for circuit-level and high-level SNN simulations. Fig. 6(d) shows the AND-type synaptic array consisting of dual-gate FET synapses in Fig. 6(a). In this array, the source line transfers the weighted sum current by summing all the currents at each synaptic device. The off-current component of each synapse is also summed and transferred through the source line because all synapses sharing a source line commonly use a drain line to perform bit-access read operations. The results in Fig. 6(c) and (d) indicate that the dependency of i_{off} on the synaptic weight can cause the i_{offsum} to vary with each source line in practical uses of the synaptic array in the SNN inference system. Because the output characteristics of the conventional and the proposed neuron circuits with i_{offsum} variations were different in circuit-level simulations, classification results of SNN inference systems adopting two types of I & F neuron circuits are also expected to be different.

TABLE 2. Hyper-parameters used in the non-spiking ANN training.

	FCN (FC800-FC400-FC10)	CNN (32C5-AP2-64C5-AP2-FC1024-FC100-FC10)
Learning algorithm	Stochastic gradient descent algorithm (SGD)	
Learning rate	0.01	0.2
Batch size	100	1000
Momentum	0.5 (first 5 epochs) 0.9 (Rest)	0.9 (all epochs)
Dropout	50 % (all layers)	30 % (convolutional layers) 50 % (fully connected layers)

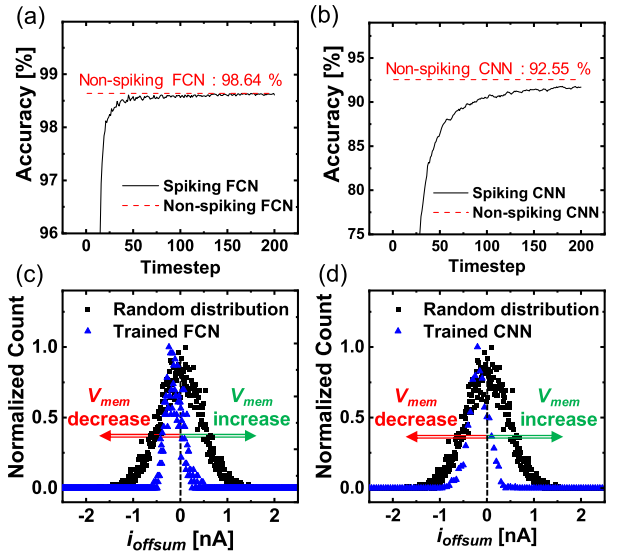

FIGURE 7. Classification accuracy of (a) the simulated FCN and (b) simulated CNN consisting of conventional neuron circuit. Normalized i_{offsum} distribution in the synaptic array: (c) the trained FCN and (d) trained CNN.

IV. SNN SIMULATION

A. SNN INFERENCE SYSTEM

To convert the trained weights of the non-spiking ANN in the SNN inference system, we trained non-spiking ANNs with two types of datasets. First, a non-spiking fully connected network (FCN) structure of 28 × 28-FC800-FC400-FC10 was trained with the MNIST dataset, where the input layer was 28 × 28 and FCm denotes a fully connected layer with m neurons. Second, a non-spiking convolutional neural network (CNN) structure of 28 × 28-32C5-AP2-64C5-AP2-FC1024-FC100-FC10 was trained with the fashion-MNIST dataset, where the input layer was 28×28 and mCn represents n filters of size $m \times m$. A 2 × 2 average pooling layer (AP2) was used after each convolutional layer. The hyper-parameters used for the non-spiking ANN training are shown in Table 2. Finally, the trained weights of the two non-spiking ANNs were imported to each SNN through a weight rescaling process to prevent the change in V_{mem} to be greater than V_T^N [38].

Figs. 7(a) and (b) show the classification results of the FCN and CNN for 10,000 samples of the MNIST and fashion-MNIST datasets, respectively. A model equivalent to the conventional I & F neuron circuit was used as a neuron in the high-level SNN simulation, but the off-current of the synaptic device was not considered. The result of the spiking FCN (SFCN) inference system in Fig. 7(a) showed 98.62% classification accuracy after 200 time steps, which is very close to the result of 98.64% obtained by the non-spiking FCN. In addition, as shown in Fig. 7(b), the classification accuracy of the spiking CNN (SCNN) inference system after 200 time steps was 91.88%, which is slightly lower than the non-spiking CNN result of 92.55%. Therefore, the

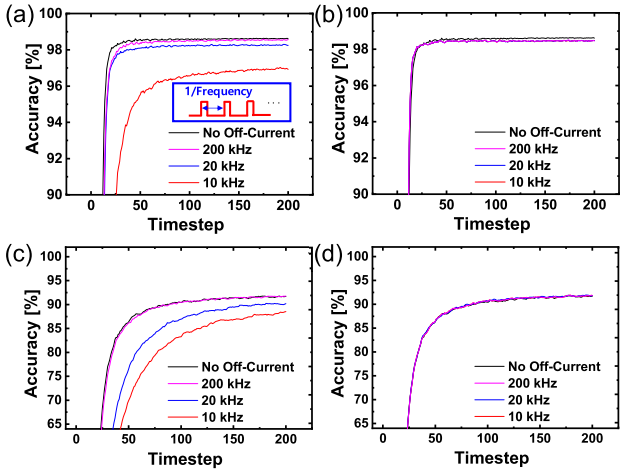

FIGURE 8. Classification accuracy of the simulated SNN for various input pulse frequencies for (a) the conventional SFCN, (b) proposed SFCN, (c) conventional SCNN, and (d) proposed SCNN.

non-spiking ANNs were well reproduced with the SFCN and SCNN inference systems having rescaled weights.

Figs. 7(c) and (d) show the normalized distribution of the i_{offsum} in SFCN and SCNN, respectively. For i_{offsum} estimation, the synaptic device shown in Fig. 6(a) and the synaptic array in Fig. 6(d) were considered. If the synaptic weights are randomly distributed within the i_{off} range, a range of i_{offsum} distributions of -2 nA to $+2$ nA is established, and currents in this range continue to flow into the neuron circuit, even in the absence of input pulses in the network. For the converted SFCN and SCNN weights from the non-spiking weights of ANNs, i_{offsum} distribution ranges were found to be -0.5 nA to $+0.5$ nA and -1.0 nA to $+0.5$ nA, respectively. Although converted weights have a relatively small i_{offsum} range compared to the randomly distributed weights, the two SNN systems are still affected by the input pulse interval if the systems do not perform the synaptic off-current blocking operation. Consequently, to determine the effect of synaptic off-currents on the network, the operation of the SNN inference system should be reconsidered by mapping i_{off} to each synaptic device in the network according to the relationship shown in Fig. 6(c).

B. SNN SIMULATION RESULT

To determine the effect of the synaptic off-current on the SNN network, a high-level SNN inference simulation was performed by considering the i_{offsum} flowing from each source line to the I & F neuron circuit model. Figs. 8(a) and (b) show the inference accuracy of the SFCN consisting of the conventional neuron circuits (i.e., the conventional SFCN) and the proposed neuron circuits (i.e., the proposed SFCN) for the time steps with various input pulse frequencies, respectively. The "frequency" used in the simulation refers to the maximum frequency of the input pulse in datasets. As shown in Fig. 8(a), in the case of the conventional SFCN, the inference accuracy decreases as the frequency decreases. The simulated inference accuracies after 200 time-steps were 98.57%, 98.25%, and 96.92% for frequencies of 200, 20, and 10 kHz, respectively. This result indicates that the effect of synaptic off-current on the membrane potential becomes dominant as the frequency decreases. In other words, the conventional SNN is strongly dependent on the input pulse intervals of the data. In contrast, for the proposed SFCN, the simulated inference accuracies after 200 time steps were 98.62% for frequencies of 200, 20, and 10 kHz, as shown in Fig. 8(b). The drop in accuracy was only 0.02%, regardless of the input pulse frequency. The simulation results for the SCNN consisting of the conventional neuron circuits (i.e., the conventional SCNN) and the proposed neuron circuits (i.e., the proposed SCNN) are shown in Figs. 8(c) and (d), respectively. In the case of the conventional SCNN, the simulated inference accuracies after 200 time steps were 91.74%, 90.21%, and 88.51% for the frequencies of 200, 20, and 10 kHz, respectively, whereas the proposed SCNN showed 91.85% regardless of the input pulse frequencies. Consequently, it was confirmed that the conventional SCNN inference system was also affected by the synaptic off-current, and the classification accuracy performance decreased. However, as shown in Figs. 8(b) and (d), the modeled OCC part of the proposed circuit impeded the charge transfer of input currents below i_{ref}, thereby improving the robustness against unintended charge transfer during the idle time of the SNN inference.

Figs. 9(a), (b), (c), and (d) show the inference accuracy of the conventional SFCN, proposed SFCN, conventional SCNN, and proposed SCNN, respectively, after 200 time steps with the weight variation (σ_w/μ_w) of the synaptic

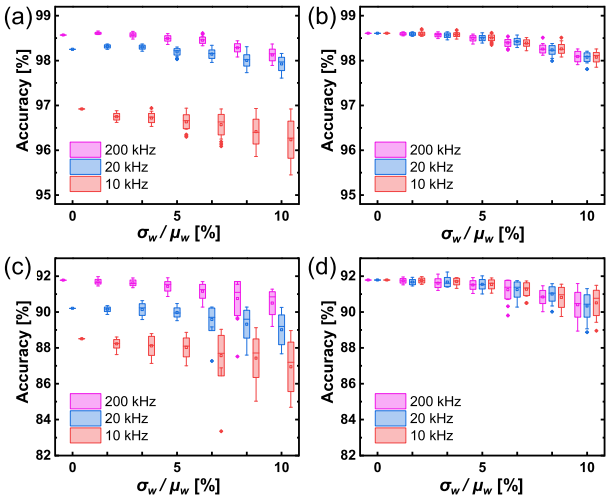

FIGURE 9. Classification accuracy of the simulated SNN with respect to the weight variation of synaptic devices: (a) the conventional SFCN (b) the proposed SFCN (c) the conventional SCNN, and (d) the proposed SCNN.

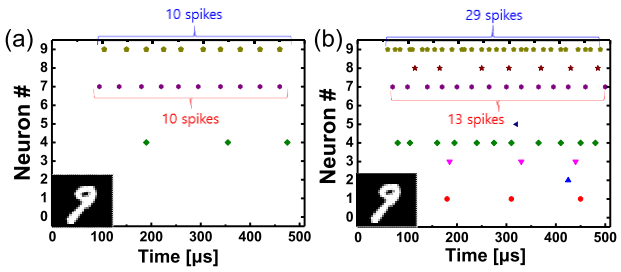

FIGURE 10. Raster plots of a sample digit "9" by SNN-high level simulation using (a) conventional and (b) proposed neuron circuit.

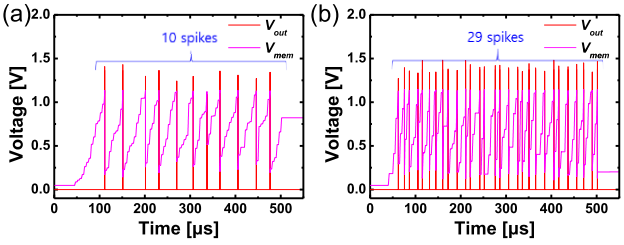

FIGURE 11. Output characteristics of the neuron #9 of a sample digit "9" by circuit-level simulation using (a) conventional and (b) proposed neuron circuit.

devices. The process variation of the FET-type synaptic device determines the standard deviation of V_T^D [39], [40], leading to a variation in the target weight for each synaptic device in the SNN inference system. The programmed weights of synaptic devices have a Gaussian distribution [39], [41]; hence, the effect of weight distribution on the inference accuracy is further investigated by applying the same distribution to the rescaled weights from the non-spiking ANN. As shown in Fig. 9, it is confirmed that the performance degradation of the network due to frequency reduction and weight variation is greater in conventional SNNs than in the proposed SNNs. If σ_w/μ_w of the dual-gate FET-type synaptic device is controlled within 6.25%, as noted in [42], the accuracies of the conventional SFCN and SCNN are expected to drop by approximately 2.07% and 4.98%, respectively, when an input pulse frequency of 10 kHz is used. However, the accuracy drops of the proposed SFCN and SCNN are expected to be only 0.29% and 1.18%, respectively. Therefore, the proposed SNNs are also robust in terms of weight variation owing to their capability of synaptic off-current management.

Fig. 10 shows raster plots of the sample digit "9" obtained from 10 neurons in the last layer of the SFCN inference system. An input pulse frequency of 200 kHz was used for the simulation. In Fig. 10(a), the conventional SFCN has the same number of spikes for neurons #7 and #9; therefore, the classification fails. On the other hand, in Fig. 10(b), the proposed SFCN has more spikes for neuron #9 than for neuron #7; therefore, the inference system successfully classifies the answer. The synaptic off-current distribution in Fig. 7(c) for the rescaled weights of the non-spiking FCN is concentrated at a negative value; therefore, the overall firing rate increases in the case of the proposed SFCN, which blocks synaptic off-currents from the synaptic array.

Fig. 11 shows the output characteristics of neuron #9 in the last layer of the SFCN using a circuit-level simulation. To determine the input currents of unit neurons i_{exc} (t) and i_{int} (t), we extracted all the time-dependent currents from synaptic devices connected to neuron #9 from high-level SNN simulation and applied them to the circuit simulation. In Fig. 11(a), the conventional I & F neuron circuit has an identical number and timing of output spikes as compared to that in the results obtained from Fig. 10(a). Hence, the conventional SFCN cannot classify the correct answer in a circuit-level simulation. This result indicates that the discrepancy between the output characteristics of the modeled circuits in the high-level SNN simulation and that in the circuit-level simulation is sufficiently small to be neglected. The reliability of the two simulation methods was validated when using the proposed circuit. In Fig. 11(b), neuron #9 of the proposed SFCN generated 29 spikes during the simulation time, which is the same number as the high-level SNN simulation results in Fig. 10(b). Therefore, it is confirmed that the difference between the conventional and proposed neuron circuits in the SNN inference system is reproducible, even in a circuit-level simulation.

V. CONCLUSION

In this study, we presented an analog CMOS I & F neuron circuit for a synaptic off-state current-blocking operation. The off-state current of the synaptic device, that is, the synaptic current when no pre-layer spike is applied, can be actively blocked by the OCC part of the proposed circuit. The proposed circuit can generate i_{ref} from 40 nA to 500 nA and handle the spiking pulse width of the input current longer than 200 ns with a charge transfer efficiency of more than 98.5%. In addition, the OCC part of the proposed circuit consumes down to 0.076 pJ/spike for a spiking rate of up to 1×10^7 spikes/sec, thereby demonstrating the potential for a synaptic off-current blocking module applicable to low-power neuron circuits. To confirm the range of the off-state current in a synaptic device, a dual-gate FET-type synaptic device was fabricated, and relevant measurements were obtained. Subsequently, the distribution of i_{offsum} flowing to each neuron was estimated using the measurement results of the dual-gate FET-type synaptic device. Finally, we performed a high-level SNN simulation that compares the inference accuracy and the raster plot of the proposed neuron circuit with those of the conventional neuron circuit, and successfully demonstrated the managing operation of the off-state current in the proposed circuit. Herein, the proposed CMOS I & F neuron circuit utilizes an AND-type synaptic array and shows the practical feasibility of robust SNN hardware for the time interval of the input data. Hardware SNNs consisting of proposed neuron circuits can use various synaptic devices and arrays without considering the performance drop due to synaptic off-state currents. In addition, in future studies, the current blocking operation of the proposed circuit could be applied to network pruning to reduce the computational resources of the neural network.

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SEUNGHWAN SONG received the B.S. and M.S. degrees in electronics engineering from Sogang University, Seoul, South Korea, in 2013 and 2015, respectively. He is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering, Seoul National University (SNU), Seoul. His current research interest includes neuromorphic systems and its application in computing.

BOSUNG JEON (Student Member, IEEE) received the B.S. degree in electrical engineering from Seoul National University (SNU), Seoul, South Korea, where he is currently pursuing the combined master's and Ph.D. degree with the Department of Electrical and Computer Engineering. His current research interest includes neuromorphic systems and its application in computing.

SUNGMIN HWANG (Student Member, IEEE) received the B.S. degree from Hanyang University, Seoul, South Korea, in 2014. He is currently pursuing the combined master's and Ph.D. degree with the Department of Electrical and Computer Engineering, Seoul National University (SNU), Seoul. His research interests include nanoscale silicon devices and neuromorphic systems.

MYUNG-HYUN BAEK (Student Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Seoul National University (SNU), Seoul, South Korea, in 2013 and 2020, respectively. His main research interests include nonvolatile memory technologies and neuromorphic systems.

JONG-HO LEE (Fellow, IEEE) received the Ph.D. degree in electronic engineering from Seoul National University (SNU), Seoul, in 1993. He was a Postdoctoral Fellow with Massachusetts Institute of Technology, Cambridge, MA, USA, from 1998 to 1999. He has been a Professor with the School of Electrical and Computer Engineering, SNU, since 2009.

BYUNG-GOOK PARK (Fellow, IEEE) received the B.S. and M.S. degrees in electronic engineering from Seoul National University (SNU), Seoul, South Korea, in 1982 and 1984, respectively, and the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, USA, in 1990. In 1994, he joined the School of Electrical Engineering, SNU, as an Assistant Professor, where he is currently a Professor.