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Comparative Evaluation of Efficiency and Reliability of Single-Phase Five-Level NPC Inverters for Photovoltaic Systems

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ABSTRACT It is required to reduce the cost of PV energy to be competitive as an alternative energy source. The efficiency and reliability of PV inverters are important aspects to be enhanced to reduce the cost of PV energy since they contribute to the reduction of operational and maintenance costs and to the increase of annual energy production. Therefore, more comprehensive analysis on both efficiency and reliability together including the impacts of various factors is required. In this paper, single-phase five-level NPC inverter topologies for photovoltaic systems are comparatively evaluated in terms of efficiency and reliability by simulations and experiments, in which the impacts of pulse width modulation (PWM) methods and installation locations are considered. The results are expected to give an insight to determine the proper topology and PWM method depending on its installation location considering the reliability as well as the efficiency and total harmonic distortion (THD).

INDEX TERMS PV inverter, NPC inverter, photovoltaic, reliability, efficiency.

I. INTRODUCTION

Renewable energy based electricity generation is rapidly growing in the last decade to replace fossil fuels for reducing carbon emission. Solar photovoltaic (PV) energy is one of the promising solutions for clean electric power generation [1]. Nevertheless, it is still needed to reduce the cost of PV energy to be competitive as an alternative energy source by increasing its penetration levels [2]. The cost of energy is defined by the capital cost, operation and maintenance costs and annual energy production [3]. As the capital cost and operation and maintenance costs are decreased and annual energy production is increased, the cost of energy is reduced. Therefore, for PV systems, the efficiency and reliability improvements of PV inverters are important aspects to decrease the cost of PV energy since they contribute to the reduction of operational and maintenance costs and also contribute to the increase of annual energy production.

One of the most relevant components to the efficiency and reliability of PV inverters is power devices. Most power loss in PV inverters occurs in power devices and it is also considered as one of the vulnerable components [4], [5]. Accordingly, there are various attempts to improve the efficiency of PV inverters in different aspects such as inverter topologies, power device technology and pulse width modulation methods [6]–[11]. Furthermore, the reliability of PV inverters has been analyzed by considering the impact of various factors such as mission profile [12]–[16], inverter topology [12], [13], DC-to-AC ratio [14], [15], and panel degradation rate [16]. However, there is a still lack of study on more comprehensive analysis on both efficiency and reliability together including the impacts of various factors.

The single-phase five-level NPC inverters are attractive due to their outstanding efficiency, lower total harmonic distortion (THD) which leads to smaller passive components and lower leakage current [17]–[19]. The I-type NPC inverter has been proposed first and then some other extended five-level topologies have been proposed such as T-type, Active NPC, asymmetric I-type and T-type NPC inverters for improving its performance in terms of efficiency, cost, leakage current and THD with specific operating methods [7], [20]–[23]. In [6], [20], asymmetric single-phase five-level T-type and I-type NPC inverters have been proposed, where one T-type

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leg and one I-type leg are replaced with half-bridge leg, respectively. These topologies reduce the number of power devices and also improve the efficiency compared with conventional I-type and T-type NPC inverters. However, these topologies are not able to control two capacitor voltages when the deviation occurs between them. Therefore, there is a limited applicability of the asymmetric NPC inverters due to their lack of ability to balance two DC-link capacitor voltages by themselves. On the other hands, conventional T-type and I-type NPC inverters can balance two capacitor voltages by themselves and thus they are more applicable to various PV systems.

In this paper, the comparative performance analysis of single-phase five-level PV inverters is performed by considering the impacts of topology, pulse width modulation method and installation location. The representative single-phase five-level NPC inverter topologies, which are I-type and T-type NPC inverters are considered based on a 7 kW PV system as a case study. The efficiency and reliability of two NPC inverters are analyzed with unipolar pulse width modulation (UP-PWM), which is the most conventional method and one-pole clamping pulse width modulation (OPC-PWM), which is the common method for reducing the power loss [8]. To emulate different installation locations, two mission profiles from Iza in Spain and from Aalborg in Denmark are taken into account. The lifetime evaluation of NPC inverters with two PWM methods under different locations are performed first at component-level and then system-level reliability assessment is carried out. The efficiency of both inverters depending on the PWM methods at different switching frequencies and power levels are analyzed and then verified by experiments with prototype PV inverter systems.

II. SINGLE-PHASE FIVE-LEVEL NPC INVERTERS

A. CONFIGURATIONS OF I-TYPE AND T-TYPE NPC INVERTERS

Fig. 1 (a) and (b) show single-phase five-level I-type and T-type NPC inverter topologies, respectively. The I-type NPC inverter uses two power devices connected in series to block the full DC-link voltage. Therefore, power devices having a lower voltage rating can be used and they have comparatively low switching losses. However, two-series connected power devices with half of the rated blocking voltage leads to the higher conduction loss than that of a single power device having the full blocking voltage rating.

The T-type NPC inverter is composed of power devices having different voltage ratings. Two-series connected power devices are replaced to a single power device ($T_{A1(T)}$, $T_{A4(T)}$, $T_{B1(T)}$ and $T_{B4(T)}$) to block the whole DC-link voltage. Since there are no series-connected power devices for blocking the DC-link voltage, the conduction loss can be reduced. However, power devices with the full blocking voltage rating have higher switching loss compared with that having half of the blocking voltage rating used in the I-type NPC inverter.

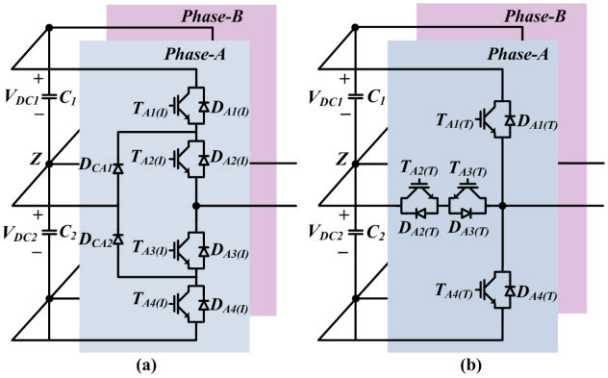

FIGURE 1. Single-phase three-level inverter topologies (a) I-type NPC inverter (b) T-type NPC inverter.

Power devices with half of the voltage rating can be used for bidirectional power devices connected to the neutral-point ($T_{A2(T)}$, $T_{A3(T)}$, $T_{B2(T)}$ and $T_{B3(T)}$) that results in lower switching loss and acceptable conduction loss. More detailed analysis on the power losses of the NPC inverters will be dealt in the following section. The parameters of the NPC inverters considered in this paper are listed in the TABLE 1.

TABLE 1. Parameters for I-Type and T-Type NPC inverters.

Parameters	Value
DC-link voltage (V_{DC})	400 V
Grid phase voltage (V_g)	220 V_{rms}
Switching frequency (f_{sw})	20 kHz
Grid frequency (f_g)	60 Hz
Inductor (L)	2 mH
Power factor	1
IGBT module (I-type)	10-FZ07NIA060SM-P926F43
IGBT module (T-type)	10-12NMA040SH-M267F

B. UNIPOLAR AND ONE-POLE CLAMPING PULSE WIDTH MODULATION METHODS

Each leg of five-level inverters has three switching states of [P], [O] and [N]. The switching state [P] indicates that T_{x1} and T_{x2} are turned on in Fig. 1 and thus the corresponding pole voltage becomes $+V_{DC}/2$. The switching state [O] means that the pole voltage is 0 by turning on T_{x2} and T_{x3}. In switching state [N], T_{x3} and T_{x4} are turned on which results in $-V_{DC}/2$ of pole voltage.

Fig. 2 (a) shows the reference voltages (V_{A_ref} and V_{B_ref}) of the I-type and T-type NPC inverters for a unipolar pulse width modulation (UP-PWM) method. There is a phase difference of 180 ° between the two reference voltages of V_{A_ref} and V_{B_ref} and thus they are expressed as

$$\begin{aligned} V_{A\_ref} &= V_m sin(2\pi f_g t) \\ V_{B\_ref} &= V_{A\_ref} \end{aligned} \tag{1}$$

where V_m = amplitude of reference voltage and f_g = grid frequency.

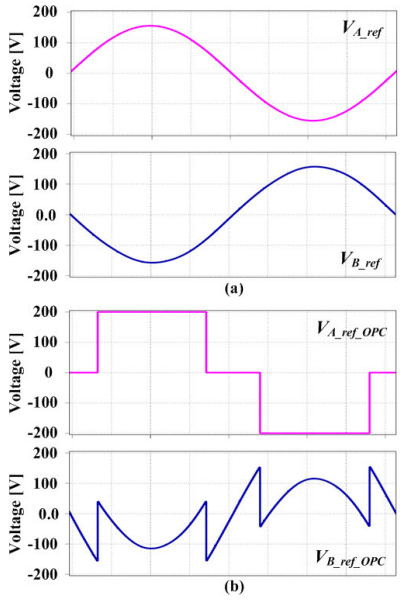

FIGURE 2. Comparison of reference voltages (a) UP-PWM (b) OPC-PWM.

The reference voltages are modified for a one-pole clamping (OPC) PWM, where the V_{A_ref} is modified to only have value of $V_{DC}/2$, 0 or $-V_{DC}/2$ depending on the magnitude of V_{A_ref}. If V_{A_ref} / V_m is more than 0.5, the reference voltage of phase-A for the OPC-PWM ($V_{A\_ref\_OPC}$) is modified to $V_{DC}/2$. Accordingly, the reference voltage of phase-B ($V_{B\_ref\_OPC}$) is modified to V_{B_ref} + ($V_{DC}/2$-V_{A_ref}) to maintain the magnitude of the voltage difference between two phases. If V_{A_ref}/V_m is between -0.5 and 0.5, the $V_{A\_ref\_OPC}$ and the $V_{B\_ref\_OPC}$ become 0 and $V_{B\_ref} - V_{A\_ref}$, respectively. Finally, $V_{A\_ref\_OLC}$ is clamped to $-V_{DC}/2$ and $V_{B\_ref\_OPC}$ is changed to $V_{B\_ref} - (V_{DC}/2 + V_{a\_ref})$ when V_{A_ref}/V_m is less than -0.5. Consequently, the modified reference voltages for the OPC-PWM are defined as

$$\begin{aligned}
&(\text{if } V_{A_ref}/V_m > 0.5),\\
V_{A_ref_OPC} &= V_{DC}/2\\
V_{B_ref_OPC} &= V_{B_ref} + (V_{DC}/2 - V_{A_ref})\\
&= V_{DC}/2 - 2V_{A_ref}\\
&(\text{if } 0.5 > V_{A_ref}/V_m > -0.5),\\
V_{A_ref_OPC} &= 0\\
V_{B_ref_OPC} &= V_{B_ref} - V_{A_ref}\\
&= -2V_{A_ref}\\
&(\text{if } V_{A_ref}/V_m < -0.5),\\
V_{A_ref_OPC} &= -V_{DC}/2\\
V_{B_ref_OPC} &= V_{B_ref} - (V_{DC}/2 + V_{A_ref})\\
&= -V_{DC}/2 - 2V_{A_ref}
\end{aligned} \tag{2}$$

The modified reference voltages for the OPC-PWM are shown in Fig. 2 (b). The OPC-PWM method is able to decreases the switching loss of clamped leg by keeping its switching state to [P], [O], and [N] depending on the magnitude of reference voltage.

III. COMPARATIVE ANALYSIS OF POWER LOSS AND JUNCTION TEMPERATURE DISTRIBUTIONS

In this section, the power losses and junction temperature (T_j) distributions of the I-type and T-type NPC inverters under two PWM methods are comparatively analyzed.

The power losses of devices are composed of conduction and switching losses. The conduction loss (P_{cond}) averaged in one switching cycle is represented as

$$P_{cond} = \frac{1}{T_s}\int_0^{T_S} V_{CE(I_C,\,T_j)} \cdot I_C\, dt \tag{3}$$

where T_s = switching period, I_C = collector current, V_{CE} = collector-emitter voltage as functions of collector current (I_C) and junction temperature (T_j). V_{CE} can be replaced to forward voltage (V_F) for diodes.

The switching loss (P_{sw}) of the IGBT is calculated as

$$P_{sw} = E_{sw(I_C,\,T_j)} \cdot f_{sw} \tag{4}$$

where f_{sw} = switching frequency of the device, $E_{sw(Ic,Tj)}$ = switching energy as functions of I_C, and T_j. E_{sw} can be substituted to reverse recovery energy (E_{rec}) for the diodes. The related values of V_{CE} (or V_F) and E_{sw} (or E_{rec}) are provided by manufacturers through the datasheets of power devices.

The junction temperature has to be considered for the power loss analysis because the forward voltage drop and switching energy of devices are influenced by junction temperature. The junction temperatures (T_j) of the devices in the target IGBT modules in this paper can be modeled by the Foster thermal model as shown in Fig. 3.

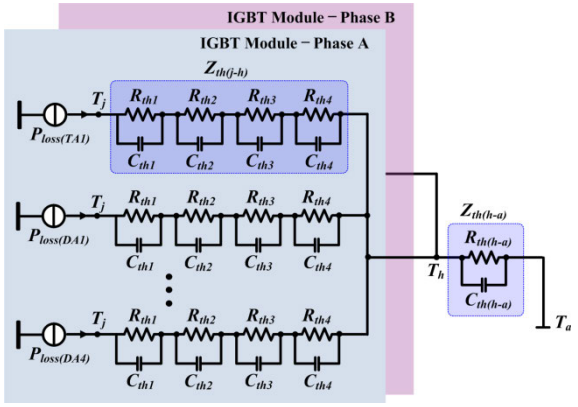

FIGURE 3. Thermal model of the IGBT module for T-type NPC inverter: P_{loss} – power loss of device, $Z_{th(j-h)}$ – junction-to-heatsink thermal impedance, $Z_{th(h-a)}$ – heatsink-to-ambient thermal impedance, R_{th} – thermal resistance, C_{th} – thermal capacitance, T_j – junction temperature, T_h – heatsink temperature, T_a – ambient temperature.

Then, the junction temperature can be obtained as

$$\begin{aligned}
T_j(t) &= P_{loss(device)}(t) \cdot Z_{th(j-h)}(t)\\
&\quad + P_{loss(Module)}(t) \cdot Z_{th(h-a)}(t) + T_a
\end{aligned} \tag{5}$$

where $P_{loss(device)}$ = power loss of device, $Z_{th(j-h)}$ = junction to heatsink thermal impedance, $P_{loss(Module)}$ = power loss

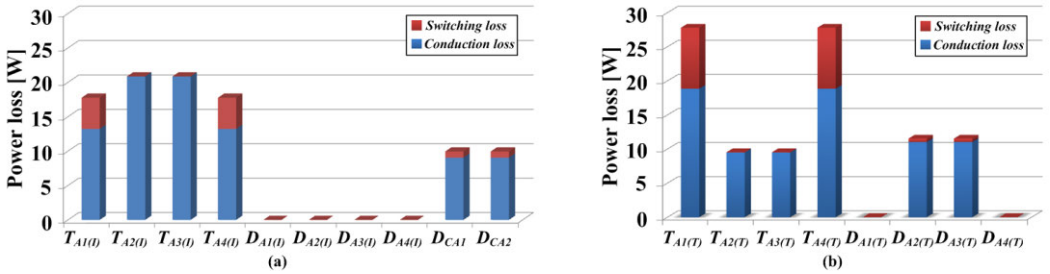

FIGURE 4. Power loss distributions of three-level NPC inverters at 7 kW with UP-PWM (a) I-type NPC inverter (b) T-type NPC inverter.

of IGBT module, $Z_{th(h-a)}$ = heatsink to ambient thermal impedance and T_a = ambient temperature.

The $Z_{th(j-h)}$ of power devices are expressed as

$$Z_{th(j-h)}(t) = \sum_{i=1}^{n} R_i(1 - e^{-t/\tau}) \tag{6}$$

where $\tau_i = R_i C_i$, R is the thermal resistance, C is the thermal capacitance and i means the number of RC combinations for the Foster model [24]. The related parameters for the thermal model, which are R and τ can be obtained from the datasheets.

It has to be guaranteed that the junction temperatures of power devices at the rated power of NPC inverters are below the maximum rated junction temperature (T_{jmax}) of the devices. Therefore, typically, the cooling capacity is chosen so that the junction temperature (T_j) is about 70-80 % of the T_{jmax} at the rated power [25]. Accordingly, in this study, it is assumed that the heat-sink to ambient thermal resistance $R_{th(h-a)}$ is 0.2 K/W and ambient temperature is 40 °C. In addition, two IGBT modules are placed on the same heat-sink.

The power loss distribution of the I-type NPC inverter at 7 kW with the UP-PWM is illustrated in Fig. 4 (a). Since both legs have the symmetric power loss distribution when the UP-PWM is applied, the phase-A of each inverter is considered for the analysis. The conduction losses are mainly concentrated in the IGBTs of $T_{A2(I)}$ and $T_{A3(I)}$ and they have the highest power loss among the devices.

In the case of IGBTs of $T_{A1(I)}$ and $T_{A4(I)}$ and clamping diodes of D_{CA1} and D_{CA2}, there are not only the conduction losses but also some switching losses and the switching losses are increased as switching frequency increases. There are almost zero power losses in the diodes $D_{A1(I)}$, $D_{A2(I)}$, $D_{A3(I)}$, and $D_{A4(I)}$. The corresponding junction temperature distribution of the I-type NPC inverter is shown in Fig. 5(a). $T_{A2(I)}$ and $T_{A3(I)}$ have the highest junction temperature of 104.5 °C. The temperature difference between the inner IGBTs of $T_{A2(I)}$ and $T_{A3(I)}$ and the outer IGBTs of $T_{A1(I)}$ and $T_{A4(I)}$ are about 3 °C.

In the case of T-type NPC inverter, the power losses in $T_{A1(T)}$ and $T_{A4(T)}$ are dominant as shown in Fig 4 (b). It can be seen that $T_{A1(T)}$ and $T_{A4(T)}$ have higher switching losses than $T_{A1(I)}$ and $T_{A4(I)}$, whereas they have lower conduction losses compared to two series connected power devices having half of the blocking voltage rating as expected in previous section II. Even though the bidirectional devices have lower power losses than the IGBTs of $T_{A1(T)}$ and $T_{A4(T)}$, they also take a large portion of the total power loss of the T-type NPC inverter, where the conduction losses are mainly contributed. Nearly no power losses occur in the diodes of $D_{A1(T)}$ and $D_{A4(T)}$. The corresponding junction temperature distribution can be seen in Fig. 5 (b).

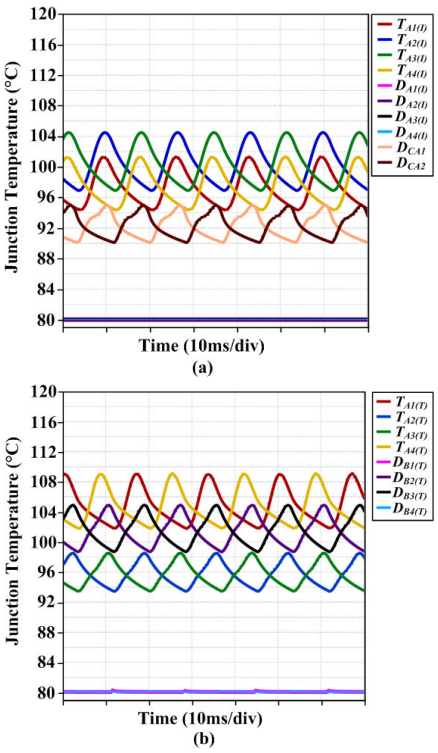

FIGURE 5. Junction temperature distributions with UP-PWM (a) I-type NPC inverter (b) T-type NPC inverter.

The IGBTs of $T_{A1(T)}$ and $T_{A4(T)}$ have the highest junction temperature of 109 °C and are followed by $D_{A2(T)}$ and $D_{A3(T)}$ as 105 °C and $T_{A2(T)}$ and $T_{A3(T)}$ as 98.5 °C. It can be seen from above results that $T_{A2(I)}$, $T_{A3(I)}$ and $T_{A1(T)}$, $T_{A4(T)}$ are the most reliability-critical parts, in the I-type and T-type NPC inverters, respectively.

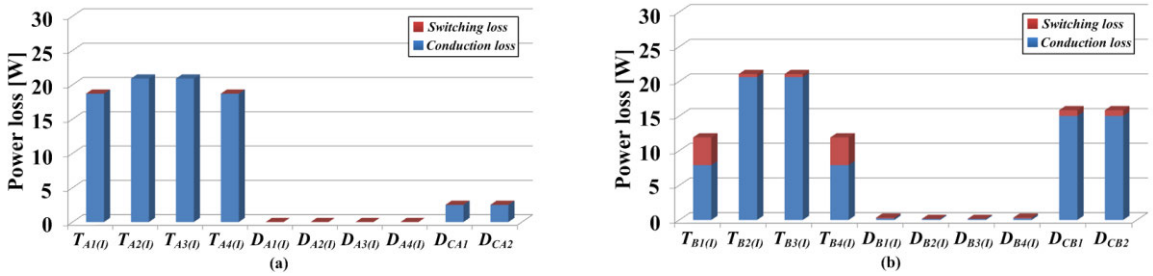

FIGURE 6. Power loss distributions of I-type NPC inverters at 7 kW with OPC-PWM (a) phase-A (b) phase-B.

The power loss distribution of the I-type NPC inverter when OPC-PWM is applied can be seen from Fig. 6. In the case of power devices in the phase-A as shown in Fig. 6 (a), there are almost zero switching losses in all power devices because the switching state of the phase-A is fixed to [P], [O], and [N] for a certain period of time according to the magnitude of the reference voltage.

The switching losses of $T_{A1(I)}$ and $T_{A4(I)}$ are replaced to conduction losses and the total losses of them are slightly raised. No remarkable power loss variation can be seen in $T_{A2(I)}$ and $T_{A3(I)}$. Further, while the switching state is fixed to [P] or [N], the conduction losses of D_{CA1} and D_{CA2} are significantly reduced since the current does not flow thorough the bidirectional devices. The magnitude of the modified reference voltage of the phase-B ($V_{B\_ref\_OPC}$) is generally reduced compared with the original reference voltage of the phase-B (V_{B_ref}). It means that the period of the switching state [O] increases, while that of the switching state [P] or [N] decreases due to the reduced modulation index. Therefore, the conduction losses of $T_{B1(I)}$ and $T_{B4(I)}$ are dropped but the conduction losses of D_{CB1} and D_{CB2} are increased as shown in Fig. 6 (b). The junction temperatures of the power devices in the phase-A of the I-type NPC inverter are shown in Fig. 7 (a). Even though the power loss of each IGBT is almost similar with that under the UP-PWM, the maximum junction temperatures of the devices are slightly decreased since the overall power loss of the IGBT module is reduced. There are remarkable temperature drops of 13 °C in the clamping diodes of D_{CA1} and D_{CA2}. In the phase-B as shown in Fig. 7 (b), the junction temperatures of D_{CB1} and D_{CB2} are raised from 95 °C to 102.5 °C but the junction temperatures $T_{B1(T)}$ and $T_{B4(T)}$ decrease from 101.5 °C to 91 °C which are corresponding to the power loss distribution shown in Fig. 6 (b). It can be seen that D_{CB1} and D_{CB2} have the maximum junction temperature as 102.5 °C and $T_{A2(I)}$, $T_{A3(I)}$, $T_{B2(I)}$ and $T_{B3(I)}$ also have the similar junction temperature as about 102 °C.

Fig. 8 (a) shows the power losses of the devices in the phase-A of the T-type inverter with the OPC-PWM. The switching losses of $T_{A1(T)}$ and $T_{A4(T)}$ are replaced to the conduction losses and total losses of $T_{A1(T)}$ and $T_{A4(T)}$ are a bit reduced. Further, it can be seen that the power losses of the bidirectional power devices are notably decreased due

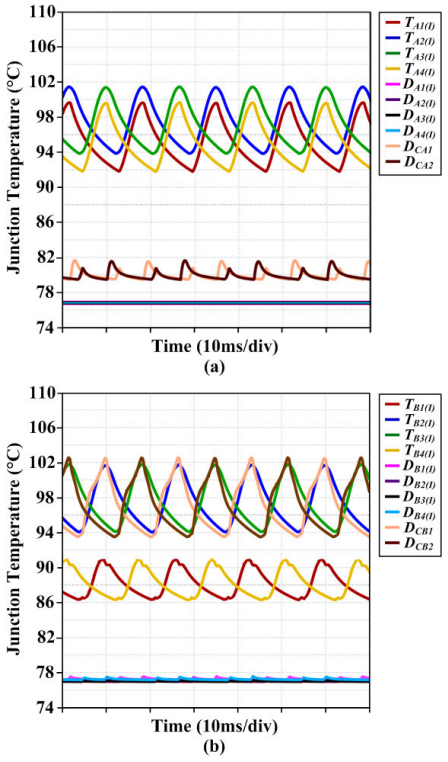

FIGURE 7. Junction temperature distribution of I-type NPC inverter with OPC-PWM (a) phase-A (clamped leg) (b) phase-B.

to the same reason as explained for the clamped leg of the I-type NPC inverter. The junction temperatures of the devices in the phase-A are illustrated in Fig. 9 (a). Because of the reduced power losses, the junction temperatures of all devices are fallen. Especially, there are large temperature drops in $T_{A2(T)}$, $T_{A3(T)}$, $D_{A2(T)}$, and $D_{A3(T)}$.

In the case of phase-B, as shown in Fig. 8 (b), the conduction losses of $T_{B1(T)}$ and $T_{B4(T)}$ are decreased. The conduction losses of $T_{B2(T)}$, $T_{B3(T)}$, $D_{B2(T)}$, and $D_{B3(T)}$, on the other hand, are increased compared with those of under UP-PWM due to the reduced magnitude of the modified reference voltage of the phase-B ($V_{B\_ref\_OPC}$) as explained before for the I-type NPC inverter. The significant junction temperature rises can be seen in $T_{B2(T)}$, $T_{B3(T)}$, $D_{B2(T)}$, and $D_{B3(T)}$ from Fig. 9 (b) owing to the increased power losses. The junction

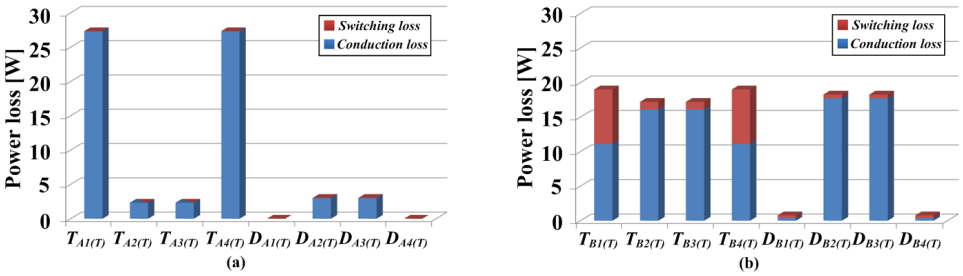

FIGURE 8. Power loss distributions of T-type NPC inverters at 7 kW with OPC-PWM (a) phase-A (b) phase-B.

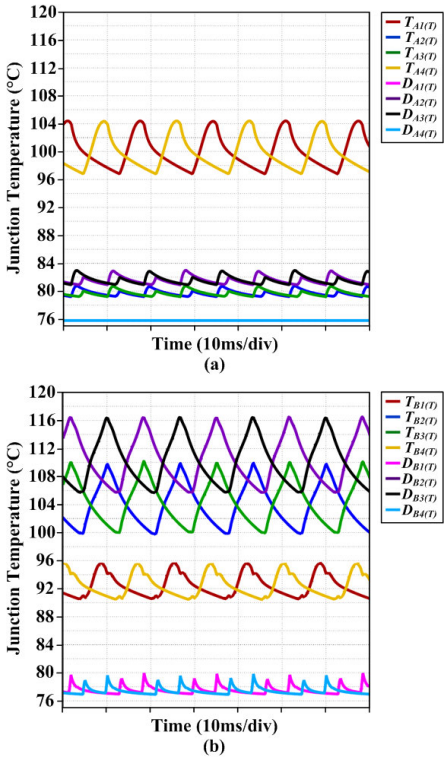

FIGURE 9. Junction temperature distribution of T-type NPC inverter with OPC-PWM (a) phase-A (clamped leg) (b) phase-B.

temperatures of $T_{B2(T)}$ and $T_{B3(T)}$ are increased from 98.5 °C to 110 °C and the junction temperatures of $D_{B2(T)}$, and $D_{B3(T)}$ are raised from 105 °C to 116.5 °C which is the highest junction temperature in the T-type NPC inverter with the OPC-PWM. On the contrary, the junction temperatures of $T_{B1(T)}$ and $T_{B4(T)}$ go down from 109 °C to 96 °C.

The total power losses of the I-type and T-type NPC inverters at the different power levels are summarized in TABLE 2. Under the UP-PWM, the T-type inverter has lower power loss than the I-type NPC inverter at 1, 2 and 4 kW output powers. However, the I-type NPC inverter has lower power loss than the T-type NPC inverter at 7 kW output power. When the OPC-PWM is applied, both NPC inverters have lower power losses than those of under UP-PWM. Furthermore, the I-type

TABLE 2. Power losses of the I-Type and T-Type NPC inverters under different output powers (at f_{sw} = 20 kHz).

Modulation	NPC inverter	Power loss (W)			
	Output power	1 kW	2 kW	4 kW	7 kW
UP-PWM	I-type	17.7	40.3	94.4	194.3
	T-type	16.9	37.9	90.0	195.1
OPC-PWM	I-type	17.0	38.2	89.3	183.1
	T-type	15.0	34.1	80.3	174.6

NPC inverter has higher power loss than the T-type NPC inverters at all considered power ratings. The power losses of the I-type NPC inverter are decreased by 4 %, 5.2 %, 5.4 % and 5.8 % at 1 kW, 2 kW, 4 kW and 7 kW, respectively. In the case of T-type NPC inverter, it has reduced power losses by 8.3 %, 10 %, 10.6 % and 10.5 % at 1 kW, 2 kW, 4 kW and 7 kW, separately. It can be seen from the results that the OPC-PWM is more effective for the T-type NPC inverter than the I-type NPC inverter for reducing the power loss. Furthermore, the power losses at 7 kW under the different switching frequencies are presented in TABLE 3. The result shows that the I-type NPC inverter has higher efficiency than the T-type NPC inverter at the relatively low switching frequencies when the UP-PWM is applied and vice versa at relatively high switching frequencies. The T-type NPC inverter applying OPC-PWM has the lowest power losses under all considered switching frequency ranges.

TABLE 3. Power losses of the I-Type and T-Type NPC inverters under different switching frequency (at P_{out} = 7 kW).

Modulation	NPC inverter	Power loss (W)			
	Switch. freq. (f_{sw})	5 kHz	10 kHz	20 kHz	30 kHz
UP-PWM	I-type	178.2	183.4	194.3	205.8
	T-type	165.0	174.5	195.1	217.2
OPC-PWM	I-type	175.5	177.8	183.1	188.7
	T-type	160.5	165.1	174.7	185.1

The highest junction temperatures of 104.5 °C in the I-type NPC inverter with the UP-PWM is 4.5 °C lower than that of the T-type NPC inverter with the UP-PWM which is 109 °C. When the OPC-PWM is applied, the highest junction

temperatures of the devices in the I-type NPC inverter are changed from $T_{A2,3(I)}$ and $T_{B2,3(I)}$ to D_{CB1} and D_{CB2} and temperature is decreased from 104.5 °C to 102.5 °C. In T-type NPC inverter, however, the highest junction temperature is raised to from 109.0 °C to 116.5 °C where the devices having the highest junction temperatures are changed from $T_{A1,4(T)}$ and $T_{B1,4(T)}$ to $D_{B2(T)}$ and $D_{B3(T)}$ when the same cooling capacity, which is represented as $R_{th(h-a)}$ is taken into account. The highest junction temperatures of the I-type and T-type NPC inverters at 7 kW with two PWM methods are summarized in TABLE 4.

TABLE 4. The highest junction temperatures in I-type and T-type NPC inverters.

Modulation	NPC inverter	Device	Junction Temperature
UP-PWM	I-type	$T_{A2,3(I)}$, $T_{B2,3(I)}$	104.5 °C
	T-type	$T_{A1,4(T)}$, $T_{B1,4(T)}$	109.0 °C
OPC-PWM	I-type	$D_{CB1,2}$	102.5 °C
	T-type	$D_{B2,3(T)}$	116.5 °C

From above results, it is clearly seen that the T-type NPC inverter with the OPC-PWM has the superiority in terms of efficiency but higher cooling capacity is required because the highest junction temperature is higher than the others. From the maximum junction temperature point of view, the I-type NPC inverter has better performance than the others.

IV. LIFETIME EVALUATIONS OF POWER DEVICES

As analyzed in the section III, the power devices in the I-type and T-type NPC inverters have different thermal loadings. Furthermore, the thermal loadings of the power devices and their distributions are also affected by the PWM methods. In this section, the mission profile based comparative reliability evaluation of the I-Type and T-type NPC inverters with two PWM methods are carried out by focusing on the lifetimes of power devices because power devices are typically treated as one of the most reliability-critical components in PV inverters [4], [5]. Further, the thermal stress is taken into consideration since it is the main cause of wear-out failure of power devices such as bond-wire fatigue and solder-joint fatigue [5]. The mission profiles of PV systems composed of solar irradiation and ambient temperature recorded from Iza in Spain per 1minute and from Aalborg in Denmark per 5 minutes for about a year are considered as shown in Fig. 10. The lifetime evaluation is implemented first at a component-level to obtain the accumulated damage of each device. Then, a system-level reliability assessment is carried out by employing the Monte Carlo analysis method.

A. THERMAL LOADINGS OF POWER DEVICES UNDER MISSION PROFILES OF PV SYSTEMS

The input power of PV inverter generated from the PV array is determined depending on the solar irradiation and ambient temperature based on PV model. Afterwards, the junction

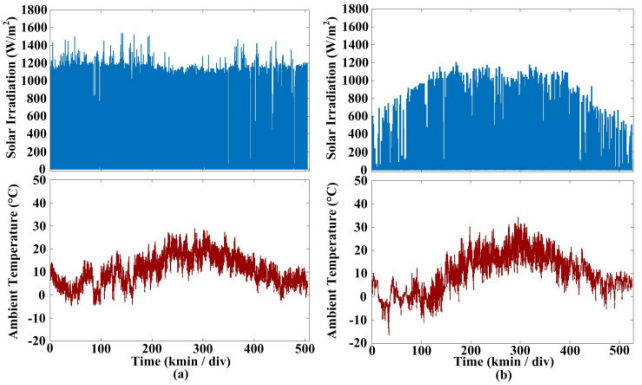

FIGURE 10. Mission profiles of PV system recorded in (a) Iza in Spain (b) Aalborg in Denmark.

temperature of each device at the given input power is calculated by the thermal modeling as expressed in (5) and (6). Then, the thermal loadings of power devices during the given mission profile are obtained through a look up table, which is built in connection with the input power and ambient temperature. Consequently, the thermal loadings of power devices are obtained when the input power and ambient temperature are given.

Fig. 11 shows the thermal loadings of $T_{A2(I)}$ and $T_{A3(I)}$ in the I-type NPC inverter with the UP-PWM when it is operated under the mission profiles recorded in Iza and Aalborg, respectively. Even though the same topology and IGBT module are considered, it can be seen that $T_{A2(I)}$ and $T_{A3(I)}$ under the mission profile from Iza have higher thermal loading than $T_{A2(I)}$ and $T_{A3(I)}$ under the mission profile from Aalborg. It is because of that Iza has relatively higher solar irradiation than Aalborg throughout the year and thus higher power is generated.

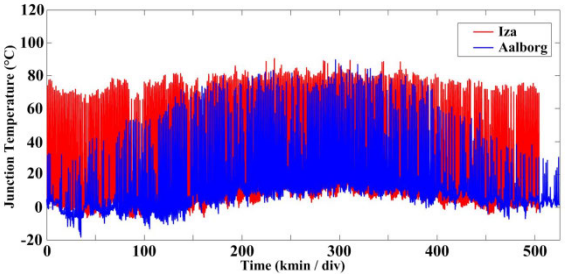

FIGURE 11. Thermal loading of $T_{A2,3(I)}$ in I-type NPC inverter under the mission profiles recorded in Iza in Spain and Aalborg in Denmark.

B. TRANSLATION OF THERMAL LOADING INTO ACCUMULATED DAMAGE

The accumulated damage of each device can be obtained from the thermal loading. The accumulated damage (AD) of power devices is computed based on the Miner's rule as

$$AD = \sum_{i=1}^{k} \frac{n_i}{(N_f)_i} \tag{7}$$

TABLE 5. Accumulated damages of power devices in the I-type and T-type NPC inverters.

Location	NPC inverter	Modulation	Accumulation Damage [%] (Lifetime [Years])							
			$T_{A1,4}$	$T_{A2,3}$	$D_{CA1,2}$	$D_{A2,3}$	$T_{B1,4}$	$T_{B2,3}$	$D_{CB1,2}$	$D_{B2,3}$
Iza	I-Type	UP-PWM	0.617 (162)	0.867 (115)	0.437 (228)	-	0.617 (162)	0.867 (115)	0.437 (228)	-
	I-Type	OPC-PWM	0.630 (158)	0.719 (139)	0.161 (621)	-	0.327 (305)	0.726 (137)	0.841 (119)	-
	T-Type	UP-PWM	0.953 (105)	0.480 (208)	-	0.825 (121)	0.953 (105)	0.480 (208)	-	0.825 (121)
	T-Type	OPC-PWM	0.746 (134)	0.123 (813)	-	0.161 (321)	0.380 (263)	1.039 (96)	-	1.835 (54)
Aalborg	I-Type	UP-PWM	0.184 (543)	0.265 (377)	0.138 (724)	-	0.184 (543)	0.265 (377)	0.138 (724)	-
	I-Type	OPC-PWM	0.191 (523)	0.215 (465)	0.057 (1754)	-	0.106 (943)	0.217 (460)	0.248 (403)	-
	T-Type	UP-PWM	0.260 (384)	0.141 (709)	-	0.240 (416)	0.260 (384)	0.141 (709)	-	0.240 (416)
	T-Type	OPC-PWM	0.204 (490)	0.043 (2423)	-	0.054 (1851)	0.116 (862)	0.278 (359)	-	0.506 (197)

where n_i is the number of cycles accumulated at a certain thermal stress (S_i) and $(N_f)_i$ is the number of cycles to failure at S_i. The AD indicates how much damage is accumulated or how much life is consumed when it is operated with mission profiles. The power device is considered to reach its end-of-life when AD becomes 1 (or 100 %) [26], [27].

The composition of thermal stress is dependent on the lifetime model parameters. It is typically a combination of junction temperature swing (ΔT_j), minimum junction temperature (T_{jm}) and heating time (t_{on}) extracted from thermal loading by using a Rainflow counting method [28]. Then, the number of cycles to failure at the given thermal stress is determined by putting them into the lifetime model of power devices. In this study, the lifetime model regarding bond-wire failure presented in [29] is used because lifetime models of the IGBT modules considered in this study are not available. Therefore, it is recommended that the results should be considered only for the purpose of the comparison.

Fig. 12 shows the accumulated damages of $T_{A2(I)}$ and $T_{A3(I)}$ in the I-type NPC inverter corresponding to the thermal loadings shown in Fig. 11. $T_{A2(I)}$ and $T_{A3(I)}$ under the mission profile recorded in Iza have higher accumulated damage as 0.867 % than $T_{A2(I)}$ and $T_{A3(I)}$ under the mission profile from Aalborg as 0.265 %. It can be expected that $T_{A2(I)}$ and $T_{A3(I)}$ of the I-type inverter located in Iza has shorter lifetime than those of the I-type inverter located in Aalborg.

The accumulated damage of the power devices in the I-type and T-type NPC inverters with the UP-PWM and OPC-PWM under two mission profiles are listed in TABLE 5, respectively. Among the power devices in the I-type NPC inverter operated with the UP-PWM under the mission profile of Iza, $T_{A2,3(I)}$ and $T_{B2,3(I)}$ have the highest AD as 0.867 %, and thus it can be expected that they are the most reliability-critical devices. When the OPC-PWM is applied, the power devices having the highest AD becomes $D_{CB1,2}$ as 0.841 %. AD of each device is generally reduced except for $D_{CB1,2}$ and $T_{A1,4(I)}$. In the case of T-type inverter located in Iza, $T_{A1,4(T)}$ and $T_{B1,4(T)}$ have the highest AD of 0.953 %. It is higher than those of the I-type NPC inverter by 0.112 %. When the OPC-PWM is applied, almost all power devices of the clamped leg which is the phase-A have lower AD than that of the phase-A with the UP-PWM. However, there are significant increases in AD of $D_{B2,3(T)}$ and $T_{B2,3(T)}$ of the phase-B even though AD of $T_{B1,4(T)}$ is reduced. The highest value is increased from 0.953 % of $T_{A1,4(T)}$ and $T_{B1,4(T)}$ to 1.835 % of $D_{B2,3(T)}$. The power devices of the I-type and T-type NPC inverters under the mission profile from Aalborg have the lower AD but similar tendency with that under the mission profile from Iza.

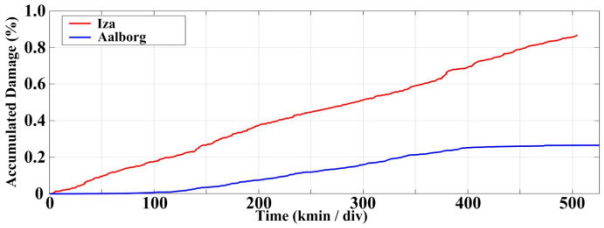

FIGURE 12. Accumulated damages of $T_{A2,3(I)}$ in I-type NPC inverter under the mission profiles recorded in Iza in Spain and Aalborg in Denmark.

As it can be seen from the results, the PWM method and mission profile have the significant effects on the accumulated damage of the power device. Further, each power device has different AD and thus different lifetime. Therefore, the system-level reliability assessment is required.

C. SYSTEM-LEVEL LIFETIME ASSESSMENT BASED ON MONTE CARLO ANALYSIS METHOD

In practice, the lifetime is expressed in terms of statistical value. Accordingly, a percentile lifetime is widely used to present the lifetime of a population of items. However, lifetime models including statistical information are rarely

provided and also difficult to develop lifetime models through a lot of testing of power devices such as power cycling test [30]–[33]. Even though a lifetime model is given, that lifetime is a certain percentile lifetime model (e.g B_{10}) or lifetime model without statistical analysis as provided in [29], [34]. The lifetime model used in this paper is also not having the statistical information. Therefore, the Monte Carlo method is employed to have the lifetime distributions of the power devices. Since there are various thermal stresses consists of different magnitudes of ΔT_j, T_{jm} and t_{on} during the given one-year mission profile, it is required to convert them into the static equivalent ΔT_{j_eq}, T_{jm_eq} and t_{on_eq} to simplify the Monte Carlo method. It means that the same damage accumulated for the given one-year mission profile is obtained when the static equivalent thermal stress is applied to the lifetime model. To reduce the degree of freedom for choosing the equivalent values, the average values of T_{jm} and t_{on} during the mission profile are used for the T_{jm_eq} and t_{on_eq} and then the corresponding ΔT_{j_eq} is found based on the lifetime model and (7). The Monte Carlo method is implemented with a population of 10,000 samples by considering the 5 % variations with a normal distribution in the lifetime model parameters and equivalent thermal stresses according to previous research in [12], [31], [35]. The lifetime distribution of each power device based on the Monte Carlo simulation is fitted with the Weibull distribution, which is expressed as

$$f(t) = \frac{\beta}{\eta}\left(\frac{t}{\eta}\right)^{\beta-1} e^{-\left(\frac{t}{\eta}\right)^{\beta}} \tag{8}$$

where $f(x)$ is probability density function of the Weibull distribution. t, β and η are the operating time, shape parameter and scale parameter, respectively. Then, the cumulative density function of the Weibull distribution and also called unreliability function is obtained as

$$F(t) = \int_0^t f(t)\,dx \tag{9}$$

Since the individual power device failure will cause the overall inverter failure, based on the reliability block diagram approach in [36], the unreliability function of the entire inverter system $F_{inv}(t)$ can be represented as

$$F_{inv}(t) = 1 - \prod_{k=1}^{n}(1 - F_k(t)) \tag{10}$$

where $F_k(t)$ is the unreliability of the k_{th} power device in the inverter.

Finally, the percentile lifetime (B_x lifetime) is determined based on the unreliability function. B_x lifetime presents the lifetime of a population of items. It is a time by which a certain percentage of the items might have failed. For example, B_{10} lifetime means the time by which 10 % of the power devices are failed. In other words, the reliability is 0.9 at that time.

Fig. 13 shows the unreliability function of the I-type NPC inverter with the UP-PWM under the mission profile from Iza. It can be seen from Fig. 13 (a) that $T_{A2,3(I)}$ and $T_{B2,3(I)}$ have the shortest lifetime among power devices in the I-type NPC inverter. This result is corresponding to the accumulated damage analysis in the previous section B of III. The unreliability function of overall I-type NPC inverter is shown in Fig. 13 (b) and B_1 and B_{10} lifetimes are 20.5 and 40.5 years, respectively. It indicates that 1 % of the population is expected to fail after 20.5 years and 10 % of the population is forecasted to be failed after 40.5 years.

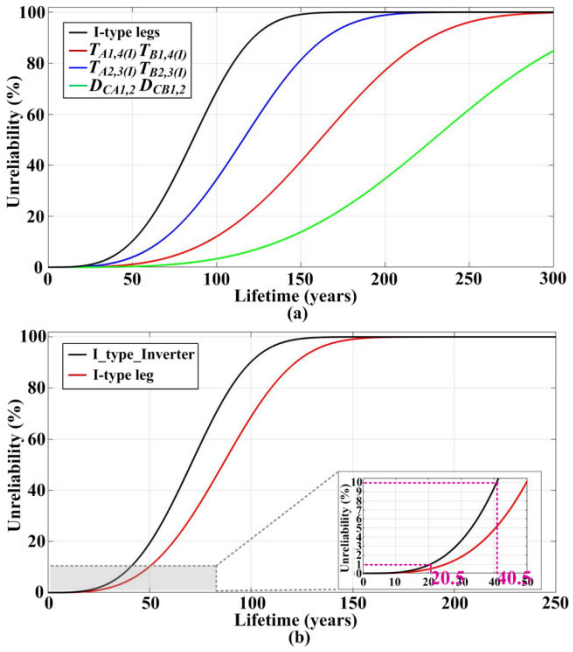

FIGURE 13. Unreliability functions of the I-type NPC inverter with UP-PWM under the mission profile in Iza in Spain (a) power devices in the I-type NPC inverter (b) I-type NPC inverter.

In the case of power devices in the T-type NPC inverter, $T_{A1,4(T)}$ and $T_{B1,4(T)}$ have the lowest life expectancy as shown in Fig. 14 (a). Further, as shown in Fig. 14 (b), the B_1 and B_{10} lifetimes of the T-type NPC inverter are expected as 17 years and 34 years, respectively. It can be seen that the I-type NPC inverter has longer lifetime than the T-type NPC inverter under the mission profile from Iza when the UP-PWM is applied. Thus, the I-type NPC inverter has higher reliability than the T-type NPC inverter.

As it can be seen from Fig. 15 (a), in the clamped leg which is the phase-A, D_{CA1} and D_{CA2} are the critical power devices in terms of reliability, whereas $T_{B2(I)}$ and $T_{B3(I)}$ have the shortest lifetime in the non-clamped leg which is the phase-B as illustrated in Fig. 15 (b). The two legs have the different unreliability functions due to the asymmetric thermal loadings. The clamped leg has the shorter lifetime than the non-clamped leg. The unreliability function of the I-type NPC inverter with the OPC-PWM is given in Fig. 15 (c), where B_1 and B_{10} lifetimes are expected as 22 years and 43.5 years, respectively. It can be seen that the lifetime of the I-type NPC inverter with OPC-PWM is slightly increased compared with that of the I-type NPC inverter with UP-PWM. It is due to

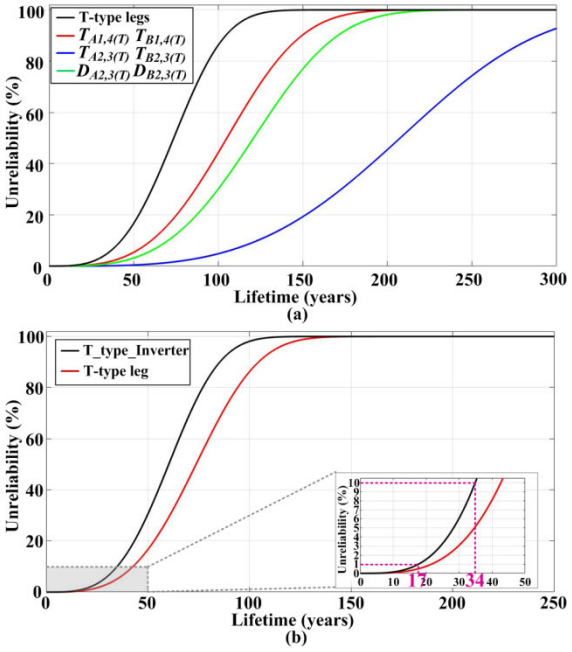

FIGURE 14. Unreliability functions of the T-type NPC inverter with UP-PWM under the mission profile in Iza in Spain (a) power devices in the T-type leg (b) T-type NPC inverter.

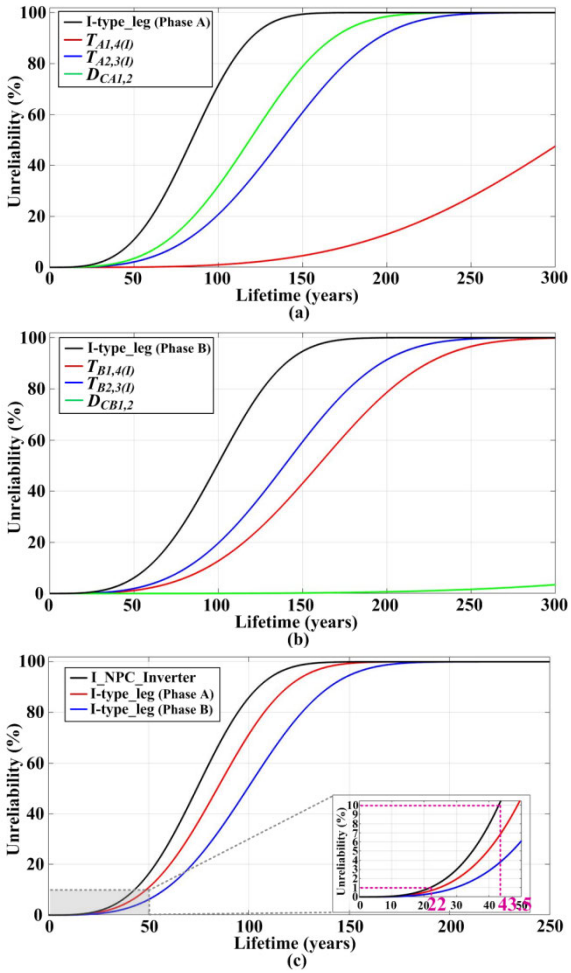

FIGURE 15. Unreliability functions of the I-type NPC inverter with OPC-PWM under the mission profile in Iza in Spain (a) power devices in the T-type leg (b) T-type NPC inverter.

that the lifetime of the clamped leg is not much changed but the lifetime of the non-clamped leg is increased.

The unreliability function of the T-type NPC inverter with OPC-PWM is shown in Fig. 16. Even though, the lifetime of the clamped-leg of the phase-A is increased compared with that of the T-type NPC inverter with the UP-PWM (see Fig. 14 (a)) as shown in Fig. 16 (a), the lifetime of the T-type inverter is decreased when the OPC-PWM is applied as shown in Fig. 16 (c). The B_1 and B_{10} lifetimes are reduced from 17 to 11 and from 34 to 23, respectively. It is because of that the lifetime of the non-clamped leg of the phase-B is significantly reduced as shown in Fig. 16 (b), where $D_{B2,3(T)}$ play a crucial role in the reliability of the T-type NPC inverter.

The unreliability functions of the I-type and T-type NPC inverters with the UP-PWM and OPC-PWM under the mission profile from Aalborg are shown in Fig. 17. The similar results with previous case can be seen with increased lifetimes in all cases. It can be seen that the lifetime of the I-type NPC inverter is higher than that of the T-type NPC inverter when the UP-PWM is applied. Further, the lifetime of the T-type NPC inverter is reduced when the OPC-PWM is applied. On the other hand, the I-type NPC inverter has increased lifetime when the OPC-PWM is applied.

It is worthwhile to mention that the power devices which have the negligible thermal stress such as $D_{A1,B1(I)}$, $D_{A2,B2(I)}$, $D_{A3,B3(I)}$, $D_{A4,B4(I)}$, $D_{A1,B1(T)}$ and $D_{A4,B4(T)}$ are not taken into account for the system-level reliability analysis.

The B_1 and B_{10} lifetimes of the I-type and T-type NPC inverters under different PWM methods and mission profiles are summarized in TABLE 6. As it can be seen from the results, the modulation methods have the significant effect not only on the efficiency but also on the lifetime of both NPC inverters. Furthermore, the mission profiles also have the enormous influence on the lifetime of the PV inverters. Based on the analysis results, the T-type NPC inverter is generally superior to the I-type NPC inverter in terms of

TABLE 6. B_1 and B_{10} lifetimes of I-type and T-type NPC inverters.

Location	NPC inverter	Modulation	Lifetime (years)	
			B_1	B_{10}
Iza	I-Type	UP-PWM	20.5	40.5
	I-Type	OPC-PWM	22.0	43.5
	T-Type	UP-PWM	17	34
	T-Type	OPC-PWM	11	23
Aalborg	I-Type	UP-PWM	88	160
	I-Type	OPC-PWM	95	172
	T-Type	UP-PWM	82.5	149
	T-Type	OPC-PWM	52	99

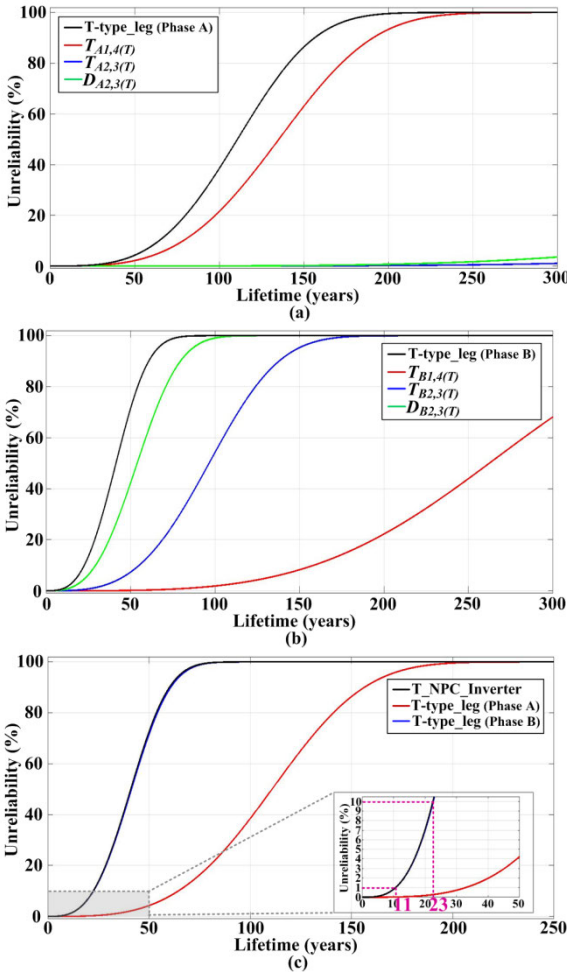

FIGURE 16. Unreliability functions of the T-type NPC inverter with OPC-PWM under the mission profile in Iza in Spain (a) power devices in the T-type leg (b) T-type NPC inverter.

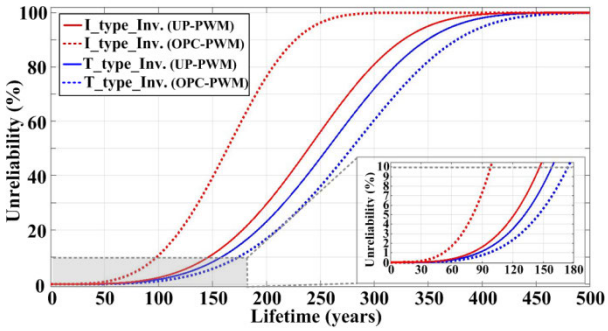

FIGURE 17. Unreliability functions of the I-type and T-type NPC inverters with UP-PWM and OPC-PWM under the mission profile of Aalborg in Denmark.

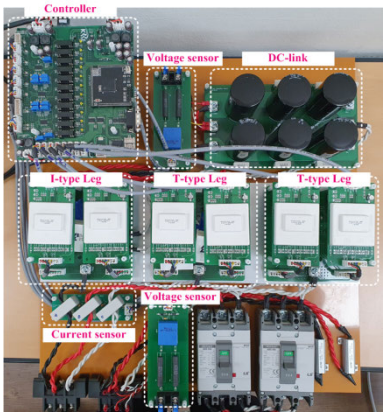

FIGURE 18. Prototype of the I-type and T-type NPC inverters.

the efficiency when the OPC-PWM is applied. However, the I-type NPC inverter has the longer lifetime than the T-type NPC inverter. If it is assumed that the required B_1 lifetime is 20 years and the reliability and efficiency are emphasized, the T-type NPC inverter is not recommended for the mission profile in Iza due to the relatively low B_1 lifetime under both UP-PWM and OPC-PWM even if it has the highest efficiency especially when the OPC-PWM is applied. The I-type NPC inverter would be a better choice. However, in Aalborg, the T-type inverter with the OPC-PWM is recommended because the lifetime is satisfied and it also has the best efficiency.

It should be noted that the when the OPC-PWM is applied to the NPC inverters, the total harmonic distortion (THD) of the output current is increased compared with THD when the UP-PWM is applied. There is a tradeoff between the efficiency and THD, and therefore, either UP-PWM or OPC-PWM can be properly chosen depending on which aspect is focused between the efficiency and THD. In addition, it is worthwhile to mention that the verification of the estimated lifetime is difficult and time consuming tasks and thus it is still an open challenge. However, this result can be useful for a qualitative comparison of the reliability as studied in this paper.

V. EXPERIMENTAL RESULTS

Experiments have been performed to compare the efficiency of the I-type and T-type NPC inverters with UP-PMW and OPC-PWM. Fig. 18 shows the prototype of the I-type and T-type NPC inverters where one T-type leg is replaced to the I-type leg when the I-type NPC inverter is assembled. The experiments are performed under the condition summarized in TABLE 1.

It is worthwhile mentioning that the outputs of I-type NPC inverter are representatively shown since the output of both NPC inverters are the same each other.

Fig. 19 (a) shows the reference voltages and corresponding output pole voltages (V_A and V_B) of the I-type NPC inverter when the UP-PWM is applied. There is a phase difference of 180 ° between the reference voltages and pole voltages of two legs. The reference voltages of the I-type NPC inverter with OPC-PWM and the output pole voltages are shown in Fig. 19 (b). The output pole voltage of the phase-A (V_A) is clamped to $V_{DC}/2$, 0 or $-V_{DC}/2$ for a certain period of time, separately and its state is changed only 4 times during a fundamental period of the reference voltage. Therefore,

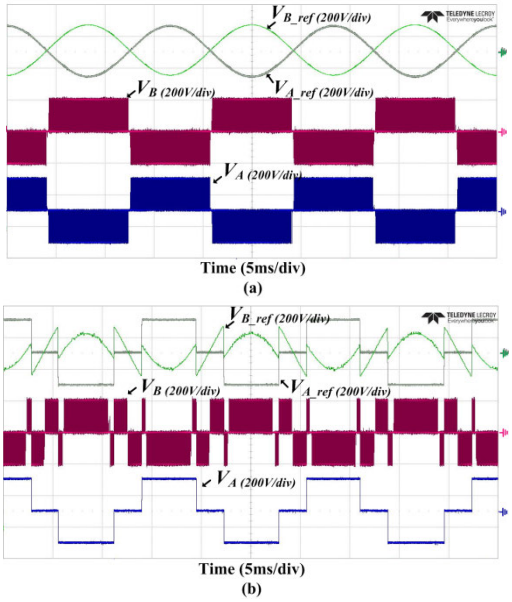

FIGURE 19. Reference voltages (V_{A_ref} and V_{B_ref}) and output pole voltages (V_A and V_B) of the I-type NPC inverters with (a) UP-PWM (b) OPC-PWM.

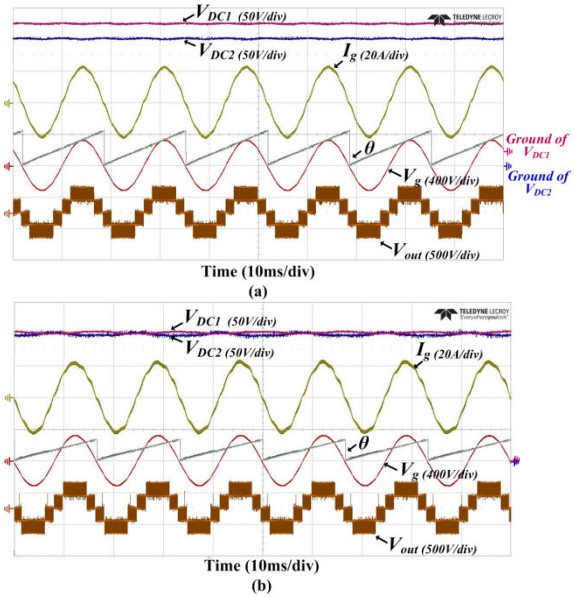

FIGURE 20. Output voltage (V_{out}), output current (I_g), grid voltage (V_g) and two capacitor voltages (V_{DC1} and V_{DC2}) of the I-type NPC inverter under the grid-connected operation with (a) UP-PWM (b) OPC-PWM.

there are almost no switching losses in the devices of the phase-A. The phase-B is operated with the modified reference voltage. There is no significant difference in the number of switching in output pole voltage of phase-B (V_B) compared with conventional one but its modulation index is reduced. The corresponding outputs of the I-type NPC inverter with UP-PWM and OPC-PWM under the grid-connected operation are shown in Fig. 20 (a) and (b), respectively. The output voltages (v_{out}) are five-level and two capacitor

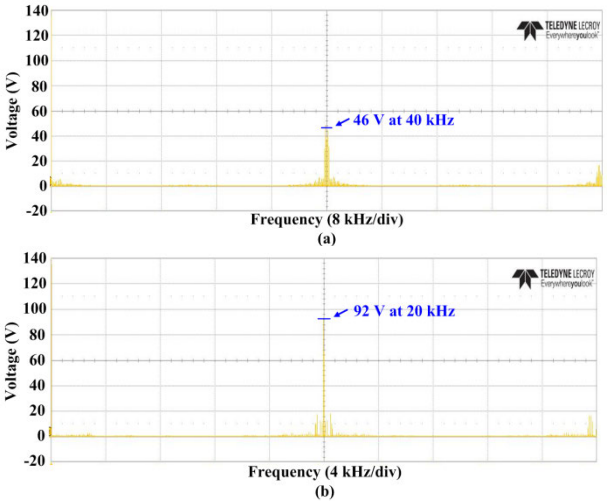

FIGURE 21. FFT of output voltage (V_{out}) of the I-type NPC inverter under the grid-connected operation with (a) UP-PWM (b) OPC-PWM.

voltages are maintained at 200 V under both modulation methods. Furthermore, the grid voltage and output current are in phase that means the power factor is 1. As it can be seen in Fig. 20, however, the output current (i_g) is more distorted when OPC-PWM is applied than that when UP-PWM is applied. The reason is that because of the switching frequency of 20 kHz, the switching frequency of the output voltage is 40 kHz since the output voltage is the difference between two pole voltages. Therefore, the output voltage has a dominant harmonic component at 40 kHz as shown in Fig. 21 (a) which is about 46 V. However, if OPC-PWM is applied, the switching frequency of the output voltage is about 20 kHz since the phase-A is clamped. It can be seen that output voltage has a dominant harmonic component of 92 V at 20 kHz as shown in Fig. 21 (b). Due to the lower order harmonic component with increased value in the output voltage, THD of the output current is increased when OPC-PWM is applied. The THD of the output current of the NPC inverter at 3.4 kW with the UP-PWM and OPC-PWM are 1.01 % and 2.16 %, respectively.

The efficiencies of the I-type and T-type NPC inverter with UP-PWM and OPC-PWM at different output powers are shown in Fig. 22. When the UP-PWM is applied, the I-type NPC inverter has higher efficiency than the T-type NPC inverter in all considered power range. The maximum efficiency of the I-type NPC inverter is about 97.09 % at 2 kW which is about 0.15 % higher than that of the T-type NPC inverter. The efficiencies of the I-type and T-type NPC inverters are raised when OPC-PWM is applied. The T-type NPC and I-type NPC inverters have the highest efficiencies of 97.352 % and 97.253 % at 2 kW, respectively.

The experimental results clearly show that the OPC-PWM leads to improved efficiency of both NPC inverters. Furthermore, it is more effective for the T-type NPC inverter than for the I-type NPC inverter. However, it is kept in mind that there

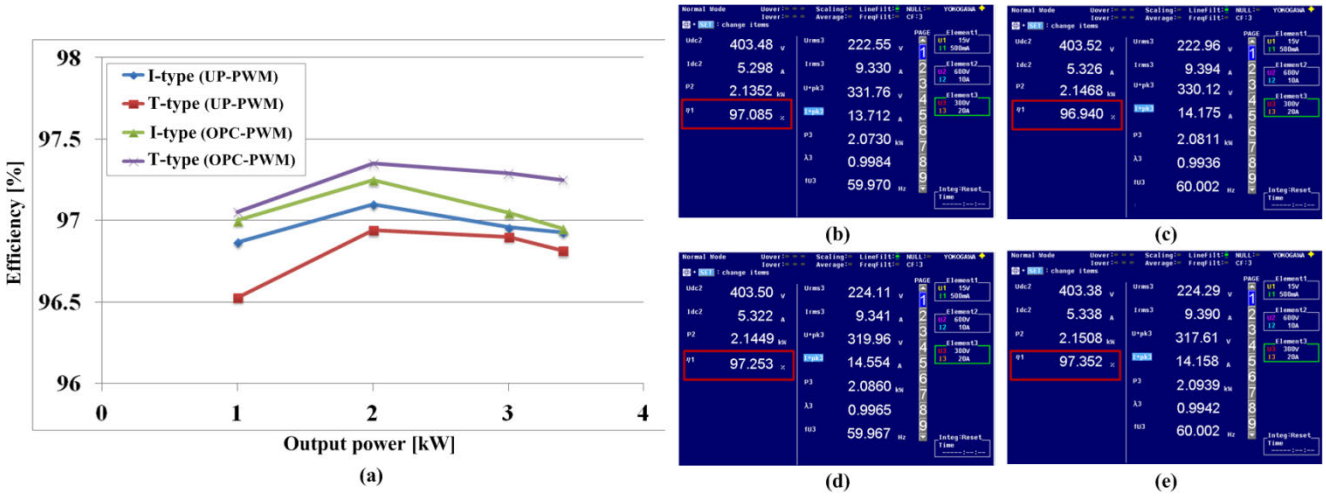

FIGURE 22. Efficiencies of the I-type and T-type inverters with UP-PWM and OPC-PWM, respectively (a) efficiencies at different output power levels (b) the highest efficiency of the I-type NPC inverter with UP-PWM (c) the highest efficiency of the T-type NPC inverter with UP-PWM (d) the highest efficiency of the I-type NPC inverter with OPC-PWM (e) the highest efficiency of the T-type NPC inverter with OPC-PWM.

is a tradeoff between the efficiency and THD for choosing the PWM method as mentioned in the previous section IV.

VI. CONCLUSION

In this paper, the efficiency and lifetime of single-phase five-level I-type and T-type NPC inverters are comparatively evaluated with two PWM methods under the mission profiles from Iza and Aalborg. The analysis results show that the PWM methods have the significant effects on both efficiency and lifetime of the NPC inverters. For the I-type and T-type NPC inverters, the OPC-PWM gives the positive effect on the efficiency compared with the UP-PWM and it is more effective on the T-type NPC inverter. However, the OPC-PWM method leads to the negative impact on the output THD of both inverters. In terms of the reliability, the PWM method has the different impacts on the T-type and I-type NPC inverter, respectively. Compared with the UP-PWM, The OPC-PWM reduces the lifetime of the T-type NPC inverter but the lifetime of the I-type NPC inverter is slightly increased. It shows that depending on the mission profiles, the lifetime reduction by the PWM method is critical or not. Therefore, the reliability performance has to be taken into account for choosing the suitable topology and modulation method depending on installation locations. It is expected that the results give an insight to determine the proper topology and PWM method depending on its installation location considering the reliability as well as efficiency and THD.

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