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Extraction of Nitride Trap Profile in 3-D NAND Flash Memory Using Intercell Program Pattern

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ABSTRACT The extraction of nitride trap density (N_t) filled with electrons emitted by thermal emission (TE) in the charge-trapping layer of 3-D NAND flash memory is demonstrated. The intercell program (IP) pattern was adopted to intentionally inject electrons into the intercell region to minimize the influence of lateral migration (LM) on the trap profiles. This was confirmed by the retention characteristics observed at 120 °C, where the charge loss is mainly caused by the TE of the trapped electrons in the nitride layer. The extracted peak value of N_t at E_C-E_T value of 1.20 eV using the IP pattern was as low as 1.01×10^{19} cm^{-3}eV^{-1}, in the scan range of 0.96 eV to 1.27 eV. This value was 17% lower than that from the conventional adjacent cell program (P-P-P) pattern. Therefore, the IP pattern can be used in extracting trap profiles in the SiN layer in scaled 3-D NAND memories.

INDEX TERMS 3D NAND flash memory, data retention, lateral migration, trap profiling.

I. INTRODUCTION

The three-dimensional (3-D) charge-trap (CT) NAND flash memory has been dominated in non-volatile memory (NVM) applications due to its higher bit density and lower bit cost [1]–[3]. The large cell size and gate-all-around (GAA) channel structure of 3-D NAND have improved its reliability when compared with the conventional planar NAND. These properties have led to the successful introduction of 3- and 4-bits/cell (quadruple-level cell, QLC) in the industry [4], [5]. Also, 5- (penta-level-cell, PLC) and 6-bits/cell (hexa-level-cell, HLC) have been newly demonstrated [6], [7]. Data retention is one of the key challenges in realizing those future memory devices [8]–[10].

In a CT based 3-D NAND, the continuous silicon nitride (SiN) layer along the pillar causes a lateral migration (LM) of trapped charges due to the Poole–Frenkel (PF) conduction [11]–[15]. LM depends strongly on the neighboring V_T patterns and becomes more severe with the scaling of 3-D NAND [16]–[20]. Also, the energy and location of traps in the nitride layer affect the overall memory parameters such as the program/erase (P/E) speed, retention, and bit error rate. Trap centers in SiN layer could mainly originate from H incorporated defects, mostly likely H atom incorporated N vacancy and Si substitute N defects [21], [22].

An adjacent cell program (P-P-P) pattern which is naturally appeared during the storage process, was adopted to extract nitride trap density (N_t) in CT layer [23]. It can reduce LM and separate the thermal emission (TE) component from the total charge loss. Compared to the adjacent cell erase (E-P-E) pattern, the extracted N_t profile from the P-P-P pattern showed a lower trap density. However, the P-P-P pattern is still insufficient to precisely determine the N_t profile because of the movement of trapped charges into the space region, resulting in an overestimation of trap distributions.

Recently, the space region surrounded by word-line (WL) metals has received attention because the narrow space region is affected by the fringing electric field from the adjacent

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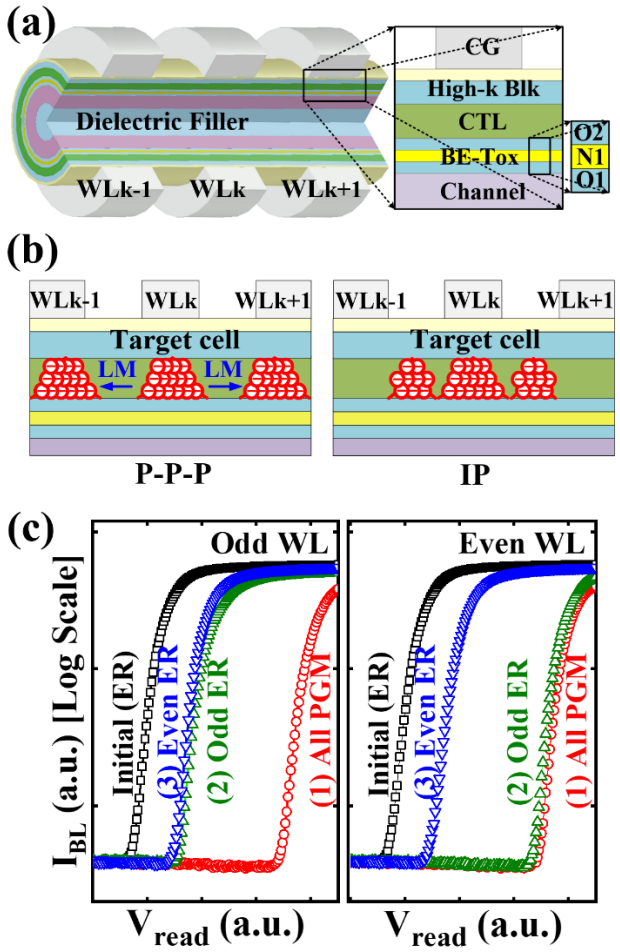

FIGURE 1. (a) Schematics of 3-D NAND flash memory. (b) Comparison of the electron distribution between P-P-P pattern and IP pattern with a programmed target cell. (c) The measured $I_{BL} - V_{read}$ curves of odd-WL (left) and even-WL (right) with IP pattern which is performed as follows; (1) all program (PGM) – (2) odd erase (ER) – (3) even ER.

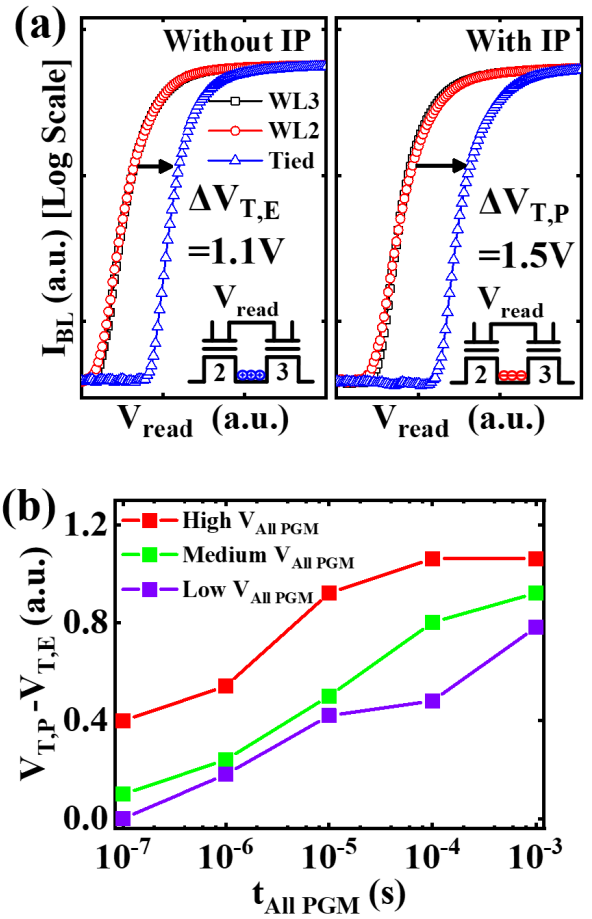

FIGURE 2. (a) Representative $I_{BL} - V_{read}$ curves of WL2, WL3 and tied two WLs with and without IP pattern. (b) $V_{T,P} - V_{T,E}$ versus all WLs program time ($t_{All\ PGM}$) at different WLs program voltage ($V_{All\ PGM}$).

WLs [24]. The intercell program (IP) or space program was adopted to achieve a reliable triple-level cell (TLC) operation and to analyze the impact of P/E cycling on the retention mechanism [25]–[27]. As 3-D NAND continues to scale, the influence of charges in intercell regions on the memory performance becomes significant.

Here, the trap profiles of the SiN layer and the related charge loss characteristics are presented using the IP pattern. Firstly, the quantitative influence of IP on LM is evaluated based on the retention characteristics with various IP charges. The comparison of V_T variation between IP and P-P-P at different temperatures confirms the validity of the IP pattern, which mitigates the charge loss along the channel direction. Finally, the trap density using the IP pattern based on a novel cylindrical retention model is extracted and compared with the P-P-P pattern.

II. RESULTS AND DISCUSSION

Fig. 1(a) shows a schematic diagram of 3-D NAND flash memory consisting of a dielectric filler, poly-Si channel, band engineering (BE)-tunneling oxide (O1/N1/O2), charge trap layer (CTL), blocking oxide with a high-κ layer. **Fig. 1(b)** shows the trapped electron distribution in a continuous SiN layer after applying IP and P-P-P patterns. The experimental procedures for comparing the retention efficiency of target programmed cells by each pattern are as follows: After setting an initial erase state of a string to remove the remaining electrons, (1) for the P-P-P pattern, firstly the adjacent WLs are programmed and then the target cell is programmed until V_T of the PV7 is reached. (2) For the IP pattern, firstly all gates are programmed and then odd-WLs are erased. Next even-WLs are erased. Finally, the target cell is programmed by applying the same PV7 condition. (3) For the E-P-E pattern, only the target cell is programmed. **Fig. 1(c)** shows the measured BL current (I_{BL})-read voltage (V_{read}) curves for odd and even WLs. All WLs were simultaneously programmed with high program voltages ($V_{All\ PGM}$) at a fixed program time ($t_{All\ PGM}$), and the fringing electric field caused electrons to accumulate in the intercell region. The variation in the threshold voltage (V_T) is clearly observed due to the trapped charges in the intercell region. Then during the erase operation, the protect bias ($V_{protect}$) is sequentially applied to odd WLs and even WLs to prevent the intercell electrons from being de-trapped through a tunneling layer.

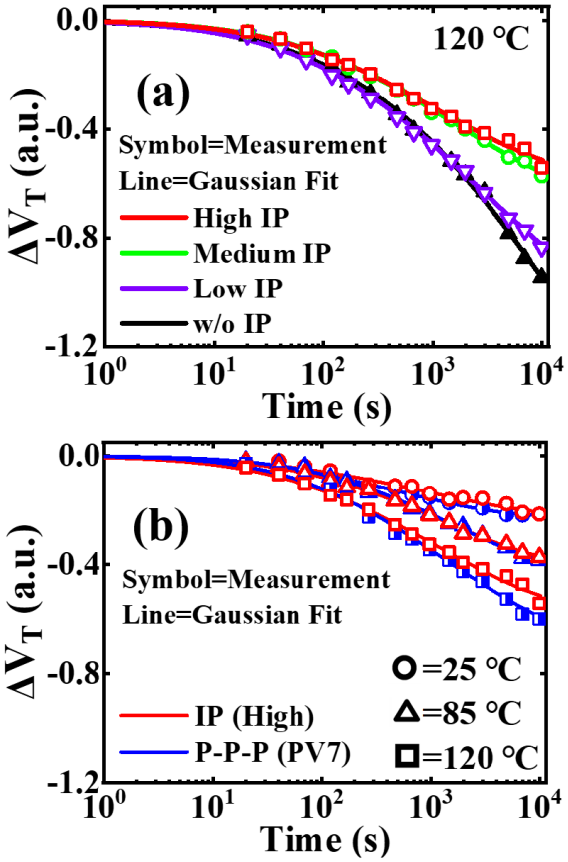

FIGURE 3. Retention characteristics of a programmed target cell with (a) different IP conditions ($t_{All\ PGM} = 10^{-4}$ s) at 120 °C. (b) Comparison of IP and P-P-P patterns at 25 °C (circle), 85 °C (triangle) and 120 °C (square).

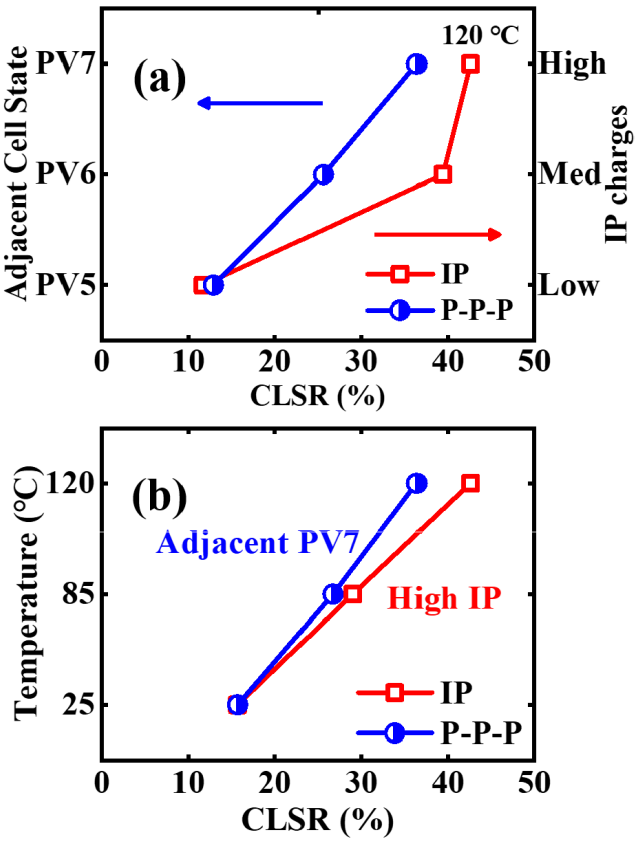

FIGURE 4. (a) Comparison of charge loss suppression ratio (CLSR) extracted from the retention characteristics at 10^4 s with IP and P-P-P patterns. (b) CLSR vs. temperature of IP and P-P-P patterns.

Fig. 2(a) shows a comparison of the V_T shift with IP and without IP pattern using the measured I_{BL}-V_{read} curves. WL2 and WL3 are electrically tied to evaluate the effect of trapped electrons on the I_{BL}-V_{read} characteristics in the intercell region. When all WLs and intercell areas of CTL were erased (without IP), the $\Delta V_{T,E}$ increases compared to individual WL because of the intercell region. The larger $\Delta V_{T,P}$ than $\Delta V_{T,E}$ suggests that the electrons are filled in the intercell region caused by the fringing field during the IP pattern. **Fig. 2(b)** shows ΔV_T $(= V_{T,P} - V_{T,E})$ shifts with varying $V_{All\ PGM}$ and $t_{All\ PGM}$ values. At medium and low $V_{All.PGM}$ values, $\mathbf{\Delta} V_T$ increases monotonously. A high $V_{All.PGM}$ values, $\mathbf{\Delta} V_T$ saturates after a $t_{All\ PGM}$ value of 10^{-4}s. Such a $\mathbf{\Delta} V_T$ saturation indicates that the concentration of trapped electrons is close to its maximum value in the intercell region.

Fig. 3(a) shows the retention characteristics of the target programmed cell in different IP conditions with a fixed $t_{All\ PGM}$ of 10^{-4}s at 120 °C. The retention characteristics largely improve for high and medium $V_{All.PGM}$ values. This confirms the validity of the IP pattern that the trapped electrons in the intercell region can effectively suppress the LM. **Fig. 3(b)** shows the retention characteristics of the IP and P-P-P patterns at different temperatures. At 120 °C, IP with a high $V_{All.PGM}$ shows less $\mathbf{\Delta} V_T$ variation than that of the P-P-P pattern, indicating that IP can more effectively suppress LM via PF mechanism at high retention temperatures in the range of 1 s to 10^4 s. A charge loss suppression ratio (CLSR) is introduced as the value of V_T loss is normalized by $\mathbf{\Delta} V_T$ of E-P-E at 10^4 s:

$$CLSR\,(\%) = \frac{|\Delta V_T(pattern) - \Delta V_T(E-P-E)|}{|\Delta V_T(E-P-E)|} \times 100 \tag{1}$$

Fig. 4(a) shows a comparison of the CLSR under various IP conditions and P-P-P patterns at 120 °C. CLSR is calculated to be as high as 43% and 39% for high and medium IP conditions, respectively. The CLSR of P-P-P pattern at PV7 level is calculated to be 36%, which is even lower than that for the medium IP. **Fig. 4(b)** shows a comparison of the CLSR between high IP and P-P-P at different temperatures. Adjacent cells are programmed at PV7 level. This clearly shows that the IP pattern is more effective in suppressing the LM at elevated temperatures.

To further understand the effect of IP patterns on the LM, the energy band diagram in the CT layer is analyzed using a technology-computer aided design (TCAD) simulation. Hurkx Band-to-band tunneling model for GIDL erase at SSL and GSL junction, Shockley-read-hall (SRH) recombination model was adopted. Acceptor-like trap with the density of 4.0×10^{19} cm^{-3} was used in the entire SiN layer [12]. Transient simulation with non-local tunneling model was

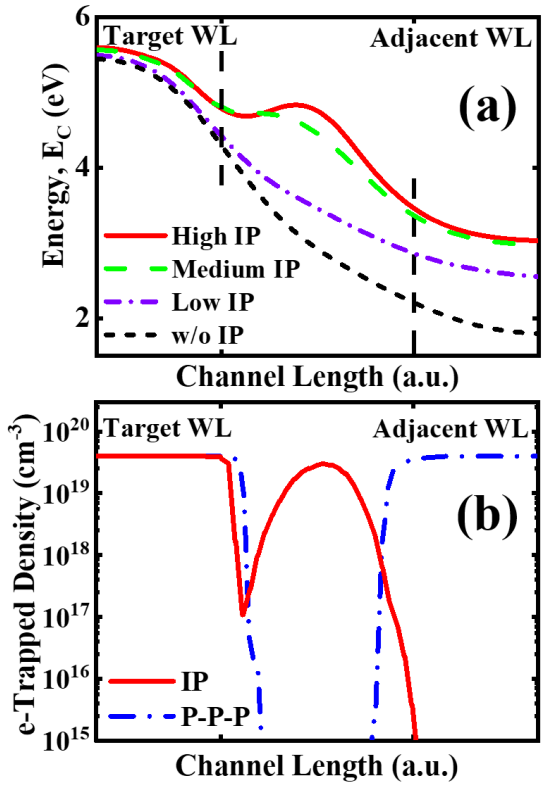

FIGURE 5. (a) A schematic conduction energy band diagram (E_C) of nitride layer along the channel direction under different IP charges. (b) Concentrations of trapped electron along the channel direction using TCAD simulation.

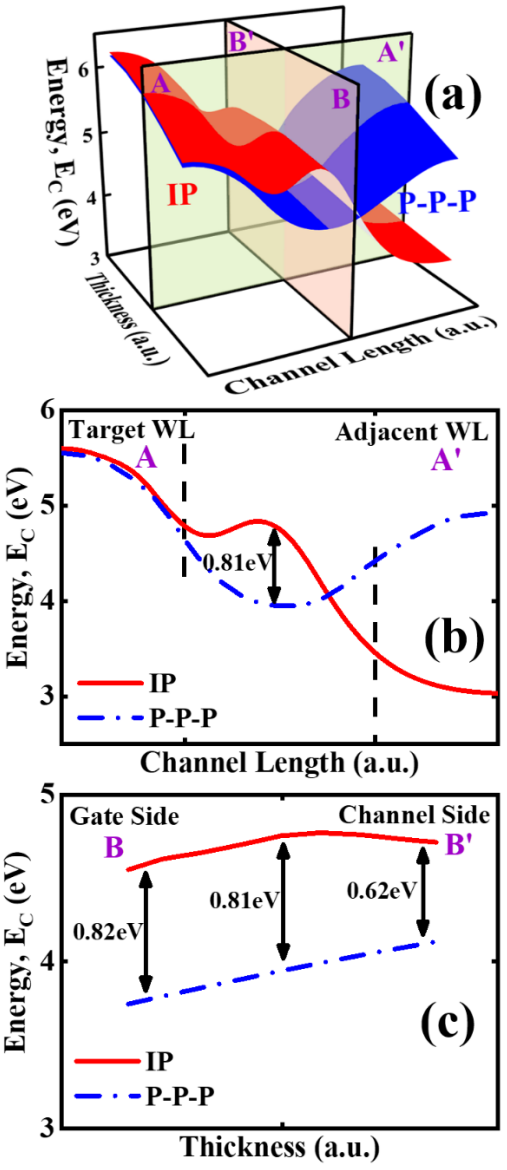

FIGURE 6. (a) 3-D E_C profile in CT layer with P-P-P and IP patterns. Comparison of E_C of nitride layer with P-P-P and IP patterns (b) along the channel direction (A-A') and (c) the vertical direction (B-B').

used to obtain the distribution of trapped electrons in the CTL layer.

Fig. 5(a) shows the conduction energy band (E_C) along the channel direction under different IP conditions. For high and medium IP conditions, the peak of the potential barrier is observed closer to the target WL in the intercell region. **Fig. 5(b)** shows the concentration of trapped electrons along the channel direction in the middle of the CT layer using TCAD simulation. The concentration of trapped electrons of IP pattern is as high as 3×10^{19} cm^{-3} in the middle and 4×10^{15} cm^{-3} in the gate edge, respectively. The V_T of each cell for the IP and P-P-P patterns and tied ΔV_T ($= V_{T,P} - V_{T,E}$) shifts for IP pattern are confirmed to be the same both in the simulation and the measurement.

Fig. 6(a) shows the variation in 3-D E_C with IP and P-P-P patterns. **Fig. 6(b)** shows the E_C variation along the channel direction (A-A'). The potential barrier is minimum in the middle of the intercell region and increases towards adjacent cells for the P-P-P pattern. **Fig. 6(c)** shows a comparison of the E_C difference between the P-P-P and IP along the vertical direction (B-B'). While the E_C of the P-P-P pattern decreases monotonously towards the gate side, the maximum E_C value of the IP pattern is located near the center of the CT layer. An energy difference of 0.82 eV at the blocking oxide-CT layer interface is obtained. The higher E_C difference suggests an exponential increase of trapped electrons in the intercell region, resulting in a significant LM reduction.

The V_T-loss at high temperature can be mainly caused by the trap-assisted tunneling (TAT) and thermal emission (TE) process, which can be expressed by using the following expressions:

$$\frac{\partial \Delta V_T(t)}{\partial log(t)} = \frac{\partial \Delta V_{T,TAT}(t)}{\partial log(t)} + \frac{\partial \Delta V_{T,TE}(t)}{\partial log(t)} \quad (2)$$

Firstly, the TAT from CTL to the channel consists of two components; tunneling from CTL through O2 to N1 and tunneling from N1 through O1 to the channel. These tunneling processes can be characterized by a time constant τ_{TB} [28]. If the tunneling probability from N1 to the channel is 1, then τ_{TB} from CTL to the channel can be

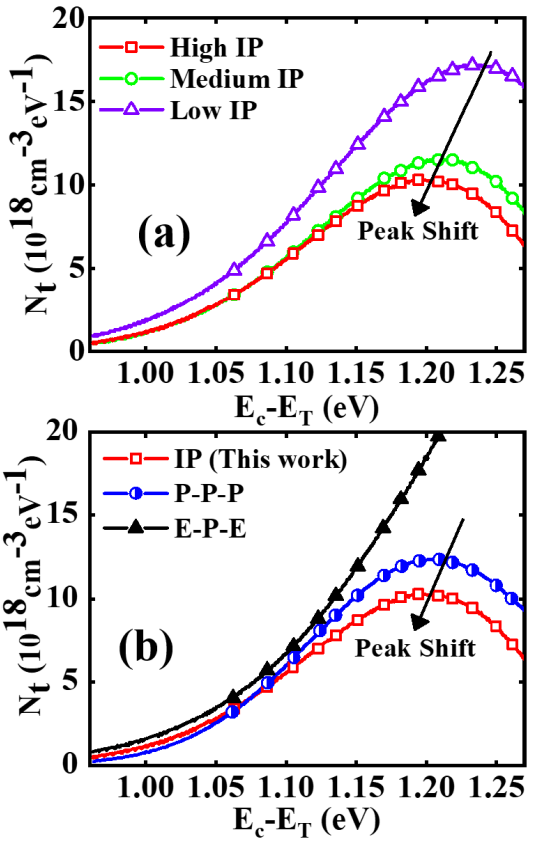

FIGURE 7. The extracted N_t vs. $E_C - E_T$ at 120 °C (a) using IP pattern with different IP values and (b) comparison with P-P-P and E-P-E patterns.

expressed as [29],

$$\tau_{TB}^{-1} = \tau_{TB0}^{-1} \cdot exp\left(-\alpha_{ox}\left(R_{O2} - R_{N1}\right)\right) \cdot \frac{1}{R_{CTL} - R_{O2}} \int_0^{R_{CTL}-R_{O2}} exp(-\alpha_n x)\, dx \quad (3)$$

where R_{N1}, R_{O2}, R_{CTL}, τ_{TB}, τ_{TB0}, α_n, α_{ox}, x are the radii of BE-tunneling oxide (N1, O2) and CTL, the time constant of tunneling, the intrinsic time constant (1.0×10^{-13} s) of tunneling, the attenuation coefficient of nitride (7.2×10^{7}cm^{-1}), and the attenuation coefficient of oxide (1.0×10^{8} cm^{-1}), the distance from the O2-CTL interface into CTL, respectively. The V_T-loss by TAT mechanism can be modified as [30]:

$$\Delta V_{T,TAT}\,(t) \propto -C_{cyl}^{-1} \cdot \left(exp\left(-\frac{t}{TB}\right) - 1\right) \quad (4)$$

where the parameter C_{cyl} is given by

$$C_{cyl}^{-1} = \frac{1}{2\varepsilon_{nit}} \cdot \left[-R_{O2}^2 ln\frac{R_{CTL}}{R_{O2}} + \frac{1}{2}\left(R_{CTL}^2 - R_{O2}^2\right)\left(1 + \frac{2\varepsilon_{nit}}{\varepsilon_{ox}} ln\frac{R_{box}}{R_{CTL}} + \frac{2\varepsilon_{nit}}{\varepsilon_{high-\kappa}} ln\frac{R_{high-\kappa}}{R_{box}}\right)\right] \quad (5)$$

where R_{box}, $R_{high-\kappa}$, ε_{nit}, ε_{ox}, and $\varepsilon_{high-\kappa}$ are the radii of the blocking oxide and high-κ layer, the permittivity of nitride, oxide, and high-κ layer, respectively. Differentiating Eq. (4) with respect to log(t), the V_T-loss rate can be expressed as:

$$\frac{\partial \Delta V_{T,TAT}\,(t)}{\partial log(t)} \propto \frac{t}{TB} exp\left(-\frac{t}{TB}\right) \quad (6)$$

The calculated $\partial \mathbf{\Delta} V_{T,TAT}(t)/\partial log(t)$ at $t > 1$ s is insignificant because the characteristic time constant τ_{TB} from Eq. (3) is as low as 8.3×10^{-3} s. Thus the TAT component causing V_T-loss is negligible and the remaining TE component can be the main mechanism in the charge loss at high temperature. The TE process in V_T-loss is the emission of trapped electrons to the E_C of CTL. Based on the equations describing the TE in cylindrical coordinate at high temperature [31], the V_T-loss equation versus log-scale time is modified as:

$$\frac{\partial \Delta V_{T,TE}(t)}{\partial log(t)} = -2.3qk_BT \cdot C_{cyl}^{-1} \cdot N_{t,E_C-E_T} \quad (7)$$

Trap energy level (E_T) from E_C in CTL is calculated using the following equation.

$$E_C - E_T = k_BTln\left(2\sigma_n\sqrt{\frac{3k_B}{m_n^*}}\left[\frac{2\pi m_n^* k_B}{h^2}\right]^{\frac{3}{2}} T^2 t\right) \quad (8)$$

where the effective mass (m_n^*) and the capture-cross section of electron in the SiN layer (σ_n) are $0.42m_0$ and 1×10^{-14} cm^2, respectively [11], [32].

The trap density in SiN layer is successfully extracted using Eq. (7) and Eq. (8). **Fig. 7(a)** shows the extracted N_t profile filled with electrons emitted by TE under different IP conditions in the scan range of 0.96 eV to 1.27 eV, applying Gaussian fitting curves of retention characteristics to the modified V_T-loss equation at 120 °C. The peak and amplitude of the N_t profile clearly decrease as IP level increases, suggesting that the suppression of LM largely affects the N_t profiles. **Fig. 7(b)** shows the extracted N_t profiles using IP, P-P-P, and E-P-E patterns. The E-P-E pattern seems to be improper in N_t extraction due to a severe LM effect [23]. The calculated peak N_t is as low as 1.01×10^{19} and 1.21×10^{19} cm^{-3}eV^{-1} for IP and P-P-P patterns, respectively. The peak N_t extracted by the P-P-P pattern concurs recently reported results [23], and the newly extracted N_t peak by the IP pattern reduces by 17%. Compared with P-P-P pattern, the N_t profile with a shallower E_C-E_T value and a smaller amplitude using IP pattern, indicating that LM is more suppressed in IP pattern than P-P-P pattern. Even though this work is done by measuring TEG of 3-D NAND flash memory, the result for LM suppression of IP pattern can be solutions to reduce the system operations of 3-D NAND chip at high temperature [8], [10].

While the increase of vertical stacks for further 3-D NAND flash technology, the difference of aspect ratio becomes a major issue in etching the channel hole [33]. Thus the gate length and intercell length should be shrink, which affects trapped charge distribution. The changes of gate length or intercell length can affect the total amount of intercell trapped charges associated with LM suppression [20]. Therefore, further study is needed on future technology nodes or device scaling for IP pattern and related N_t profiling.

III. CONCLUSION

The extraction of nitride trap profiles in 3-D NAND flash memories using intercell program patterns is successfully demonstrated. Compared to the P-P-P pattern, the IP pattern is more effective in mitigating the LM at elevated temperatures, as confirmed by the retention characteristics and CLSR values at 120 °C. The high IP condition shows a higher CLSR value than that of P-P-P under PV7 conditions. Using modified TE equations, trap profiles are extracted from retention characteristics. The extracted N_t peak value using the IP pattern is 17 % lower than that of the P-P-P pattern. Therefore, the intercell program pattern is very useful in determining trap profiles in the SiN layer in scaled 3-D NAND memories.

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