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Analysis and Design of a New Non-Isolated Three-Port Converter With High Voltage Gain for Renewable Energy Applications

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ABSTRACT This paper proposes a non-isolated three-port converter which integrates the input port, battery port, and load port into one converter for renewable energy applications. The coupled inductor and switched capacitor are used to achieve high voltage gain and three power switches can be utilized to realize the power flows between the sources, the battery, and the load. The energy stored in the leakage inductance is recycled to reduce the voltage stress of the power switch. In addition, various operating stages are analyzed and design considerations are presented. Compared to the relevant converters, the proposed converter can realize power flows and achieve high voltage gain by using few components. Finally, a laboratory prototype of the proposed converter with input port voltage 24 V, battery port voltage 48 V, and output voltage 400 V with 200 W rated power is implemented to validate the feasibility and effectiveness of the theoretical analyses.

INDEX TERMS Three-port converter, high voltage gain, coupled inductor, switched capacitor, renewable energy applications.

I. INTRODUCTION

Renewable energy resources(RESs)are widely used because of environmental concerns and energy resource diversity. However, the intermittent nature and unpredictability of RESs can affect the power system reliability, stability, durability and power quality [1], [2]. Therefore, energy storage systems (ESSs) are usually to smooth the output from the RESs [3]. To improve the efficiency, and reduce the cost, size and complexity of the RESs system, three-port converter (TPC) integrates converters for transferring among sustainable energy sources, ESS, and the load to provide an appropriate voltage to meet the load demand as shown in Fig.1.

The TPC topologies can be classified into three types: fully-isolated TPCs (FITPCs) [4], [5], partly-isolated TPCs (PITPCs) [6]–[8], and non-isolated TPCs (NITPCs) [9]–[23]. PITPCs and FITPCs suffer from topology complexity and low efficiency; the NITPCs are widely adopted in the ESS resulting in compact size and high efficiency. Since RESs and ESSs are low voltage, high step-up converters are required to increase the voltage gain. ESSs are employed as backup use for RESs, and the bidirectional converter must be supplied for the battery port [24].

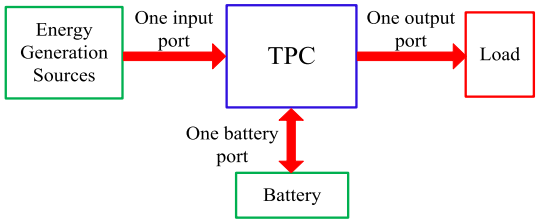

FIGURE 1. A typical renewable energy system with the TPC.

A NITPC was proposed using two high step-up converters constructed with two coupled inductors, two switched capacitors and two active clamp circuits to achieve soft-switching [9]. However, more component counts are used. A high integration TPC with a lossless passive snubber circuit was presented to reduce the voltage stress of the main switch [10]. However, too many semiconductor power devices are used. The TPC constructed with a boost converter and a bidirectional buck-boost converter was derived [11]. However, the voltage gain is very low. A high voltage gain TPC was

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presented using two coupled inductors, and the energy stored in the leakage inductors is recycled by the active clamp circuits [12]. However, two coupled inductors limit the power density. The NITPC can be operated as a step-up converter or step-up/down converter with a reconfigurable structure, but the battery port is not common grounded with the input port [13]. A family of NITPCs based on a dual-input converter and dual-output converter was derived, and a boost NITPC was presented using PWM for power management to control the power flows from source(s) to load(s); however, the voltage gain from sources to load is low [14]. Three switches and two duty cycles are used to realize the power flows from the source port(s) to the load port(s), but this NITPC cannot realize the energy transferring from battery to load independently [15]. A NITPC with the coupled inductor technique was presented to obtain high voltage gain from input to output(s); nevertheless, the power switch suffers from high voltage stress, because the energy stored in the leakage inductance is not recycled [16]. A high step-up NITPC was presented using coupled-inductor with multi-winding and voltage lift techniques [17]. In addition, the voltage spike of the power switch is suppressed by the clamp circuits. However, the battery port cannot transfer energy to the load port. A NITPC with high voltage gain was presented with a lower turns ratio, and the voltage stress of the switch is low, but one inductor and one coupled inductor are used [18]. A NITPC with single magnetic element was presented to realize high voltage gain and leakage inductance was recycled to reduce the voltage stress of the power switches. However, in order to achieve high voltage gain, more components are used [19]. A fully soft-switched NITPC was presented using coupled inductors and active clamp circuit, but the battery is always charged when the PV provides energy to the output. Thus, the battery suffers from risk of overcharge [20]. Combining boost and buck/boost, a NITPC with seven distinctive operating modes was developed [21]. However, the voltage gain is low, only 1/(1-D). For achieving high voltage gain with few numbers of devices, two extensible NITPC were developed to reduce the complexity [22], [23].

In this paper, a new NITPC with high voltage gain is proposed for renewable power applications. The proposed converter has the following evident features.

1) Only three power switches are included to achieve power flows among the input port, battery port, and load port.
2) Input port, battery port, and load port share the common ground, improving the reliability.
3) High voltage gain with one coupled inductor can be achieved without extremely duty cycle.
4) The intermediate capacitor circuit can recycle the leakage inductance to suppress the voltage spike of the main power switch.

The rest of this article is organized as follows. The proposed structure and operating stages are introduced in Section II. The detailed design considerations, efficiency estimation, and comparisons are given and discussed in Section III. Experiment results are shown in Section IV. Finally, Section V concludes this article.

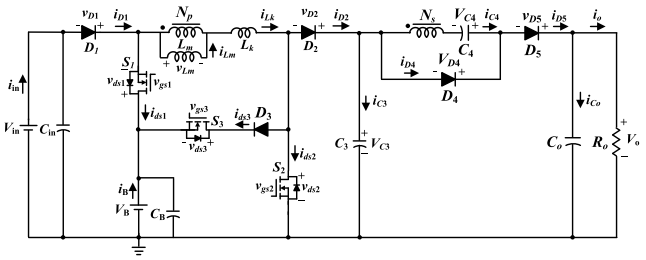

FIGURE 2. Proposed NITPC topology.

II. THE STRUCTURE OF PROPOSED NITPC AND OPERATION STAGES

A. THE STRUCTURE OF PROPOSED NITPC

The proposed NITPC is constructed with one coupled inductor, three power switches, and five diodes as shown in Fig.2. V_{in} is sustainable energy source voltage and V_{B} is the battery voltage. The capacitor C_3 is used to clamp the voltage stress of the active switches and recycle the energy stored in the leakage inductance. The extra voltage gain is obtained with the additional switched capacitor circuit consisting of a diode D_4, a capacitor C_4 and the secondary-side coupled-inductor N_{S}.

There are four different operating stages of the proposed NITPC as shown in Fig.3. In order to analyze the circuit simply, some conditions are assumed:

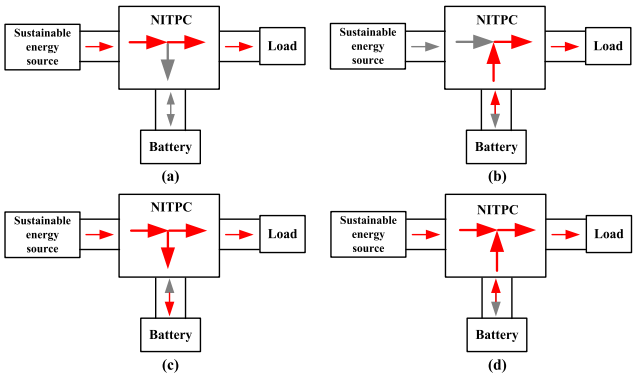

FIGURE 3. Operating stage of the proposed NITPC: (a) SISO-I stage, (b) SISO-II stage, (3) SIDO stage, (4) DISO stage.

1) The NITPC is operated at steady state under continuous conduction mode (CCM) conditions.
2) All semiconductor devices are considered ideal expect body diode, output capacitance of MOSFETs.
3) The turns ratio of coupled-inductor are defined as N_{P}: $N_{\text{S}} = 1: n$.
4) The capacitors of C_{in}, C_{B}, C_3, C_4, and C_{o} are large enough, so V_{in}, V_{B}, V_{C3}, V_{C4}, and $V_{C\text{o}}$ can be considered as constant voltages in one switching cycle.

B. OPERATIING PRINCIPLE OF SISO-I STAGE

In this stage, V_{in} provides energy to the load. Switch S_1 is the main switch of the converter, and switches S_1 and S_3

are always off in this stage. Fig.4 and Fig.5 show the key waveforms and the current-flow paths of operating modes, respectively. The operating modes are described as follows:

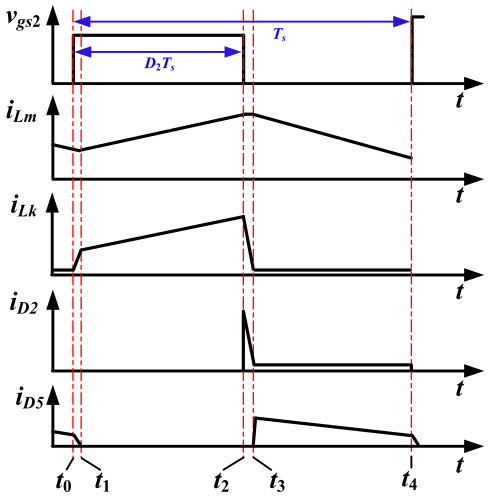

FIGURE 4. Steady-state waveforms in SISO-I at CCM.

1) Mode I (t_0-t_1) [Fig.5 (a)]: v_{gs2} becomes high at $t = t_0$, $i_{Lm} > 0$, $i_{Lk} > 0$, and $i_{Lk} < i_{Lm}$. V_{in} provides energy to L_k. V_{C3}, L_m, and V_{C4} provide energy to the load. This mode ends when i_{Lm} is equal to i_{Lk} at t_1.
2) Mode II ($t_1 - t_2$) [Fig.5 (b)]: v_{gs2} is high, $i_{Lm} > 0$, $i_{Lk} > 0$, and $i_{Lk} = i_{Lm}$. V_{in} provides energy to L_m & L_k, and i_{Lm} & i_{Lk} increase linearly. N_s, D_4, and C_4 form a switched capacitor circuit, and V_{C4} is equal to nV_{in}. This mode ends when v_{gs2} is low at t_2.
3) Mode III ($t_2 - t_3$) [Fig.5 (c)]: v_{gs2} is low. The output capacitor C_{oss2} of S_2 is charged by the i_{Lm} & i_{Lk}, and v_{ds2} increases. This mode ends when v_{ds2} is equal to V_{C3} at t_3.
4) Mode IV ($t_3 - t_4$) [Fig.5 (d)]: v_{gs2} is low. i_{Lm} decreases linearly and V_{ds2} is clamped at V_{C3}. V_{in} and L_m provide energy to C_3. V_{C3}, L_m, and V_{C4} provide energy to the load. This mode ends when v_{gs2} is high at t_4.

C. OPERATING PRINCIPLE OF SISO-II STAGE

In this stage, V_B provides energy to the load. Switch S_2 is the main switch of the converter; switch S_1 is always on and S_3 is always off in this stage. Fig.6 and Fig.7 show the key waveforms and the current-flow paths of operating modes, respectively. Since the characteristics of SISO-II are similar to SISO-I, please refer to the operating principles in the previous stage.

D. OPERATING PRINCIPLE OF SIDO STAGE

In this stage, V_{in} provides energy to V_B and the load. Switches S_2 and S_3 are the main switches of the converter, and S_1 is always off in this stage. Fig.8 and Fig.9 show the key waveforms and the current-flow paths of the operating modes, respectively. The operating modes are described as follows:

1) Mode I ($t_0 - t_1$) [Fig.9 (a)]: v_{gs2} & v_{gs1} become high at $t = t_0$, $i_{Lm} > 0$, $i_{Lk} > 0$, and $i_{Lk} < i_{Lm}$. V_{in} provides

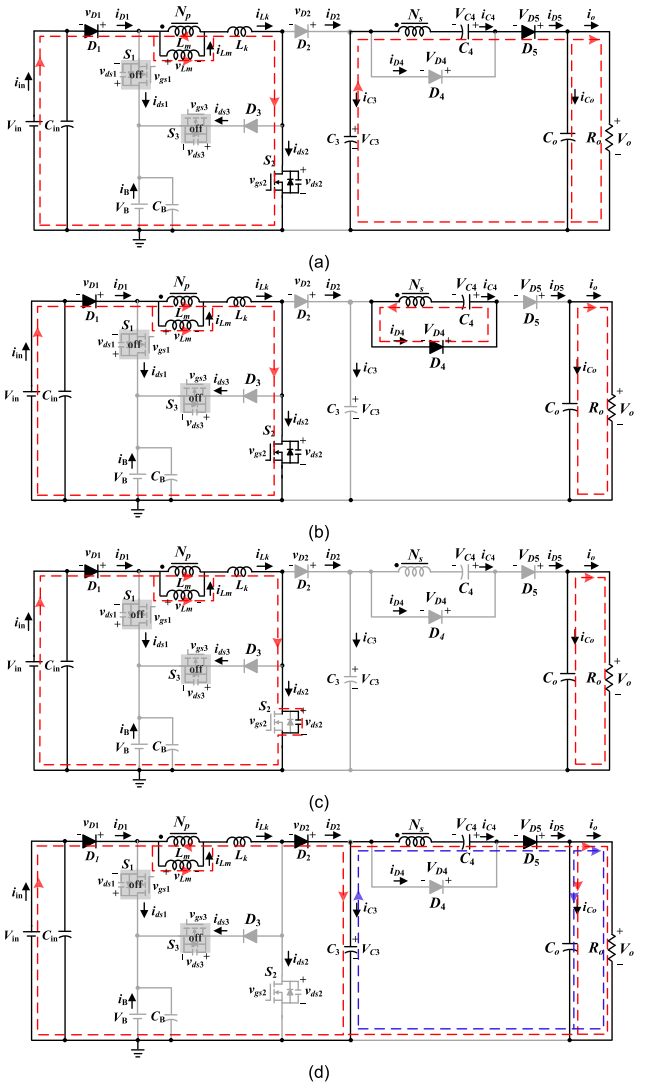

FIGURE 5. Operating processes of the proposed converter in SISO-I stage: (a) mode I, (b) mode II, (c) mode III, (d) mode IV.

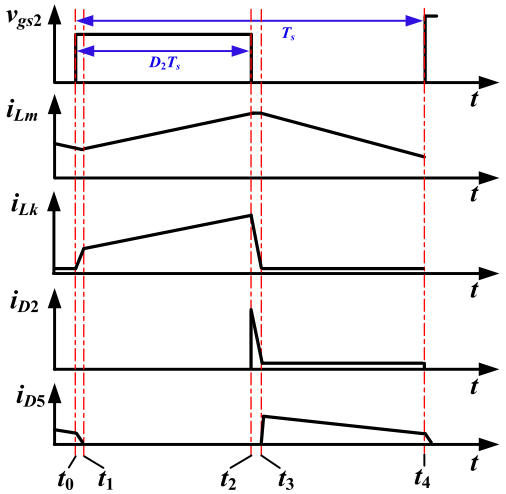

FIGURE 6. Steady-state waveforms in SISO-II at CCM.

energy to L_k. V_{C3}, L_m, and V_{C4} provide energy to the load. This mode ends when i_{Lm} is equal to i_{Lk} at t_1.

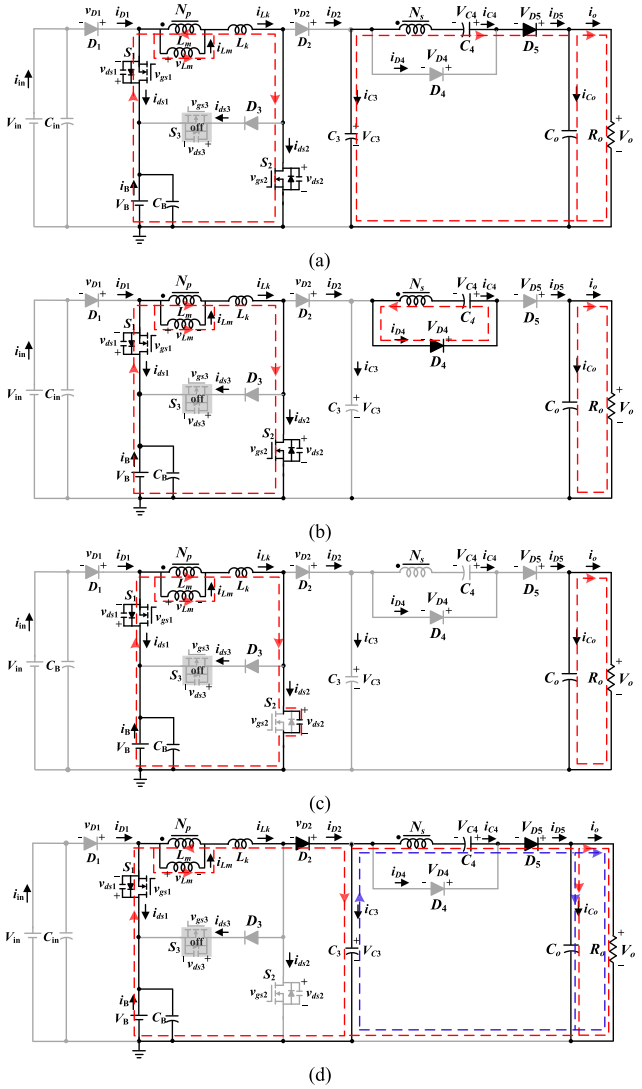

FIGURE 7. Operating processes of the proposed converter in SISO-II stage: (a) mode I, (b) mode II, (c) mode III, (d) mode IV.

2) Mode II ($t_1 - t_2$) [Fig.9 (b)]: v_{gs2} & v_{gs1} are high, $i_{Lm} > 0$, $i_{Lk} > 0$, and $i_{Lk} = i_{Lm}$. V_{in} provides energy to L_m & L_k, and i_{Lm} & i_{Lk} increase linearly. N_s, D_4, and C_4 form the switched capacitor circuit, and V_{C4} is equal to nV_{in}. This mode ends when v_{gs2} is low at t_2.
3) Mode III ($t_2 - t_3$) [Fig.9 (c)]: v_{gs2} is low. v_{gs3} is high. The output capacitor C_{oss2} of S_2 is charged by i_{Lk}, and v_{ds2} increases. This mode ends when v_{ds2} is equal to V_B at t_3.
4) Mode IV ($t_3 - t_4$) [Fig.9 (d)]: v_{gs2} is low. v_{gs3} is high. i_{Lm} decreases linearly and $i_{Lm} > 0$. V_{in} and L_m provide energy to V_B. This mode ends when v_{gs3} is low at t_4.
5) Mode V ($t_4 - t_5$) [Fig.9 (e)]: v_{gs2} & v_{gs1} are low. The output capacitor C_{oss3} of S_3 is charged by i_{Lk}. This mode ends when v_{ds3} is equal to $(V_{C3} - V_2)$ at t_5.
6) Mode VI ($t_5 - t_6$) [Fig.9 (f)]: v_{gs2} & v_{gs1} are low. i_{Lm} decreases and $i_{Lm} > 0$. V_{ds3} is clamped at $(V_{C3} - V_B)$. V_{ds2} is clamped at V_{C3}. V_{in} and L_m provide energy to C_3. V_{C3}, L_m, and V_{C4} provide energy to the load. This mode ends when v_{gs2} & v_{gs1} are high at t_6.

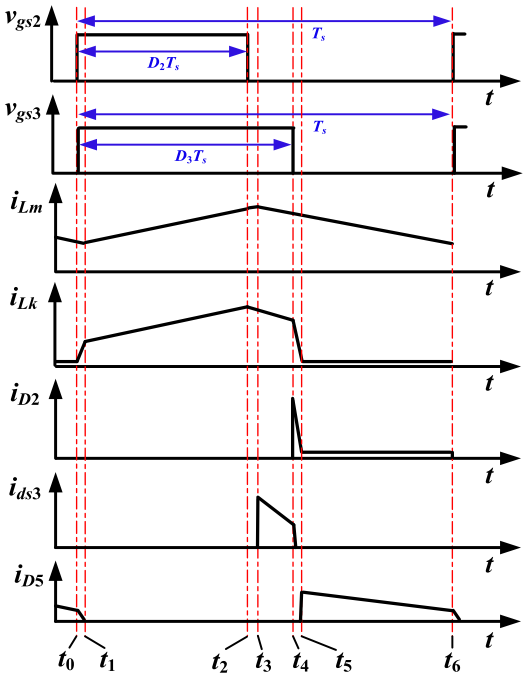

FIGURE 8. Steady-state waveforms in SIDO at CCM.

E. OPERATING PRINCIPLE OF DISO STAGE

In this stage, V_{in} and V_B provide energy to the load. Switches S_1 and S_2 are the main switches of the converter, and switch S_3 is always off in this stage. Fig.10 and Fig.11 show the key waveforms and the current-flow paths of the operating modes, respectively. The operating modes are described as follows:

1) Mode I ($t_0 - t_1$) [Fig.11 (a)]: v_{gs2} & v_{gs1} become high at $t = t_0$, $i_{Lm} > 0$, $i_{Lk} > 0$, and $i_{Lk} < i_{Lm}$. Since V_B is greater than V_{in}, D_1 is off. V_B provides energy to L_k. V_{C3}, L_m, and V_{C4} provide energy to the load. This mode ends when i_{Lm} is equal to i_{Lk} at t_1.
2) Mode II ($t_1 - t_2$) [Fig.11 (b)]: v_{gs2} and v_{gs1} are high, $i_{Lm} > 0$, $i_{Lk} > 0$, and $i_{Lk} = i_{Lm}$. V_B provides energy to L_m & L_k, and i_{Lm} & i_{Lk} increase linearly. N_s, D_4, and C_4 form a switched capacitor circuit, and V_{C4} is equal to nV_B. This mode ends when v_{gs1} is low at t_2.
3) Mode III ($t_2 - t_3$) [Fig.11 (c)]: v_{gs2} is high. v_{gs1} is low, $i_{Lm} > 0$, $i_{Lk} > 0$, and $i_{Lk} = i_{Lm}$. V_{in} provides energy to L_m & L_k, and i_{Lm} & i_{Lk} increase linearly. This mode ends when v_{gs2} is low at t_3.
4) Mode IV ($t_3 - t_4$) [Fig.11 (d)]: v_{gs2} & v_{gs1} are low. The output capacitor C_{oss2} of S_2 is charged through the i_{Lk}, and v_{ds2} increases. This mode ends when v_{ds2} is equal to V_{C3} at t_4.
5) Mode V ($t_4 - t_5$) [Fig.11 (e)]: v_{gs2} & v_{gs1} are low. i_{Lm} decreases linearly and $i_{Lm} > 0$. V_{ds2} is clamped at V_{C3}. V_{in} and L_m provide energy to C_3. V_{C3}, L_m, and V_{C4} provide energy to the load. This mode ends when v_{gs2} & v_{gs1} are high at t_5.

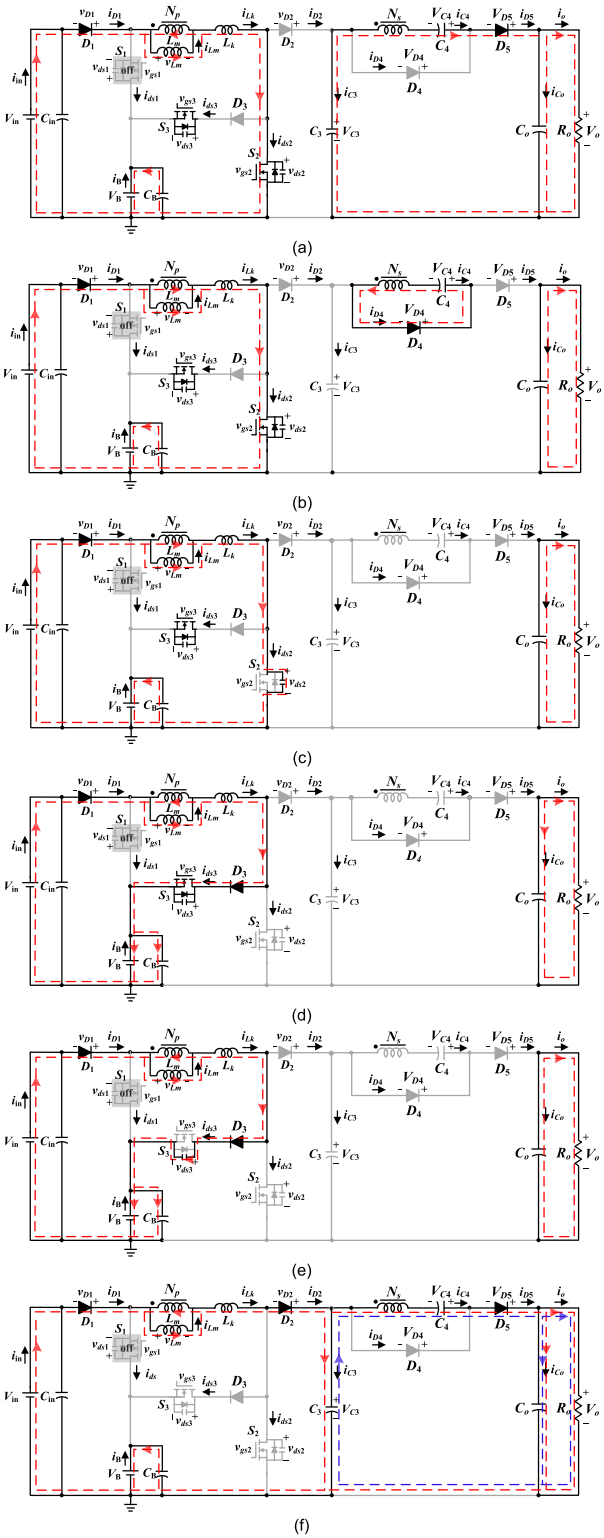

FIGURE 9. Operating processes of the proposed converter in SIDO stage: (a) mode I, (b) mode II, (c) mode III, (d) mode IV, (e) mode V, (f) mode VI.

III. DESIGN CONSIDERATIONS, EFFICIENCY ESTIMATION, AND COMPARISON OF PROPOSED NITPC

To simplify the analysis, it is assumed that the leakage inductance L_k is ignored and the converter is operated under steady-state conditions. D_1, D_2, and D_3 represent the duty ratios of switches S_1, S_2, and S_3, respectively.

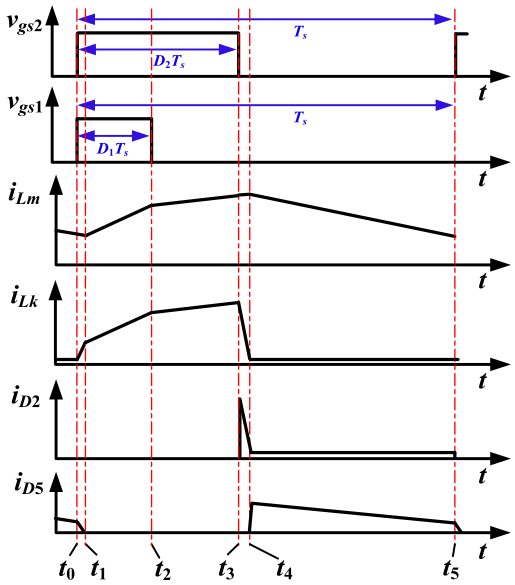

FIGURE 10. Steady-state waveforms in DISO at CCM.

A. SISO-I STAGE DESIGN CONSIDERATIONS

When the main switch S_2 is on, L_m and C_4 are charged through V_{in}.

$$V_{Lm} = V_{in}. \tag{1}$$

$$V_{Ns} = n \quad V_{in} = V_{C4}. \tag{2}$$

When the main switch S_2 is off, the voltage of L_m is

$$V_{Lm} = \frac{V_{in} + nV_{in} - V_o}{n+1}. \tag{3}$$

Using the volt-balance principle of magnetic inductor L_m, by (1) and (3), the voltage gain can be obtained by (4)

$$V_o = \frac{(1+n)V_{in}}{1-D_2}. \tag{4}$$

B. SISO-II STAGE DESIGN CONSIDERATIONS

Since the characteristics of SISO-II are similar to SISIO-I, the voltage gain can be derived by applying the same technique discussed above as

$$V_o = \frac{(1+n)V_B}{1-D_2}. \tag{5}$$

C. SIDO STAGE DESIGN CONSIDERATIONS

When S_2 and S_3 are on,

$$V_{Lm} = V_{in}. \tag{6}$$

$$V_{Ns} = n \quad V_{in} = V_{C4}. \tag{7}$$

When S_2 is off and S_3 is on,

$$V_{Lm} = V_{in} - V_B. \tag{8}$$

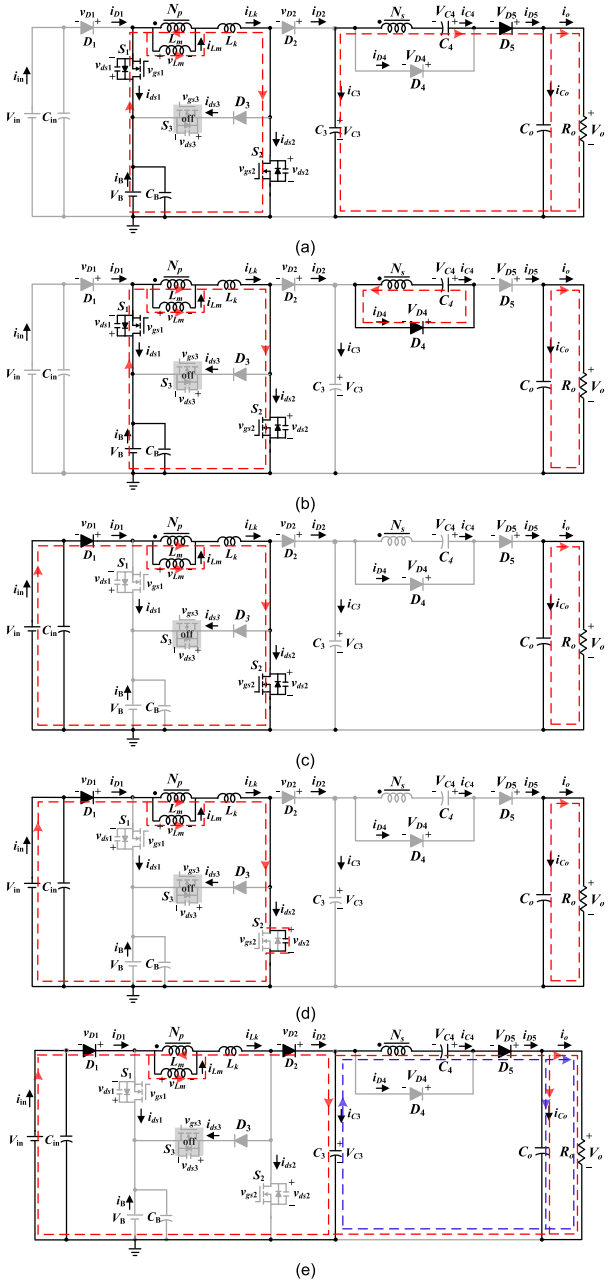

FIGURE 11. Operating processes of the proposed converter in DISO stage: (a) mode I, (b) mode II, (c) mode III, (d) mode IV, (e) mode V.

When S_2 is off and S_3 is off,

$$V_{Lm} = \frac{V_{in} + nV_{in} - V_o}{n+1}. \tag{9}$$

Using the volt-balance principle,

$$V_o = (n+1)\frac{V_{in} + D_2V_B - D_3V_B}{1 - D_3}. \tag{10}$$

D. DISO STAGE DESIGN CONSIDERATIONS

When S_2 and S_1 are on,

$$V_{Lm} = V_B. \tag{11}$$

$$V_{Ns} = n \quad V_B = V_{C4}. \tag{12}$$

When S_2 is on and S_1 is off,

$$V_{Lm} = V_{in}. \tag{13}$$

When S_2 and S_1 are off,

$$V_{Lm} = \frac{V_{in} + nV_B - V_o}{n+1}. \tag{14}$$

Using the volt-balance principle of magnetic inductor L_m, the voltage gain can be obtained:

$$V_o = \frac{V_{in} + nV_B + (V_B - V_{in})(nD_1 - nD_2 + D_1)}{1 - D_2}. \tag{15}$$

E. COUPLED INDUCTOR DESIGN

Based on SISO-I and SISO-II, two different inductance values are calculated. Under CCM, the circuit performance has the good dynamic respond, independent on the load, and high stability. Thus, selecting the larger inductance values between SISO-I and SISO-II makes the modes to be under CCM mode. Assuming V_{in} is larger than V_B, the inductance L_m can be design only in SISO-II.

From Fig.7 (b) in SISO-II, according to KCL, the following equations can be written as

$$i_B = -i_{Cin} + i_{CB}. \tag{16}$$

$$i_{Lk} = i_{Lm} + ni_{D4}. \tag{17}$$

$$i_{D4} = -i_{C4}. \tag{18}$$

$$i_{Co} = -i_o. \tag{19}$$

Also, from Fig.7 (d) in SISO-II, according to KCL, the following equations can be written as

$$i_{Lk} = i_{D2} = i_{Lm} - ni_{D4}. \tag{20}$$

$$i_{D2} = i_{C3} + i_{C4}. \tag{21}$$

$$i_{C4} = i_{D5} = i_{Co} + i_o. \tag{22}$$

Since L_m is continuous, the current ripple of L_m can be derived as follows:

$$\Delta I_{Lm} = \frac{V_B}{L_m} D_2 T_s. \tag{23}$$

By using the current-balance principles, the average currents flowing through the capacitors are equal to zero during one period time. So the following expression can be obtained as

$$I_{D2,ave} = I_{D4,ave} = I_{D5,ave} = I_o. \tag{24}$$

Moreover, by using charge balance, the average currents of the diodes during the condition are written as follow;

$$I_{D4,ave(0-D_2Ts)} = \frac{I_o}{D_2}. \tag{25}$$

$$D2,ave(D_2T_s - T_s) = \frac{I_o}{1 - D_2}. \tag{26}$$

$$I_{D5,ave(D_2T_s - T_s)} = \frac{I_o}{1 - D_2}. \tag{27}$$

By (22), (26) and (27), using KCL. The average current through the L_{m} can be derived as

$$\begin{aligned} I_{Lm,ave} &= I_{D2,ave(D_2T_s-T_s)} + nI_{D5,ave(D_2T_s-T_s)} \\ &= \frac{(n+1)\,I_o}{1-D_2} \end{aligned} \tag{28}$$

In boundary continuous mode (BCM), the average current in (28) is equal to a half of the current ripple in (23). Thus, the following equation can be written as

$$\begin{aligned} I_{Lm,ave} &= \frac{1}{2}\Delta I_{Lm} \\ \Rightarrow L_m &= \frac{V_B D_2\,(1-D_2)\,T_s}{2\,(n+1)\,I_{o,\mathrm{BCM}}} \end{aligned} \tag{29}$$

where $I_{\mathrm{o,BCM}}$ is the load current in BCM.

F. VOLTAGE STRESSES OF SEMICONDUCTOR COMPONENTS

Diode D_2 and capacitor C_3 are used as the clamp circuits. The voltage stress of S_2 is equal to V_{C3}. The follow equation can be written as

$$V_{S2\_\mathrm{stress}} = V_{C3} = \frac{V_{in}}{1-D_2}. \tag{30}$$

In DISO, the voltage stresses of S_2 and S_3 can easily obtain as

$$V_{S1\_\mathrm{stress}} = V_{\mathrm{B}} - V_{in}. \tag{31}$$

$$V_{S2\_\mathrm{stress}} = \frac{V_{in}}{1-D_2} - V_{\mathrm{B}}. \tag{32}$$

The voltage stresses of the diodes can be derived as follows:

$$V_{D1\_\mathrm{stress}} = V_{\mathrm{B}} - V_{in}. \tag{33}$$

$$V_{D2\_\mathrm{stress}} = V_{C3}. \tag{34}$$

$$V_{D3\_\mathrm{stress}} = \frac{V_{in}}{1-D_2} - V_{\mathrm{B}}. \tag{35}$$

G. CAPACITORS DESIGN

By the voltage ripple on the capacitors, capacitances can be obtained [25]. By (24), the following equations can be written as

$$C_3 = \frac{P_o}{V_o \Delta V_{C3} f_s}. \tag{36}$$

$$C_4 = \frac{P_o}{V_o \Delta V_{C4} f_s}. \tag{37}$$

$$C_{\mathrm{B}} = \frac{P_B}{V_B \Delta V_{C\mathrm{B}} f_s}. \tag{38}$$

where ΔV_{C3}, ΔV_{C4}, $\Delta V_{C\mathrm{B}}$ are the voltage ripple of capacitors C_3, C_4, and C_{B}, respectively.

H. EFFICIENCY ESTIMATION

Since the proposed converter can be operated in different stages, only SISO-II is calculated and other stages can use the same calculation method. And transient time ($[t_{\mathrm{o}} - t_1]$, $[t_2 - t_3]$) is very insufficient, the losses can be ignored. By using KCL, the following equation in SISO-II can be written as

$$i_{Lk} = -i_{ds1} = i_B + i_{C\mathrm{B}} = i_{Lm} - ni_{C4} \tag{39}$$

Applying the current-balance principles to capacitors, the following equation can be written as

$$I_B = I_{Lm} \tag{40}$$

Assuming M is the voltage gain, by (5), the input current IB can be obtain as

$$I_B = MI_o \tag{41}$$

1) SWITCHES LOSSES

The power switches losses contain conduction losses and switching losses. During S_2 on, from Fig.7 and KCL, the lowest current I_{S_low} and highest current I_{S_high} though the power switches can be derived as follows:

$$I_{S\_\mathrm{low}} = I_{Lm} - \frac{\Delta I_{Lm}}{2} + \frac{nI_o}{2} \tag{42}$$

$$I_{S\_\mathrm{high}} = I_{Lm} - \frac{\Delta I_{Lm}}{2} \tag{43}$$

During S_2 off, the current flowing through S_2 is zero. The current following through S_1 is equal to i_{D2}. By (26), (40), (42) and (43), the conduction losses on the power switches can be obtained as

$$P_{S1\_\mathrm{con}} = \sqrt{\int_0^{D_2T_s} \frac{1}{T_s} A^2 r_{ds1}\,dt + \int_{D_2T_s}^{T_s} \frac{1}{T_s} B^2 r_{ds1}\,dt} \tag{44}$$

where

$$A = \frac{I_{S\_\mathrm{high}} - I_{S\_\mathrm{low}}}{D_2T_s} t + I_{S\_\mathrm{low}}$$

$$B = \frac{I_{S\_\mathrm{low}} - I_{S\_\mathrm{high}}}{(1-D_2)\,T_s} t + \frac{I_{S\_\mathrm{high}} - D_2 I_{S\_\mathrm{low}}}{1-D_2} + \frac{2I_o}{(1-D_2)^2\,T_{\mathrm{s}}} t - \frac{2I_o}{(1-D_2)^2}$$

$$P_{S2\_\mathrm{con}} = \sqrt{\int_0^{D_2T_s} \frac{1}{T_s} \left(\frac{I_{S\_\mathrm{high}} - I_{S\_\mathrm{low}}}{D_2T_s} t + I_{S\_\mathrm{low}} \right)^2 r_{ds2}\,dt} \tag{45}$$

where r_{ds1} and r_{ds2} are the conduction resistances on the power switches S_1 and S_2, respectively.

Due to S_1 always on, only S_2 has the switching loss. By (30) and (43), the switching loss can be written as

$$P_{S2\_sw} = \frac{1}{2} V_{S2} I_{S\_\mathrm{high}} t_{\mathrm{on}} + \frac{1}{2} V_{S2} I_{S\_\mathrm{high}} t_{\mathrm{off}} \tag{46}$$

where t_{on} and t_{off} are the rising time and falling time of S_2. By (44), (45) and (46), the switches losses can be written as

$$P_{S\_\mathrm{loss}} = P_{S1\_\mathrm{con}} + P_{S2\_\mathrm{con}} + P_{S2\_\mathrm{sw}} \tag{47}$$

2) DIODES LOSSES

By (26), the conduction losses of D_2 are found as

$$P_{D2\_loss} = V_{f2} I_{D2,ave} + I_{D2,ave}^2 r_{D2} \tag{48}$$

where V_{f2} and r_{D2} are the conduction voltage drop and conduction resistance of D_2. Using the same method for D_4 and D_5, the total losses of diodes can be written as

$$P_{D\_loss} = P_{D2\_loss} + P_{D4\_loss} + P_{D5\_loss} \tag{49}$$

3) INDUCTOR LOSSES

During S_2 on, the rms current on the primary side is equal to rms current through S_2. The conduction loss on the secondary side can be derived as

$$P_{Lp\_con\_on} = \sqrt{\int_0^{D_2 T_s} \frac{1}{T_s} \left(\frac{I_{S\_high} - I_{S\_low}}{D_2 T_s} t + I_{S\_low} \right)^2 r_{Lp} dt} \tag{50}$$

where r_{Lp} is the conduction resistance of primary side. And the conduction loss on the secondary side can be derived as

$$P_{Ls\_con\_on} = \sqrt{\int_0^{D_2 T_s} \frac{1}{T_s} \left(\frac{2I_o}{D_2} - \frac{2I_o}{D_2^2 T_s} t \right)^2 r_{Ls} dt} \tag{51}$$

where r_{Ls} is the conduction resistance of secondary side. When S_2 is off, the conduction loss on the primary side is equal to $P_{S2\_con\_off}$, and by (44), the following equation can be written as, (52), as shown at the bottom of the next page.

During S_2 off, the current flowing through secondary side is equal to the current flowing through D_5. The conduction loss on the secondary side can be derived as

$$P_{Ls\_con\_off} = \sqrt{\int_{D_2 T_s}^{T_s} \frac{1}{T_s} \left(\frac{2I_o}{(1-D_2)^2} - \frac{2I_o}{(1-D_2)^2 T_s} t \right)^2 r_{Ls} dt} \tag{53}$$

The total losses of inductor are obtained as

$$P_{L\_loss} = P_{Lp\_con\_on} + P_{Ls\_con\_on} + P_{Lp\_con\_off} + P_{Ls\_con\_off} \tag{54}$$

4) CAPACITORS LOSSES

In mode IV of SISO-II, it is a dynamic process for capacitor charging and discharging. For the convenience of analysis, the charging time and discharging time each account for a half for C_3. By (25), (26) and (27), the conduction losses of capacitors can be written as

$$P_{C3\_loss} = I_{D5,ave(D_2 T_s - T_s)}^2 r_{C3} (1 - D) \tag{55}$$

$$P_{C4\_loss} = I_{D4,ave(0 - D_2 T_s)}^2 r_{C4} D + I_{D5,ave(D_2 T_s - T_s)}^2 r_{C4} (1 - D) \tag{56}$$

$$P_{Co\_loss} = I_o^2 r_{Co} D + \left(I_{D5,ave(D_2 T_s - T_s)} - I_o \right)^2 r_{Co} (1 - D) \tag{57}$$

where r_{C3}, r_{C4}, and r_{Co} are the parasitic resistances of C_3, C_4, and C_o, respectively. The total losses of capacitors are obtained as

$$P_{C\_loss} = P_{C3\_loss} + P_{C4\_loss} + P_{Co\_loss} \tag{58}$$

The theoretical efficiency of the proposed converter can be expressed as

$$\eta = \frac{P_o}{P_o + P_{S\_loss} + P_{D\_loss} + P_{L\_loss} + P_{C\_loss}} \tag{59}$$

where P_o is the output power of this converter.

I. COMPARISONS

A comparison study between the proposed NITPC and the revealed structures is illustrated in Table 1. The number of devices, voltage gain, voltage stress on the power switch, and the maximum full load efficiency are selected as the comparison. Moreover, in order to compare voltage gain per number of components [22], the voltage gain per component counts is shown based on the given input and output voltages, and according to Table 1, the proposed NITPC utilizes few components for achieving high voltage in comparison with other revealed structures.

IV. EXPERIMENTAL RESULTS

In order to verify the feasibility of the proposed converter, a 200 W laboratory prototype is built and tested to verify the theoretical analyses and the system specifications of the prototype are shown in Table 2.

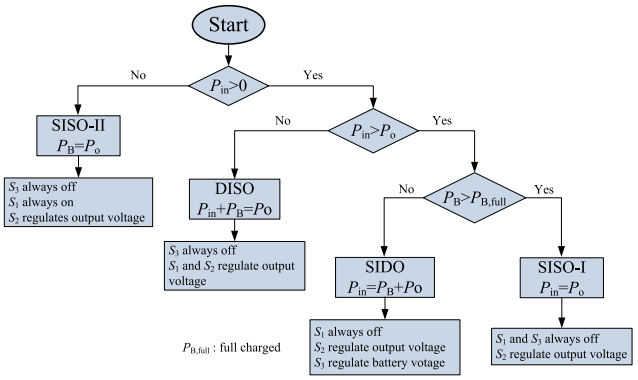

FIGURE 12. Control flow-chart of the proposed converter.

Based on the power of input port, battery port and load port, the control flow-chart is shown in Fig.12. When the P_{in} cannot provide energy, the converter is operated in SISO-II stage. When P_{in} provides less energy than P_o requiring, the converter is operated in DISO. When P_{in} can provide more energy than P_o requiring and P_B is not full charged, this converter is operated in SIDO; otherwise in SISO-I.

Under different turns ratio, the voltage gain versus the duty cycle D_2 in SISO-I and SISO-II are shown in Fig.13. Since D_3 should be larger than D_2 in SIDO, n is chosen as 4 to obtain high efficiency in SISO-I and SISO-II and avoid D_3

TABLE 1. Comparison between proposed NITPC and reveled structures.

Topology	Converter in [9]	Converter in [10]	Converter in [14]	Converter in [18]	Converter in [20]	Proposed converter
No. of switches	4	3	3	3	4	3
No. of diodes	5	7	3	5	4	5
No. of inductors	2	2	1	2	1	1
Component counts	11	12	7	10	9	9
Voltage source 1 (V)	36	40	35	24	20	24
Voltage source 2 (V)	72	48	70	48	24	48
Output voltage (V)	400	400	100	400	200	400
Rated output power (W)	150	200	500	300	125	200
Voltage gain	11.1	10	2.86	16.7	10	16.7
Voltage gain per component counts	1	0.83	0.41	1.67	1.1	1.86
Voltage stress on power switch	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$
The maximum full load efficiency (%)	95.8	93.9	98	95.8	96	95.8

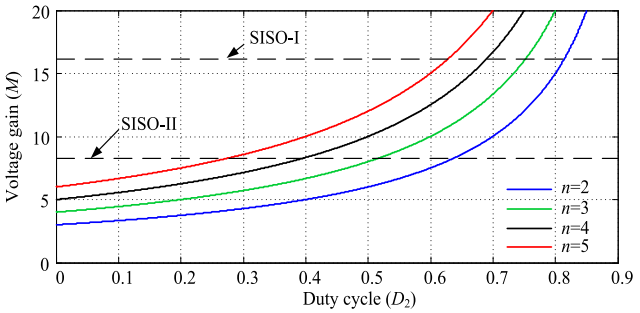

FIGURE 13. Voltage gain versus D_2 in SISO-I and SISO-II.

TABLE 2. System specifications and key parameters.

Parameters	Values
Voltage of input port (V_{in})	24 V
Voltage of battery port (V_B)	48 V
Rated Voltage of the load (V_o)	400 V
Maximum input port power ($P_{in,\,max}$)	220 W
Maximum battery port power ($P_{B,\,max}$)	200 W
Rated output power (P_L)	200 W
Switching frequency (f_s)	50 kHz
Power MOSFET(S_1 - S_3)	IXFK230N20T
Magnetizing inductor	Ferrite Core: ETD49 Material: 3C90 Magnetizing inductance L_m: 65 μH Leakage nductance L_k: 3 μH
Turns ratio (N_p : N_s)	17: 68
Didoes (D_1, D_2, D_3, D_4, D_5)	D_1: DSSK80-0045B D_2: 1N4935 D_3: MBR20200CT D_4 & D_5: MUR160
Capacitors (C_3, C_4)	C_3: 47μF, C_4: 22μF

being too high. Thus, the energy flows are controlled. Table 3 shows the relationship of D_3 and D_2 in SIDO under different output power sharing conditions with $n = 4$ which reveals that D_2 and D_3 are varied from (0.54∼0.71) and (0.74∼0.95), respectively.

A. WAVEFORMS MEASURED IN SISO-I STAGE

Fig.14 (a) and (b) show the key waveforms of v_{gs2}, v_{ds2}, $i_{D2,}$ and i_{D5} under $P_L = 100$ W and $P_L = 200$ W at input voltage 24 V, respectively. When S_2 is turned off and D_2 is on, V_{in} and L_m provide energy to the load and v_{ds2} is clamped by the clamp diode D_2 and the intermediate capacitor C_3.

$$P_{Lp\_con\_off} = \sqrt{\int_{D_2T_s}^{T_s} \frac{1}{T_s}\left(\frac{I_{S\_low} - I_{S\_high}}{(1-D_2)\,T_s}t + \frac{I_{S\_high} - D_2 I_{S\_low}}{1-D_2} + \frac{2I_o}{(1-D_2)^2\,T_s}t - \frac{2I_o}{(1-D_2)^2}\right)^2 r_{Lp}dt} \tag{52}$$

TABLE 3. The relationship of D_3 and D_2 in SIDO under different output power sharing conditions.

V_{in}	V_B	V_o	Output power and sharing conditions in SIDO	D_2	D_3
24 V	48 V	400 V	P_{in}=P_B(20 W)+P_L(200 W)	0.71	0.75
			P_{in}=P_B(200 W)+P_L(20 W)	0.54	0.95
			P_{in}=P_B(20 W)+P_L(160 W)	0.69	0.74
			P_{in}=P_B(160 W)+P_L(20 W)	0.55	0.95
			P_{in}=P_B(20 W)+P_L(120 W)	0.68	0.74
			P_{in}=P_B(120 W)+P_L(20 W)	0.54	0.93
			P_{in}=P_B(20 W)+P_L(80 W)	0.66	0.74
			P_{in}=P_B(80 W)+P_L(20 W)	0.58	0.90

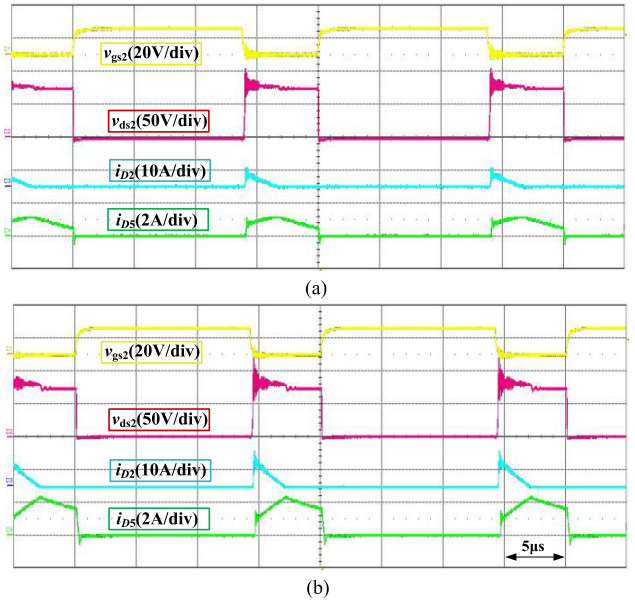

FIGURE 14. Waveforms v_{gs2}, v_{ds2}, i_{D2}, and i_{D5} in SISO-I (a) P_L = 100 W (b) P_L = 200 W.

The voltage spike of v_{ds2} is less than 150 V, and thus a power switch with low on-resistance R_{ds_on} can be used to decrease conduction loss.

B. WAVEFORMS MEASURED IN SISO-II STAGE

The key waveforms of v_{gs2}, v_{ds2}, i_{D2}, and i_{D5} under P_L = 100 W and P_L = 200 W at input voltage 48 V are shown in Fig.15 (a) and (b), respectively. V_B and L_m provide energy to the load and v_{ds2} is clamped by clamp diode D_2 and intermediate capacitor C_3. Compared with the 100% load when S_2 is off, v_{ds2} appears at a certain resonance in 50% load because this stage is in discontinuous conduction mode. i_{D2} and i_{D5} at P_L = 200 W are higher than that at P_L = 100 W.

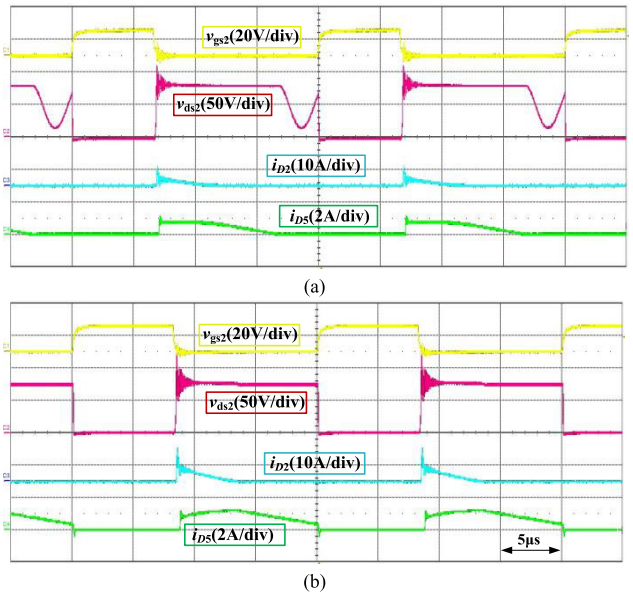

FIGURE 15. Waveforms, v_{gs2}, v_{ds2}, i_{D2}, and i_{D5} in SISO-II (a) P_L = 100 W (b) P_L = 200 W.

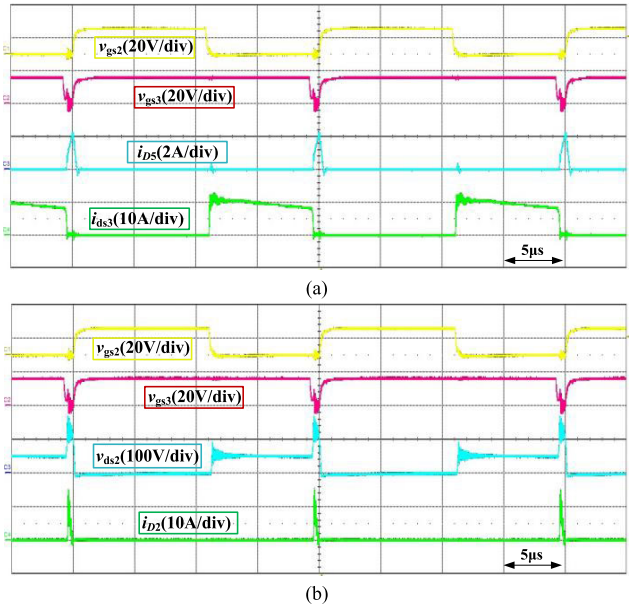

FIGURE 16. Waveforms in SIDO at P_{in} = P_B (200 W) + P_L (20 W) (a) v_{gs2}, v_{gs3}, i_{D5}, i_{ds3} (b) v_{gs2}, v_{gs3}, v_{ds2}, i_{D2}.

C. WAVEFORMS MEASURED IN SIDO STAGE

Fig.16 (a) and Fig.16 (b) show the key waveforms of v_{gs2}, v_{gs3}, i_{D5}, i_{ds3}, v_{ds2}, and i_{D2} at P_B = 200 W and P_L = 20 W. When S_2 is off and S_3 is on, V_{in} and L_m provide energy to V_B, and v_{ds2} is clamped by clamp diode D_2, intermediate capacitor C_3 and output capacitor C_B. When S_2 and S_3 are off, V_{in} and L_m provide energy to the load, and v_{ds2} is clamped by D_2 and C_3. The key waveforms of v_{gs2}, v_{gs3}, i_{D5}, i_{ds3}, v_{ds2}, and i_{D2} at P_B = 20 W and P_L = 200 W are shown in Fig.17 (a) and Fig.17 (b). i_{D5} in Fig.17 (a) is higher than that in Fig.16 (a), and conversely, i_{ds3} is lower because V_{in}

transfers more energy to V_B in Fig.16 and less energy to V_B in Fig.17.

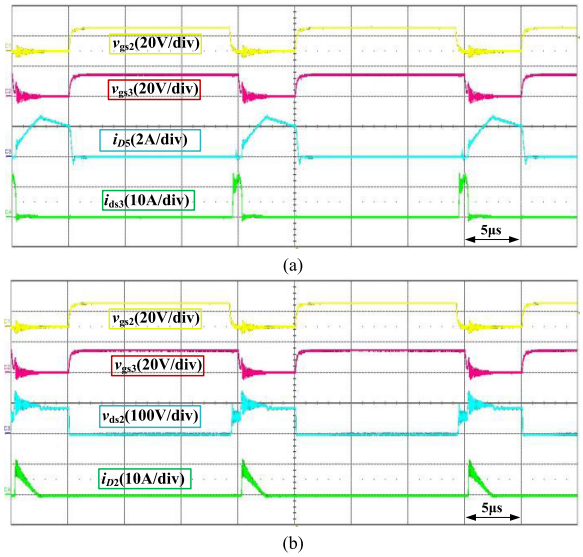

FIGURE 17. Waveforms in SIDO at $P_{in} = P_B$ (20 W) + P_L (200 W) (a) v_{gs2}, v_{gs3}, i_{D5}, i_{ds3} (b) v_{gs2}, v_{gs3}, v_{ds2}, i_{D2}.

D. WAVEFORMS MEASURED IN DISO STAGE

Fig.18 (a) and Fig.18 (b) show v_{gs2}, v_{gs1}, i_{ds1}, and i_{D2} at P_{in} = 160W and P_B = 40W, and P_{in} = 40W and P_B = 160W, respectively. It reveals that i_{ds1} becomes higher when V_B provides more energy to the load.

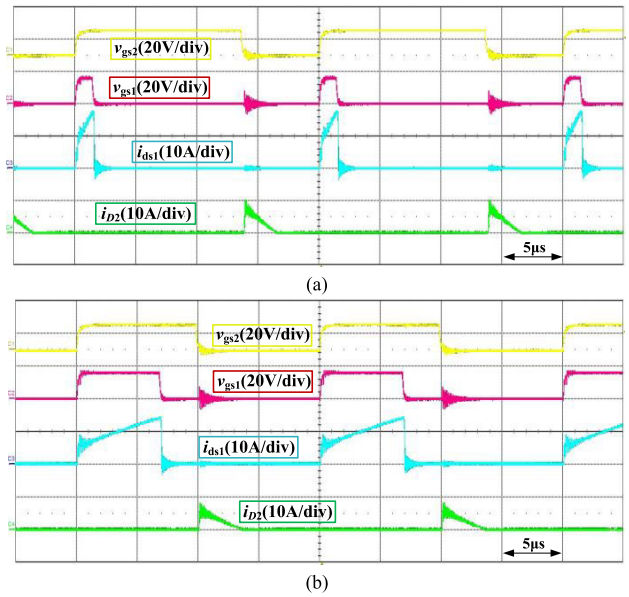

FIGURE 18. Waveforms of v_{gs2}, v_{gs1}, i_{ds1}, and i_{D2} in DISO (a) P_{in} = 160W, P_B = 40W, and P_L = 200W (b) P_{in} = 40W, P_B = 160W, and P_L = 200W.

E. EXPERIMENTAL RESULTS IN SIDO MODE WITH CONSTANT VOLTAGE

Fig.19 shows dynamic response of the proposed converter between 50% load P_o = 100 W and full load P_o = 200W.

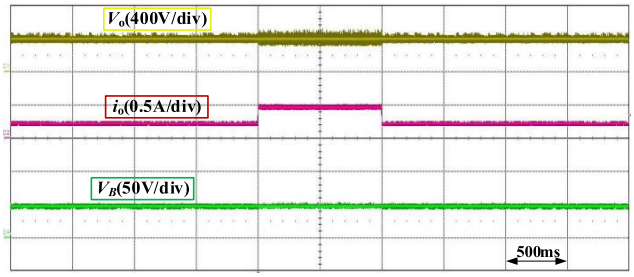

FIGURE 19. Load variation between P_o = 100 W and P_o = 200 W in SIDO mode.

To simulate the condition of constant voltage to the battery port, the battery port operates at a very light load i_B = 0.05 A. Change of i_o has a slight impact on V_o and V_B remains constant.

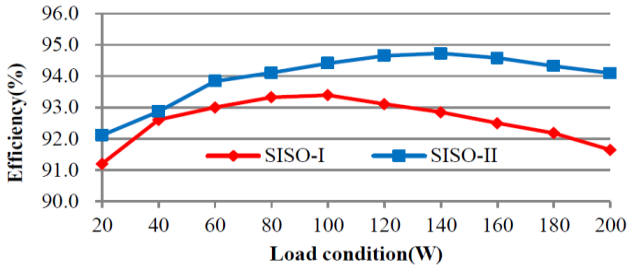

FIGURE 20. Efficiency curves of the proposed NITPC in SISO-I and SISO-II.

F. MEASURED EFFICIENCY

The efficiency curves of the proposed NITPC in SISO-I and SISO-II during the load range of 10%-100% are shown in Fig.20. It reveals that the maximum efficiencies are 93.4% in SISO-I and 94.7% in SISO-II, respectively. Meanwhile, the efficiencies of the full load are 91.7% in SISO-I and 94.1% in SISO-II, respectively. The efficiency of SISO-II is higher than that of SISO-I because of severe conduction losses in SISO-I. In SIDO, the efficiency curve under various battery load ranges while keeping the output load power at 20 W is shown in Fig.21 (a). The maximum efficiency is 93.7% at P_B = 120 W, and the efficiency is 92.4% at P_B = 200 W. In SIDO, the efficiency curve under various output load ranges while keeping the battery load power at 20 W is shown in Fig.21 (b). The maximum efficiency is 93.4% at P_L = 20 W, and the efficiency is 90.9% at P_L = 200 W. Fig.22 shows the efficiency curve of NITPC in DISO with various input sharing conditions at full load. It reveals that the efficiency is increased when the battery port shares more load power. The maximum efficiency is 95.8% at P_{in} = 40 W and P_B = 160 W.

Considering selected active and passive components based on Table 2 under V_B = 48 V, V_o = 400 V, and P_o = 200 W, the calculated efficiency of the proposed converter is shown in Fig.23. The total losses are 10.8 W and the inductor losses are mainly the losses, accounting for 60% of the total losses. The calculated efficiency is 94.9% and the measured efficiency value is 94.1%.

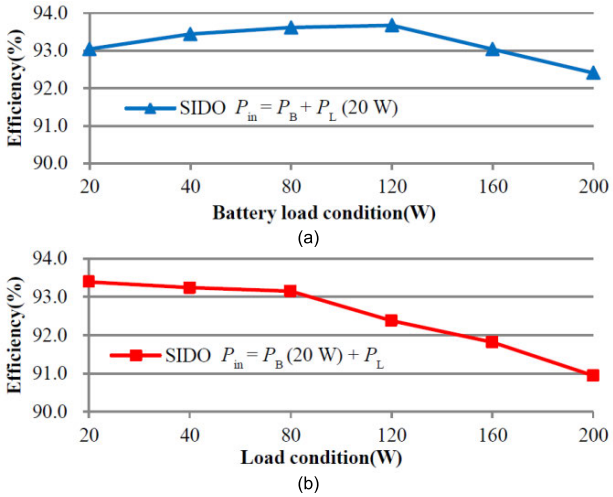

FIGURE 21. Efficiency curves of the proposed NITPC in SIDO (a) $P_L = 20$ W (b) $P_B = 20$ W.

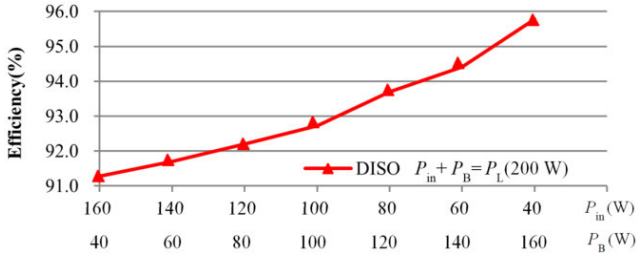

FIGURE 22. Efficiency curve of NITPC in DISO with various input sharing conditions at full load.

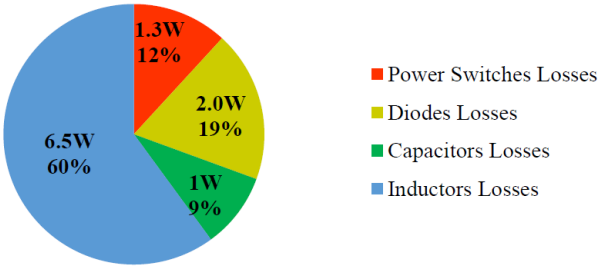

FIGURE 23. Distribution of the calculated losses under $V_B = 48$ V, $V_O = 400$ V, and $P_O = 200$ W.

V. CONCLUSION

This paper proposed a NITPC for renewable energy applications with few components count. A coupled inductor and switched capacitor techniques are used to improve the voltage gain. The proposed converter can realize power flows with one port for renewable energy sources, one bidirectional port for energy storage system, and one port for the high voltage load. Moreover, the clamp circuit is employed to recycle the leakage inductance energy and clamp the voltage stress of the power switch. The efficiency can be further improved with low on-resistances of the power switches. The detailed analysis and consideration of the proposed converter were presented. A 200 W laboratory prototype with renewable energy port of 24 V, battery port of 48 V, and output port of 400 V was developed and tested. The experimental results verify the feasibility of the proposed NITPC with high step-up voltage gain and high efficiency. The measured highest efficiency is 95.8%.

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