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Impact of Channel Thickness on the Performance of GaAs and GaSb DG-JLMOSFETs: An Atomistic Tight Binding Based Evaluation

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ABSTRACT In this paper, the performance of GaAs and GaSb based sub-10 nm double-gate junctionless metal-oxide-semiconductor field-effect transistors (DG-JLMOSFETs) have been studied for high-performance switching applications. The quantum transmitting boundary method (QTBM) has been considered for electron transport, and the band structures are accounted for sp3d5s* tight-binding modeling. The channel thickness, t_{ch} is varied from 1.7 to 4.7 nm to evaluate the device figure of merits (FOMs). The thinner channel's device shows a lower OFF-state current, while the ticker channel device allows a higher ON-state current. The threshold voltage is approximately 0.4 V for GaAs DG-JLMOSFETs with $t_{ch} = 1.7$ nm, whereas it reduces to ∼0.05 V for that of $t_{ch} = 4.7$ nm. Similar characteristics have been shown in GaSb devices. Besides, a significant impact of t_{ch} on the subthreshold swing (SS) and drain-induced barrier lowering (DIBL) is found in GaSb DG-JLMOSFETs compared with those of GaAs devices. The devices show a higher leakage-power dissipation in both channel materials and low-intrinsic delay for thicker t_{ch} due to a substantial amount of energy drop. The above results indicate that III-V-based DG-JLMOSFETs are very promising for next-generation high-performance switching technology.

INDEX TERMS GaAs, GaSb, double gate, junctionless MOSFETs, nano-scaled device, short-channel effects (SCEs), high-performance switching.

I. INTRODUCTION

The roadmap of enhancing transistor density through miniaturization initiates several drawbacks in conventional MOSFETs such as Short Channel Effects (SCE's), Drain Induced Barrier Lowering (DIBL), Hot Carrier Effects (HCEs), Channel Length Modulation (CLM), etc [1], [2]. The successful fabrication of junctionless transistor (JLT) in 2010 has mitigated the significant drawbacks of existing MOSFETs [3]. The junctionless MOSFETs (JLMOSFETs) have overcome the challenges that originate from the requirement of too high gradients in doping concentration in present transistors, mainly designing for sub-10 nm gate length [4]. Recently, the JLMOSFETs have received significant attention for their technological feasibility and theoretical modeling. In the last decades, several device architectures for JLMOSFETs were proposed, such as Thin Film JLMOSFET [5], [6], FinFET [7], [8], Tunnel FET [9], [10], gate-all-around (GAA) FET [11], [12], single-gate JLT (SG-JLT) [13], [14], double-gate JLMOSFETs (DG-JLMOSFETs) [15]–[18], etc. The DG-JLMOSFETs are becoming more promising due to their superior performances in high speed and low power applications [19]. Most of the reports on DG-JLMOSFETs are limited to studying the

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performances using Si as a channel material. However, with the advancement of small-scale device technology, Si is becoming less interested in ultra-scale minimization material. The III-V semiconductors have been reported as potential alternative channel materials as they can overcome the scaling limit of traditional Si-based CMOS technology [20]–[22]. The III-V semiconductor is becoming a better choice for future transistor technology because of their superior performances, including extremely-low OFF-state leakage current, suppressed trapping effect, high-linearity characteristics, and excellent gate controllability [23]–[25]. Nonetheless, few reports are analyzing the performances of JLMOSFETs using III-V semiconductors as channel materials. InGaSb has been used in a cylindrically surrounding gate JLMOSFET, and the device performances have been compared with the Si counterpart [26]. Recently, GaN and GaAs based JLTs with GAA gate arrangement have also been subjected to simulation and characterization using TCAD [27]. Khan *et al.* presented surface potential-based analytical modeling of electrostatic and transport phenomena of GaN Nanowire JLMOSFETs [28]. Other reports consider different approaches of device architecture of III-V based JLMOSFETs [29], [30]. However, the research using III-V semiconductor as a channel material in DG-JLMOSFET is scarce despite the novel features of these promising materials.

In JLMOSFETs, attaining full depletion is challenging as it requires ultra-thin channel ($\leq$5 nm) [31]. With such an extremely confined channel the performance analysis of III-V based DG-JLMOSFET is critically essential since both tight-binding calculations [32], [33] and the empirical pseudo-potential process [34] reported the increases of electron effective mass with the decrease of t_{ch} due to the remarkable quantum confinement effect (QCE). Moreover, the bandgap of III-V semiconductors increases as the channel is made thinner [35]. The QCE needs critical importance since it could affect the threshold voltage, which touches the other figure of merits (FOMs) of a transistor [36]. Still, inadequate data are available on the QCEs, on the device performance, and studies on III-V based DG-JLMOSFETs are lacking. However, such results are crucial to design the next-generation high-performance nanoscale devices. Therefore, more detailed understandings and the proper inclusions of the QCEs or impact of t_{ch} on the device performance of III-V based DG-JLMOSFETs are immensely important.

In this work, the performances of GaAs and GaSb based DG-JLMOSFETs have been analyzed considering various channel thicknesses using the modeling tool NEMO5. The band structures are accounted here from sp3d5s* based tight-binding modeling, and the quantum transmitting boundary method (QTBM) has been considered for electron transport in the devices. An assessment related to the FOMs of GaAs and GaSb based DG-JLMOSFETs have been realized depending on the effective masses of electrons in the channel materials. Moreover, the effect of t_{ch} on both transistors' performances such as conduction band profile, voltage-dependent drain current characteristic, the threshold voltage (V_{th}), sub-threshold swing (SS), and drain induced barrier lowering (DIBL) have been studied meticulously. Furthermore, the power dissipation and energy consumption in both GaAs and GaSb based DG-JLMOSFETs have been analyzed considering various channel thicknesses.

II. COMPUTATIONAL METHODOLOGY

Figure 1 shows the schematic device structure (left-side) and the possible fabrication process steps (right-side) for DG-JLMOSFETs. The device performances have been analyzed for two channel materials such as GaAs and GaSb. For both cases, the t_{ch} has been varied from 1.7 to 4.7 nm. The device has the gate length, $L_G = 10.6$ nm, and effective oxide thickness (EOT) of 0.59 nm which is equivalent to the physical oxide thickness of 3.33 nm and dielectric constant of 22 [37]. The channel is doped with 1×10^{18} cm^{-3} and the doping level in both source and drain is 2×10^{19} cm^{-3}. No underlap has been considered for the simulation. The materials and structural parameters that have been considered in this work are given in **Table 1**. Very low resistive ohmic (source and drain) contacts are considered [38]. Rest of other physical parameters' values are considered from Refs. 37 and 38.

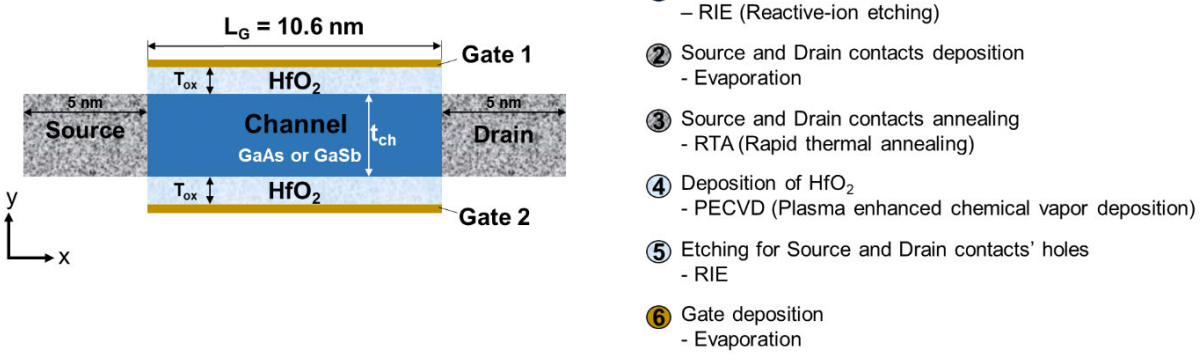

FIGURE 1. The schematic device structure (left-side) and the possible fabrication process steps (right-side) for DG-JLMOSFETs.

TABLE 1. Details of double gate junctionless MOSFETs.

Parameter	Value
Channel Materials	GaAs or GaSb
Electron Mobility (300K)	8000 $cm^2 V^{-1}s^{-1}$ (GaAs) 5000 $cm^2 V^{-1} s^{-1}$ (GaSb)
Hole Mobility (300K)	400 $cm^2 V^{-1}s^{-1}$ (GaAs) 1500 $cm^2 V^{-1} s^{-1}$ (GaSb)
L_G	10.6 nm
Lead Length (Source/Drain)	5 nm
Doping	2×10^{19} cm^{-3} (for Drain and Source)
	1×10^{18} cm^{-3} (for Channel)
EOT (HfO_2, where k = 22)	0.59 nm

The transport simulations have been performed using parallel multiscale nano-electronics modeling tool NEMO5 [39], [40]. In this work, ballistic transport model has been considered which self consistently solves Schrodinger's and Poisson's equation. In NEMO5, the ballistic transport method is implemented using the Quantum Transmitting Boundary Method (QTBM). The QTBM approach cannot capture inelastic scattering; thus, we have neglected the scattering effects. This transport simulation is conducted by non-equilibrium Green's function (NEGF) [41], [42], which uses the recursive Green's function (RGF) algorithm [43]. Both NEGF and QTBM methods are capable of capturing the quantum mechanical effects in nano-devices. However, RGF is usually slower than QTBM since the calculation of Green's function requires matrix inversion. Besides, NEGF is numerically expensive when applied to atomistic tight-binding representations [40].

For the ultra-thin body (UTB) channel DG-JLMOSFETs, sp3d5s* tight binding method is adopted to calculate parabolic dispersion which is used to calculate carrier density. It is required to calculate the total carrier density in the channel region for estimating the ballistic drain current. The carrier density is computed as [44]–[47]:

$$n_i = \int dE \sum\nolimits_c g_i^c(E) \frac{1}{A} \sum\nolimits_{k_i} f\left(E + \varepsilon\left(|k_i|\right), E_f^c\right) \quad (1)$$

The total carrier density is obtained by multiplying the probability density $\left|\Psi_{k_i}^c\right|^2$ with the corresponding occupancy function in contact c before summing over all the contacts, injection energies E, and transverse in the first Brillouin zone. Here, $\varepsilon(|k_i|)$ is given by the parabolic dispersion relation along the transverse directions. After calculating the carrier density, the total drain current, I_D is calculated using the Landauer-Buttiker formula [46]:

$$I_D = -\frac{e}{h} \int \frac{dE}{2\pi} T(E) \left[F\left(E, E_f^L\right) - F(E, E_f^R)\right] \quad (2)$$

Here, $T(E)$ is the transmission function, which relates the transmitted and backscattered flux of an incoming Bloch wave of energy E as follows [46]:

$$T(E) = \frac{\left|\Psi_N^L(E)\right|^2 \left|v^R(E)\right|}{\left|\Psi_1^L(E)\right|^2 \left|v^L(E)\right|} \quad (3)$$

where, the quantities $v^L(E)$ and $v^R(E)$ correspond to the electron group velocities at energy E in the left and right contact, respectively. Here, the transport properties of the device are fully characterized by the transmission probability. The active region is considered as a "black box" through which injected electrons can either be transmitted or reflected back. According to the equation 2, an I_D is given by the flux difference between right-flowing carriers originating from the source and left-flowing carriers injected from the drain. The floating boundary condition has been imposed to solve the transport problem in NEMO5 [47].

The calculated electron effective mass of both GaAs and GaSb for different thicknesses is shown in Fig. 2. The effective masses have been extracted from the sp3d5s* based tight-binding approach using the modeling tool NEMO5. These results are in close agreement with other works [32], [48]. For all the cases, source and drain resistances are not included in the simulation or post-processing stage. The parameters which are essential to calculate the Figure of Merits (FOMs) of GaAs and GaSb based DG-JLMOSFETs have been extracted. The detailed extracted formulas and procedures are mentioned in our previous work [49]. The GaAs and GaSb based UTB DG-JLMOSFET structures that have been studied in this work is different from the FinFET or gate-all-around FET as the UTB structure significantly considers the QCE. The similar studies had been performed for different UTB III-V devices such as GaAs, GaSb, and Ge based UTB ballistic nMOSFETs and FETs [33], [38], [50]–[52]. The strong QCE has been attributed in GaAs and GaAs to the transport phenomena caused by different band valleys. To maximize the device performance, the Γ-valley electron transport with high DOS and high injection velocity are the key concerns. Thus, the isotropic Γ-valley transport has been considered here.

III. RESULTS AND DISCUSSION

A. CONDUCTION BAND PROFILE

To study the effect of channel thickness, t_{ch} on the ON- and OFF-states of both GaAs and GaSb based DG-JLMOSFETs with a fixed gate length, $L_G = 10.6$ nm, we have analyzed the conduction band (CB) profile along the channel length with various t_{ch}. The devices are switched from OFF- to ON- states by varying the gate-to-source voltage (V_{GS}) from 0 to 0.8 V with a fixed drain-to-source voltage (V_{DS}) = 0.75 V. From the OFF-state behaviors as depicted in **Figs. 3 (a)** and **(c)**, it is observed that the devices having thinner t_{ch} show better OFF characteristics. This characteristic is due to the higher source-to-channel barrier height, which might be attributed to the one-dimensional QCE that becomes pronounced at thinner t_{ch} [35]. More QCE is observed in GaSb based DG-JLMOSFETs at OFF-state in compare with GaAs. On the

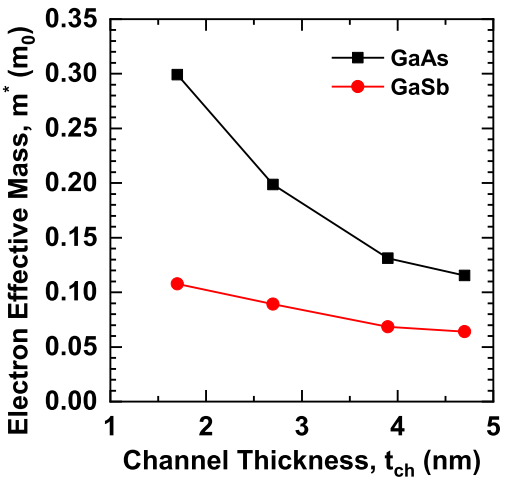

FIGURE 2. Channel-thickness dependent electron effective mass of GaAs and GaSb.

other hand, at higher t_{ch}, the QCE degrades as the tunneling widths are found to be narrower and source-to-channel barrier heights become smaller for both device structures [52]. The higher QCE at lower t_{ch} for both GaAs and GaSb is reflected by the enhancement of electron effective mass as shown in **Fig. 2**. Significance changes in conduction band energy are observed in source and drain regions for different t_{ch} of GaAs devices (**Fig. 3 (a)**) due to high reduction rate (∼exponential) of electron effective mass (**Fig. 2**) for GaAs, whereas no significance change in conduction band energy is found in source region for GaSb devices (**Fig. 3 (c)**) because of low reduction rate (∼linear) of electron effective mass (**Fig. 2**) for GaSb devices. Conduction band energies of GaAs are higher than those of GaSb which insure the less tunneling probability leading to low leakage current. Besides, better ON-state behavior is noticeable from the CB profile for GaSb based devices for lower t_{ch}, as shown in **Fig. 3 (d)**. For GaAs based devices, the ON-state CB profile is shown in **Fig. 3(b)** turns into the flat condition allowing high electron flow. As results, the effective gate length becomes enhanced. For GaSb devices, the CB's lowering starts and shifts to the drain side at thicker t_{ch}, which may lower the electron carrier density as compared to those of GaAs devices.

B. DC CHARACTERISTICS

To further investigate the effect of t_{ch} on the drain current in both GaAs and GaSb based DG-JLMOSFETs at ON-and OFF-states, the DC characteristics of those devices have been studied in detail. **Figure 4** shows the typical output characteristics of GaAs **(a)** and GaSb **(b)** based DGJLMOSFETs. For both the devices, the drain to source voltage, V_{DS} is varied from 0 V to 0.75 V for each of the applied gate voltage, V_{GS}. It is found that the GaAs based structure depicts the better output behavior in comparing with GaSb counterpart for the same channel thickness. In GaAs based DG-JLMOSFETs, the ON-state current is found to be higher than the GaSb. **Figures 5(a) and (b)** show the devices' transfer characteristics for different t_{ch}. The lower OFF-current is achieved for the devices having a thinner channel than a thicker one. The devices with thicker, t_{ch} have a lighter effective mass of the electron and suffer from stronger source-drain tunneling (SDT), consequently increasing the OFF-state current [53]. However, high ON-current is achievable for both the devices with an increase of t_{ch}. The figures inset show the details of ON-current characteristics of both devices for various t_{ch} at $V_{GS} = 0.8$ V. The rising behavior of ON-current with t_{ch} is explained using the generalized theoretical model in Ref. 54 where it has been concluded that the current become less sensitive to extrinsic scattering in the thicker channels (<14 nm) compared to extremely thin channel. More details of the effect of t_{ch} on the OFF-state current as well as I_{ON}/I_{OFF} have been visualized in **Fig. 6**. The calculated results indicate that with the increase of t_{ch} in both devices, the OFF-state current increases considerably, and as a result, the I_{ON}/I_{OFF} decreases. Nevertheless, in this analysis, the maximum I_{ON}/I_{OFF} is observed up to $\sim 9.84 \times 10^{10}$ when t_{ch} (GaAs) is 1.7 nm.

To explain the transfer characteristics more illustratively, the formation of channel in both GaAs and GaSb based DG-JLMOSFETs have been explored using the contour plot of carrier concentration. The contour plots in the channel region of both the devices have been shown in Fig. 7 for different t_{ch} as 1.7, 2.7, 3.9, and 4.7 nm. Both the OFF- and ON-states have been observed with a fixed drain-to-source voltage, $V_{DS} = 0.75$ V. During OFF-state, the channel region in both GaAs and GaSb based DG-JLMOSFETs is depleted. Thus, no majority electron carrier concentration is found in the channel region. Besides, considering the highly doped channel region in JLMOSFETs, an ultrathin t_{ch} is required to achieve full depletion. During ON-state, a positive gate voltage drives the channel region from depletion to the flat band condition. For GaAs based DG-JLMOSFET, it is found that the carrier concentration becomes higher for the thicker channel devices with similar gate bias. Similar increasing behavior of the carrier concentration with t_{ch} has also been observed for the GaSb based devices. The carrier density in GaSb becomes smaller than the GaAs based devices for same t_{ch} and gate bias.

C. THRESHOLD VOLTAGE

To be considered as competent channel material for switching device, the threshold voltage of that device is essentially crucial to be analyzed. **Figure 8** illustrates the t_{ch} dependent threshold voltage, V_{th} for both GaAs and GaSb based DG-JLMOSFETs. It is perceived for both devices that the required V_{th} falls with the increase of t_{ch}. For GaAs based DG-JLMOSFET, we found that the V_{th} is ∼0.4 V for t_{ch} = 1.7 nm, reducing to ∼0.05 V for t_{ch} = 4.7 nm. Similar decreasing behavior of threshold voltage is also obtained for GaSb based DG-JLMOSFETs. However, this declining tendency of V_{th} is opposite to the conventional MOSFETs where higher V_{th} are required in thicker channel devices to turn ON. The DG-JLMOSFETs without gate bias remain turned OFF due to the depletion in the channel region. The channel

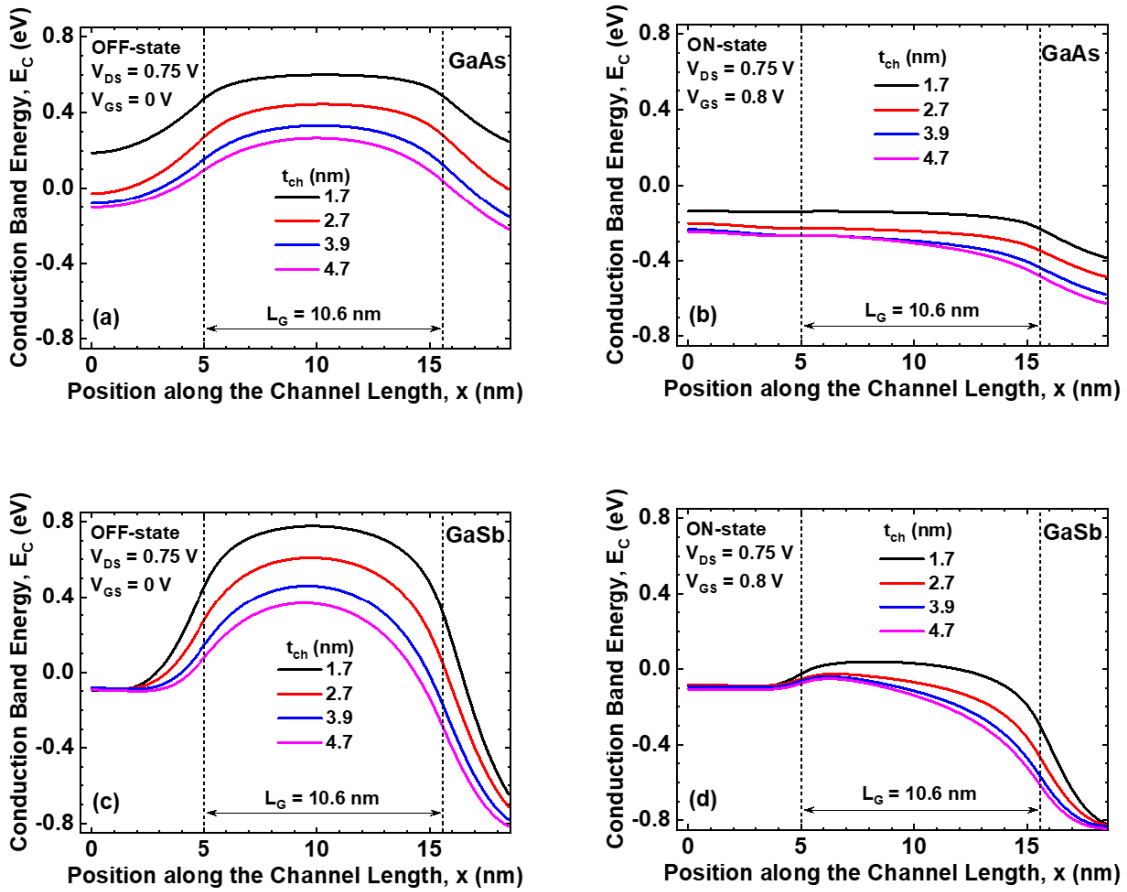

FIGURE 3. Conduction band profiles along the channel length (x) of GaAs and GaSb in DG-JLMOSFETs at ON (a and b) and OFF-states (c and d).

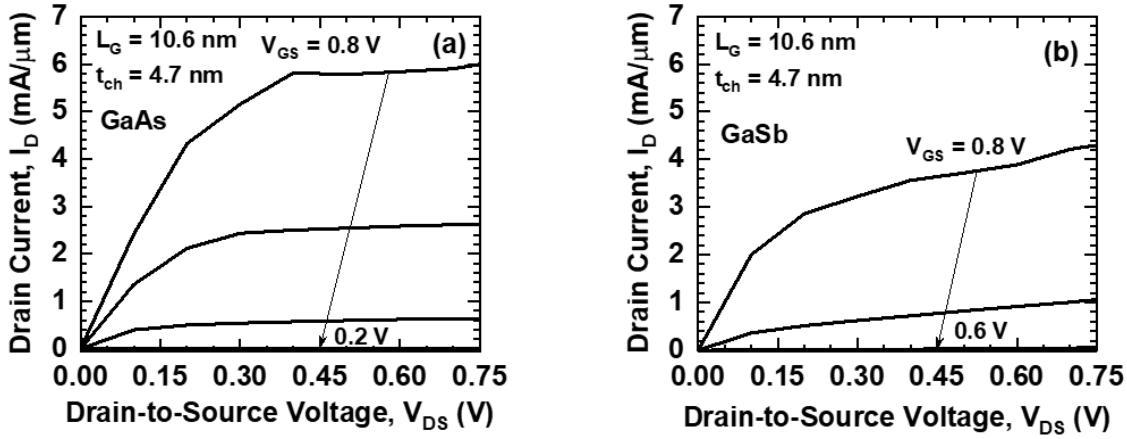

FIGURE 4. DC output characteristics of DG-JLMOSFETs using GaAs (a) and GaSb (b) as channel materials.

depletion creates a large electric field to the perpendicular direction with the drain current. When gate bias is applied above the threshold, the electric field drops to zero, and the channel becomes electrically neutral. Here, we found for both GaAs and GaSb based DG-JLMOSFETs that the required V_{th} to neutralize the electric field varies with channel material thickness. The required smaller V_{th} for thicker channel devices may be attributed to the electric field's reduced effect (due to depletion) in the channel layer's center part. With the increase of t_{ch}, the portion of channel with reduced electric field effect widens, and consequently, the bulk mobility could start with lower V_{GS} (i.e., V_{th}).

In addition, the requirement of higher V_{th} for thinner channel DG-JLMOSFETs can also be elucidated by the higher effective mass of electrons in both GaAs and GaSb channel materials at lower thickness as illustrated in **Fig. 2** which is initiated by QCE [55]. The thickness dependent change of effective mass of electron in both channel material has been

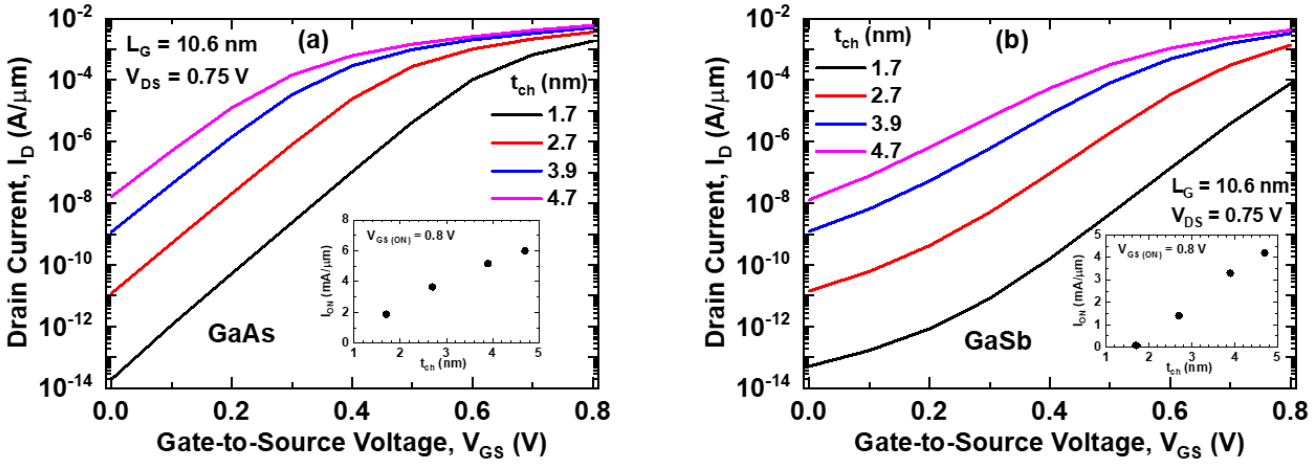

FIGURE 5. Transfer characteristics of (a) GaAs and (b) GaSb based DG-JLMOSFETs for various channel thicknesses.

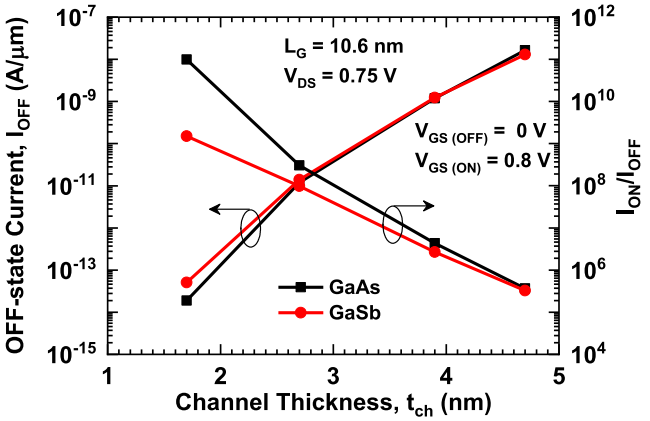

FIGURE 6. Effect of channel thickness on the OFF-state current and I_{ON}/I_{OFF} ratio for GaAs and GaSb based DG-JLMOSFETs.

discussed earlier while analyzing the CB profile. Due to the higher effective mass of electron in thinner t_{ch}, the required voltage to neutralize the electric field in the channel becomes high for both GaAs and GaSb devices. In contrast, the effective mass of electron is smaller at thicker channel devices which requires lower biasing voltage to be neutralized from the electric field that was originated at OFF-state due to the depletion in the channel region. Similar decreasing behavior of V_{th} with the increase of t_{ch} has also been reported for Si-based JL nanowire transistors [56]. More importantly, a different physics also lies behind the theory to explain the subthreshold region of DG-JLMOSFET, which is essential to analyze the subthreshold swing of JLMOSFETs.

D. SUBTHRESHOLD SWING (SS) AND DRAIN INDUCED BARRIER LOWERING (DIBL)

The subthreshold swing (SS) and drain induced barrier lowering (DIBL) for both GaAs and GaSb based DG-JLMOSFETs for various t_{ch} have been illustrated in **Fig. 9**. We observed a tiny change in SS and DIBL with the t_{ch} of GaAs-based devices as compared with GaSb. The effective mass of electron in GaAs ($0.067m_e$) is higher than GaSb ($0.041m_e$), which results in reduced SDT [53]. The reduced SDT improves SS in GaAs based DG-JLMOSFET. Despite the lower effective electron mass in GaSb, the thickness induced further reduction of electron effective mass gives rise to the SDT, which results in larger SS at higher t_{ch}. Besides, a sharp effect of t_{ch} on DIBL is observed for GaSb based DG-JLMOSFET as compared with that of GaAs based devices. In GaSb DG-JLMOSFET, the DIBL is found 40 mV/V for a t_{ch} of 1.7 nm, whereas it increases to ∼170 mV/V for t_{ch} = 4.7 nm. The DIBL has been extracted for drain bias of 0.05 and 0.75 V. In contrast, DIBL of $\sim 20 \pm 10$ mV/V is found in GaAs-based devices for the t_{ch} of 1.7 to 4.7 nm.

The SS and DIBL obtained for both GaAs and GaSb based DG-JLMOSFETs are relatively smaller than the Si based FETs. Since, the mainstream device is still the Si MOSFETs, a comparative summary of SS and DIBL including with other FOMs have been enlisted in **Table 2**. It presents the FOMs of both GaAs and GaSb based DG-JLMOSFETs together with the Si based JLFET and MOSFET. We obtained the smallest SS and DIBL for GaAs and GaSb based DG-JLMOSFETs. Additionally, I_{ON} is found 6 mA/μm and 1.9 mA/μm for GaAs device when t_{ch} is 4.7 nm and 1.7 nm, respectively. These values are higher than the Si devices. The GaSb device with t_{ch} of 4.7 nm shows I_{ON} = 4.2 mA/μm. The values of I_{ON} for both GaAs and GaSb based DG-JLMOSFETs are found to be higher than the projected values of high-performance switching devices according [38].

E. GATE CAPACITANCE

The effect of t_{ch} on the gate capacitance, C_{GG} for both GaAs and GaSb based DG-JLMOSFETs have been calculated using Ref. 59. The values of C_{GG} have been estimated for the different t_{ch}. During OFF-state (V_{GS} = 0 V), we found that C_{GG} becomes higher in case of thicker channel devices for both GaAs and GaSb DG-JLMOSFETs. In GaSb DG-JLMOSFET, C_{GG} is 0.011 aF/um for t_{ch} = 1.7 nm, while it becomes 1.156 aF/um for t_{ch} = 4.7 nm. On the other hand, during ON-state (V_{GS} = 0.8 V), thickness dependent

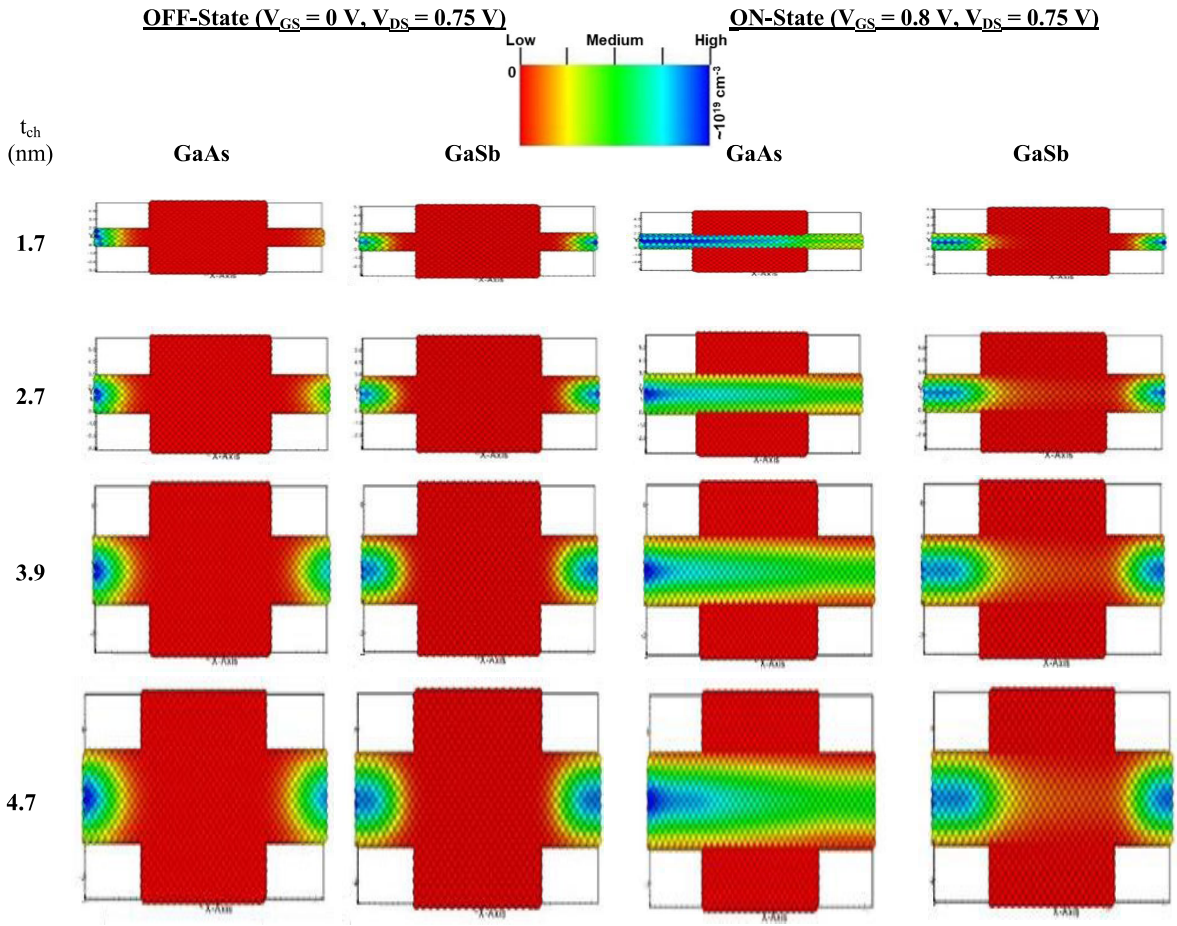

FIGURE 7. Contour plot of carrier concentration (electron) at channel region of GaAs and GaSb based DG-JLMOSFET for gate bias of 0 V and 0.8 V with different channel thicknesses as 1.7 nm, 2.7 nm, 3.9 nm, and 4.7 nm.

increasing values of C_{GG} have also been observed for both GaSb and GaAs devices. In GaSb DGJLMOSFET, C_{GG} is 4.75 aF/um for $t_{ch} = 1.7$ nm, while it increases to 22.79 aF/um when the $t_{ch} = 4.7$ nm. For ON-state, the depletion region becomes narrower which results in comparatively larger depletion capacitance. The higher value of depletion capacitance results in higher C_{GG} since it appears as a series association of the gate oxide capacitance.

F. POWER, ENERGY, AND DELAY

Furthermore, we have analyzed the effect of t_{ch} on the power dissipation and energy consumption for both GaAs and GaSb based DG-JLMOSFETs, as illustrated in **Figs. 10(a)** and **(b)**, respectively. The total power dissipated, P_{total} is calculated using the following equation as [59]

$$P_{total} \approx P_{leak} + P_{dynamic} \tag{4}$$

where, the leak power, $P_{leak} \approx nI_{leak}V_{DD}$ and the dynamic power, $P_{dynamic} \approx \frac{1}{2}(nI_{leak})V_{DD}(n\tau)\alpha$. The n is the number of identical stages of an inverter chain ($n = 50$ [59]), α is activity factor ($\alpha = 2\%$ [59]), I_{ON} is ON-state current, and I_{leak} is the leakage current flow during OFF-state with a fixed supply voltage, V_{DD}. As the source is 0 V, the supply voltage, V_{DD} is equal to V_{DS}. The total energy consumption,

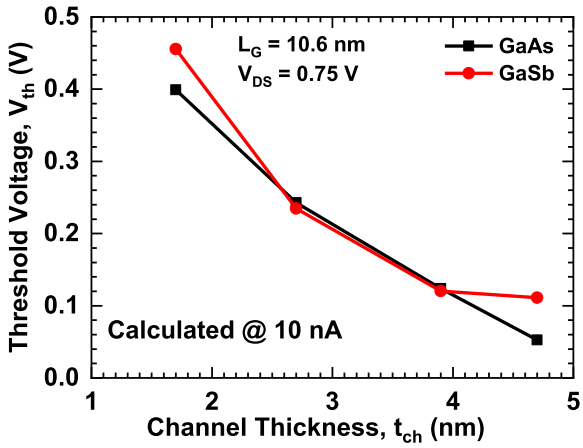

FIGURE 8. Channel thickness-dependent threshold voltage of GaAs and GaSb based DG-JLMOSFETs.

E_{total} is expressed as [59]

$$E_{total} \approx E_{leak} + E_{dynamic} \tag{5}$$

where, the leak energy, $E_{leak} \approx (nI_{leak})V_{DD}(n\tau)$ and the dynamic energy, $E_{dynamic} \approx \frac{1}{2}(nC_{GG})V_{DD}^2\alpha$. The τ is the intrinsic delay which expresses as $\tau \approx \frac{(C_{GG}V_{DD})}{I_{ON}}$ [59], [60]

TABLE 2. Comparison of figure of merits for both GaAs and GaSb based DG-JLMOSFETs with Si based devices.

Device Structure	Channel	L_G (nm)	t_{ch} (nm)	I_{ON} (mA/μm)	I_{OFF} (A/μm)	I_{ON}/I_{OFF}	SS (mV/dec)	DIBL (mV/V)
DG-MOSFET [47]	Si	10	3	0.65	6×10^{-9}	1.08×10^{6}	75	80
UTB-JLFET [57]	Si	3	1	1	6×10^{-8}	3.98×10^{5}	83	129
JL-MOSFET [58]	Si	3	1	0.1	$\sim10^{-10}$	$\sim10^{6}$	74	120
DG-JLMOSFET [In this work]	GaAs	10.6	1.7	1.9	1.9×10^{-14}	9.84×10^{10}	62	15
		10.6	4.7	6	1.64×10^{-8}	3.64×10^{5}	68	30
	GaSb	10.6	1.7	0.08	5.04×10^{-14}	1.51×10^{9}	67	40
		10.6	4.7	4.2	1.3×10^{-8}	3.26×10^{5}	137	170

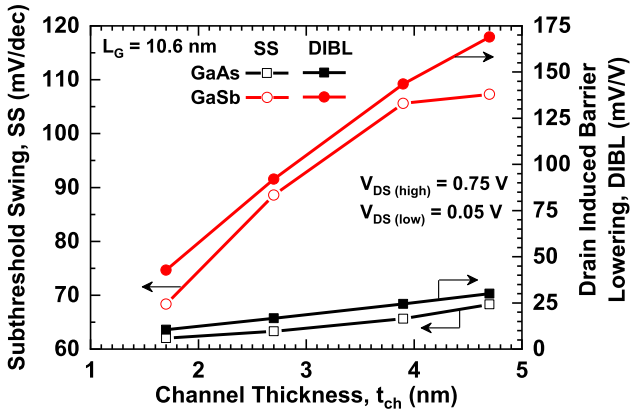

FIGURE 9. Subthreshold swing (SS) and drain-induced barrier lowering (DIBL) for GaAs and GaSb based DG-JLMOSFETs for different channel thicknesses.

and C_{GG} is switching capacitance which is known as gate capacitance.

A high leakage power, P_{leak} is found to be dissipated for thicker t_{ch} in case of all devices (**Fig. 10 (a)**). This scenario may be attributed to the thickness induced increasing behavior of OFF-state current, which originated from the lowering of electron effective mass and SDT at higher t_{ch} that have been discussed earlier. In GaAs devices, the total power dissipated is higher than that of GaSb devices, particularly, in lower t_{ch} which might occur due to the heavier electron effective mass of electrons in GaAs. Likewise, as P_{leak}, the leakage energy consumption, E_{leak} also shows similar increasing behavior with the t_{ch} for both GaAs and GaSb devices (**Fig. 10 (b)**). However, the total dissipated energy, E_{total} in GaSb devices is much higher than that of GaAs based DG-JLMOSFETs. This increase may be ascribed to the high intrinsic delay in GaSb based device which has been discussed in the later section.

The effects of t_{ch} on the intrinsic delay, τ in GaAs and GaSb based DG-JLMOSFETs are illustrated in **Fig. 11**. The τ is related to the mobile charges in the whole device at ON- and OFF-states, including I_{ON}. It can be directly related to charge quantity difference between OFF- and ON-states.

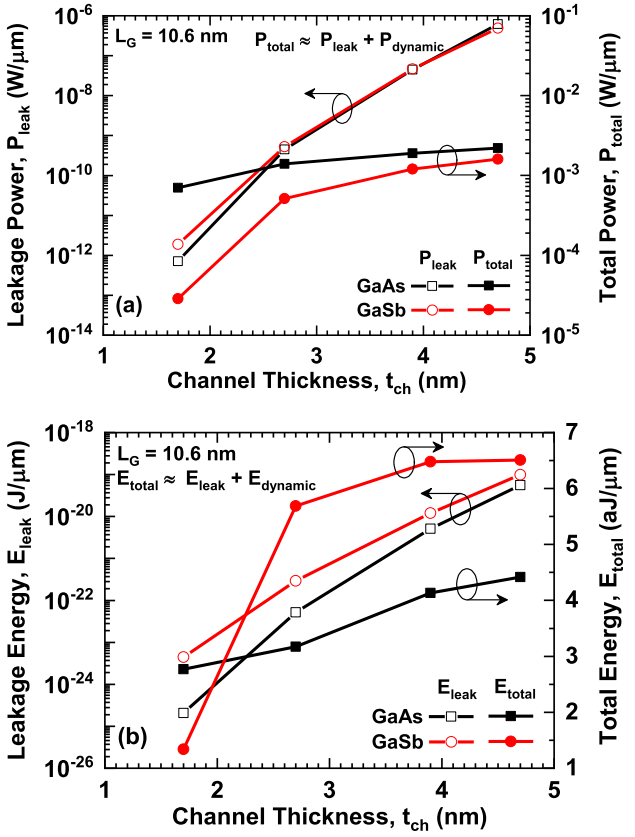

FIGURE 10. Effects of channel thickness on the (a) power dissipation and (b) energy consumption for both GaAs and GaSb based DG-JLMOSFETs.

The τ is estimated using Refs. 59 and 60. This quantity becomes smaller in GaAs based DG-JLMOSFETs due to the heavier electron effective mass (compared with GaSb) as it retards the variation of charges from OFF- to ON-states. As a result, τ becomes smaller in GaAs based devices. A slight increase in τ is observed at lower t_{ch} for GaAs, which may be attributed to the higher I_{ON}. These results indicate that GaAs channel-based DG-JLMOSFETs are more suitable for high-performance switching device than those of GaSb based devices.

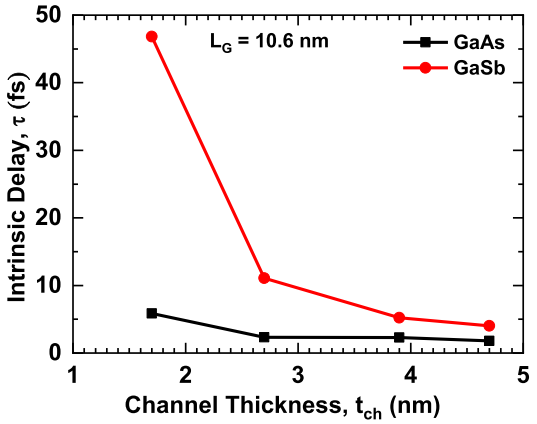

FIGURE 11. Channel thickness-dependent intrinsic delay of GaAs and GaSb based DG-JLMOSFETs.

IV. CONCLUSION

We have studied the impact of channel thickness on III-V based sub-10 nm DG-JLMOSFETs. It is found that the t_{ch} has remarkable effects on the performance of both GaAs and GaSb based DG-JLMOSFETs. For both channel materials, the lower OFF-current is obtained for the devices having thinner channels. However, higher ON-current is found for devices with thicker channels. The maximum I_{ON}/I_{OFF} is observed up to 10^{11} when GaAs' t_{ch} is 1.7 nm. It is observed that the required threshold voltage falls with the increase of t_{ch}, which is opposite to the conventional MOSFETs. We perceived a tiny change in SS and DIBL with the t_{ch} for GaAs devices compared with GaSb devices. The higher effective mass of electron in GaAs results in reduced SDT, which improves SS in GaAs DG-JLMOSFET. Moreover, a strong effect of t_{ch} on DIBL is observed for GaSb DG-JLMOSFET. For both devices, more leakage powers are found to be dissipated for thicker channels. However, due to the high intrinsic delay in GaSb, the total energy consumed in GaSb is much higher than the GaAs DG-JLMOSFET. These results could be useful to engineer the GaAs and GaSb based DG-JLMOSFETs for future high-performance switching devices applications.

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