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Modified Nearest Level Modulation for Full-Bridge Based HVDC MMC in Real-Time Hardware-in-Loop Setup

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ABSTRACT Modular Multilevel Converter (MMC) is an emerging converter topology for medium and high voltage applications. Nearest level Modulation (NLM) is the conventional control topology used to control the MMC that produces the N+1 AC output waveform. In previous research work, the Modified NLM has been already proposed, producing a 2N+1 and 4N+1 output waveform while utilizing a half-bridge (HB) submodule (SM) topology. However, half-bridge-based MMC has a similar behavior as two-level Voltage Source Converter (VSC) and cannot block DC fault current in case of DC-side short circuit fault. So, in recent years, full-bridge-based MMC topology is preferably used by manufacturers as it has DC fault blocking capabilities. This paper presents the Modified NLM for Full bridge (FB) SM topology to take the critical benefits of FB SM topology and improve power quality. The proposed method is simpler to implement and produces a 4N+1 AC output waveform. The THD of the output voltage and current reduces to half compared to the conventional NLM method. The proposed method is verified using LabVIEW Multisim co-simulation and as well as real-time simulation.

INDEX TERMS Modified NLC, full bridge, HVDC MMC, hardware-in-loop simulation.

I. INTRODUCTION

Modular Multilevel Converter (MMC) is a promising converter topology used nowadays, especially in the applications of High Voltage Direct Current (HVDC) Transmission systems and in multi-terminal DC (MTDC) grids due to its various advantages over conventional converters [1]. Series connected identical submodules (SMs) make its design simpler, modular, easily scalable in voltage and current, and provides redundancy [2], [3].

Generally, fundamental switching frequency methods such as space vector modulation, selective harmonic elimination (SHE), and nearest level modulation (NLM) are preferred in MMC to limit the switching losses [4]–[9]. For MMC with a high number of SMs, the NLM modulation method is given preference due to its attractive features such as simple implementation, not involving complex mathematics as in the SHE modulation method, and natural capacitor voltage balancing [10], [11]. In NLM, the three-phase grid voltages are taken as a reference, fed back to a modulator. These voltages are converted to the staircase waveform using a round function. The switching pulses for all SMs present in the upper and lower arm of the MMC are generated. Finally, the SMs are inserted and bypassed using a conventional sorting algorithm depending upon arm current polarity, SM voltage, and voltage required at the output [12], [13].

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The conventional NLM method generates N+1 AC output levels (N is the number of SMs in the upper/lower arm) [14]. More SMs are employed to raise the number of levels in the output, which increases the number of switches, capacitors, and gate driver circuitry and, therefore, the system's complexity [15], [16]. To increase the number of levels, the power quality of the output voltage and current Modified NLM methods are presented in various research articles. For instance, the authors in [15] proposed modified NLM for Half Bridge (HB) MMC to produce 4N+1 level output AC waveform. However, HB MMC cannot block dc fault currents in case of dc short circuit fault. The authors in [17] proposed the binary, trinary, and modified MMC-based topology to improve power quality and reduce circuit complexity. The proposed method involves complex calculations and gives higher THD. The reference [18] presented a modified NLM to improve the power quality, but this study lacks experimental verification. The research reported in [19] provided an improved NLM with fewer SMs, although their technique had a larger THD and no experimental validation. The authors in [20] also presented an increased NLM method with fewer SMs and less THD. In various other articles [21]–[25], the authors presented the Modified NLM method to improve the power quality and reduce the circuit complexity.

Nevertheless, the studies presented were only limited to the half-bridge topology of MMC. Full bridge SM topology has many advantages such as inherent DC fault blocking capability, increased AC output voltage, and twice the number of output voltage levels [26], [27]. Thus, there is a tire need to develop a Modified NLC method for full-bridge SM topology to get the above-discussed features of full-bridge topology. In this paper, a modified NLC approach to operate full-bridge SM-based MMC HVDC is presented. The proposed modified NLC produces a 4N+1 AC output waveform which improves the power quality of the voltage and currents.

Offline simulation is done using LabVIEW Multisim Co-simulation to evaluate the efficacy of the proposed technique, in which the control algorithm is created in LabVIEW and the circuit is implemented in Multisim. The results are obtained for conventional and modified NLC control with various levels, and comparisons are drawn between both techniques. The Modified NLC is then implemented in FPGA-based controller Compact Reconfigurable input/output (CRIO), and the circuit is implemented in NI PXI for real-time results verification.

II. WORKING PRINCIPLE OF MMC

The topology of FB-based HVDC MMC is shown in Fig. 1. It consists of three phases, with each phase includes the upper and lower arm connected in series through an inductor. The arms are formed using FB SMs. Each SM contains four switches and a capacitor connected across them. To derive output voltage and current equations, use Kirchhoff's voltage law (KVL) and current law (KCL) in the upper and lower

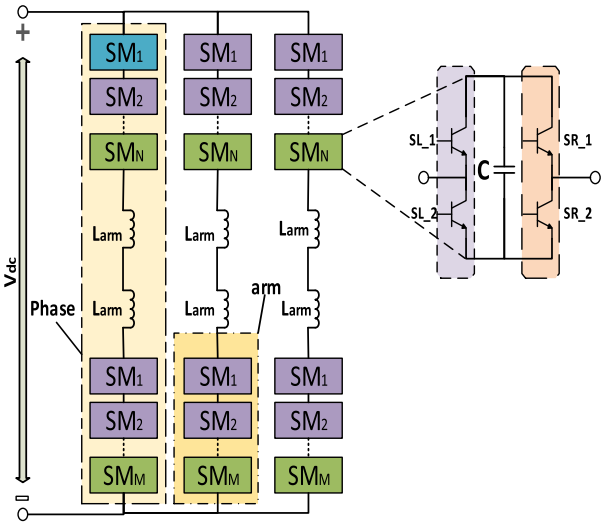

FIGURE 1. Three-phase MMC HVDC with FB SM topology.

arms of any phase. The equations can be written as

$$V_{x\_upper} = -\sum_1^N V_{SM\_N} + \frac{1}{2}V_{dc} - L_{arm}\frac{di_{upper}}{dt}, \quad (1)$$

$$V_{x\_lower} = \sum_1^M V_{SM\_M} - \frac{1}{2}V_{dc} + L_{arm}\frac{di_{lower}}{dt}, \quad (2)$$

where, V_{x_upper} and V_{x_lower} are the output voltage of the upper arm and lower arm, V_{dc} is the total DC link voltage, L_{arm} is the inductance of inductor connected to the arm, i_{upper} and i_{lower} are the upper and lower arm currents and V_{SM_N} and V_{SM_M} are the SM voltages of the upper and lower arm, respectively. Depending upon the switches, the voltages of SMs i.e., V_{SM_N} and V_{SM_M} can be positive, negative, and zero. Thus, the output current can be found by equation (3).

$$i_x = i_{upper} - i_{lower} \quad (3)$$

From equation (1) and (2), the output voltage can be written as

$$V_x = \frac{1}{2}\left(\sum_1^M V_{SM_M} - \sum_1^N V_{SM_N}\right) + \frac{1}{2}L_{arm}\frac{di_x}{dt}. \quad (4)$$

The ac equivalent voltage can be calculated by

$$V_{ac} = \frac{1}{2}\left(\sum_1^M V_{SM_M} - \sum_1^N V_{SM_N}\right). \quad (5)$$

In general, ac equivalent voltage is found as

$$V_{ac}^{ref} = \frac{mV_{dc}}{2}\cos(\omega t). \quad (6)$$

The reference voltages for upper and lower arm operation are written as

$$V_{upper}^{ref} = \frac{V_{dc}}{2}[1 - m\cos(\omega t)], \quad (7)$$

$$V_{lower}^{ref} = \frac{V_{dc}}{2}[1 + m\cos(\omega t)], \quad (8)$$

where m is the modulation index in the range $0 < m < 1$ and ω is the angular frequency.

III. NLM METHOD

The following formulae can calculate the number of SMs inserted in the upper and lower arm

$$N_{upper} = \left(\frac{V_{dc}}{2V_{SM}}\left[1 - m\cos(\omega t)\right]\right)_{round(0.5)}. \quad (9)$$

$$N_{lower} = \left(\frac{V_{dc}}{2V_{SM}}\left[1 + m\cos(\omega t)\right]\right)_{round(0.5)}. \quad (10)$$

In both the equations, V_{SM} is the SM capacitor voltage. The round function rounds the real number to the closest available integer as per its decimal fraction. The conventional NLM method produces N+1 AC output waveform as shown in the Fig. 2. Where N is the number of SMs in either arm.

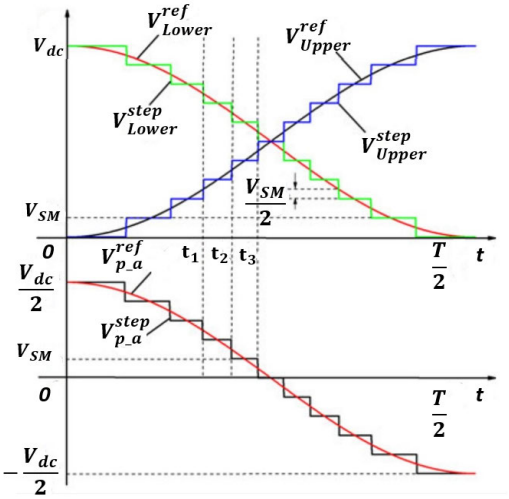

FIGURE 2. Conventional NLM method.

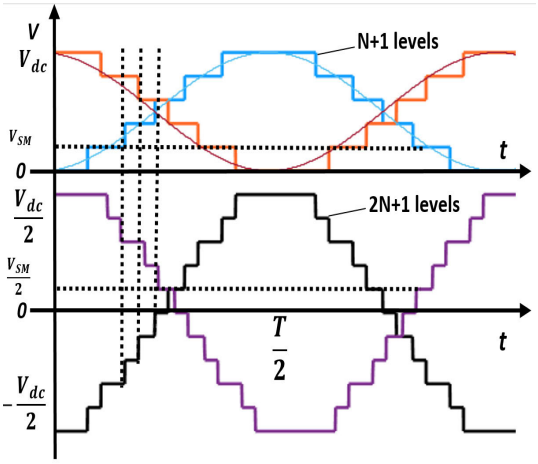

FIGURE 3. Modified NLC in FB SM for 2N+1 levels.

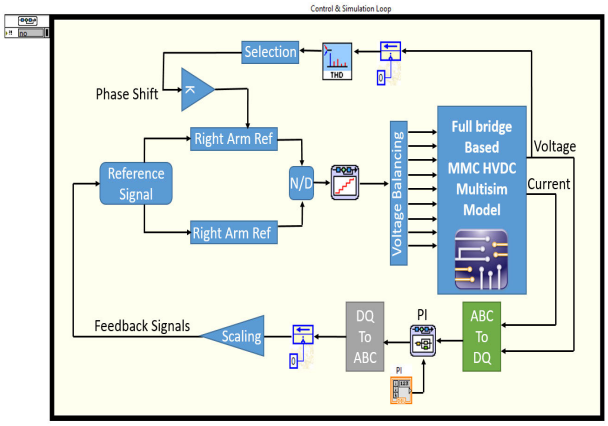

FIGURE 4. Modified NLC in LabVIEW for FB SM for 2N+1 levels.

IV. PROPOSED MODIFIED NLC

The proposed Modified NLC method for FB SM-based MMC is derived by adding a small phase shift in reference waveforms for the left and right arms of the FB SM. As shown in Fig. 1, the switches in the FB SMs are named S_{L1} and S_{L2} for the left arm and S_{R1} and S_{R2} for the right arm, respectively. The initial phase shift is introduced in the reference waveforms for all the FB SMs, as shown in Fig. 3. This phase shift produces 2N+1 AC output levels in voltage and current waveform.

$$V^{ref}_{right} = \frac{V_{dc}}{2}\left[1 - m\cos(\omega t + \propto)\right] \quad (11)$$

$$N_{right} = \left(\frac{V_{dc}}{2V_{SM}}\left[1 - m\cos(\omega t + \propto)\right]\right)_{round(0.5)} \quad (12)$$

The above equations (11) and (12) are used for the right upper and lower arm, and equations (7) and (8) are used for the left upper and lower arm of the FB MMC. The complete schematic layout of the Modified NLC for full-bridge is implemented in LabVIEW is shown in Fig. 4.

As shown in the above closed-loop LabVIEW program, three-phase voltage and current are measured and feedback to generate the reference signal for Modified NLC. The reference signal for right and left arm are then generated, and a phase shift is added in either of the respective arm (right arm in our case). The control signals are then generated and sent to the voltage balancing algorithm to select respective FB SMs. To extract the required phase shift i.e. value of the angle $\propto$, the THD of the voltage is measured and dispatched to the selection block containing previous and current value of THD. If the previous THD is less than the current value, the phase shift is retained to its previous value, otherwise the phase shift is increased by some value. To ensure the minimum THD, the phase shift is not kept constant but it is varied between 9.5 to 11 degrees, where optimum value of angle $\propto$ lies.

Moreover, to produce 4N+1 AC output levels, more phase shift is introduced in half of the SMs of the upper arm and half of the SMs in the lower arm of FB based HVDC MMC. The complete process is further illustrated in Fig. 5. When the controller achieves a stable value of the angle alpha, the levels are raised from 2N+1 to 4N+1 by inserting a small phase shift for half of the SMs in the upper and half of the SMs in the lower arm.

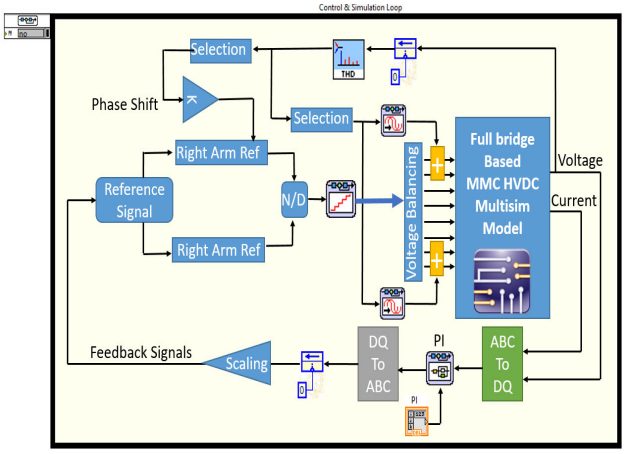

FIGURE 5. Modified NLC in LabVIEW for FB SM for 4N+1 levels.

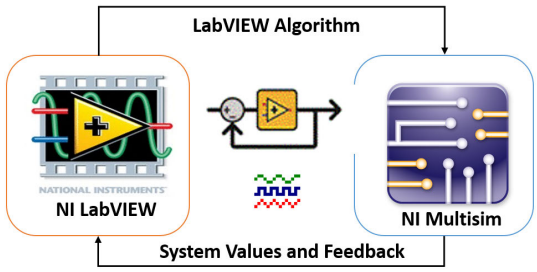

FIGURE 6. LabVIEW multisim co-simulation method.

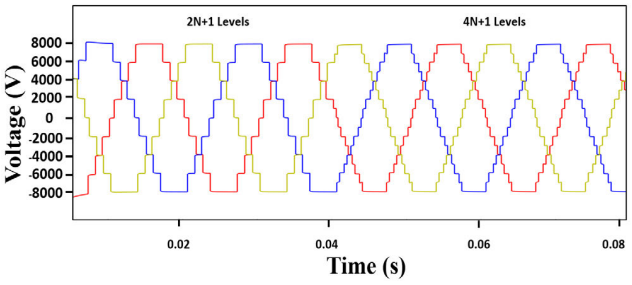

FIGURE 7. Three-phase output voltage with 9 levels and 17 levels.

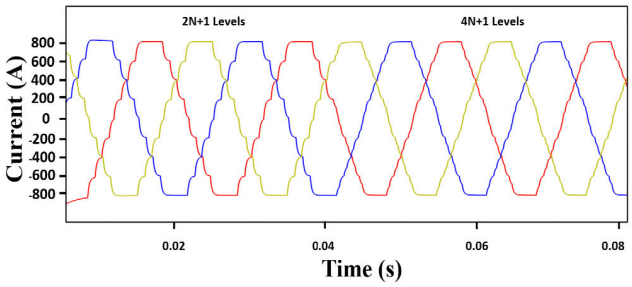

FIGURE 8. Three-phase output current with 9 and 17 levels.

V. LabVIEW MULTISIM CO-SIMULATION RESULTS

To validate the simulation results, LabVIEW Multisim Co-simulation is carried out, as shown in Fig. 6.

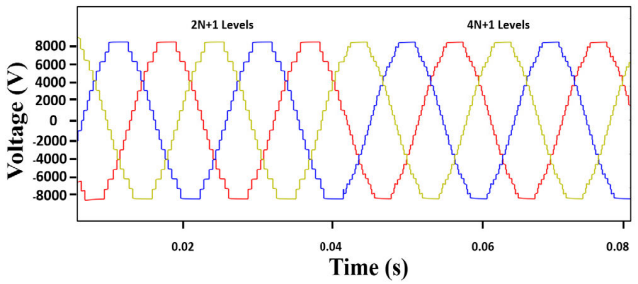

FIGURE 9. Three-phase output voltage with 17 and 33 levels.

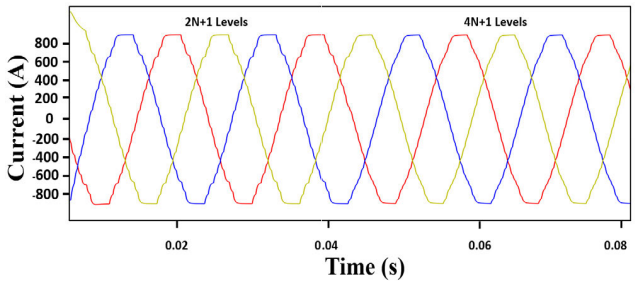

FIGURE 10. Three-phase output current with 17 levels and 33 levels.

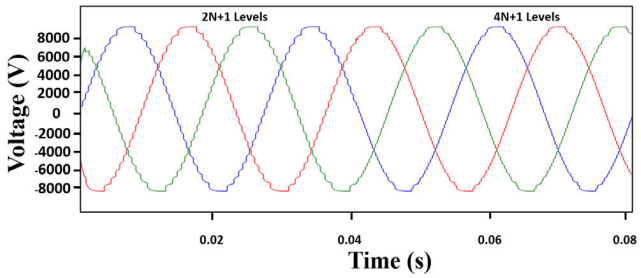

FIGURE 11. Three-phase output voltage with 23 and 49 levels.

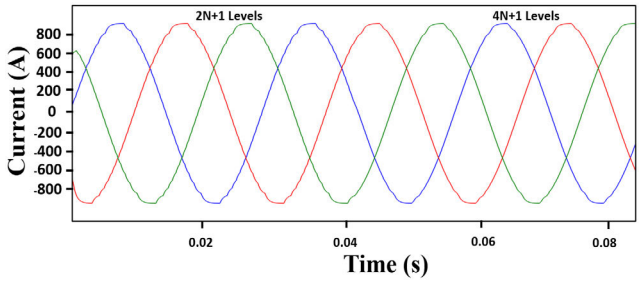

FIGURE 12. Three-phase output current with 23 and 49 levels.

Modified NLC is designed in LabVIEW, and MMC circuit is designed in Multisim. Both modified and conventional NLM method is designed in LabVIEW and activated to verify the proposed algorithm. Different AC output levels have been simulated to observe the behaviour and effectiveness of the Modified NLC.

The system parameters are shown in table 1, and simulation results are compiled using different FB SMs in the arm, such

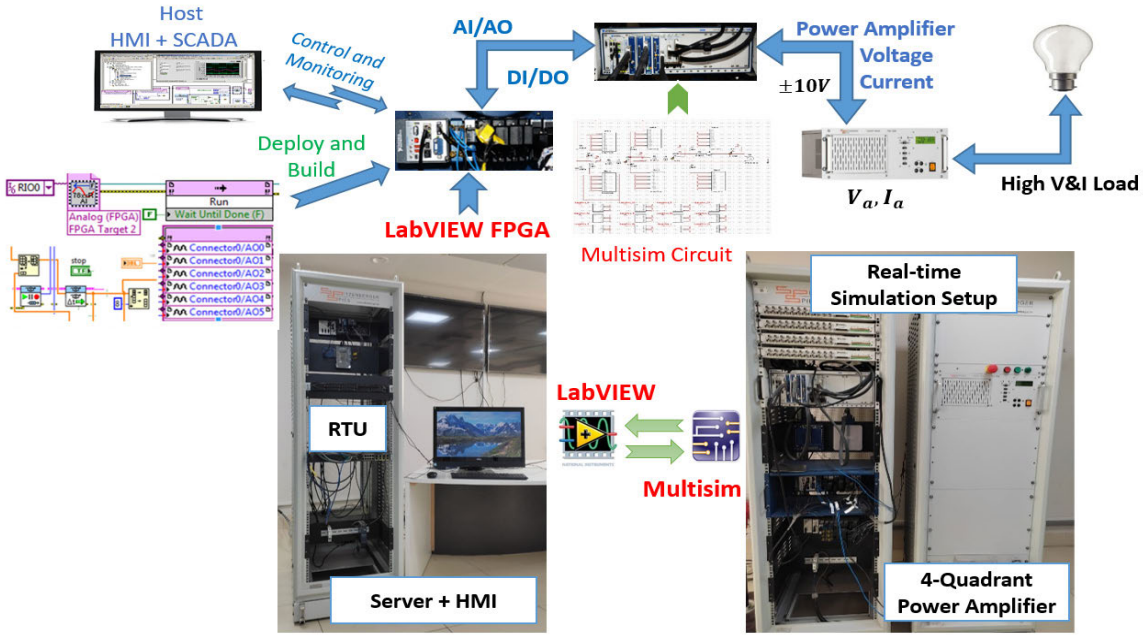

FIGURE 13. Real-time simulation Setup for result verification.

TABLE 1. Conventional and modified NLM in terms of THD.

Item No	Parameter	Value
1	Nominal Power	15 MVA
2	Grid Voltage	4.2 kV
3	DC Link Voltage	10 kV
4	System Frequency	50 Hz
5	SM Voltage	2 kV
6	SM capacitance	5000uF
7	Arm Inductance	5mH

TABLE 2. Conventional and modified NLM in terms of THD for offline simulation.

SMs	Conventional NLM % THD		Modified NLM % THD	
	Current	Voltage	Current	Voltage
4	6.36	9.50	3.14	4.71
8	3.17	4.60	1.57	2.21
12	1.52	2.19	0.80	1.09

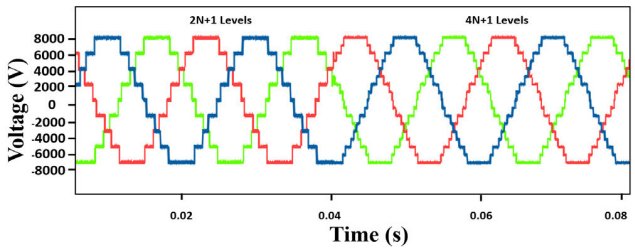

FIGURE 14. Three-phase output voltage with 9 and 17 levels.

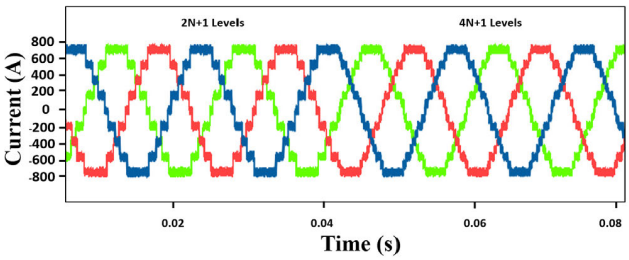

FIGURE 15. Three-phase output current with 9 and 17 levels.

as 4, 8, and 12, to obtain different AC output levels. It should be noted that prior to 0.04 seconds, conventional NLM is activated. It generates 2N+1 level AC output waveform, having 9.5% voltage THD and 6.36% current THD as shown in Fig. 7 and Fig. 8. Modified NLM is activated after 0.04 seconds. Modified NLM produces 4N+1 level and generates high-quality AC waveforms closed to the reference sinusoidal waveform. Therefore, Modified NLM has improved power quality and reduced harmonic content as compared to conventional NLM. THD of the voltage and current reduces to 4.71% and 3.14%, respectively in modified NLM. The results are further shown from figure 9 to 12 and compared in Table. 2 for the different number of levels.

VI. REAL-TIME SIMULATION RESULTS

The setup for real-time simulation is shown in Fig. 13. The three-phase MMC circuit designed in Multisim is loaded in NI PXI, an FPGA-based floating-point solver that creates a bit file of the circuit and runs it at nanoseconds on FPGA.

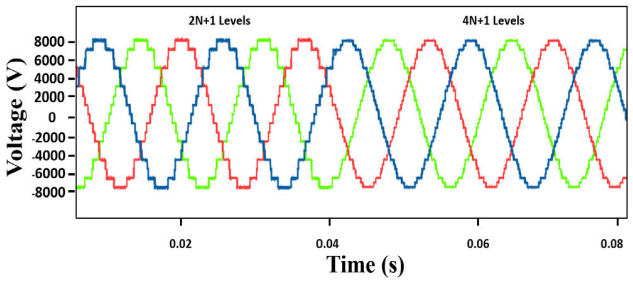

FIGURE 16. Three-phase output voltage with 17 and 33 levels.

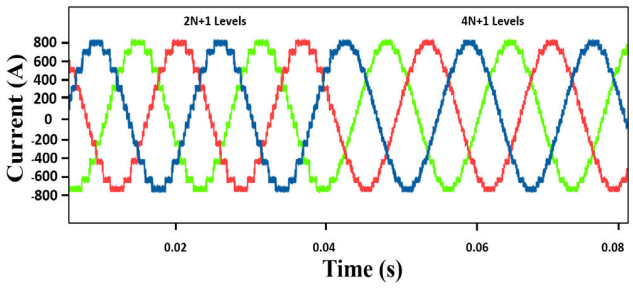

FIGURE 17. Three-phase output current with 17 and 33 levels.

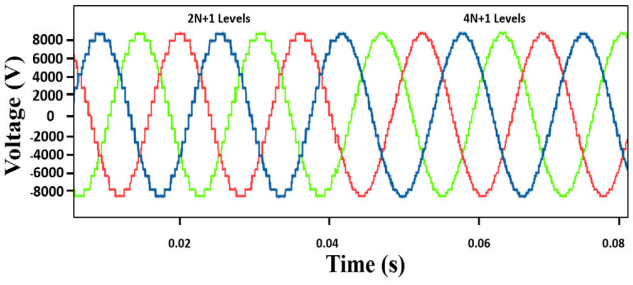

FIGURE 18. Three-phase output voltage with 23 levels and 49 levels.

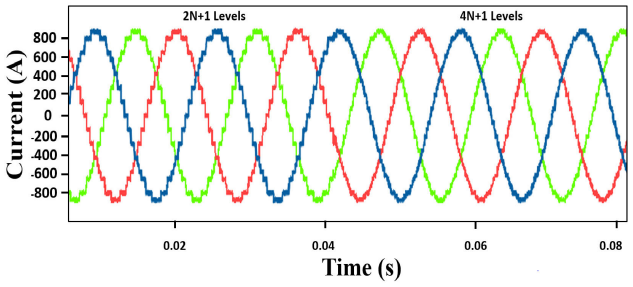

FIGURE 19. Three-phase output current with 23 levels and 49 levels.

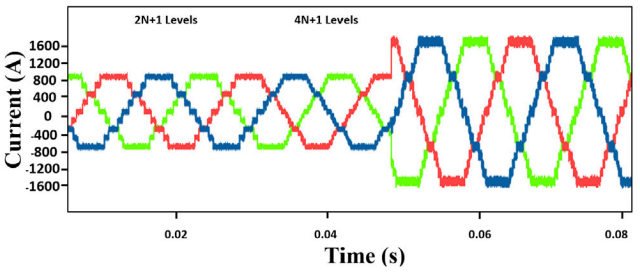

FIGURE 20. Current waveform showing load variation with 9 and 17 output levels.

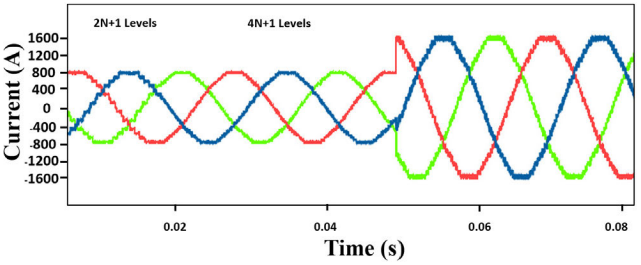

FIGURE 21. Current waveform showing load variation with 17 and 33 output levels.

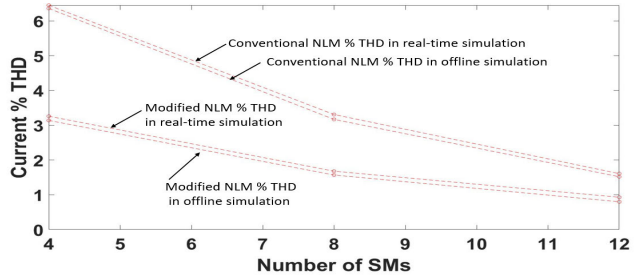

FIGURE 22. Current THD in offline and real-time simulation for modified and convention NLM.

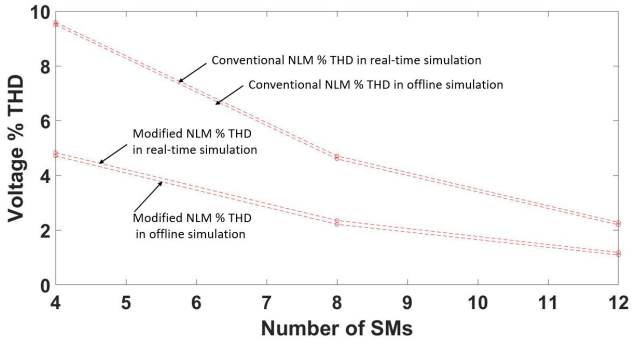

FIGURE 23. Voltage THD in offline and real-time simulation for Modified and convention NLM.

The early designed Modified NLC is then loaded on an FPGA-based Compact RIO controller to control the circuit running in PXI. The real-time simulation results are obtained from Figures 14 to 18. Conventional NLM is activated initially, and then the modified NLM is turn on at 0.04 seconds to achieve 4N+1 levels. The results are obtained and summarized in Table 3 for different number of AC output levels to show the effectiveness of the modified control. It should be noted that THD is reduced and the power quality is improved by increasing AC output levels as shown in Table 3. It can be seen from figure 14 to 19 that due to the step size of nanoseconds, ripples appeared in voltage and current. Therefore slight

TABLE 3. Conventional and modified NLM in terms of THD for real-time simulation.

SMs	Conventional NLM % THD		Modified NLM % THD	
	Current	Voltage	Current	Voltage
4	6.45	9.59	3.26	4.83
8	3.31	4.71	1.68	2.35
12	1.61	2.28	0.93	1.18

difference in THD for offline and real-time simulation can be observed. This slight difference is clearly shown graphically for current and voltage THD, considering offline and real-time simulation in Fig. 22 and 23 respectively. The load is also varied to validate the performance of proposed method. The results are shown in Fig. 20 and 21 for different number of AC output levels.

VII. CONCLUSION

Compared to previously presented Modified NLM, which was only confined to HB SMs in HVDC MMC, the Modified NLM method is developed and applied for Full Bridge MMC configuration in this paper. The Modified NLM is simple to implement and produces 4N+1 AC output levels. The method is initially verified with offline simulation using LabVIEW Multisim co-simulation and later executed in NI PXIe for real-time simulation and verification of results. Finally, the results are compared for both offline and real-time simulation in terms of THD.

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