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Bi-Directional Benes With Large Port-Counts and Low Waveguide Crossings for Optical Network-on-Chip

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ABSTRACT We propose a new variant of the Benes network using a merge-replace-fold approach. It is to realize a large port-count optical switch with low waveguide crossings. A bidirectional switch is built instead of a unidirectional switch. Compared to the classical Benes, it requires the same number of switches but far fewer intersections. The novel designs enable a 24-percentage reduction in waveguide intersections. Moreover, it has a worst-case insertion loss of 12.01 dB and a comparable crosstalk level of −13.67 dB between the neighbouring paths. Thus, it offers an energy-efficient way to solve the optical on-chip design problem in a bidirectional manner.

INDEX TERMS Optical interconnections, optical NoC, silicon photonics, optical resonators, optical switches.

I. INTRODUCTION

To handle the network society traffic, robust data centers increasingly rely on unconventional inter-chip and intra-chip communication methods [1], [2]. Most current mature solutions use on-chip electrical networks. However, they are affected by severe problems such as implementation cost, power consumption and scaling. Silicon optical switches can overcome these limitations with a small footprint. They are compatible with electrically printed circuit boards and are easy to package. Thus, they likely would find more widespread deployment in on-chip optical interconnect network [3]–[5].

However, no feasible solution is available to eliminate the insertion loss and crosstalk simultaneously [3]. Currently, the most advanced large-scale architectures include Switch-and-Select [6], Benes [7], [8], Clos-Benes [9], PILOSS [10], Spanke–Benes [11], and Fat-tree [12], [13]. Among these methods, the Benes method is a promising technology as it eliminates insertion loss with the least number of optical switches [14]. Additionally, it has an acceptable crosstalk level because it has a moderate number of sources [15]. Hence, the Benes method is widely used in current high-port-counts switching fabrics.

It is challenging to achieve a high port-count Benes on a single chip. When connecting the paths, the waveguide intersections will increase excessively with the Benes' size; hence, the first-generation Benes fabric will be limited [15]. The second-generation switching fabric [16] is seeking optimal operating points through a very limited number of built-in power monitors. The 32×32 switch has compressed insertion loss and crosstalk to 18.5dB and −15.1dB, respectively. However, in many studies, it causes significant on-chip losses; hence, further developments are required.

Inspired by this, bi-directional Benes with large port counts and low waveguide crossings is proposed for optical network-on-chip. The vision of a bidirectional network is no longer a switch with bidirectional ports alone. But a theory of building a bidirectional network through small bidirectional components. One may argue that Benes could put the input

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and output ports together. The rationale behind this approach is still the same. It exploited the unidirectional switches to realize an extensive unidirectional network.

Resolving the inconsistency between bidirectional components and large unidirectional networks is still critical. In the traditional Benes, this inconsistency is characterized by disordered ports. It exacerbates intersection issues and becomes the main contribution of waveguide losses [15]. This disorder can lead to hundreds of intersections, in the case of the network size, as low as just sixteen intersections [16]. For this reason, we propose a merge-replace-fold method to address this issue. For the first time of our knowledge, we offer a solution in a bidirectional manner.

In this article, we have addressed this issue in a bidirectional manner. It all used bidirectional elements. They include bidirectional switches, links, ports, and the bidirectional method named merge-replace-fold. The benefit of the approach is to reduce the size and the number of intersections of the switch. As a result, the optical loss is minimized while the crosstalk level is acceptable. Also, the ports may be equipped with a dedicated converter. It makes the structure adapt to the unidirectional world. The ultimate expectation is to change the unidirectional switch with the bidirectional concept. Thus, it is of paramount importance to develop solutions for future on-chip optical networks.

This paper has five sections. Section II introduces the primary building blocks and discusses preliminary work. Section III presents the Bi-directional Benes (Bi-Benes) principle. Also, the non-blocking algorithm and port converter design are presented. Section IV is the simulation results and discussions. Finally, Section V concludes the paper.

II. PRIMARY BUILDING BLOCKS AND PRELIMINARY

A. PRIMARY 2 × 2 SWITCH AND 4 × 4 SWITCHES

Before describing the proposed switching fabric, we first introduce the 2 × 2 optical resonator switches used as the building block of all switching modules presented hereafter [17], [18]. It comprises two parallel waveguides and a single-ring resonator between waveguides. As shown in Fig. 1, it has two input ports (1 and 2) and two output ports (1' and 2'). The incident light and the ring resonator have the same frequency in each state. When the rings were switched off in the low-absorption condition, the switch is in the "cross" state. Subsequently, the two incoming lights are directed from 1 and 2 to 2' and 1', respectively. When the ring resonators are switched on in the high-absorption condition, the switch is in the "bar" state. The two incident lights are switched from 1 to 1' and from 2 to 2'. Hence, the optical resonator switch behaves as a 2 × 2 switch [19].

We use the same definition as that in [20]. At first glance, the state definition may seem counter intuitive. One can understand state definitions either from resonator properties or switch functions. Note that they exhibited the opposite state's explanation. In general, the cross-state switch implies that one can swap output ports. The bar-state switch means that the port keeps its original direction and does not change.

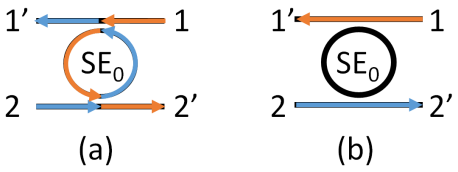
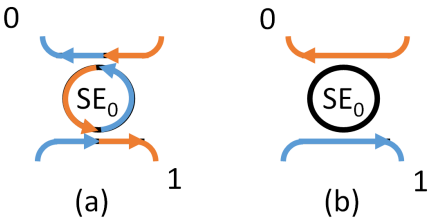


FIGURE 1. Optical resonator switch: (a) "Cross" state (b) "Bar" state.

Keep this definition in mind. It can help readers gain a better understanding of the subsequent network-level simulations.

Then, we introduce the first switching element (SE), as shown in Fig. 2. Unlike the switch mentioned above, they have added bends on both sides of the input and output, successfully switching the input and output ports from horizontal to vertical. Fig. 2(a)-(b) show two simplified forms of the same 2×2 switch. Their switching function is the same as that shown in Fig. 1. A control unit is used to switch each SE and state. It can change and activate SE conditions according to flow routing requirements [21]. Fig. 2(c) shows the simple logic, which helps map the traditional building block to a simplified form.



(c)

No.	1	2	1'	2'
#1	-	-	0	1

FIGURE 2. Basic 2 × 2 optical switching element: (a)-(b) Simplified form, (c) simple logic.

Let us consider a simple logic in three subsequent steps. First, the routing algorithm assumed in this article does not use the exact location of the input port but rather the output port. It implies that the input port symbols are not useful that we can remove them. Second, once the propagation direction is known, the bidirectional links can distinguish the output from input ports. It means that we can mark the location and the name above any link. Third, the symbol is simplified to serve the subsequent routing algorithm. We use 0,1,0',1' to mark the output port, where 0,1 represents the output of SE_1, and 0',1' represents the output of SE_2.

In subsequent sections, we will find that the position of the two-port switch is unique. It only appears in bridging the path from one half of the network to the other half. The effect is to change the signal path from horizontal to vertical.

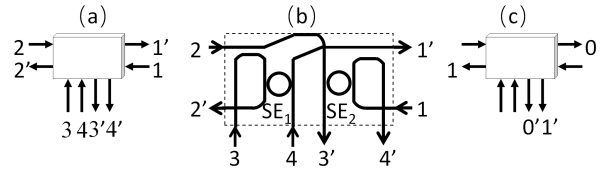
Fig. 2 is chosen to replace Fig. 1. The purpose is to ensure the consistency of the transmission results between Bi-Benes and traditional Benes. Conceptually, recall that the outcome of Cross is to allow the port to be swapped. In comparison,

the role of Bar is to enable the port to continue its original direction.

Although Fig. 1 has the same function and lower insertion loss. The results of the bar and cross states are precisely the opposite of the expectations mentioned above. For instance, in the all-Bar case, we will always observe an exchanged signal at the receiver end. In the network-level simulation, this will cause the results of all-Bar and all-Cross to be inconsistent with traditional transmission results.

Another core component in our switching fabric is the 4 × 4 optical switch. Our idea is to use bidirectional switches instead of unidirectional optical switches. Therefore, the switch is bi-directional; that is, the input port i and the output port i' are placed together, where $i = 1,2,3$, and 4. Traditionally, the 4 × 4 switch can achieve $4! = 24$ complete permutations. Compared with a traditional router, the 4 × 4 optical switch used in this study is much simpler, where only four switching functionalities are required, namely {*bb*, *bc*, *cb*, *cc*}. It comprises a collection of waveguides and uses two identical 2 × 2 SEs. It serves as add/drop switch or cross-connect switches. In this article, we present two types of optical routers in four different manners.

The first type of 4 × 4 switch module is known as the add/drop module. It has only one manner, as shown in Fig. 3(a)-(c). A transparent 4 × 4 add/drop module is presented. If any add port or drop port is idle, then this signal can always identify a path to establish an optical path with the traversed links. Their switching functionalities, the states of SEs, and simple logic are shown in Fig. 3(d)-(f), respectively. The control unit realizes all switching functions. They include establishing an optical path and maintaining the optical paths [22], [23].



(d)

No.	States of SEs
#1	cc
#2	cb
#3	bc
#4	bb

(e)

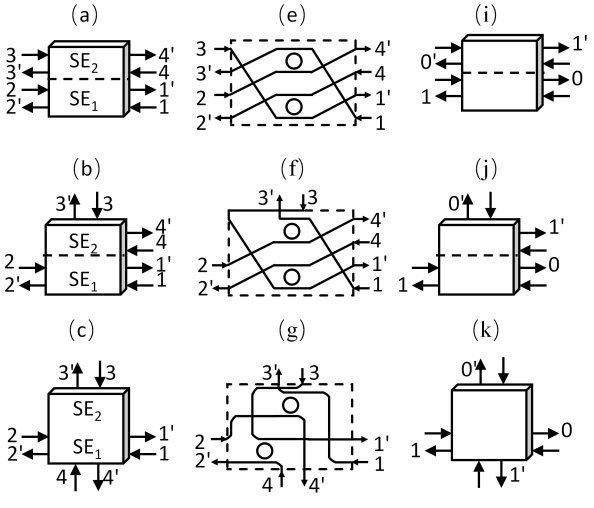
No.	1	2	3	4
#1	3′	4′	1′	2′
#2	4′	3′	1′	2′
#3	3′	4′	2′	1′
#4	4′	3′	2′	1′

(f)

No.	1	2	3	4
#1	-	-	-	-
No.	1′	2′	3′	4′
#2	0	1	0′	1′

FIGURE 3. 4 × 4 transparent add/drop module. (a) ideal building block, (b) functionality, (c) implementation form, (d) states of SEs ("cross" or "bar"), (e) simplified form, and (f) simple logic.

The second type of a 4 × 4 switch module is known as the cross-connect module. It comes in three different manners, as shown in Fig. 4 (a)-(c). When the port count is below eight, only one type of module is shown in Fig. 4(a). Fig. 4(b) and Fig. 4(c) did not appear in the network until the port count reaches 16 and 32, respectively. They differ by the direction



(d)

No.	1	2	3	4
#1	3′	4′	1′	2′
#2	4′	3′	1′	2′
#3	3′	4′	2′	1′
#4	4′	3′	2′	1′

(h)

$SE_{2\text{-}1}$	(e)	(f)	(g)
#1	bb	bb	bb
#2	cb	cb	cb
#3	bc	bc	bc
#4	cc	cc	cc

(l)

No.	1	2	3	4
#1	-	-	-	-
No.	1′	2′	3′	4′
#2	0	1	0′	1′

FIGURE 4. 4 × 4 contention-less cross-connect modules. (a)-(c) ideal building blocks, (d) functionalities,(e)-(g) implementation forms, (h) states of SEs ("cross" or "bar"), (i)-(k) simplified forms, and (l) simple logic.

and names of the optical traversed links. This attribute is known as the contention-less behavior in a center line manner. We can switch the ports above the center line to the ports below the center line without contention. Similarly, their switching functionalities, implementation forms, the states of SEs, simplified forms, and corresponding logic are shown in Fig. 4(d)-(l), respectively.

Indeed, there are some bends in each module. Through careful design, one can make the optical loss and crosstalk even better. The challenge is twofold. It is widely known that sharp bending with a radius less than 5μm will cause a significant loss. At the same time, macro bending will increase the size and loss. Thus, we adjusted it within the range of 5-12μm. When it is near 9.2μm, the response flattens most with no ripples in the software.

The same radius is applied for all bends throughout this article. To avoid excessive loss, we avoided the 180-degree turns in our design. Instead, we can replace it with two 90-degree turns and a section of the straight waveguide. Later, we will discuss the issue of cascaded bends in Section IV. A lot of work [24], [25] has discussed effective bends and their technical difficulties. There is no doubt that these extensions will provide better performance. But the deployment of this technology is beyond the scope of this work.

B. PRELIMINARY

Conventionally, the Benes network comprises three stages: the input, intermediate, and output stages. The $N \times N$ switching fabric contains $2\log_2 N - 1$ stages and $N/2$ switches in

each stage [26]. As mentioned earlier, the Benes method is considered a promising technique as it can minimize the insertion loss with the least number of 2×2 switches. Correspondingly, because the noise source is the least, the crosstalk is significantly reduced.

However, when connecting the paths, the waveguide crossings overgrew with the size of the Benes [27]. The term "crossing" and "intersection" are used interchangeably in this article. The crossings were induced by the perfect shuffle method. The shuffle and reverse shuffle methods shifted the order of inputs in the next stage of the outputs from the previous stage, enabling the inputs (1,2,. . .,*N*) to be rearranged into outputs (1, *N*/2+1,2,*N*/2+2,. . .,*N*/2,*N*), and vice versa. Therefore, it is imperative to develop a switch fabric with a high port-count but avoid waveguide intersections.

III. BI-DIRECTIONAL BENES METHOD

This section first describes the general method to transfer the uni-directional switch to the bi-directional switch. Then, we address the further intersection problem by a multi-layer approach. The details of the non-blocking routing algorithm are also described. Finally, we give a method to change from a bidirectional input and output ports back to uni-directional.

A. N×N SWITCHING FABRIC

To solve the challenges of intersections, we envisioned a bidirectional switching fabric, see Fig. 5. They are used to illustrate the mapping from Benes to our new structure. The first structure is a unidirectional network. Signals travel only in one direction (left to right). The second structure is the traditional Benes decomposition method. The third structure is our bi-directional Benes decomposition method, and the fourth structure is our final resulting bidirectional network.

We focus on the transition from the second structure to the third structure to illustrate the one-to-one mapping from Benes to our new design. Using the generalized method, we can introduce changing the existing unidirectional Benes to bidirectional Benes. The main target is to maintain the switching connectivity while reducing the waveguide crossings in the topology.

B. MERGE-REPLACE-FOLD METHOD

1) Merge the input and output module with the add and drop module. Four variables are used to label a conventional 2×2 SE. Assume that input module $(2i-1)$ has four ports $\{2i-1, 2i, N+2i-1, N+2i\}$, where $i = 1,2,\ldots,N/2$. Assume output module $(2i)$ has four ports $\{5N+2i-1, 5N+2i, 6N+2i-1, 6N+2i\}$, where $i = 1,2,\ldots,N/2$. Subsequently, these modules are merged as $\{2i-1, 2i\}$, which contains eight ports. For the add and drop functions, ports $\{2i-1, 2i, 6N+2i-1, 6N+2i\}$ are used. For the cross-connect functions, ports $\{5N+2i, N+2i, N+2i-1, 5N+2i-1\}$ are used.
2) Replace two intermediate subnetworks from unidirectional to bidirectional. Conventionally, two $N/2 \times N/2$ modules are in the intermediate stages. The first module has only one direction, from $\{2N+1, \ldots, 2N+i+1, \ldots, 5N/2\}$ to $\{3N+1, \ldots, 3N+i+1, \ldots, 7N/2\}$. The second module has only one direction, from $\{5N/2+1, \ldots, 5N/2+i+1, \ldots, 3N\}$ to $\{7N/2+1, \ldots, 7N/2+i+1, \ldots, 4N\}$. In our proposal, they are changed to the bidirectional form. The first module has bidirectional directions, with $\{\{3N+1, 2N+1\}, \ldots, \{3N+i+1, 2N+i+1\}, \ldots, \{7N/2-1, 5N/2-1\}\}$ and $\{\{2N+2, 3N+2\}, \ldots, \{2N+i, 3N+i\}, \ldots, \{5N/2, 7N/2\}\}$. The second module has bidirectional directions, with $\{\{5N/2+1, 7N/2+1\}, \ldots, \{5N/2+i, 7N/2+i\}, \ldots, \{3N-1, 4N-1\}\}$ and $\{\{7N/2+2, 5N/2+2\}, \ldots, \{7N/2+i+1, 5N/2+i+1\}, \ldots, \{4N, 3N\}\}$. In addition, their locations change from the south-north direction to the east-west direction. The second module is on the left, whereas the first module is on the right.
3) Fold back the input links and merge them with the output links to obtain a bidirectional link. In the traditional method, input module $2i-1$ has two connecting paths from ports $\{N+2i-1, N+2i\}$ to ports $\{2N+i, 5N/2+i\}$. By contrast, output module $2i$ has two connecting paths from ports $\{3N+i, 7N/2+i\}$ to ports $\{5N+2i-1, 5N+2i\}$. In our proposal, the add/drop module $\{2i-1, 2i\}$ transmits the signal from ports $\{N+2i, N+2i-1\}$ to ports $\{5N/2+i, 2N+i+1\}$. Subsequently, it receives signals from ports $\{7N/2+i, 3N+i+1\}$ through the $\{5N+2i, 5N+2i-1\}$ ports. After these three steps, we changed the unidirectional structure to a bidirectional design.

C. SWITCH TOPOLOGIES STUDY

Understanding the above-mentioned $N \times N$ theory is still only half of the picture. In essence, our network belongs to a multi-layer structure, and its decomposition process includes three steps. First, using the *N*-port theory, replace the input and output stages with add/drop modules. Second, replace the intermediate stage with a cross-connect module and a two-port module with bends. We discuss their functions in the previous section. Finally, when there are fewer than eight ports, all the waveguides are placed on the same layer. When the subsequent ports are increased by four times, the network is increased by one layer.

Fig. 6 gives a 32-port example. We added two intermediate steps to illustrate the merge-replace-fold method. Fig. 6a shows a conventional recursive Benes structure, which repeated the Benes principle of Fig. 5b twice. We use three tags (i, j, k) to represent the address of the module. Here, i is the module address, j is the direction address, and k is the port address. The input symbols are not entirely useless. As an intermediate step, it explains their one-to-one correspondence between the subsequent steps. Fig. 6b represents the merge-fold process. The principle of Fig. 5c is used twice to make the outermost layers suitable for bidirectional design. We used simple logic to remove the labels of the

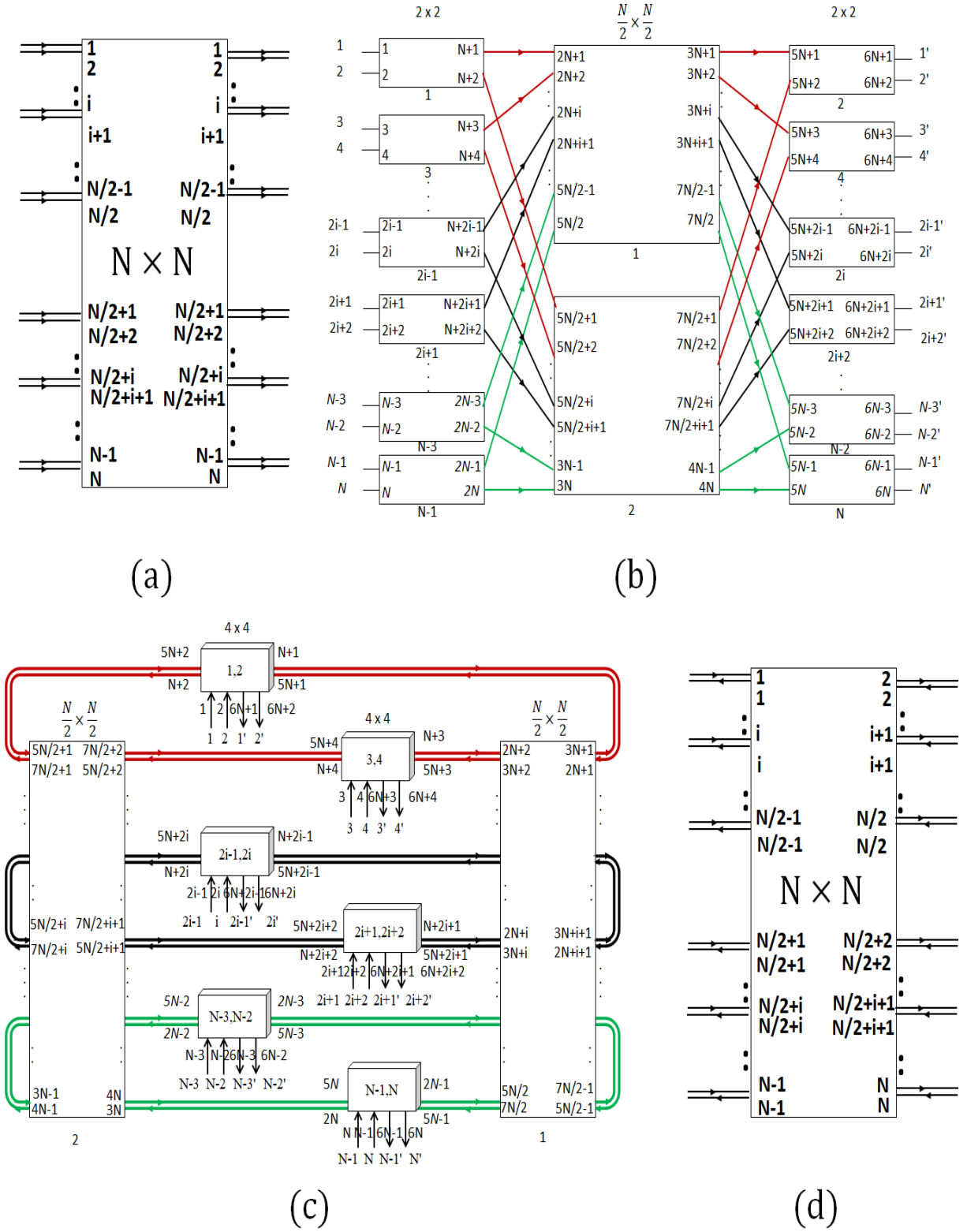


FIGURE 5. Four $N\times N$ optical switching fabrics. (a) unidirectional $N\times N$ network, (b) the traditional Benes network, (c) the ring-based network, and (d) bidirectional $N\times N$ network.

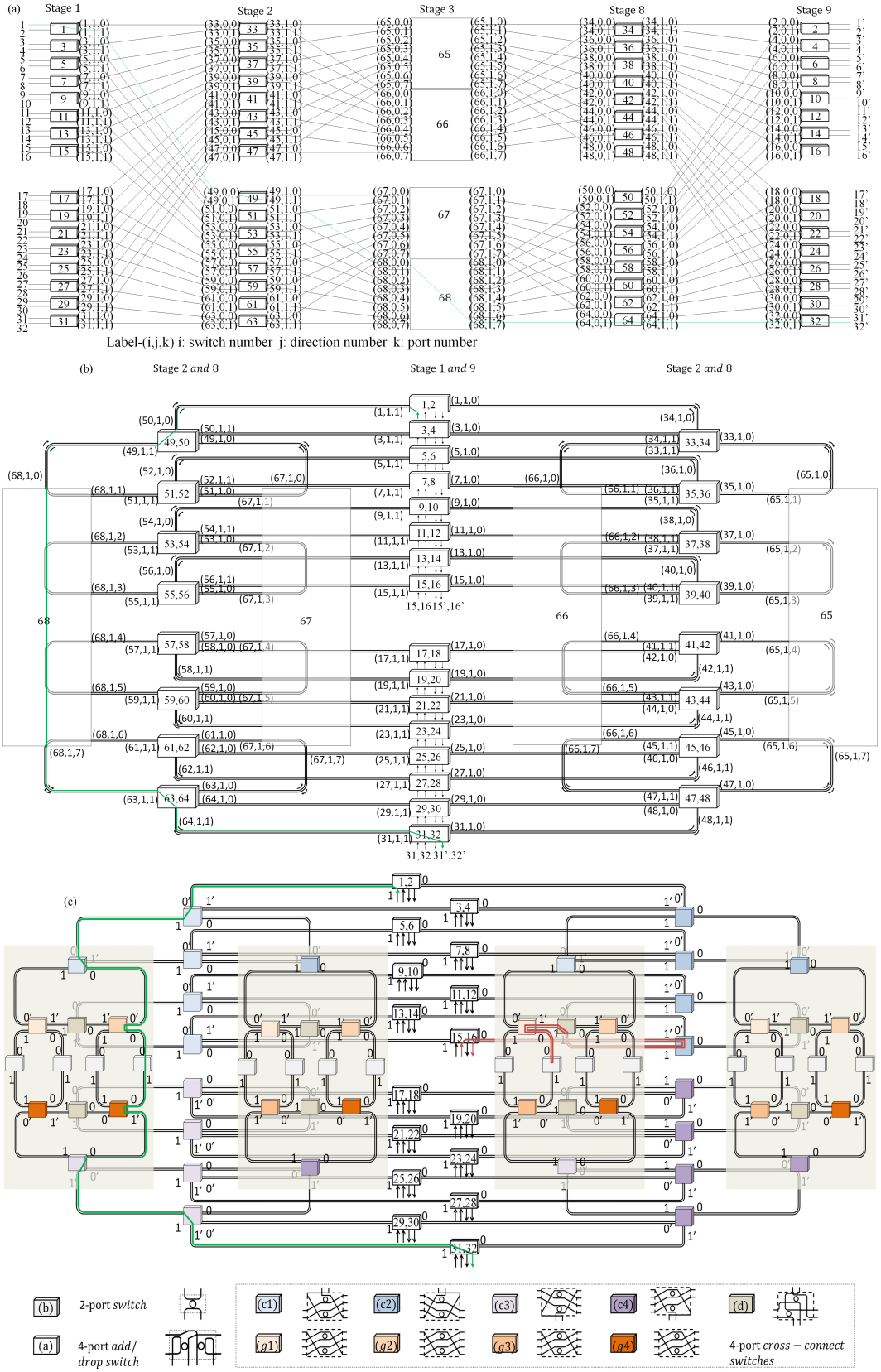


FIGURE 6. (a) Recursive Benes, (b) Merge and fold method, (c) Merge-replace-fold method. The red and green lines represent the shortest path and the longest path from 16 to 16′ and from 1 to 32′, respectively.

TABLE 1. Comparison between three types of Benes.

Case	Benes [28]	Benes [8]	Bi-Benes
♯of SEs	$N\log N$-0.5N	4$N\log N$-2N	$N\log N$-0.5N
♯of intersections	2N^2-$N\log N$-2.5N	2N^2-$N\log N$-2.5N	3$N\log N$-N
♯ of intersections along a path	2N-2log$N$-2.5N	2N^2-$N\log N$-2.5N	3log$N$-1
♯of bends along a path	-	4log$N$-2	2log$N$-2

TABLE 2. Time and space complexity of the routing algorithms.

Algorithm complexity	Time in serial/in parallel	Space
Work-efficient algorithm [26]	$O(N\log N)/O(N)$	$O(N\log N)$
Looping algorithm [31]	$O(N\log N)/O(\log^2 N)$	$O(N)$

input ports. Finally, Fig. 6c shows the whole picture of the merge-replace-fold method, which replaced the intermediate module with 8 × 8 switches.

It is worth mentioning that our topology advantage is not obvious in the case of small ports. For example, the total number of intersections we have achieved is the same as the traditional Benes for the eight-port situation. There are 16 crossings in the topology and 20 crossings in the switches, so there are 36 crossings in total. A new schematic of the 8 × 8 non-blocking photonic switch reduces the waveguide crossings to zero. However, it uses $6\times4.3\times4=36$ crossings, which equals that of the traditional Benes.

As the number of ports increases, our topological advantage begins to be significant. For example, we analyze the intersections in a 32-port switch. The conventional Benes network includes nine stages and 144 two-port small switches. It results in $\sum_{K=1}^{log_2(N)} 2^{(K-1)}(2^K-1)=416$ waveguide crossings in the topology, requires no waveguide bend, and contains $Nlog_2N-N/2=144$ waveguide crossings inside owing to the 2×2 switches. Hence, there are a total of 560 waveguide crossings. Our design uses a total of 32 rings, as well as 16, 4 × 4 add/drop switches, 48, 4 × 4 cross-connect switches and 16, 2 × 2 switches. A part of the 8 × 8 module is built on top of the double-layer chip. It results in 8 × 4.32 waveguide crossings in the topology, creates 32 × 8.10 = 25.6 waveguide crossings due to bends, and results in 56 × 6.8×4 = 368 waveguide crossings inside. In this way, the intersections reduces from 560 to 425.6, around 24% of the reduction.

Table 1 compares three Benes networks in switching elements, intersections, and bends along a route. The advantage of our structure is evident. It minimizes the number of SEs and crossings simultaneously. In specific, it reduces the total intersections from $O(N^2)$ to $O(N\log_2 N)$, where $O(N\log_2 N)$ denotes the number of 4 × 4 switches. The penalty is to increase the bends along the path by $O(N)$.

For the 32-port switch, the design area is estimated at around 2.90 × 2.17mm^2. While our structure has a compact size, this necessitates a multi-layer design. Note that two interface designs are used most. First, the add/drop module must realize the coupling from one plane to another. Second, the cross-connect modules use a polarization-insensitive adiabatic coupler. It changes direction from the horizontal of a plane to the vertical part. The former could use an overlay junction [6], while the latter could be found [29]. Thus, the four-port modules will not cause technical problems when adding layers.

Unlike the previous work [30], the optical switch works at a single wavelength, and all resonators have the same resonant wavelength. Due to the cyclic filtering characteristics of resonators, we can choose the best resonant wavelength as the working wavelength in many free spectral ranges (FSRs), which will be discussed in subsequent sections.

D. NONBLOCKING ROUTING ALGORITHM

In principle, our network satisfies the Benes network's conditions so that it is rearrangeable non-blocking. It points out that the number m of intermediate stages should not be less than the input port n each time it is decomposed. In our design, m is equal to $n=2$ in each decomposition. Hence, it provides full connectivity to each pair of ports. An additional advantage of using the Benes network is its low end-to-end latency. This depends on the number of hops in the Benes network, $O(\log N)$.

The path diversity in Benes topology is enormous, $2^{N^2 logN}$. Its routing problem is a variant of the edge-coloring problem. Traversing all paths are unbearable, and it will significantly increase the space and time complexity. To solve this problem, Table 2 discusses two efficient algorithms [26], [31]. The $O(N\log N)$ time penalty indicates that we can find all solutions in a reasonably short time. Table 3 presents a pseudo-code of the routing algorithm; more details are in [26]. After testing, we measured that the running time of the 32-port network is short, only 0.006μs, which will not pose a bottleneck in configuration. The simulation environment is a Windows workstation that has an Intel-Xeon 3.1GHz CPU and 64G RAM. The following example is going to verify the effectiveness of the algorithm.

Assume that the point-to-point requests are {(1, 4, 3, 2, 7), (5, 8), (6)}. The three path-searching steps involved are as follows, see Fig. 7. First, n-bit preambles are generated, where $n=2N\log_2 N-1$. The most critical first m preambles are acquired with a work-efficient scheme,

TABLE 3. The pseudo-code of the work-efficient algorithm, where $n = \log N$.

Work-efficient Algorithm [26]	**Looping algorithm** [31]
Input: N-port permutation	**Input:**N-port permutation
Output: n-arrays of Preambles permutation	**Output:** two-arrays of Preambles
1: Predefine a Matrix named R	**1:** For i=1; i<=n-1; i++ do
2: For i=1; i<=2logN-1; i++ do	**2:** Draw bi-color mappings.
3: Call looping algorithm to search ci,	**3:** Get two columns of the preambles ci.
4: Call Matrix balance to verify ci.	**4:** End for.
5: If verified then pass ci.	**Matrix balance algorithm** [26]
6: End for	**Input:** two-arrays of Preambles.
7: Convert Destinations to $B_1,\cdots,B_n$.	**Output:** Verified or not.
8: Collect matrix [C,B].	**1:** For i=1; i<=logN-1; i++ do
9: Configure ring resonators according to matrix.	**2:** Verify matrix balance condition ci.
10: Non-blocking paths established.	**3:** End for.

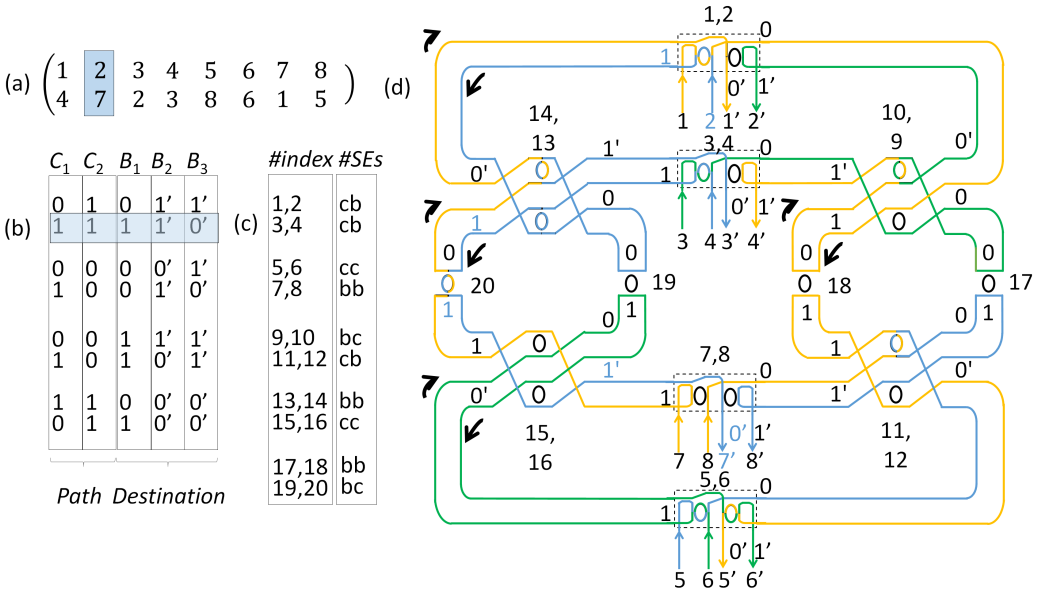


FIGURE 7. Three steps to calculate the path of the 8 × 8 optical switching fabrics. (a) requests, (b) 5-bit preambles, (c) the management of MRRs, and (d) simplified switching fabric and non-overlapping optical circuits upon requests.

where $m = N\log_2 N - 1$. The algorithm specifies the states of each 2 × 2 SEs, where '1' represents 'c' and '0' represents 'b'. The $N/2$ SEs on the same stage together form an array of the preamble. According to the switch states, some bits are flipped and swapped. Subsequently, m preambles are generated, including $\{C_1, C_2\}$. The subsequent n-m preambles are obtained directly, such as $\{B_1, B_2, B_3\}$. Decrease the destination address by 1, and then convert decimal to binary numbers.

Since our structure is different from the traditional structure, an additional step is required before using this preamble. Add ' to the last m preambles, such as $\{B_2', B_3'\}$. Second, the edges labels are deleted and all 4 × 4 and 2 × 2 modules are replaced with simplified versions.

When used as a wavelength selector, MRR operates with its resonance by tuning to a specific wavelength. Consider the example of Fig. 7. According to the calculation results, the management of the MRRs is executed, see Fig. 7(d). In the cross-state, MRR switches the input signal to another waveguide actively. MRR in the bar state allows the input signal to propagate along the input waveguide. Finally, optical paths are established using the preambles. Different colors indicate N paths. Non-overlapping paths simultaneously establish all-optical circuits.

E. PORTS CONVERTER DESIGN

Our design has a unique feature in that the add and drop ports appear in the middle of the structure. If this problem is not solved, it will generate new crossings that do not exist in the original design, offsetting the advantages of structural design. We proposed a simple yet effective method that is compatible with our design. In Fig. 8, we address this problem by changing bi-directional input and output ports back to uni-directional. Double-layer interconnection architecture is exploited to overcome the intersection problem caused by the input and output ports in the second layer. The penalty is an onboard loss of 4dB.

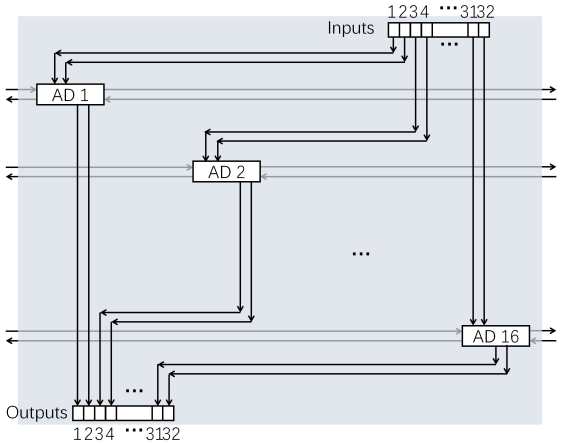


FIGURE 8. Port converter design of the 32 × 32 network.

IV. SIMULATION RESULTS

This section performs a series of the simulation with INTERCONNECT software. All parameters are summarized in Table 4. It is worth mentioning that most of the system parameter values are obtained from the series coupling example [32]. In particular, we collect the effective refractive index, group refractive index, and maximum attenuation from [32]. Next, the coupling coefficients are scanned and selected via the INTERCONNECT software. The goal is to realize the bar and cross functions as well as reducing loss and crosstalk.

TABLE 4. Parameters in Lumerical software. [32].

Case	Parameters
Bends radius	9.2 μm
Coupling efficient (Bar state)	$1 \times 10^{-4}/1 \times 10^{-4}$
Coupling efficient (Cross state)	$0.5/0.5$
Effective refractive index	4.306
Free spectrum range	17.3nm
Group refractive index	4.306
Maximum attenuation	300dB/m
Perimeter of rings	29.6181μm

The INTERCONNECT software can undoubtedly test the crosstalk of each module here. However, it seems inefficient to explore the details of all four-port modules. Recall that a 32-port switch uses 16 two-port small modules and 64 four-port modules. The four-port modules can be categorized as add/drop modules and cross-connect modules mentioned above. Those cross-connect modules can be further classified into nine groups, see Fig. 6(c). Each module is slightly different in terms of labels, input, and output ports. The performance of the network is often more appropriate than discussing the crosstalk of each module.

We develop and implement experiments in five steps. 1) The schematic diagram of the primary switch module is shown in Fig. 9. Our architecture uses it to build the entire network, see Fig. 6 (c). 2) The optical network analyzer (ONA) module is added from the component library. The effect

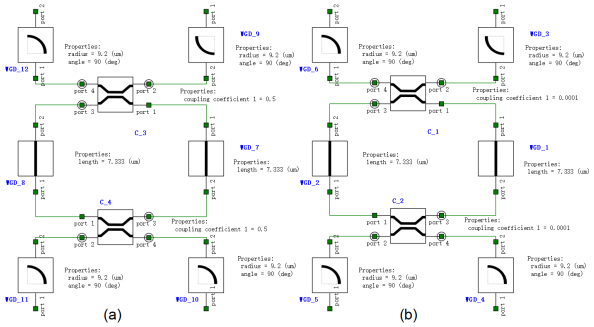


FIGURE 9. Experimental setup of the 2 × 2 switch with bends using INTERCONNECT: (a) cross and (b) bar.

of cascading extra waveguide bends is explored to select the appropriate operating wavelength. 3) A network-level simulation is conducted. The ONA generates a broadband spectrum. It records the transmission spectrum as a function of wavelength, giving an estimate of loss and crosstalk. 4) The data is modulated at 25Gb/s at 1594.41nm using an Mach-Zehnder interferometer modulator. A pulse pattern generator puts out a 2^7-1 pseudo-random bit sequence and then serves as modulator input. Evaluation is estimated based on the worst-case end-to-end link, i.e., the green link in Fig. 6 (c). 5) The maximum transmission waveguide lengths of 120nm and the loss of 4dB in the second layer are considered jointly.

A. LIMITATIONS OF BENDS

Compared to the conventional work [7], where the central part of the switch uses no bends, substantial bends appear in our structure. Therefore, it is necessary to explore their use in building a scalable network. The construction and functions of the basic modules can be referred to in the previous section, which will not repeat here. Essentially, each path in the Bi-Benes network can be viewed as a cascade of the essential 2×2 modules. Similarly, we considered two extreme cases, including the all-bar case and all-cross case. The cascade of the individual module without intersections is essential to our network.

The FSR depends on the small ring radius of 7.33nm, which is 2.16THz (around 17.3nm), see Fig. 10. Thanks to the periodic property, there are a total of eight operating wavelengths that can send signals simultaneously. When the maximum N is 61, the received signal is beyond the scope of the current software (−120dB), and the results become invalid. Due to cumulative effect of the bends, the insertion loss at each of the spectrum sides is substantial, about −30dB. Insertion loss is less than 7.22dB even after bending into 60 turns with 9.22μs radius. Meanwhile, the accumulated loss will be beyond the receiver sensitivity (−27dB) after continuous cascading of 45 resonators. As consequences, only five operating wavelengths (1499.11, 1517.25, 1535.84, 1554.89 and 1574.41nm) satisfied both target values.

In general, changes in the effective index and group index will cause resonance wavelength and FSR to change.

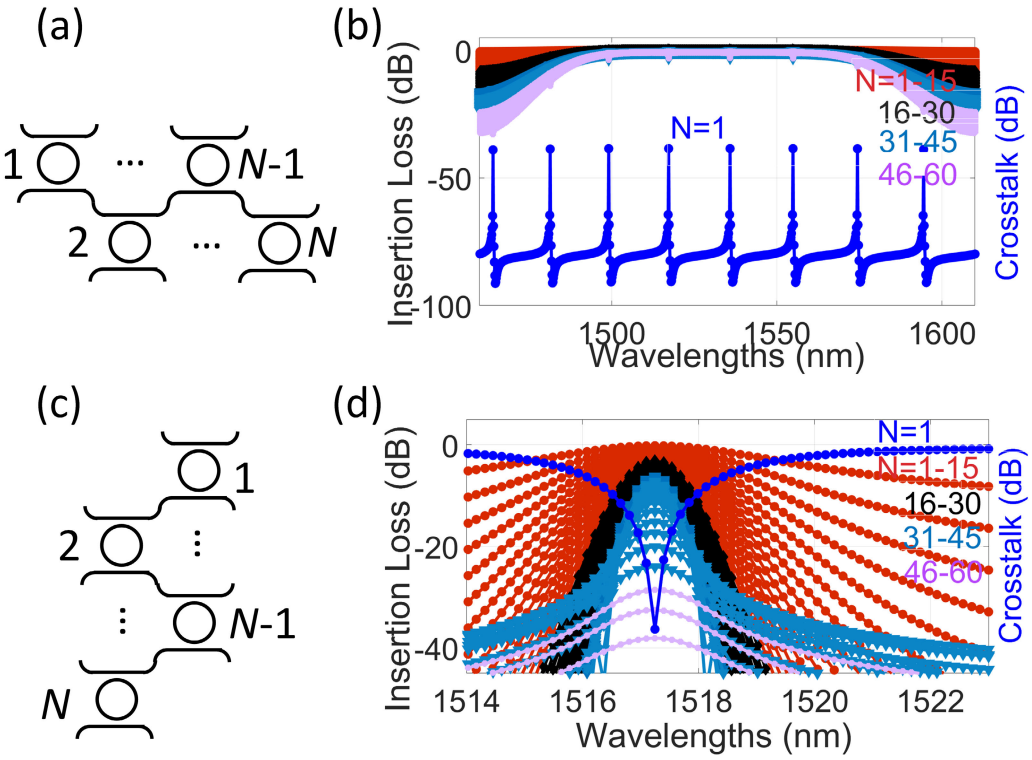


FIGURE 10. Cascading of *N* resonators with bends: (a) all-bars case, (b) transmission spectra from 1460-1610nm, (c) all-cross case, and (d) transmission spectra at 1574.41nm.

TABLE 5. Eight operating wavelengths and FSRs.

Operating wavelengths	1464.09	1481.39	1499.11	1517.25	1535.84	1554.89	1574.41	1594.41
FSR	-	17.3	17.72	18.14	18.59	19.05	19.52	20.00

When neither of the above changes, the resonance wavelength does not change so much. But we can still observe the red-shift. Table 5 shows the FSRs between the original resonance wavelengths. In the worst case, the path difference will cause a wavelength shift of ≈2.70nm. The reason is that when the length of the waveguide changes, the resonant wavelength changes almost linearly. In practical applications, active tuning is required to lock the resonance of each micro-ring resonator (MRR) simultaneously. However, the use of active tuning is beyond the scope of this article.

B. INSERTION LOSS AND CROSSTALK

Insertion loss and crosstalk level are two key performance indicators of optical switches. They determined the feasibility and scalability of network-on-chip. Using the method proposed above, we can record the performance indicators of each path. For a 32×32 network, there are in total $32! = 2.63 \times 10^{35}$ realizable permutations. Testing all optical paths are too complicated and time-consuming. Our analysis examine two extreme cases using a wavelength of 1574.41nm.

Fig. 11 shows the detailed path power loss for the all-Bar case and the all-Cross case. The insertion loss is in the black square, and the crosstalk is in the blue diamond. In the case of all-Cross and all-Bar, the insertion loss is reduced by about 5.97dB and 6.49dB compared with the traditional method [16]. At the same time, we reduced the fluctuation of optical loss from 2.05dB to 1.21dB. The crosstalk level ranges from −26.76dB to −13.67dB. Thus, our design basically meets the essential criteria for NoC applications: low insertion loss, low crosstalk, and nonblocking [33].

Table 6 summarizes the critical performance of the 32 port-count silicon optical switch fabrics. Our work has balanced superior performance on loss, footprint, and power compared to other switch fabrics. One can see that our work has significantly improved the chip size and power penalty. The reason is that Bi-Benes uses compact, energy-efficient MRR switches and minimizes waveguide crossings. Next, we decreased the fluctuation of optical loss from 2.05dB to 1.21dB. The contribution comes at the cost of a slight reduction in crosstalk. The worst-case crosstalk level drops to −13.67dB, slightly lower than the traditional −15dB level. In future research, we can increase the level of crosstalk by using more elaborately designed switching elements.

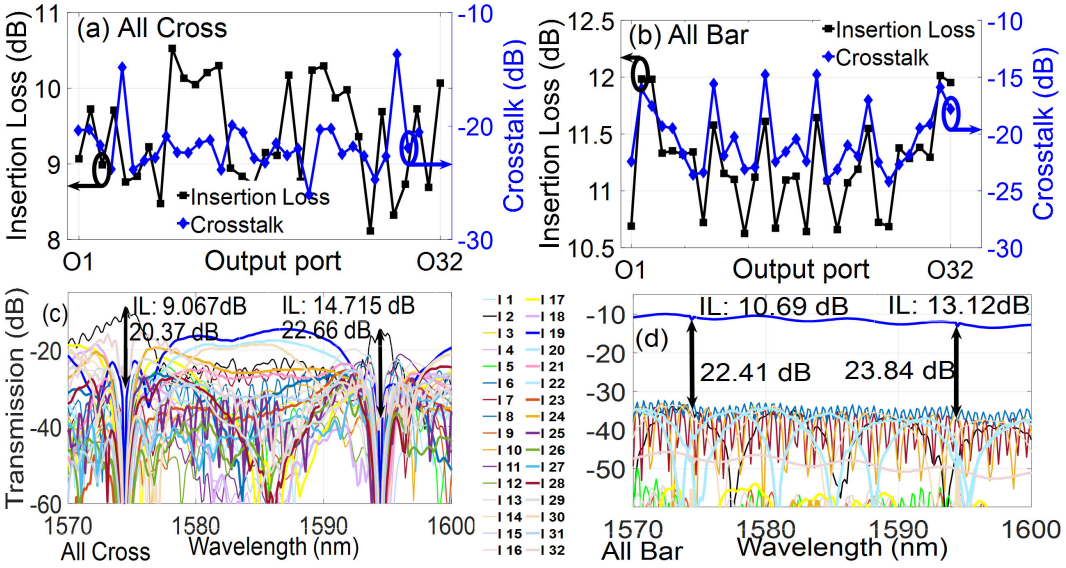


FIGURE 11. Performance of the 32 × 32 Bi-Benes network: (a) All-cross case (b) All-bar case (c)-(d) Two transmission spectra for output port 1 of the optical switch in all cross case and all bar case.

TABLE 6. Comparison between Piloss, Benes and Bi-Benes.

♯of topology	Piloss [34]	Benes [16]	Bi-Benes
♯of of port-count	32×32	32×32	32×32
♯of insertion loss (dB)	15.8±1	12.9 to 18.5	8.11 to 12.01
♯ of crosstalk (dB)	-20	-24.8 to -15.1	-26.76 to -13.67
♯of power consumption(mW)	2930	247.2 to 542.3	2.5984
♯of reconfiguration Time(μs)	30	-	0.006
♯Footprint(mm^2)(μs)	11×25	5.2×12.1	2.9×2.17
♯Technology	MZI, TiN	MZI, WG heater	MRR

Next, we study the end-to-end delay in the 32-port switch. The spectrum transmission program executes the entire wavelength bandwidth with N channels simultaneously. For the 32-port solution, the group delay response is indeed observed at the receiving end. The delay of each channel independently fluctuates from −25ps to 25ps.

But at the critical operating wavelength, the group delay is not significant, illustrated in Fig. 12. After the measurement, the all-bar state exhibits a delay from −3.8ps to 25ps, while the all-cross state presents a group delay between −1.3ps and 22ps. The average delay is approximately 20ps, which is one half of the sampling period.

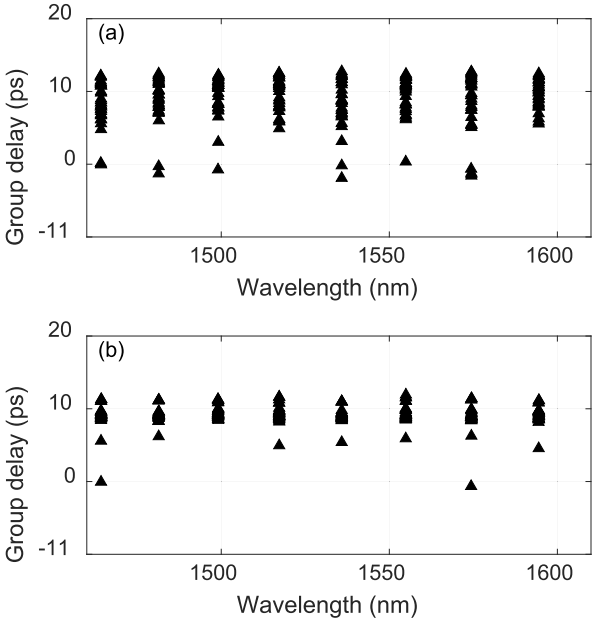


FIGURE 12. Group delay spectra for all 32 optical paths at eight operating wavelengths. (a) All bar state (b) All cross state.

C. BIT-ERROR-RATE EXPERIMENTAL SETUP AND RESULTS

The Bit-error-rate (BER) experimental setup is as follows. A 25Gb/s amplitude shift keying coded pseudo-random binary sequence (PRBS) with a length of 2^7-1 is employed. The signal is modulated and driven by an external Mach-Zehnder modulator (D1 = 1000μm). The modulated data then enter the switch with a polarization controller at the same wavelength of 1594.41nm. Thirty-two channels were transmitted simultaneously. The device's output is fed into a PIN photodiode. Then, an electrical amplifier and a pass-band filter are used before connecting to the error detector.

The results of the BER performance are presented in Fig. 13. Here we reported it as a function of the received optical power. The back-to-back transmissions are recorded as usual. Specifically, two representative cases shown in Fig. 6(c) are studied. The red line indicates the shortest routing path from 16 to 16'. And the green line points to the longest route from 1 to 32'. The eye diagrams of these cases are open and clean.

The input power ranges from −5dBm to −35dBm. For all three cases above, error-free measurement results are recorded. The result shows that the received optical power is the same initially but gradually decreases as the path length

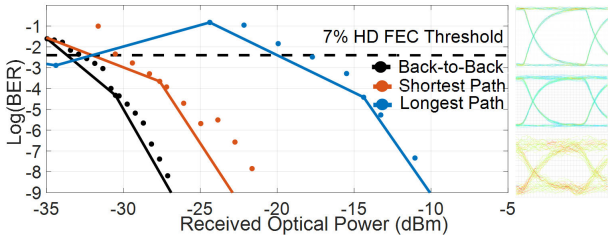


FIGURE 13. Corresponding BER measurements (left) of 25Gb/s error-free transmissions across the 32-port Bi-Benes switch. The line through the data points is the segmental polynomial fit of the points. Eye diagrams (right) of different paths.

increases. But after the turning point of 10^{-4} BER, the fundamental trends of the three curves are almost the same. The longest route consumes the most power. The optimum 10^{-9} BER is recorded with a power penalty of -10.9dBm. Therefore, the total power consumption per path is at most 0.0812mW. In other words, the overall power penalty of the 32-port switch is roughly 2.5984mW. Compared to other methods, the improvement in the optical power penalty is significant, see Table 6. This advantage contributed to the substantial reduction in switch size and intersections by using MRR and Bi-Benes.

V. CONCLUSION

Based on the concept of the Benes network, a new bidirectional network architecture was proposed herein. A bidirectional switch is to replace a unidirectional switch. Both the 8×8 and $N \times N$ switches exhibited the following advantages. First, they resolved the contention problem in the traditional ring-based system. Second, they resulted in significantly fewer crossings than the unidirectional Benes structure. Consequently, the total number of waveguide crossings decreased from $O(N^2)$ to $O(N\log_2 N)$. The bidirectional Benes has emerged as an attractive alternative to the traditional Benes network. Their costs are similar, but the size and power consumption are better.

REFERENCES

[1] P. Guo, W. Hou, L. Guo, W. Sun, C. Liu, H. Bao, L. H. K. Duong, and W. Liu, "Fault-tolerant routing mechanism in 3D optical network-on-chip based on node reuse," *IEEE Trans. Parallel Distrib. Syst.*, vol. 31, no. 3, pp. 547–564, Mar. 2019.

[2] Q. Chen, F. Zhang, R. Ji, L. Zhang, and L. Yang, "Universal method for constructing N-port non-blocking optical router based on 2×2 optical switch for photonic networks-on-chip," *Opt. Exp.*, vol. 22, no. 10, pp. 12614–12627, 2014.

[3] J. H. Lee, J.-C. Yoo, and T. H. Han, "System-level design framework for insertion-loss-minimized optical network-on-chip router architectures," *J. Lightw. Technol.*, vol. 32, no. 18, pp. 3161–3174, Sep. 15, 2014.

[4] J. L. Benjamin, T. Gerard, D. Lavery, P. Bayvel, and G. Zervas, "PULSE: Optical circuit switched data center architecture operating at nanosecond timescales," *J. Lightw. Technol.*, vol. 38, no. 18, pp. 4906–4921, Sep. 15, 2020.

[5] A. Theonitsa, T. Nikolaos, P. Stelios, M.-P. Miltiadis, M. Pavlos, V. Christos, M. Charoula, M.-A. George, T. K. George, M. Amalia, V. Konstantinos, and P. Nikos, "Optics in computing: From photonic network-on-chip to chip-to-chip interconnects and disintegrated architectures," *J. Lightw. Technol.*, vol. 37, no. 2, pp. 363–379, Jan. 15, 2019.

[6] R. Konoike, K. Suzuki, K. Tanizawa, S. Suda, H. Matsuura, S. Namiki, H. Kawashima, and K. Ikeda, "SiN/Si double-layer platform for ultralow-crosstalk multiport optical switches," *Opt. Exp.*, vol. 27, no. 15, pp. 21130–21141, 2019.

[7] D. Nikolova, S. Rumley, D. Calhoun, Q. Li, R. Hendry, P. Samadi, and K. Bergman, "Scaling silicon photonic switch fabrics for data center interconnection networks," *Opt. Exp.*, vol. 23, no. 2, pp. 1159–1175, Jan. 2015.

[8] F. Dehghani, S. Mohammadi, B. Barekatain, and M. Abdollahi, "Power loss analysis in thermally-tuned nanophotonic switch for on-chip interconnect," *Nano Commun. Netw.*, vol. 26, Nov. 2020, Art. no. 100323.

[9] R. Yao and Y. Ye, "Toward a high-performance and low-loss Clos–Benes-based optical network-on-chip architecture," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 39, no. 12, pp. 4695–4706, Dec. 2020.

[10] K. Suzuki, S. Namiki, H. Kawashima, K. Ikeda, R. Konoike, N. Yokoyama, M. Seki, M. Ohtsuka, S. Saitoh, S. Suda, H. Matsuura, and K. Yamada, "Nonduplicate polarization-diversity 32×32 silicon photonics switch based on a SiN/Si double-layer platform," *J. Lightw. Technol.*, vol. 38, no. 2, pp. 226–232, Jan. 15, 2020.

[11] T. Zhou and H. Jia, "Method to optimize optical switch topology for photonic network-on-chip," *Opt. Commun.*, vol. 413, pp. 230–235, Apr. 2018.

[12] Z. Wang, Z. Wang, J. Xu, J. Feng, S. Chen, X. Chen, and J. Zhang, "Reduce loss and crosstalk in integrated silicon-photonic multistage switching fabrics through multichip partition," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 40, no. 1, pp. 101–114, Jan. 2021.

[13] M. Nikdast, J. Xu, L. H. Duong, X. Wu, Z. Wang, X. Wang, and Z. Wang, "Fat-tree-based optical interconnection networks under crosstalk noise constraint," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 1, pp. 156–169, Jan. 2015.

[14] D. Zheng, J. D. Doménech, W. Pan, X. Zou, L. Yan, and D. Pérez, "Low-loss broadband 5×5 non-blocking Si_3N_4 optical switch matrix," *Opt. Lett.*, vol. 44, no. 11, pp. 2629–2632, 2019.

[15] L. Lu, S. Zhao, L. Zhou, D. Li, Z. Li, M. Wang, X. Li, and J. Chen, "16×16 non-blocking silicon optical switch based on electro-optic Mach-Zehnder interferometers," *Opt. Exp.*, vol. 24, no. 9, pp. 9295–9307, 2016.

[16] L. Qiao, W. Tang, and T. Chu, "32×32 silicon electro-optic switch with built-in monitors and balanced-status units," *Sci. Rep.*, vol. 7, no. 1, pp. 1–7, Sep. 2017.

[17] B. E. Little, S. T. Chu, H. A. Haus, J. Foresi, and J.-P. Laine, "Microring resonator channel dropping filters," *J. Lightw. Technol.*, vol. 15, no. 6, pp. 998–1005, Jun. 1997.

[18] H. Shoman, H. Jayatilleka, N. A. Jaeger, S. Shekhar, and L. Chrostowski, "Measuring on-chip waveguide losses using a single, two-point coupled microring resonator," *Opt. Exp.*, vol. 28, no. 7, pp. 10225–10238, 2020.

[19] H. Du, X. Zhang, C. G. Littlejohns, D. T. Tran, X. Yan, M. Banakar, C. Wei, D. J. Thomson, and G. T. Reed, "Nonconservative coupling in a passive silicon microring resonator," *Phys. Rev. Lett.*, vol. 124, no. 1, Jan. 2020, Art. no. 013606.

[20] R. A. Soref and B. E. Little, "Proposed N-wavelength M-fiber WDM crossconnect switch using active microring resonators," *IEEE Photon. Technol. Lett.*, vol. 10, no. 8, pp. 1121–1123, Aug. 1998.

[21] S. Matsuura, N. Yamasaku, Y. Nishijima, S. Okazaki, and T. Arakawa, "Characteristics of highly sensitive hydrogen sensor based on Pt-WO_3/Si microring resonator," *Sensors*, vol. 20, no. 1, p. 96, Dec. 2019.

[22] D. Zhang, L. Men, and Q. Chen, "Tuning the performance of polymeric microring resonator with femtosecond laser," *Opt. Commun.*, vol. 465, Jun. 2020, Art. no. 125571.

[23] B.-C. Lin, S. Chen, Y. Huang, and C.-T. Lea, "Power minimization in microring-based Benes networks," *IEEE Trans. Commun.*, vol. 66, no. 8, pp. 3517–3525, Aug. 2018.

[24] M. Behadori, M. Nikdast, Q. Cheng, and K. Bergman, "Universal design of waveguide bends in silicon-on-insulator photonics platform," *J. Lightw. Technol.*, vol. 37, no. 10, pp. 3044–3054, Jul. 2019. [Online]. Available: http://jlt.osa.org/abstract.cfm?URI=jlt-37-13-3044

[25] W. Bogaerts, P. De Heyn, T. Van Vaerenbergh, K. De Vos, S. K. Selvaraja, T. Claes, P. Dumon, P. Bienstman, D. Van Thourhout, and R. Baets, "Silicon microring resonators," *Laser Photon. Rev.*, vol. 6, no. 1, pp. 47–73, Jan. 2012.

[26] H. Cam and J. A. B. Fortes, "Work-efficient routing algorithms for rearrangeable symmetrical networks," *IEEE Trans. Parallel Distrib. Syst.*, vol. 10, no. 7, pp. 733–741, Jul. 1999.

[27] H. Mehrvar and E. Bernier, "Fast photonic switch architecture for interconnect applications," in *Proc. Eur. Conf. Opt. Commun. (ECOC)*, Sep. 2018, pp. 1–3.

[28] B. G. Lee and N. Dupuis, "Silicon photonic switch fabrics: Technology and architecture," *J. Lightw. Technol.*, vol. 37, no. 1, pp. 6–20, Jan. 1, 2019.
[29] S. Han, T. J. Seok, K. Yu, N. Quack, R. S. Muller, and M. C. Wu, "Large-scale polarization-insensitive silicon photonic MEMS switches," *J. Lightw. Technol.*, vol. 36, no. 10, pp. 1824–1830, May 15, 2018.
[30] L. Huang, H. Gu, Y. Tian, and T. Zhao, "Universal method for constructing the on-chip optical router with wavelength routing technology," *J. Lightw. Technol.*, vol. 38, no. 15, pp. 3815–3821, Aug. 1, 2020.
[31] A. Chakrabarty and M. Collier, "O ($\log\overline{m}$ log N) routing algorithm for (2log N-1)-stage switching networks and beyond," *J. Parallel Distrib. Comput.*, vol. 74, no. 10, pp. 3045–3055, 2014.
[32] R. Boeck, N. A. F. Jaeger, N. Rouger, and L. Chrostowski, "Series-coupled silicon racetrack resonators and the Vernier effect: Theory and measurement," *Opt. Exp.*, vol. 18, no. 24, pp. 25151–25157, 2010.
[33] A. W. Poon, X. Luo, F. Xu, and H. Chen, "Cascaded microresonator-based matrix switch for silicon on-chip optical interconnection," *Proc. IEEE*, vol. 97, no. 7, pp. 1216–1238, Jul. 2009.
[34] S. Zhao, L. Lu, L. Zhou, D. Li, Z. Guo, and J. Chen, "16×16 silicon Mach–Zehnder interferometer switch actuated with waveguide microheaters," *Photon. Res.*, vol. 4, no. 5, pp. 202–207, 2016.

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