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Ultra-Low Energy CNFET-Based Ternary Combinational Circuits Designs

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ABSTRACT The embedded systems, IoT (Internet of Things) devices, and portable electronic devices spread very quickly recently. Most of them depend on batteries to operate. The target of this work is to decrease energy consumption by (1) using Multiple-valued logic (MVL) that shows notable enhancements regarding energy consumption over binary circuits and (2) using carbon nanotube field-effect transistors (CNFET) that show better performance than CMOS. This work proposes ternary combinational circuits using 32 nm CNFET: Ternary Half Adder (THA) with 36 transistors and Ternary Multiplier (TMUL) with 23 transistors. To reduce energy consumption by utilizing the unary operator of the ternary system and employing two voltage supplies (V_{dd} and $V_{dd}/2$). The result of extensive HSPICE simulations regarding PVT (Process, Voltage, and Temperatures) variations and Noise Immunity Curve (NIC) show the improvements of the proposed designs up to 25% in transistors count and up to 98% in energy consumption reductions. Further, increasing the robustness of process variations and the noise tolerance compared to recent similar designs.

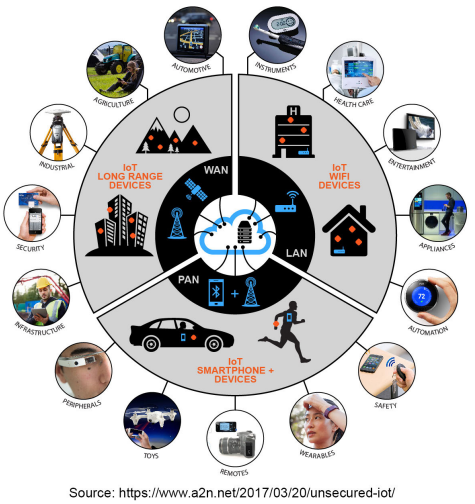
INDEX TERMS Noise immunity curve (NIC), CNTFET, MVL, PVT variations, ternary logic circuits.

I. INTRODUCTION

Embedded systems, IoT (Internet of Things) devices are used almost in all fields, such as smart home security systems, smart cities, medical and healthcare applications, military applications, environmental monitoring, as illustrated in Fig. 1. The challenge is how to reduce the energy consumption of the embedded systems for getting the best performance out of real-time applications and devices.

To achieve our aim, there are two essential things to be considered for designing the proposed circuits: (1) Carbon Nano-Tube Field-Effect Transistor (CNTFET) and (2) Multiple-Valued Logic (MVL).

The limitations of CMOS in nanoscale systems are mainly due to large current leakage, tight channel effects, and losing gate control [1]. Among all different transistor technologies, CNTFETs proved to have the highest performance [2].



Source: https://www.a2n.net/2017/03/20/unsecured-iot/

FIGURE 1. Embedded systems and IoT applications.

On the other hand, in MVL each digit can hold multiple states which results in a better performance than binary circuits [3].

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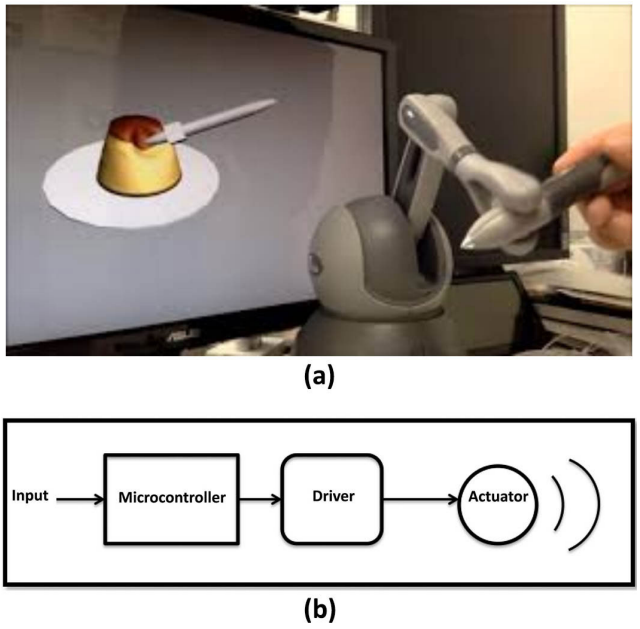

FIGURE 2. Haptic device: (a) Touch application, and (b) the components inside.

This paper uses CNTFET transistors and unbalanced ternary logic system (Low: 0, Middle: 1, High: 2) that is equivalent to (0, $V_{dd}/2$, V_{dd}).

A. APPLICATIONS OF THE PROPOSED TERNARY CIRCUITS

Researchers became highly interested in MVL and implemented it in different scopes such as healthcare applications [4], Memory [5], [6], RRAM (Resistive Random Access Memory) [7], Ternary Logic Systems [8], [9], and Ternary to Binary converter [10].

And for the first time, to the best of our knowledge, we will use the proposed ternary circuits in Haptic device inside the microcontroller to speed up the response delay between the input and the actuator.

Figure 2 shows (a) Touch application, and (b) the components inside the haptic device.

In the next work, we will implement the proposed ternary circuits to haptic device to be used for our MOALEM Platform.

B. TERNARY CIRCUITS CHALLENGE: HOW TO GET LOGIC 1 ($V_{dd}/2$)?

In ternary logic circuits, most of the researchers reached logical state 1 using one power supply. They divided the voltage using two diode-connected transistors that act similar to resistors. However, this technique is not very efficient because of a direct current path that passes from V_{dd} to the ground, which generates heat in the circuit (Joule effect power) resulting in a remarkable increase in static power, as described in equation (1a).

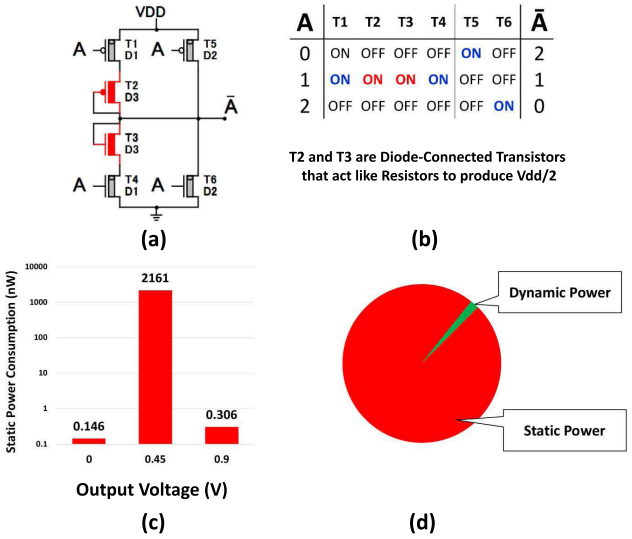

FIGURE 3. Static power analysis of the STI [11]: (a) Transistor-level, (b) Truth table, (c) Static power is 2000 times higher, and (d) 98% of the average power consumption is from static power.

The circuit's total power consumption is divided into two types: static power and dynamic power.

$$P = P_s + P_d \tag{1}$$

$$Static: P_s = N_d * R * Id^2 + N * V_{dd} * Id \tag{1a}$$

$$Dynamic: P_d = N * V_{dd}^2 * f * CL \tag{1b}$$

Where,

N	: Transistor's count
Nd	: Transistor's count of the Diode-Connected
R	: Resistance
V_{dd}	: Power Supply
Id	: Current used by transistors
f	: The frequency generated by Vinput
CL	: Internal Capacitance and Load Capacitor

To illustrate that, we analyze in Fig. 3 the static power of STI (Standard Ternary Inverter) [11], a typical example for the generation of logic state 1 using one power source V_{dd}. The circuit in Fig. 3 has 6 transistors, where two of them T2, T3 are diode-connected transistors, which are used to divide the voltage (a). While, in (b) the truth table shows that to reach the output "A" = 1, the transistors (T1, T2, T3, and T4) must turn on, which create a direct current path between V_{dd} and the ground resulting in high static power, as shown in (c). Whereas (d) concludes that 98% of the average power consumed in this circuit is from static power.

This paper uses a power supply that generates two voltage supplies V_{dd} and $V_{dd}/2$ to remove these two transistors and accordingly decrease the overall energy consumption in the circuit. However, this technique also has the drawback of increasing the interconnections in the circuits.

C. LITERATURE REVIEW

Many publications addressed different Ternary Half-Adders (THAs) and Ternary Multipliers (TMULs) based on CNTFET, Table 1 describes the most important and latest ones.

The authors of [12]–[15] used the traditional designs. They reached ternary outputs by using a Ternary Decoder (TDecoder), basic binary gates, and a ternary encoder. In addition, authors of [14], [15] used RRAM with CNTFETs.

The authors of [16], [17] used cascading Ternary Multiplexers (TMUXs) with two voltage supplies (V_{dd}, $V_{dd}/2$).

The authors of [18]–[22] used unary operators with TMUXs to decrease the number of used transistors.

In [23]–[27], the authors used different or mixed designs such as logic synthesis algorithms.

In previous works [28], [29], two THAs and a TMUL were designed using unary operators with TGs, two voltage supplies (V_{dd}, $V_{dd}/2$), and special arrangements of 34, 35, and 26 transistors, respectively.

D. CONTRIBUTIONS

All the designs noted above suffer from a high transistor count, high energy consumption, weak process robustness, and/or poor noise tolerance.

This work proposes a circuit implementation that minimizes battery usage in IoT devices and embedded systems. It employs novel concept unary operators, transmission gates, two voltage supplies (V_{dd}, $V_{dd}/2$), and special transistors arrangements to design a THA with 36 CNFETs and TMUL with 23 CNFETs.

The contributions of our work are:

1) The proposed designs do not use standard logic gates, ternary decoders, or ternary encoders, which produce high transistors count and PDP ([12]–[15], [25], [26]).
2) The proposed designs work on unary operators, which reduces the number of transistors ([17]–[22], [28], [29]).
3) The proposed designs employ two voltage supplies (V_{dd} and $V_{dd}/2$) to get rid of the direct current between the V_{dd} and the ground, which significantly reduces the energy consumption.

Therefore, the proposed designs decrease the number of transistors used in the circuit, reduce the overall energy consumption in the system, provide better robustness to process variations, and strengthen noise tolerance.

II. CNFET TRANSISTOR

This paper uses the Stanford CNFET model [30]–[32], as shown in Fig.4. The advantage of the CNFET transistor is that its threshold voltage depends on its CNT diameter as shown in equation (2), which is suitable to be used in MVL circuits.

$$V_{\text{th}} \approx \frac{0.43}{Dcnt} \tag{2}$$

Table 2 describes the operations of a CNFET transistor with relevance to its diameter and threshold voltage.

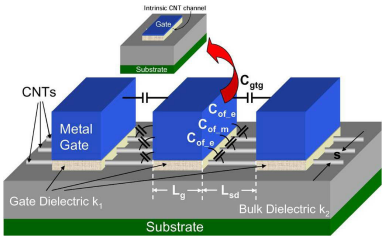

FIGURE 4. Stanford CNFET Model [30].

Ternary input A	f_1	f_2	f_3	f_4	f_5	f_6	f_7	f_8	f_9	f_{10}	f_{11}	f_{12}	f_{13}	f_{14}	f_{15}	f_{16}	f_{17}	f_{18}	f_{19}	f_{20}	f_{21}	f_{22}	f_{23}	f_{24}	f_{25}	f_{26}	f_{27}
0 (0V)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	2	2	2	2	2	2	2	2	2
1 (Vdd/2)	0	0	0	1	1	1	2	2	2	0	0	0	1	1	1	2	2	2	0	0	0	1	1	1	2	2	2
2 (Vdd)	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2

FIGURE 5. 27 unary operators of ternary system.

III. PROPOSED UNARY OPERATOR

The one-input-one-output logic gate is called the unary function or unary operator of the i-valued logic system, and the total number of functions is i^i.

The binary logic system ($i = 2$) has four unary functions while the ternary system ($i = 3$) has twenty-seven unary operators, as shown in Fig. 5.

Table 3 shows the eight selected unary functions to be used in the design of the THA and TMUL.

The first three A_p, A_n and $\bar{A}$ represent a Positive Ternary Inverter (PTI), a Negative Ternary Inverter (NTI), and a Standard Ternary Inverter (STI). The fourth and the fifth functions are referred to the cycle operators, A^1 is $A + 1$ (successor or single shift operator) and A^2 is $A \; \bar{+} \; 2$ (Predecessor or dual shift operator). The sixth function $\bar{A^2}$ represents a complement of A^2, and the final two are $1 \cdot \bar{A_n}$ and $1 \cdot \bar{A_p}$, as described in [33].

Figure 6 shows the five existing unary operators in [29].

This paper proposes three unary operators as shown in Fig. 7: (a) A^2, (b) A^1, and (c) A_1. Their operations are summarized in Table 4.

Table 5 shows a comparison between the number of transistors used in the proposed unary operators and other unary operators used in [19]–[22] and [29].

IV. PROPOSED TERNARY COMBINATIONAL CIRCUITS

This paper proposes a THA with 36 CNFETs and a TMUL with 23 CNFETs using transmission gates (TGs), unary operators, two voltage supplies (V_{dd}, $V_{dd}/2$), and special transistors arrangements.

A. PROPOSED TERNARY HALF-ADDER

A 1-trit THA adds two ternary inputs and outputs two ternary values (Sum & Carry), as shown in Table 6.

$$\begin{aligned} Sum &= A.B_0 + A^1.B_1 + A^2.B_2 \\ Carry &= 0.B_0 + (1 \cdot \bar{A_p}).B_1 + (1 \cdot \bar{A_n}).B_2 \end{aligned} \tag{3}$$

TABLE 1. Summary of literature review.

Techniques	Ref.	Year	Details	Transistor count THA	Transistor count TMUL	Limitation
Conventional Design	[12]	2020	- Ternary Decoder with 16 CNFETs - Binary gates - Ternary encoder	108	-	- High PDP
	[13]	2019	- Ternary Decoder with 9 CNFETs - Basic gates - V_{dd} and $V_{dd}/2$	85	61	- Medium Transistors count
	[14]	2020	- Ternary Decoder with 16 CNFETs	90	62	- Medium PDP
	[15]	2021	- Binary gates - RRAM	84	-	
Cascading TMUXs	[16]	2020	- Ternary Multiplexer with 15 CNFETs	90	-	- Medium Transistors count
	[17]	2020	- V_{dd} and $V_{dd}/2$	-	60	- Medium PDP
Unary Operators & TMUXs	[18]	2016	- Ternary Multiplexer with 15 CNFETs	39	26	- Medium to Low Transistors count - Medium PDP
	[19]	2017	- Ternary Multiplexer with 18 CNFETs	64	58	
	[20]	2018	- Ternary Multiplexer with 22 CNFETs - V_{dd} and $V_{dd}/2$	54	23	
	[21]	2019	- Binary NAND - Ternary Multiplexer with 18 CNFETs	76	-	
	[22]	2020	- Unary Operators using cascading TMUX - Ternary Multiplexer with 12 CNFETs	48	30	
Synthesis	[23]	2020	- Modified Quine-McCluskey Algorithm	48	-	- High PDP
Cascading TGs	[24]	2020	- Lots of cascading TGs	50	38	- Medium PDP
Mixed	[25]	2017	- Ternary Multiplexer with 8 CNFETs - Ternary encoder	94^1 66^2	-	
	[26]	2018	- Ternary Multiplexer with 10 CNFETs	64	-	- Medium Transistors count - Medium PDP
	[27]	2021	- Ternary Encoder - Special transistors arrangements	60	-	
Unary Operators & TGs	[28]	2021	- V_{dd} and $V_{dd}/2$	34	-	- Low Transistors count - Low PDP
	[29]	2021	- Special transistors arrangements	35	26	

TABLE 2. CNFET operation for D1 = 1.487 nm, D2 = 0.783 nm.

Type	Diameter	Threshold voltage	Voltage Gate 0V	0.45V	0.9V
P-CNFET	D1	- 0.289 V	ON	ON	OFF
	D2	- 0.559 V	ON	OFF	OFF
N-CNFET	D1	0.289 V	OFF	ON	ON
	D2	0.559 V	OFF	OFF	ON

TABLE 3. Selected 8 unary operators to be used in the designs.

Ternary Input A	PTI A_p	NTI A_n	Cycle Operators A^1	A^2	$\bar{A^2}$	Decisive literal A_1	$1 \cdot \bar{A_n}$	$1 \cdot \bar{A_p}$
0	2	2	1	2	0	0	0	0
1	2	0	2	0	2	2	1	0
2	0	0	0	1	1	0	1	1

where

$$B_i = \begin{cases} 2 & if\ B = i \\ 0 & if\ B \neq i \end{cases}$$

This paper proposes a THA with 36 CNFETs design based on unary operators, TGs, and two voltage supplies (V_{dd}, $V_{dd}/2$), which is based on equation 3 and shown in Fig. 8.

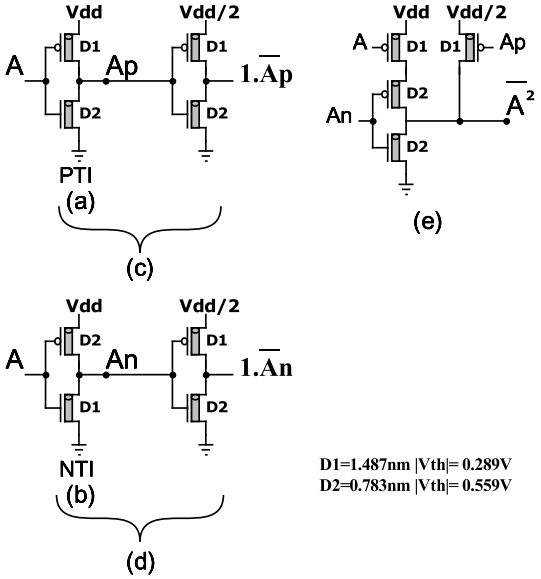

FIGURE 6. Existing 5 unary operators in [29]: (a) A_p, (b) A_n, (c) $1 \cdot \bar{A_p}$, (d) $1 \cdot \bar{A_n}$, and (e) $\bar{A^2}$.

The maximum propagation delay in this design takes place from the input "A" to the output "Sum". This path is referred as the critical path (the red dotted line), it occurs when the

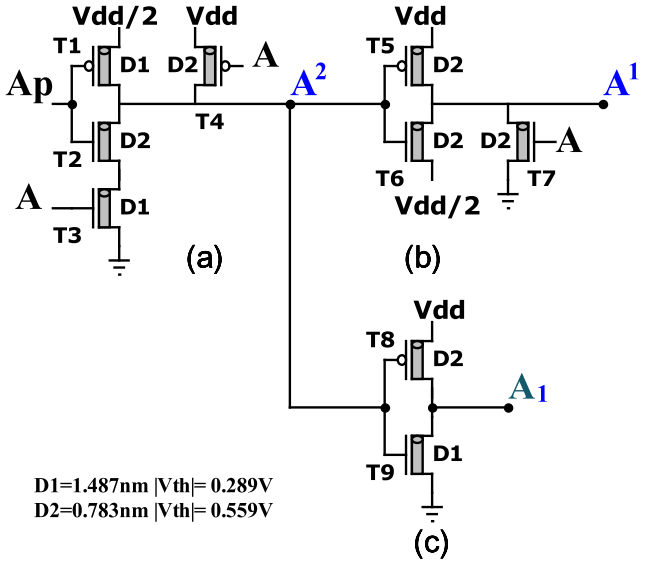

FIGURE 7. Proposed 3 unary operators: (a) A^2, (b) A^1, and (c) A_1.

TABLE 4. Operation of the proposed unary operators.

Fig. 7	A	A_p	Transistors Status ON	Transistors Status OFF	Output	
(a)	0	2	T2,T4	T1,T3	2	$\mathbf{A^2}$
	1	2	T2,T3	T1,T4	0	
	2	0	T1,T3	T2,T4	1	
(b)	0		T6	T5,T7	1	$\mathbf{A^1}$
	1		T5	T6,T7	2	
	2		T7	T5,T6	0	
(c)	0		T9	T8	0	$\mathbf{A_1}$
	1		T8	T9	2	
	2		T9	T8	0	

TABLE 5. Unary operators transistors count comparison.

	[19]	[20]	[21]	[22]	[29]	Proposed
$\mathbf{A^2}$	7	17	10	18	3	4
$\mathbf{A^1}$	7	17	10	18	4	3
$\mathbf{A_1}$	6	10	12	-	3	2
Total	20	54	32	36	10	9
Improvement	55%	83%	72%	75%	11%	

TABLE 6. THA truth table.

Sum

A/B	B_0 (0)	B_1 (1)	B_2 (2)
A_0 (0)	0	1	2
A_1 (1)	1	2	0
A_2 (2)	2	0	1
	$\mathbf{A}$	$\mathbf{A^1}$	$\mathbf{A^2}$

Carry

A/B	B_0 (0)	B_1 (1)	B_2 (2)
A_0 (0)	0	0	0
A_1 (1)	0	0	1
A_2 (2)	0	0	1
	$\mathbf{0}$	$\mathbf{1 \cdot \overline{A_p}}$	$\mathbf{1 \cdot \overline{A_n}}$

input "A" changes from 1 to 2, "B" = 2, and the Sum changes from 0 to 1.

B. PROPOSED TERNARY MULTIPLIER

A 1-trit TMUL multiplies two ternary inputs and outputs two ternary values (Product & Carry), as shown in Table 6.

$$Product = 0 \cdot B_0 + A \cdot B_1 + \bar{A}^2 B_2 \tag{4}$$

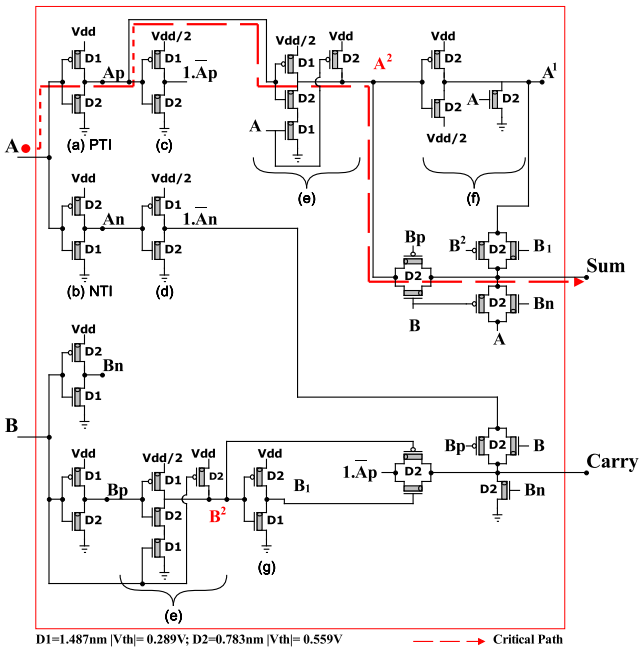

FIGURE 8. Proposed THA with 36 CNFETs: (a) PTI, (b) NTI, (c) $1 \cdot \bar{A_p}$, (d) $1 \cdot \bar{A_n}$, (f) A^1, and proposed (e) A^2 (& B^2), (g) B_1. Using unary operators based design in Eq. (3).

TABLE 7. TMUL truth table.

Product

A/B	B_0 (0)	B_1 (1)	B_2 (2)
A_0 (0)	0	0	0
A_1 (1)	0	1	2
A_2 (2)	0	2	1
		$\mathbf{A}$	$\mathbf{\overline{A^2}}$

Carry

A/B	B_0 (0)	B_1 (1)	B_2 (2)
A_0 (0)	0	0	0
A_1 (1)	0	0	0
A_2 (2)	0	0	1

$$Carry = 1 \cdot \overline{(A_p + B_p)} \tag{5}$$

This paper proposes a TMUL with 23 CNFETs design using unary operators, TGs, and two voltage supplies (V_{dd}, V_{dd}/2), which is based on equations 4 and 5 as shown in Fig. 9.

The dotted red line is the critical path between the input "A" and the output "Product". It occurs when the input "A" changes its state from 1 to 2, "B" = 1, and the Product changes from 1 to 2. we expect this critical path because there are two cascading TGs that produce more propagation delays.

1) HOW IS CARRY EQUATION (5) GENERATED?

Step 1: We insert A_p and B_p in the Carry truth table of Table 7 to get Table 8.

Step 2: We remove A and B from Table 8 to get Table 9.

Step 3: Because A_p and B_p are binary, then we implement the binary logic *OR*, *NOR*, and $1 \cdot NOR$ in Table 10.

Step 4: As shown in Tables 9 and 10, then $Carry = 1 \cdot \overline{(A_p + B_p)}$

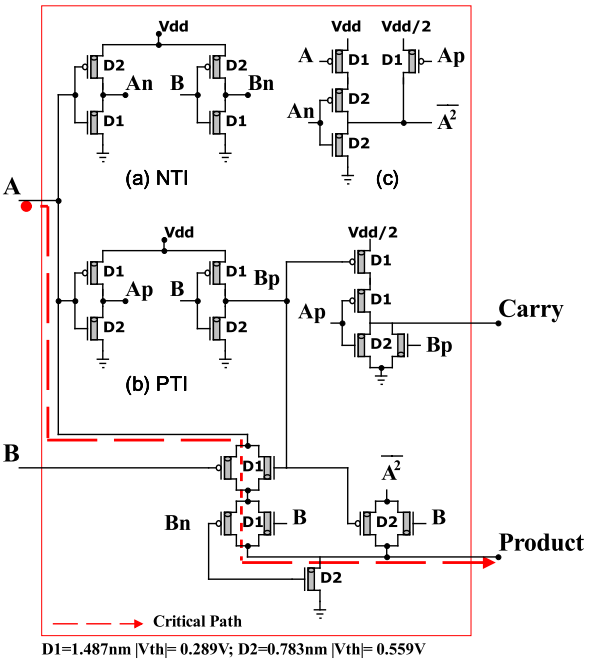

FIGURE 9. Proposed TMUL with 23 CNFETs: (a) NTI, (b) PTI, (c) $\bar{A^2}$. Using Eq. (4) and (5).

TABLE 8. Carry truth table version 2.

B	B_p	A	A_p	Carry
0 or 1	**2**	0 or 1	2	0
				0
		2	0	0
2	**0**	0 or 1	2	0
				0
		2	0	1

TABLE 9. Carry truth table version 3.

B_p	A_p	Carry
0	0	1
0	2	0
2	0	0
2	2	0

TABLE 10. Binary truth table of A_p and B_p.

B_p	A_p	OR	NOR	$1 \cdot NOR$
0	0	0	2	1
0	2	2	0	0
2	0	2	0	0
2	2	2	0	0

V. SIMULATION RESULTS AND COMPARISONS

The two proposed designs for the THA and TMUL are extensively simulated using the HSPICE simulator and compared with 32-nm CNFET-Based ternary circuits [12]–[14], [16]–[19], [22]–[29] with temperature varying within the range 0 °C to 70 °C, and a V_{dd} varying within the range 0.8 V to 1 V.

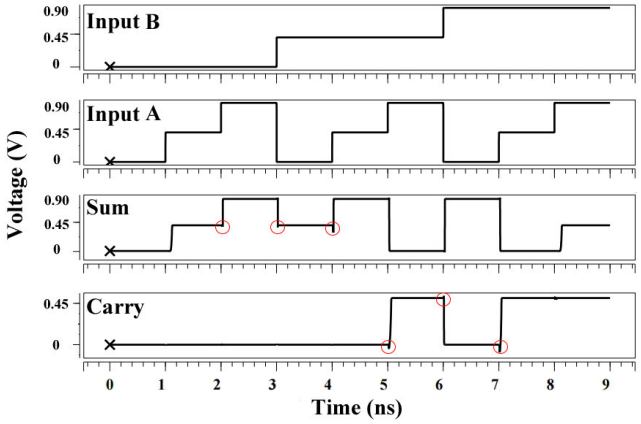

FIGURE 10. Proposed THA transient analysis.

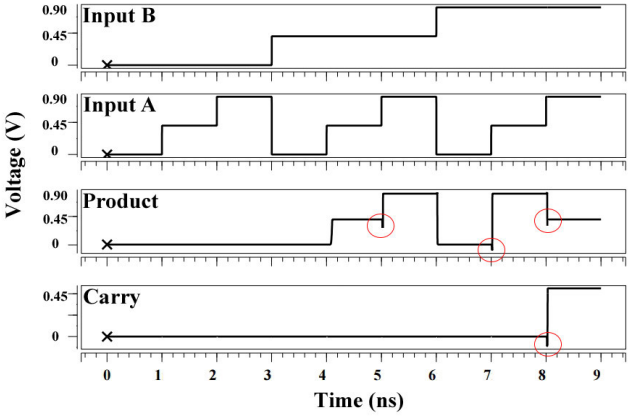

FIGURE 11. Proposed TMUL transient analysis.

Also, the fundamental process variations (CNT's Count, CNT Diameter, Channel length, and TOX) and NIC are studied.

Figures 10 and 11 display the transient analysis of the two designs. The simulation is performed with the following parameters: temperature = 27 °C, V_{dd} = 0.9 V, and frequency = 1 GHz. The fall and rise time of all signals set to 20 ps.

Minimizing energy consumption is the main goal of this work. The number of transistors used in the circuit is a critical parameter that must be monitored while designing a model. A high number of transistors results in higher power dissipation and higher delays.

Tables 11 and 12 show a comparison to all previously mentioned designs regarding the number of the transistor, the average power consumption (in μW), the maximum propagation delay (in ps), and the PDP (x10^{-18} J), with temperature = 27 °C, V_{dd} = 0.9 V, and frequency = 1 GHz.

A. VOLTAGE AND TEMPERATURE VARIATIONS

Figure 12 shows the voltage variation compared to existing THA and TMUL of [13], [16], [17], [19], [24], [28], [29] regarding the energy consumption PDP. The parameters used

TABLE 11. THAs comparison.

THA / Year	CNTFETs Count	Power (μW)	Max. Delay (ps)	PDP (x10^{-18} J)
In [12] 2020	108	0.26	38.7	10.06
In [13] 2019	85	0.53	74.63	39.55
In [16] 2020	90	0.14	10.66	1.49
In [18] 2016	39	9.42	18.29	172.3
In [19] 2017	64	0.99	8.52	8.43
In [22] 2020	48	0.43	51.86	22.29
In [23] 2020	48	0.14	35.5	4.97
In [24] 2020	50	0.32	**4.3**	1.37
In [25] 2017	94	0.59	17.62	10.39
In [25] Design 2	66	0.25	16.52	4.13
In [26] 2018	64	0.37	23.45	8.67
In [27] 2021	60	0.18	7.27	1.31
In [28] 2021	**34**	0.128	9.5	1.21
In [29] 2021	35	0.12	7.74	0.99
Proposed THA	36	**0.09**	8.7	**0.78**
Improvement w.r.t [22]*	25%	79%	83%	96%
w.r.t [29]**	-3%	25%	-12%	21%

* Compared to the highest PDP among similar method
** Compared to the lowest PDP among other circuits

TABLE 12. TMULs comparison.

TMUL / Year	CNTFETs Count	Power (μW)	Max. Delay (ps)	PDP (x10^{-18} J)
In [13] 2019	61	0.42	54.82	23
In [14] 2020	62	0.12	129	15.5
In [17] 2020	60	0.17	9.65	1.6
In [18] 2016	26	0.68	15.7	10.7
In [19] 2017	58	0.64	16.63	10.6
In [20] 2018	**23**	0.17	12.6	2.1
In [22] 2020	30	0.22	46.06	10.1
In [24] 2020	38	0.28	**4.81**	1.35
In [29] 2021	26	0.06	9.33	0.56
Proposed TMUL	**23**	**0.04**	5.14	**0.21**
Improvement w.r.t [22]*	23%	82%	89%	98%
w.r.t [29]**	12%	33%	45%	63%

* Compared to the highest PDP among similar method
** Compared to the lowest PDP among other circuits

are temperature set with the value 27 °C, frequency value at 1 GHz, and supply voltages varying from 0.8 V to 1 V.

Figure 13 shows the temperature variation compared to existing THA and TMUL of [13], [16], [17], [19], [24], [28], [29] regarding the energy consumption PDP. The parameters are frequency value set at 1 GHz, power supply at 0.9 V, and temperatures varying within the range 10 °C to 70 °C.

Figures 12 and 13 show that the proposed designs resulted in the lowest PDP compared to other designs regarding voltage and temperature variations.

B. PROCESS VARIATIONS

During the manufacturing process of integrated circuits (ICs), errors in the dimensions of transistors (oxide width, length,...) called process variations occur, which highly affects the robustness and behavior of nanoscale circuits.

This study employs Monte Carlo analysis, a model that performs statistics with the following assumptions: a Gaussian distribution of ±5%, ±10%, and ±15% with fluctuations at the ±3 *sigma* level and 100 running simulations.

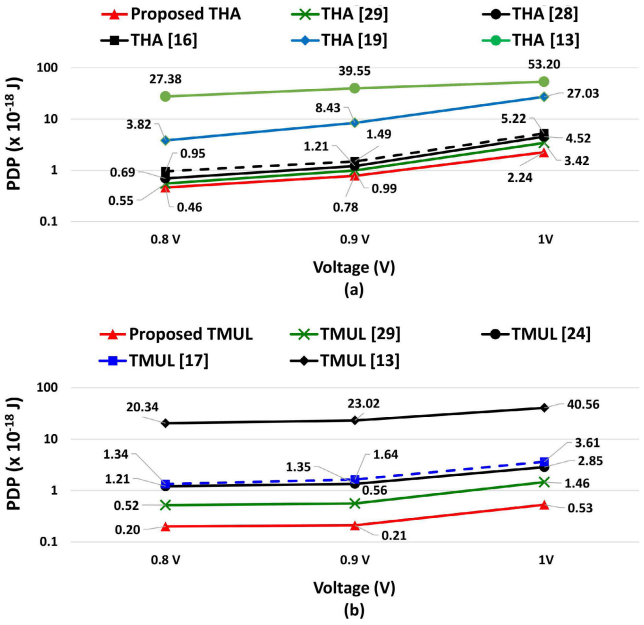

FIGURE 12. Voltage variation with T = 27 °C and F = 1 GHz: (a) THAs, (b) TMULs.

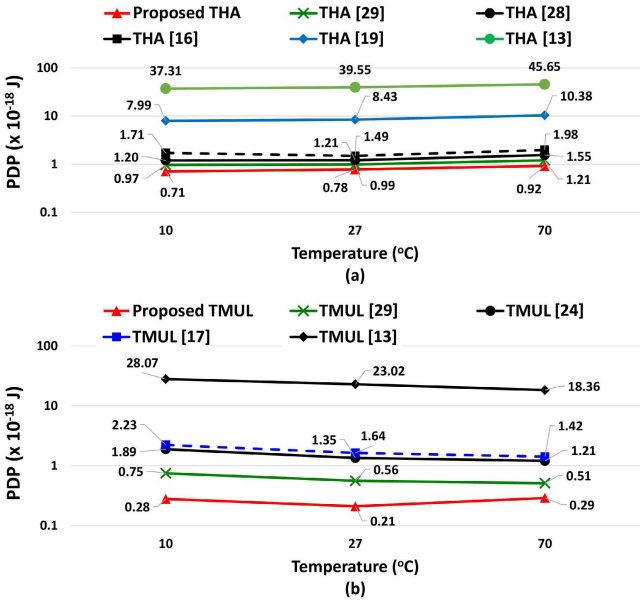

FIGURE 13. Temperature variation with V_{dd} = 0.9 V and F = 1 GHz: (a) THAs, (b) TMULs.

Figure 14 displays the PDP variations of THAs and TMULs compared to existing THA and TMUL of [13], [16], [17], [19], [24], [28], and [29] in the presence of major process variations (CNT's Count, CNT Diameter, Channel length, and TOX). The proposed designs have the lowest PDP variations, and therefore, the highest robustness among other designs.

C. NOISE EFFECT

Noise signals of high width and large amplitude affect digital circuits.

The noise signal with amplitude (V_n) and pulse width (W_n) shown in Figure 15 is injected into the inputs of both THAs

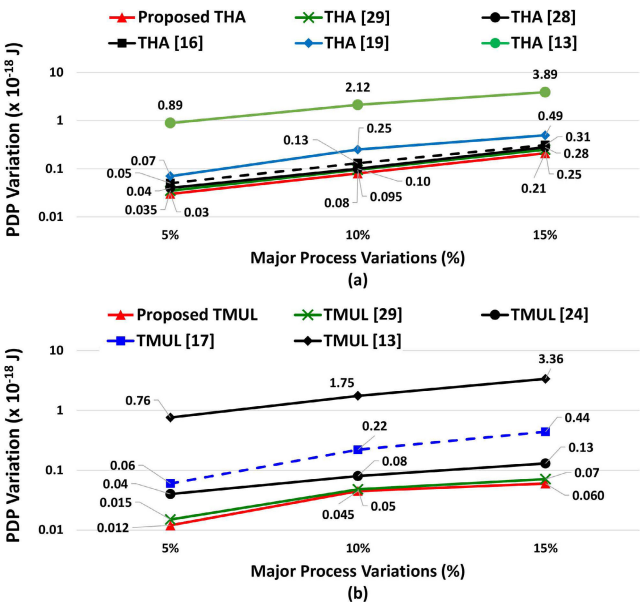

FIGURE 14. Major process variations (CNT's Count, CNT Diameter, Channel length, and TOX) for: (a) THAs, (b) TMULs.

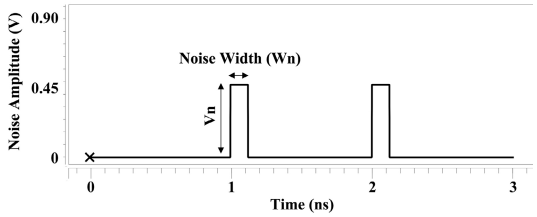

FIGURE 15. Noise signal.

and TMULs. The Noise Immunity Curve (NIC) defines how noisy inputs affect all circuits. Every point sketched on the NIC curve has a noise width *Wn* and a noise amplitude *Vn*. Over that value, an output error will be generated. As a result, a circuit with a higher NIC means a circuit has more noise-tolerant [34].

The proposed THA and TMUL show higher noise immunity compared to the other designs, as shown in Fig. 16.

D. RESULTS DISCUSSION

As previously stated in the introduction, the generation of the logical state 1 ($V_{dd}/2$) in ternary circuits using only one power supply requires the addition of diode-connected transistors to divide the voltage, which drastically increased the static power.

To decrease the power consumption, the static power must be minimized because it consumes about 98% of the average power consumption as described in equation (1a) and analyzed in Fig. 3(c) and (d).

Static power is minimized by (a) using dual-voltage supplies (V_{dd}, $V_{dd}/2$) and removing the diode-connected transistors (b) employing unary operators of the ternary logic system to reduce the number of transistors and (3) dumping standard logic gates, ternary decoders, or ternary encoders because they produce high PDP.

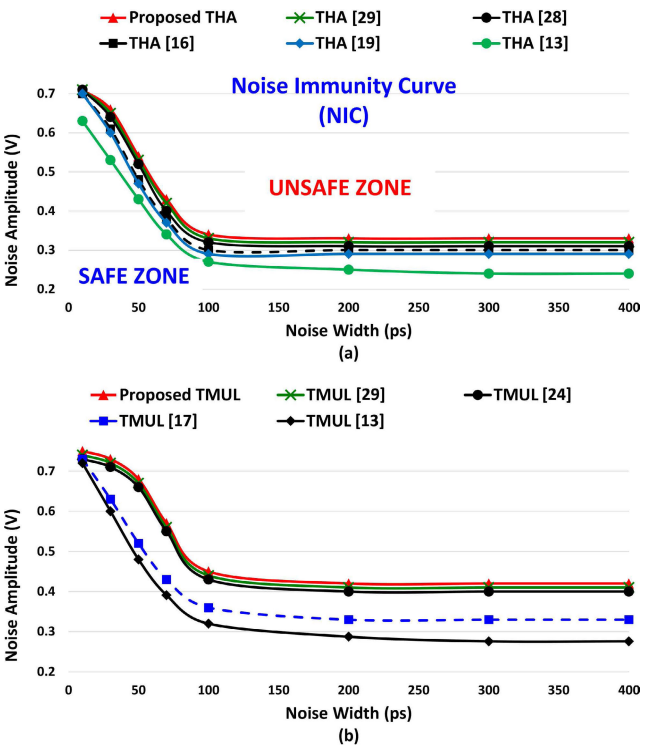

FIGURE 16. Noise Immunity Curve (NIC) for: (a) THAs, (b) TMULs.

The proposed designs take all of the above into consideration to reduce the power consumption by more than 80% in comparison to other designs that employ diode-connected transistors [12]–[15], [18], [19], [21]–[27]. Also, they reduced the power consumption between 21% and 65% compared to [16], [17], [20], [28], [29] that do not employ diode-connected transistors.

This paper adopts techniques similar to our previous work in [29], which proposed a THA and a TMUL using 35 and 26 transistors. However, in this paper, improved designs for unary operators are proposed and employed to design a THA and TMUL with 36 and 23 transistors.

Regarding THA, even though the number of transistors in this work is higher than previous work by one transistor, the new arrangement of transistors in this work proved to be more efficient. In the previously proposed THA in Fig. 17, the unary operator A^1 designed with four transistors and A^2 with 3 transistors, whereas in this work, Fig. 8 presents new designs for the unary operator A^2 with four transistors and A^1 with 3 transistors to get better performance. Also, we use in this paper B^2, which is similar to A^2 instead of B^1 in the previous work.

As for the TMUL, the two unary operators B^1 (3 CNFETs) and $\bar{B}^1$ (2 CNFETs) in Fig. 18 are replaced by one transmission gate (2 CNFETs) in Fig. 9, which reduces the number of transistors by three and provides better results.

VI. CONCLUSION

This paper proposed novel 32 nm channel CNFET-based designs of eight Unary Operators to design a Ternary Half

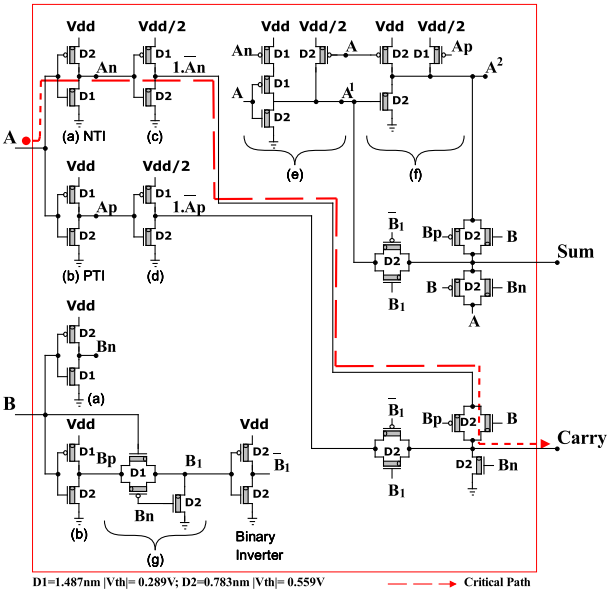

FIGURE 17. Previous THA with 35 CNTFETs [29]: (a) NTI, (b) PTI, (c) $1 \cdot \bar{A_n}$, (d) $1 \cdot \bar{A_p}$, (e) A^1, (f) A^2, and (g) B_1.

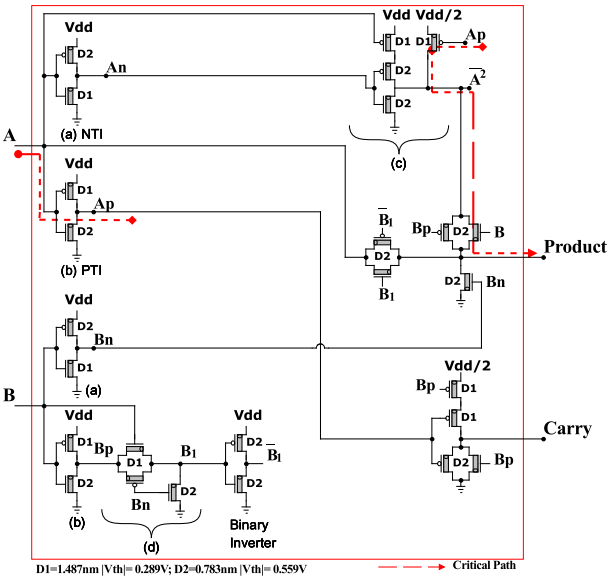

FIGURE 18. Previous TMUL with 26 CNTFETs [29]: (a) NTI, (b) PTI, (c) $\bar{A^2}$, and (d) B_1.

Adder with 36 transistors and a Ternary Multiplier with 23 transistors.

To achieve the objective, the design process employed different techniques to decrease the overall energy consumption in the circuit by using unary operators, two voltage supplies V_{dd} and $V_{dd}/2$, and transmission gates.

After simulating the proposed designs using HSPICE, the proposed circuits achieved a lower PDP against all the investigate circuits for different simulation parameters, PVT variations, and noise effects studies. In addition, the proposed designs proved to have a higher noise tolerance and higher robustness to process variations.

This is aligned with the main purpose of this work, to reduce battery consumption, provide an energy-efficient implementation for low-power portable electronics and embedded devices.

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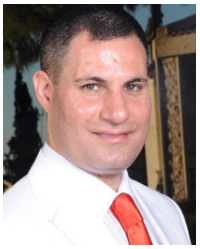

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