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High-Gain Switched-Capacitor DC-DC Converter With Low Count of Switches and Low Voltage Stress of Switches

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ABSTRACT This paper presents a novel concept of a high-voltage-gain DC-DC converter. The converter is made up of switched capacitors and passive resonant branches. A significant reduction in the count of switches and low voltage stress on the switches is achieved in this proposed converter topology, in comparison to that of a classical SC series-parallel converter. It is essential from the cost, volume, and efficiency of the converter standpoint. The reduction in the count of switches is threefold. The highest voltage stress on the switches depends on the output voltage and is decreased in the proposed converter as well, as the output voltage is divided into two series-connected capacitors. The presented results demonstrate the operation of the converter with the use of resonant branches, its switching strategies, voltage stresses of switches, efficiency, voltage gain, and output voltage regulation as well as the zero-voltage switching (ZVS) operation. The paper also presents novel issues related to analytical loss modeling, extended concepts of topology, converter start-up, and operation during transient states. The demonstrated concept of the converter, the analytical discussion and its design, as well as the experimental setup and results clearly demonstrate the optimization achievements.

INDEX TERMS Boost converters, DC-DC converters, high voltage gain converter, switched-capacitor converter.

I. INTRODUCTION

SWITCH-CAPACITOR (SC) circuits can be used in one of the methods for DC energy conversion [1], [2]. The major advantages of the switched-capacitor-based DC-DC converters are high voltage gain and magneticless design. It allows for the decrease in the volume of the converter and its operation in high temperatures, as the converter is not equipped with ferrite-based chokes. Therefore, such converters can be applied to operate at a high ambient temperature. High-voltage-gain converters, especially those in topologies with a common input and output ground, can be applied in low-power photovoltaic systems where the conversion of energy from a low-voltage photovoltaic (PV) string to the grid requires significant voltage boost. Other applications, where the proposed converter could be better suited, can be found in fuel cell energy harvesting systems in automotive applications or DC microgrid systems [3], [4], as well as in high-intensity discharge lamp supply units in vehicle headlights.

The SC converters, which belong to the family of series-parallel systems, have various advantages such as simple topology and control, modular construction, simple gate driver circuits [5], and a regulated number of voltage gains [6]. Therefore, such converters can be attractive when a suitable optimization is introduced. In [7], the authors of this article have presented an optimization of the SCVM topology towards a decrease in the number of switches and the voltage stresses of the components. As a result, the number of switches has been reduced by 50%, which is a great development compared to the SCVM [5]. This idea of optimization is continued in the presented work. The converter

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with a dual output, presented in [7], is further optimized in the novel topology with an intermediate passive branch presented in this paper and a decreased number of switches. For the six-fold voltage gain, four switches are required. Furthermore, the voltage stress of switches is significantly reduced compared to that of the classical series-parallel converter [5], which decreases C_{oss} loss. The output capacitance parameter, its large signal characterization, as well as the energy stored (E_o) and dissipated versus drain-source voltage (V_{DS}) are discussed [8].

High-voltage-gain SC converters and converters with a low number of switches have been the subject of interest in [9]–[22]. In [9], an SC converter is demonstrated that uses two switches. The converter uses diodes as well, and the number of diodes depends on the voltage gain. The first switching cell is made up of two transistors, a switched capacitor, and a resonant inductor. The connection in a series of the next switching cells, composed of diodes and capacitors, allows the converter to be extended by larger voltage gains. The converter [9] has a series structure, while the concept proposed in this paper assumes operation in a series/parallel topology to achieve a higher voltage gain. For this purpose, it uses four switches. The concept proposed in [9] has been improved to the symmetric structure composed of two switched-capacitor cells, which is presented in [10]. It allowed the ZVS operation and output voltage regulation [10]. High voltage gain can also be effectively designed in cascaded converters [16] and [19]. In [19] and [20], a high-voltage-gain multilevel SC converter has been presented. Such a converter, as presented in [20], is very attractive, as it allows bidirectional operation. Furthermore, all switches have the same voltage stress that is significantly below the value of the converted voltage. The converter presented in [21] allows for bidirectional operation with high voltage gain using the SC topology, which provides a small and low-weight converter implementation. The converter proposed in this paper has a lower switch count and is attractive in unidirectional systems. It derives from the series-parallel SC concept that, in an appropriate design, can achieve a high power density [22].

The major disadvantages of the SC converters are a significant number of switches, high voltage stress of switches, and substantial losses associated with the output capacitance discharge (C_{oss} loss). An optimization towards these directions makes a great development in the SC converter technique. In an SC converter based on the series-parallel concept, such as the SC voltage multiplier (SCVM) presented in [5], $2(n-1)$ switches are required to achieve an n-fold voltage gain. Furthermore, the voltage stresses on the switches are not equal in such a topology and reach the output voltage. This limits the voltage gain of such a converter and increases C_{oss} power losses. The transistors of an SCVM do not turn on at zero voltage when the converter operates in the zero current switching mode (ZCS) and the charge stored in the output capacitance of the MOSFET-based SCVM is discharged in each switching period. This produces losses strongly dependent on the voltage stress of the switches. The problem of C_{oss} loss can be overcome by the reduction of voltage stresses on the switches in the SC topology or by the development of a converter where ZVS is applicable. In references [23]–[28], SC converters with the ZVS operation have been presented. In [24], a method of phase shift is applied in a bidirectional SC doubler and voltage regulation is demonstrated. In [25] and [26], research of this method demonstrates a very high efficiency of the converter in this topology and a phase-shift method. The ZVS operation is presented for the Dickson resonant SC converter in [23] and in [27], [28] for families of resonant SC converters.

In some concepts, such as [17] and [18], the converter uses switched capacitors and inductors to achieve high voltage gain, decrease in the number of switches, and output voltage regulation by duty cycle control. However, the concepts assume the use of significant inductors when compared to the inductive resonant components used in the converter analyzed in this paper. In the resonant SC converter discussed in this paper, the resonant inductors of L=1.27μH designed as planar PCB components are implemented. In the switched capacitor and inductor converters, inductive parts with higher values are implemented (220 μH in [17], 150 μH in [18]).

The topology proposed in this paper allows for a reduction of C_{oss} loss by the ZVS operation and the limitation of the number of switches despite a relatively high voltage gain. The ZVS method allows one to turn on a switch at zero drain-source voltage. It requires reverse current flow just before the switch turns on, which is achieved by the special control presented in Sections II H and III D.

The output voltage regulation is an essential feature of power converters; however, some SC-based topologies operate with a fixed voltage ratio. In [29] and [30], the output voltage change of the SC converter is possible, but only in the step mode. However, continuous voltage control can be achieved using an adequate topology and switching method, which has been demonstrated in [23]–[25], [27], [28], and [31]. In this paper, we propose a converter that allows for a continuous voltage change over a wide range. In the proposed topology, this is accomplished by a method that uses switching frequency adjustment. In [32]–[34], resonant step-up converters have been discussed. All presented topologies are converters with PWM-controlled voltage gain and can be assigned to a switched-capacitor-inductor converters family.

An important aspect of future SC research may be the selection of durable capacitors, which is important in the commercial applications of the device. In [35] and [36], the authors have focused on identifying the stability and reliability parameters of capacitors that will withstand many reload cycles and operation at high temperatures. In the proposed SC converter, the capacitor voltage value is not even half the output voltage.

The concept of the proposed converter [37] presents a substantial improvement of the original topology demonstrated in the conference proceedings [7] by the authors of this paper. The converter is optimized towards the number of switch reduction, continuous output voltage control, and

reduced C_{oss} loss by implementing the ZVS. Therefore, the concept presented in this paper makes novel contributions to existing knowledge. Furthermore, together with the previous idea presented in the conference paper [7], a considerable progress is achieved by reducing the number of switches, the voltage stresses of switches, the current stresses of the components, and the output voltage regulation in the series-parallel SC topologies.

The paper is organized as follows. Section II presents the theoretical aspects of the proposed DC-DC converter. Section III contains the results of the laboratory measurements of the proposed system. The waveforms of the voltages and the input current are presented. An efficiency test for a variable load is included in the chart. Moreover, the possibility of the output voltage control has been tested. Section IV concludes the article and includes the proposed topics for future research.

II. CONCEPT OF THE NOVEL CONVERTER

A. PRINCIPLE OF OPERATION

The proposed converter is presented in Fig. 1. The principle of its operation assumes the charging of the output capacitors (C_{out1} and C_{out2}) independently by the switched-capacitor network. The output voltage is a sum of voltages on C_{out1} and C_{out2}. Before an output capacitor is charged, the internal capacitors (C_1–C_3) are charged from the input source. The SC network contains the intermediate resonant branch L_2C_2, which does not contain any switches or diodes, but boosts the effect of voltage gain. The converter achieves a theoretical voltage gain $G = 6$ with the utilization of four switches ($S = 4$) and is hereinafter called SCVMg6s4. Using resonant circuits, the converter can operate in the zero-current switching (ZCS) mode. By the output voltage division, the maximum voltage stress on the switches should not exceed half of the output voltage, which is very favorable from the switching power loss standpoint.

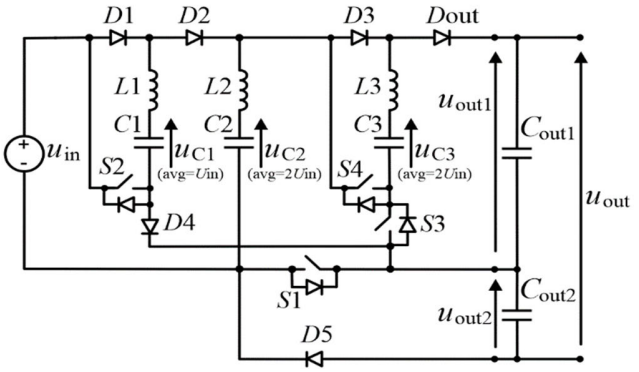

FIGURE 1. The novel concept of SC high-voltage-gain converter (voltage gain $G = 6$ and the number of switches $s = 4$) - SCVMg6s4.

The operation of the SCVMg6s4 is based on the use of the charging states presented in Fig. 2 in the following way:

- state A (S_1 = ON; S_2, S_3, S_4 = OFF): capacitor C_1 is being charged from the input source,

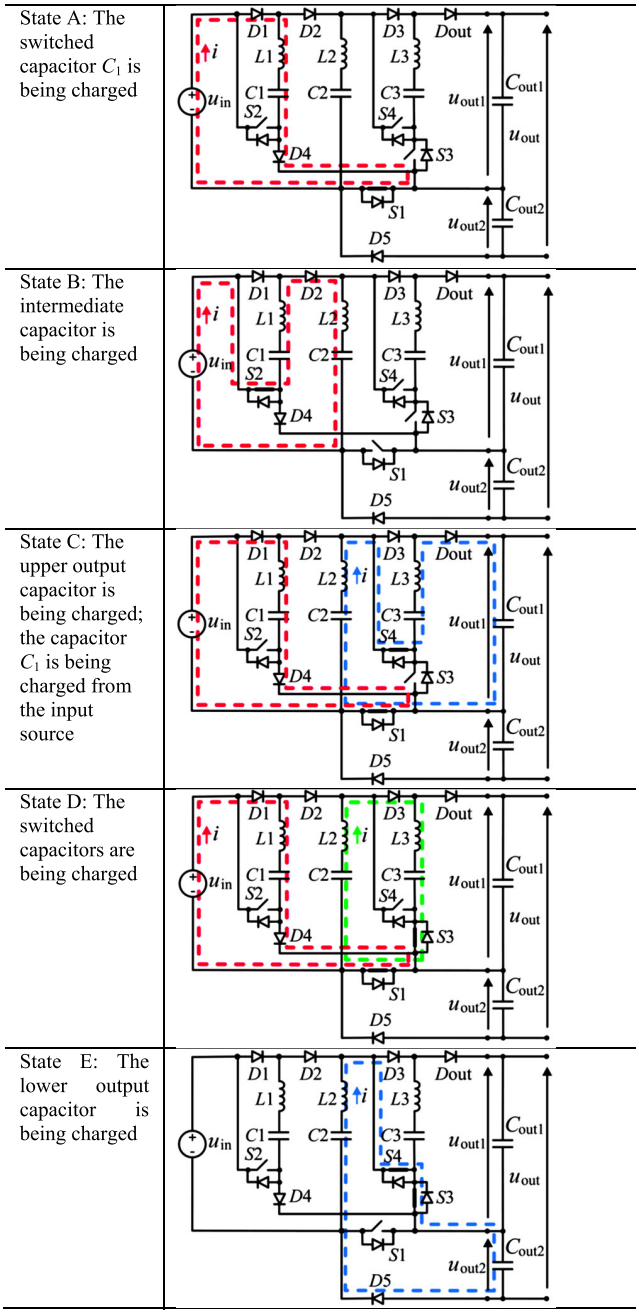

FIGURE 2. The states of charging capacitors in SCVMg6s4 (Fig. 1).

- state B (S_2 = ON; S_1, S_3, S_4 = OFF): the intermediate capacitor C_2 is being charged from the input source and capacitor C_1.

- state C (S_1, S_4 = ON; S_2, S_3 = OFF): capacitor C_1 is being charged from the input source; the upper output capacitor is being charged from capacitors C_2 and C_3.

- state D (S_1, S_3 = ON; S_2, S_4 = OFF): two switched capacitors are being charged – C_1 from the input source, while C_3 – from the intermediate capacitor C_2.

- state E (S_3, S_4 = ON; S_1, S_2 = OFF): the lower output capacitor is being charged from the intermediate capacitor C_2.

In SC converters operating in the ZCS mode, the switching periods are longer than those corresponding to the resonant frequency of the *LC* circuits. Therefore, the current pulses are separated by a dead time, which ensures a tolerance for *LC* parameter mismatch. However, a small mismatch in *LC* will not have a significant impact on the converter gain and operating conditions under the ZVS operation. For a larger difference in the *L* or *C* values in the converter, the switching subperiods can be adjusted at the design stage.

B. SWITCHING PATTERN

The switching pattern proposed for the SCVMg6s4 converter consists of the switching states (Fig. 2) that appear in a suitable order. To achieve the lowest ripples of voltages and currents in the converter, the following requirements are assumed for the proposed switching pattern:

- no internal capacitor (C_1, C_2, or C_3) is charged or discharged twice in a row,
- in each state presented in Fig. 2, the pulses of the input current should be comparable to each other. The only exception is state E, where the input current does not flow (Fig. 3).

The switching pattern that complies with the above assumptions is composed of the following states (Fig. 3):

$$\mathrm{SP1} = \{\mathrm{A}, \mathrm{B}, \mathrm{C}, \mathrm{B}, \mathrm{D}, \mathrm{B}, \mathrm{E}, \ldots\} \tag{1}$$

Fig. 3 presents the proposed switching pattern SP1 and demonstrates how the converter operates under the ZCS (zero current switching) condition. It also defines the oscillation time T_p and the operation (switching) period T_op. The oscillation time is associated with the *LC* parameters of the resonant circuits where the current flows during the charging and discharging of the switched capacitors. The resonant frequency of each of these circuits is the same. Therefore, the oscillation time T_p can be expressed as follows:

$$T_\mathrm{p} = \pi\sqrt{LC} \tag{2}$$

The operation period is made up of seven cycles:

$$T_\mathrm{op} = T_\mathrm{S} = \frac{1}{f_\mathrm{S}} = 7T_\mathrm{p} \tag{3}$$

The simulation results presented in Figs. 3 and 4 were performed in Matlab/Simulink software. The model contains parameters of nonideal switches and stray resistances of the circuits with the values corresponding to those of the experimental setup [Eq. (18)]. The parameters are assembled in Table 1 and are used in the analytical research as well. They were obtained from the datasheets of the components, measurements of the passive components, and the estimation of the other PCB stray resistances.

C. THE IDEAL VOLTAGE GAIN AT ZCS

From the switching concept presented in the previous subsection and the simulation results (Fig. 3), it follows that each internal capacitor (C_1, C_2, or C_3) has the same charging and discharging rate affected by a single pulse of current (visible in Fig. 3 as a component of the input current):

$$\Delta u = \mathrm{f}(i_{LC}, P_\mathrm{out}) \tag{4}$$

However, the idealized average value of the voltage on C_2 is:

$$U_{C1\mathrm{av}} = U_\mathrm{in} \tag{5}$$

The capacitor C_2 is charged in state B in the circuit with U_in and C_1 connected in series. In state A, the capacitor C_3 is charged from C_2. Thus, the average values are as follows:

$$U_{C2\mathrm{av}} = U_\mathrm{in} + U_{C1\mathrm{av}} = 2U_\mathrm{in} \tag{6}$$

$$U_{C3\mathrm{av}} = U_{C2\mathrm{av}} = 2U_\mathrm{in} \tag{7}$$

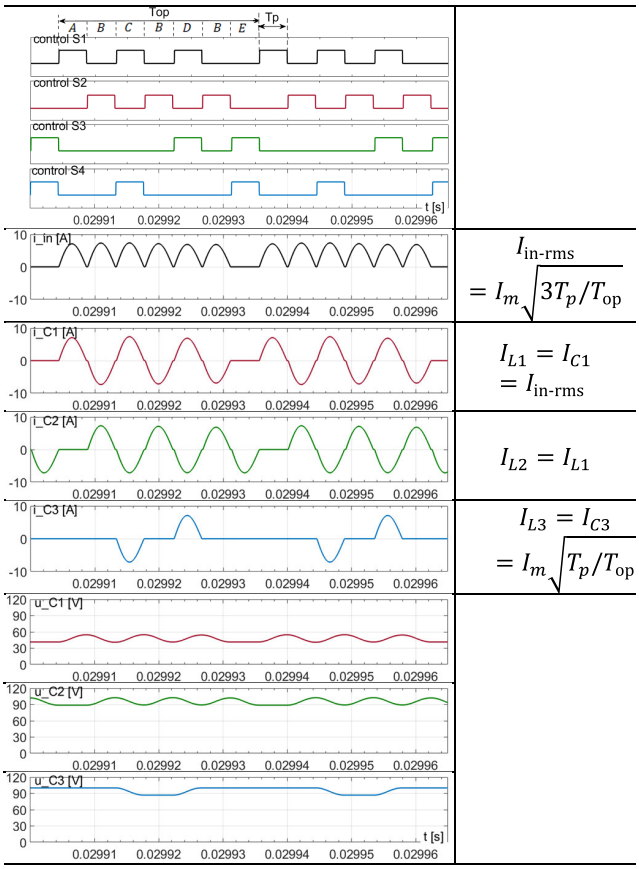

FIGURE 3. Switching strategy SP1 with typical time periods and waveforms of voltages and currents of SCVMg6s4 operating in ZCS mode. Matlab/Simulink results for 200 W of output power. Measured values of capacitor average voltages: $u_{C1\mathrm{av}} = 41.14$ V, $u_{C2\mathrm{av}} = 84.81$ V, $u_{C3\mathrm{av}} = 96.19$ V. Component parameter according to Table 1.

TABLE 1. Parameters of the converter components in the simulation model.

Parameter	$L_{1\text{-}3}$	$C_{1\text{-}3}$	$R_{\mathrm{DS(on)}}$	ΔU_{Dl} (V_F)	Inductance resistances R_{ESR}	Stray resistances $r_{l\text{-}3}$ of the *LC* branches
Value	1.27 µH	1.47 µF	16 mΩ for S_1, S_2 S_4; 42 mΩ for S_2	0.6 V for D_1 - D_4; 1.0 V for D_5, D_out	84.11 mΩ	40 mΩ

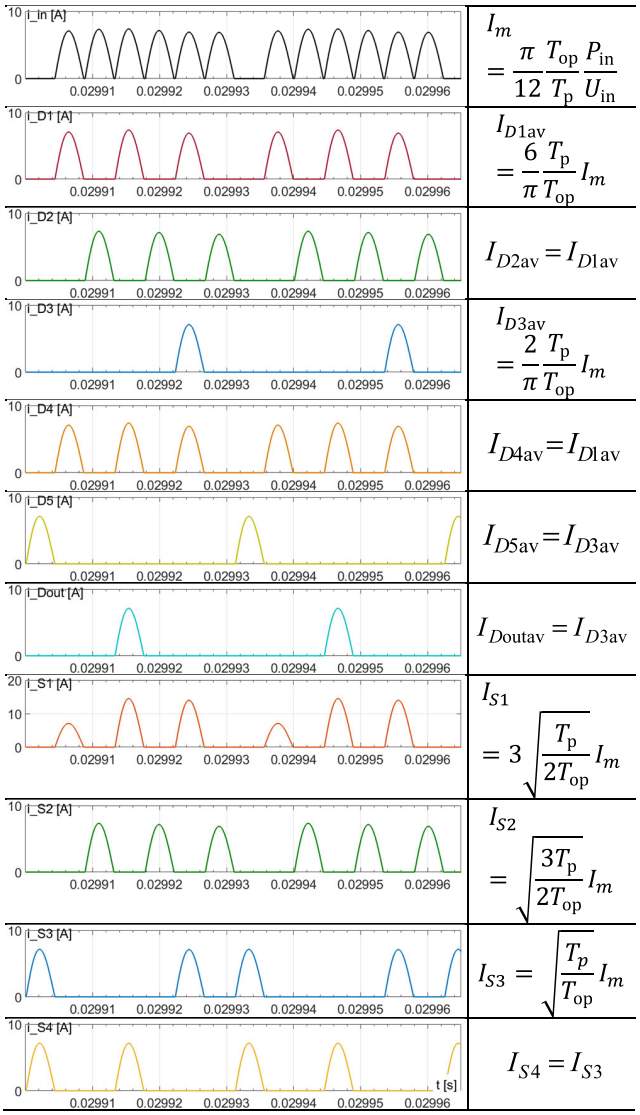

FIGURE 4. **Current stresses of diodes and switches. Parameters of the model as in Table 1.**

The output capacitor C_{out1} is charged by the capacitors C_2 and C_3 connected in series, and the output capacitor C_{out2} is charged by the capacitor C_2. Therefore, the output voltages are

$$U_{out1} = U_{C2av} + U_{C3av} = 4U_{in} \quad (8)$$

$$U_{out2} = U_{C2av} = 2U_{in} \quad (9)$$

$$U_{out} = U_{out1} + U_{out2} = 6U_{in} \quad (10)$$

In the extended version of the converter, the output voltage can be increased by the additional output section (Fig. 5a) or by the input doubler (Fig. 5b). The methods give the following voltage gains:

$$U_{out\_ex1} = 4U_{in} + 2U_{in} + 2U_{in} = 8U_{in} \quad (11)$$

$$U_{out\_ex2} = 2 \cdot (4U_{in} + 2U_{in}) = 12U_{in} \quad (12)$$

The selection of the capacitance of the switched capacitors is associated with the output power of the converter and its

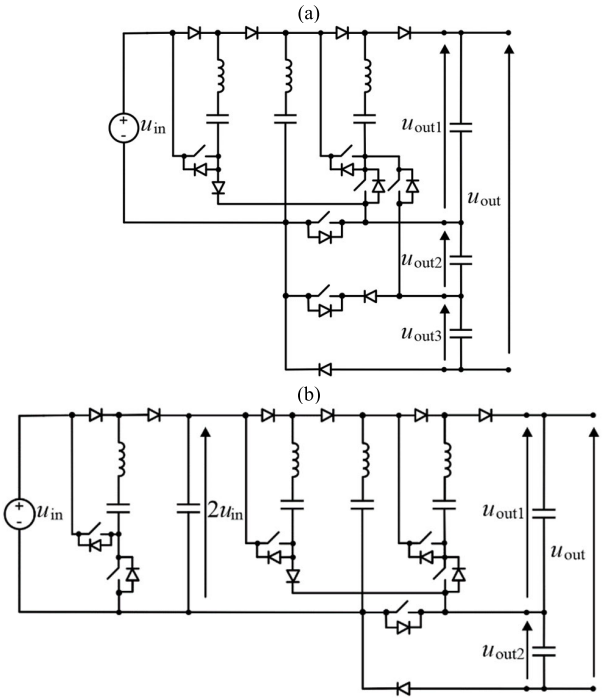

FIGURE 5. **Extended versions of the converter: a) *G*=8, b) *G*=12.**

operating frequency, similarly to that of a classical series parallel converter [5]. The switching frequency is determined by the switching losses of the semiconductor devices in the circuit. Resonant inductors are required to avoid inrush currents in the SC converters. The currents in the *LC* circuits should oscillate within the time T_p, which is comparable to the oscillation half-period. The resonant choke can be designed as an air-based one or can use parasitic inductance. However, too high a resonant frequency in relation to the switching frequency can deteriorate the efficiency of the SC converter. The approach to justifying the inductor value in such a series-parallel converter is presented in [5], [6]. For the selection of switches, voltage stresses are essential; therefore, they are presented in Section III. The voltage stress affects the blocking voltage of a switch and, finally, the drain-source resistance. The voltage stresses on the switches are associated with C_{oss} loss, as the transistors in the SC converters turn on with the output capacitance charged. The switch type selection for a high-frequency operation requires minimizing $R_{DS(on)}$ and C_{oss} together. According to the conduction loss model presented in [5], the selection of diodes for an SC series-parallel converter should assume the forward voltage (V_F) minimization.

The selection of the output capacitors should consider the frequency of energy transfer to the output capacitors. The charging of the output capacitor occurs with a frequency decreased in relation to the switching frequency. From Figs. 2 and 3, it is seen that the output capacitor (C_{out1} or C_{out2}) is being charged through the time T_p (2), but is being discharged through the time (Fig. 3):

$$T_{Cout1diss} = T_{Cout2diss} = T_{op} - T_p = 6T_p \quad (13)$$

Assuming that the output capacitor is being discharged by the constant output current I_{out} in the time interval $T_{\text{Cout1diss}}$ (13), its voltage change is as follows:

$$\Delta U_{\text{out1,2}} \geq \frac{I_{\text{out}}}{C_{\text{out1,2}}} T_{\text{Cout1diss}} \tag{14}$$

where $\Delta U_{\text{out1,2}}$ means ΔU_{out1} or ΔU_{out2}, respectively. Similarly, $C_{\text{out1,2}}$ stands for C_{out1} or C_{out2}, respectively. Therefore, the output capacitors that ensure the assumed output voltage ripples should be equal to

$$C_{\text{out1,2}} \geq 6T_{\text{p}} \frac{I_{\text{out}}}{\Delta U_{\text{out1,2}}}. \tag{15}$$

In a single operation period T_{op}, both output capacitors are charged, which increases the frequency of the output voltage ripple two times. Assuming that $I_{\text{out}} = 1$ A, $\Delta U_{\text{out1,2}} = 12$ V and $f_0 = 120$ kHz, $C_{\text{out1,2}} \geq [6/(120{\cdot}10^3)]{\cdot}(1/12) = 4.2$ μF.

The simulation results presented in Figs. 3–4 mainly demonstrate the concept of converter operation and that of the efficiency model based on the input current distribution among the devices.

D. EFFICIENCY

Figures 3, 4, 17, 18, and 22 relating to the operation under the switching strategy SP1 show that the amplitudes of all input current pulses are nearly the same. Therefore, it can be assumed that they are equal to I_{m}. This amplitude calculated from (Fig. 3):

$$I_{\text{inav}} = \frac{12}{\pi} \frac{T_{\text{p}}}{T_{\text{op}}} I_{\text{m}} = \frac{P_{\text{in}}}{U_{\text{in}}} \tag{16}$$

is equal to:

$$I_{\text{m}} = \frac{\pi}{12} \frac{T_{\text{op}}}{T_{\text{p}}} I_{\text{inav}} = \frac{\pi}{12} \frac{T_{\text{op}}}{T_{\text{p}}} \frac{P_{\text{in}}}{U_{\text{in}}} \tag{17}$$

and is also the amplitude of all current pulses of the diodes and transistors except that of transistor S_1 (two pulses of amplitude $2I_{\text{m}}$ and one pulse of amplitude I_{m}). It is essential to keep in mind that I_{inav} and I_{m} are also affected by the converter parameters such as forward voltage drops of the diodes and all parasitic resistances.

Based on the aforementioned assumption and taking into account the drain-to-source on-resistances of the transistors, the forward voltage drops on the conducting diodes, the stray resistances of the inductances and circuits on the PCB, as well as the turn-on losses in the transistors, the inverter efficiency can be calculated.

The total conduction losses are the sum of the conduction loss ΔP_1 in the transistors, the loss ΔP_2 in the diodes, and the loss ΔP_3 in other stray resistances

$$\begin{aligned} \Delta P_{\text{C}} = \Delta P_{\text{C1}} + \Delta P_{\text{C2}} + \Delta P_{\text{C3}} &= \sum\nolimits_{k=1}^{4} R_{\text{DS(on)}k} I_{Sk}^2 \\ &+ \sum\nolimits_{l=1}^{5} \Delta U_{Dl} I_{Dl\text{av}} + \Delta U_{D\text{out}} I_{D\text{out-av}} \\ &+ \sum\nolimits_{m=1}^{3} (r_{\text{ESR}m} + r_m) I_{Lm}^2 \end{aligned} \tag{18}$$

where $R_{\text{DS(on)}k}$ denotes the drain-to-source on-resistance of the transistor S_k, ΔU_{Dl} and $\Delta U_{D\text{out}}$ are the forward voltage drops across diodes D_l and D_{out}, $r_{\text{ESR}m}$ is the resistance of inductance L_m, r_m is the stray resistance of the PCB in the circuit of inductor L_m. I_{Sk} and I_{Lm} are RMS values of the transistor and inductance currents, respectively, and $I_{Dl\text{av}}$ and $I_{D\text{out}-\text{av}}$ are the average values of the diode currents.

Moreover, it is assumed that the voltage drops across the diodes remain constant in the conducting state. The values of currents I_{Sk}, I_{Lm}, $I_{Dl\text{av}}$, and $I_{D\text{out}-\text{av}}$ depend on the current shape and are given in Figs. 3–4 as functions of I_{m} (17).

The turn-off switching loss is practically zero, due to the ZCS switching. However, there is a turn-on switching loss associated with charging and discharging the output capacitances of the MOSFETs. The total switching power loss ΔP_{SW} is:

$$\Delta P_{\text{sw}} = \Delta W_{\text{sw}} f_S = \frac{\Delta W_{\text{sw}}}{T_{\text{op}}} \tag{19}$$

where: ΔW_{SW} is the energy lost at turn-ons in the MOSFETs' resistances (C_{oss} loss) in a single switching cycle T_{op}. A way to calculate these losses is presented in [40].

The overall efficiency equals:

$$\eta = 1 - \frac{\Delta P_{\text{C}}}{P_{\text{in}}} - \frac{\Delta P_{\text{sw}}}{P_{\text{in}}} \tag{20}$$

The relationship between efficiency (20) and the input power P_{in} of the converter is presented in Fig. 6. It was assumed that

$$\begin{aligned} L_1 &= L_2 = L_3 = L, C_1 = C_2 = C_3 = C, \\ \Delta U_{D1} &= \Delta U_{D2} = \Delta U_{D3} = \Delta U_{D4}; \Delta U_{D5} = \Delta U_{D\text{out}}, \\ R_{\text{DS(on)1}} &= R_{\text{DS(on)2}} = R_{\text{DS(on)4}}, r_{\text{ESR1}} = r_{\text{ESR2}} = r_{\text{ESR3}} \\ &= R_{\text{ESR}}, r_1 = r_2 = r_3. \end{aligned} \tag{21}$$

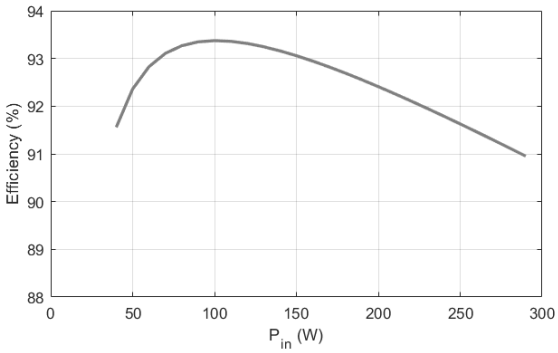

FIGURE 6. Efficiency of SCVMg6s4 operating under switching strategy SP1 versus input power. Model parameters as in Table 1 at $U_{\text{in}} = 50$ V and $\Delta W_{\text{SW}} = 60$ μJ.

The converter parameters used in the simulation are given in the caption of the figure below and approach those of the experimental model in Fig. 16 and Table 5. Furthermore, the $T_{\text{op}}/T_{\text{p}}$ ratio was assumed to be 7, as can be seen in all simulations and measurements presented in the paper.

The current I_m and efficiency are functions of the T_{op}/T_p ratio (Fig. 3), where T_p is the duration of each current pulse. The variation in the inductance L will have no effect on the efficiency if the switching period T_{op} is modified to keep the ratio T_{op}/T_p constant. However, if this ratio varies, this will affect the value of current I_m and efficiency.

Fig. 7 and Table 2 present a comparison of the types of losses in the proposed converter and the losses calculated for the particular devices. In this comparison, the voltage and current stresses of the switches related to the output voltage and the input current, respectively, are also presented. From the results, it is seen that the devices used operate at low voltage stress, which allows for the use of transistors with low $R_{DS(on)}$ and low cost. Furthermore, the current of the converter devices is only a fraction of the input current. Power losses are distributed among many devices as well. Therefore, the problem with the profitability of the proposed converter compared to a classical boost converter is typical for a multilevel converter that contains a large number of components operating at lower voltage and current stresses, as well as with lower losses in the device.

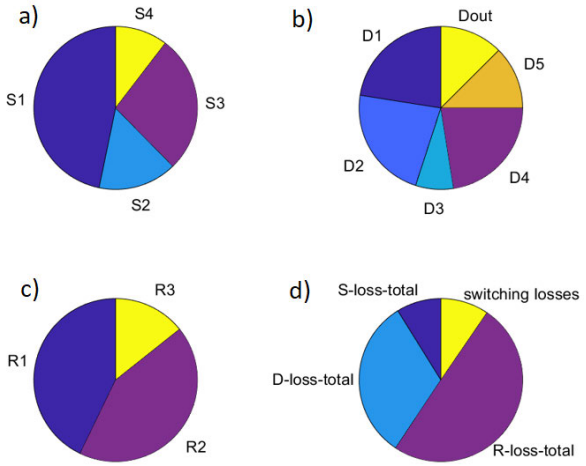

FIGURE 7. Comparison between: a) losses in transistors, b) losses in diodes, c) losses in other stray resistances, and d) various types of losses. Model parameters as in Table 1 at $U_{in} = 50$ V, $\Delta W_{SW} = 60\ \mu$ J, and $P_{in} = 250$ W.

Fig. 7d) shows a big impact of the losses in the diodes and resistances on the efficiency. It could be reduced by using diodes with possibly low forward voltage drops and minimizing the resistances of the inductors and the PCB.

E. START-UP AND TRANSIENT RESPONSE OF THE SCVM

Fig. 8 shows the simulation results of the start-up and transient response for the load change in the SCVMg6s4 converter. The start-up is carried out by connecting the converter to the 50 V input source with 2 Ω. After the 25-ms period, the charging resistor is bypassed and the output capacitor is charged to the rated voltage.

During the start-up procedure, the overcurrent approaches the two-fold value of the rated input current (for a load of 200 W). The charging resistor can be bypassed when

TABLE 2. Comparison of operational parameters of the converter components. $P_{in} = 250$ W.

	S_1	S_2	S_3	S_4	D_1	D_2	D_3	D_4	D_5	D_{out}	L_1	L_2	L_3
U_{max}/U_{out}	1/3	1/6	1/3	1/3	1/6	1/6	1/3	1/6	1/3	1/3	-	-	-
I_{av}/I_{inav}	-	-	-	-	1/2	1/2	1/6	1/2	1/6	1/6	-	-	-
I_{rms}/I_{inrms}	1.225	0.707	0.577	0.577	-	-	-	-	-	-	1	1	0.577
$P_{loss}/P_{losstotal}$	0.0413	0.0138	0.0241	0.0092	0.0717	0.0717	0.0239	0.0717	0.0398	0.0398	0.2134	0.2134	0.0711

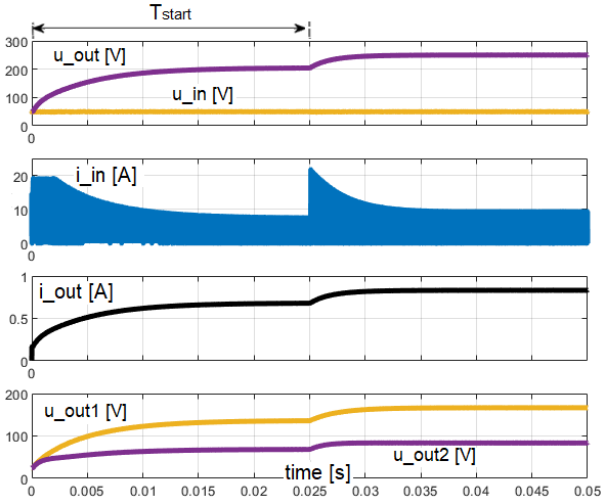

FIGURE 8. Converter start-up (T_{start}) with input charging resistor (2Ω) at 200 W of output power. Switching strategy SP1 of SCVMg6s4 operating in ZCS mode. Matlab/Simulink simulation results.

the output voltage $u_{out1} > u_{in}$. In such a case, turning on transistor S_1 does not cause the source to be shorted by capacitor C_{out1}. Further charging, without bypassing the resistor, uses LC circuits and can be continued with an overcurrent but without inrush currents. Fig. 9 shows a rapid load change – from 200 W to 0 W. From the results (Fig. 9), it follows that the converter in the open-circuit mode represents a first-order type behavior.

F. OUTPUT VOLTAGE CONTROL

The switch S_1 controls the process of charging capacitors C_1, C_3, and C_{out1}. When the switching period of switch S_1 is shorter than the oscillation time in the resonant circuit, less amount of energy is transferred from the source to capacitor C_1 and further to other capacitors (Figs. 10 - 11). The effect of output voltage regulation appears under such a switching strategy.

Similarly to the SC voltage doubler presented in [25], the proposed topology of the converter allows the termination of the transistor currents in three states A, C, and D (Fig. 10).

The operation of the SCVMg6s4 with the output voltage control can use the same switching order (1) with additional

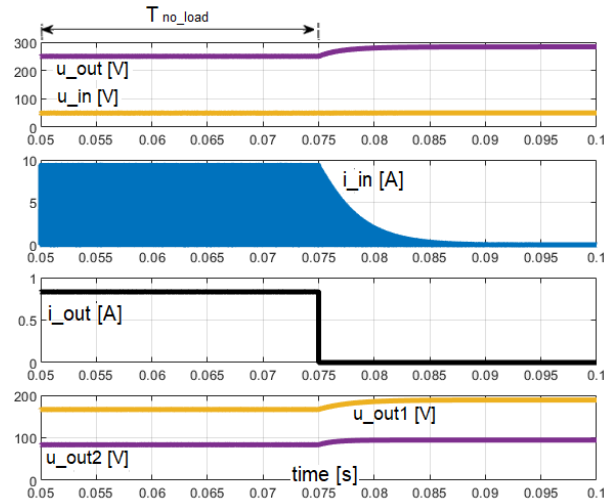

FIGURE 9. Open-circuit operation (T_{no_load}) for the switching strategy SP1 of SCVMg6s4 operating in ZCS mode. Matlab/Simulink results. Parameters of the model as in Fig. 3.

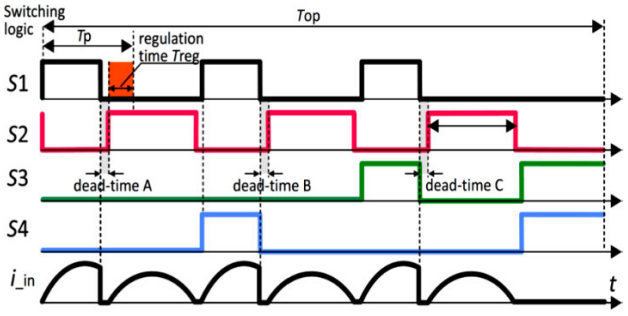

FIGURE 10. Modification of the proposed switching pattern SP1 (1) for output voltage control.

states where the appropriate diodes and freewheeling diodes are activated (Table 3). The turn-on times of the remaining switches used in states A, C, and D are shorted in the same way as in the case of S_1. Fig. 10 presents one period of the proposed switching pattern for the output voltage regulation. Fig. 11 shows the current flow in state A and state B with dead times. This phase-shift method is used in [24]–[26].

TABLE 3. Diodes activated after current termination in states (A, C, and D) (Fig. 11).

Stage	Active diodes	Active freewheeling diodes
Dead-time A	D_1	D_{S2}
Dead-time B	D_1, D_3, D_5, D_{out}	D_{S2}, D_{S3}
Dead-time C	D_1, D_3, D_5, D_{out}	D_{S2}, D_{S4}

G. INPUT CURRENT FILTERING

The input current of the converter is made up of high-frequency pulses. The use of a classical passive *LC* filter (Fig. 12) allows one to effectively reduce the source current fluctuations.

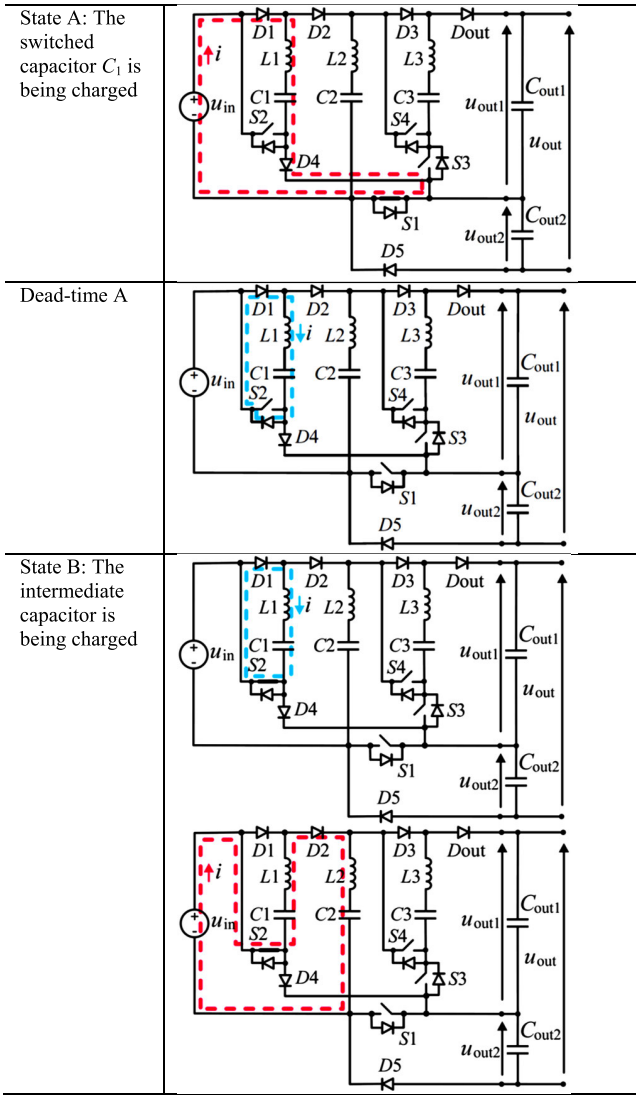

FIGURE 11. Conversion from state A to state B with the dead-time A state when the output voltage control is used.

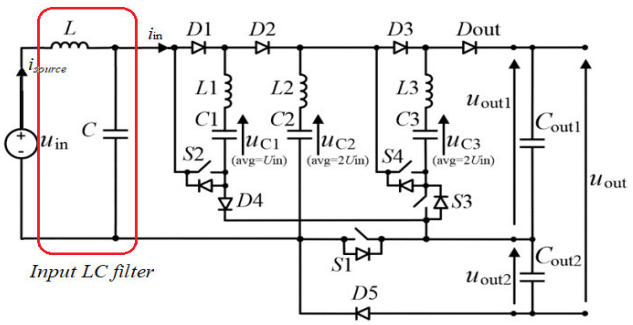

FIGURE 12. SCVMg6s4 converter with *LC* input filter.

The lowest frequency of the input current spectrum is the following:

$$f_{op} = \frac{1}{T_{op}} = \frac{1}{7T_p} \tag{22}$$

This component of the frequency f_{op} is effectively damped to approximately 5% of the average value of the input current, when an LC filter composed of a 10 μH inductor and a 100 μF capacitor is used (Fig. 12). The components with higher frequencies, especially about the frequency f_{osc}, become insignificant in the source current, as seen in Fig. 13.

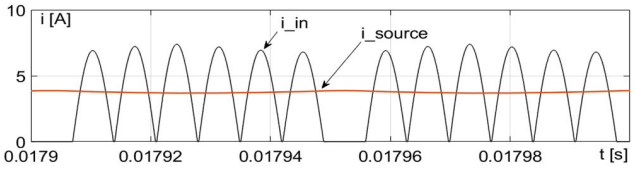

FIGURE 13. The input current of the converter (i_{in}) and the current of the supply source (i_{source}).

H. ZERO VOLTAGE SWITCHING CONDITIONS (ZVS)

The problem of energy dissipation in the structure of a transistor when it is switched on with the charged output capacitance is analyzed in depth in [38], [39]. The problem can be overcome when the output capacitance of the switch is discharged by a reverse current just before its turn-on. In [25] and [38], this is demonstrated in the converters analyzed there. In the proposed topology, transistor S_1 can be turned on at zero drain-source voltage, which is shown in Fig. 10.

When the current of switch $S_1$is terminated in state A, the current of inductor L_1 flows through the freewheeling diode of the switch S_2. The current discharges the output capacitance of the switch S_2 and allows it to be turned on at zero U_{DS} voltage (zero voltage turn-on). In the ZCS mode, switch S_2 is turned on at $U_{DS} = 50$ V. The operation in the ZVS mode reduces the loss of the converter associated with the output capacitance (C_{oss} loss) and allows for an operation at a higher frequency with assumed efficiency. The problem of C_{oss} loss and a method of its reduction by a negative switch current are presented in [38], [39].

The proposed converter derives from a family of series-parallel resonant SC converters. The classic series-parallel switched capacitor voltage multiplier (SCVM) is described in detail in [5]. Table 4 presents a comparison of the SCVMg6s4 with the SCVM and other SC converters derived from the series-parallel concept. Fig. 15 presents the previous version of the investigated converter described in the conference paper [7].

From the comparison of pure SC converters presented in Table 4 and Fig. 14, it is seen that the proposed converter has a very good proportion of the voltage gain to the number of switches and low voltage stress of switches. Therefore, this is a low-cost converter that can be suitable for high-voltage-gain applications. It is more favorable than the cascaded converter composed of a series connection of voltage multipliers. The proposed converter uses three chokes, but these devices have very low energy and volume in SC circuits. The SCVMg6s4 has better parameters than the cascaded converter composed of multipliers [19]. This cascaded

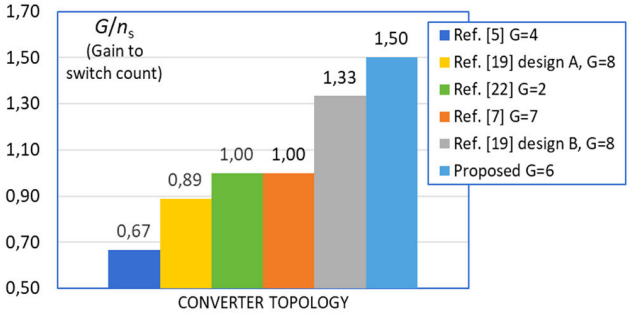

FIGURE 14. Development of SC series-parallel converter switch count. Comparison of voltage gains related to the number of switches between five optimized topologies of series-parallel SC converters.

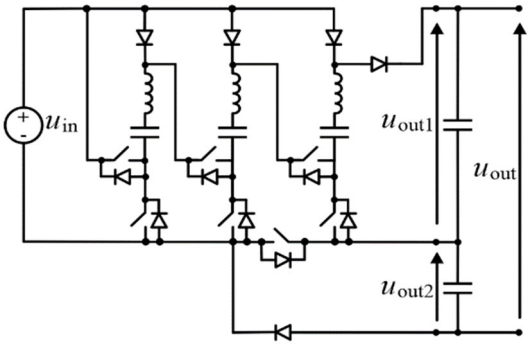

FIGURE 15. SCVMg7s7 converter presented in [7].

converter was analyzed for high-power thyristor-based applications with switches between multipliers (design A in Fig. 14). However, the intersection switches can be replaced by diodes in low-power systems, which is considered in Table 4 and in Fig. 14 (design B). The volume of the presented converter has been presented with the assembled through-hole capacitors and with adequate replacements (for the PCB designed for current tests). It brings about a substantial improvement in the power density of the SCVMg6s4. However, it can still be optimized, because voltage multipliers can achieve a much higher power density, as demonstrated in [22] for the voltage doubler. The number of states required for energy transfer in a single operation period (as in Fig. 2) is also compared with the ripple factor in Table 4, which depends on the number of states connected with the output capacitor in one complete operation period. The SCVMg6s4 requires the use of seven states, and the classical SCVM uses only two. However, the input current pulses occur in six per seven of the switching states (Fig. 4). The output capacitor (C_{out1} or C_{out2}) is charged in every third switching state, whereas in the SCVM it is charged in every second.

III. EXPERIMENTAL RESULTS

A. EXPERIMENTAL SETUP

The SCVMg6s4 has been experimentally investigated to verify the principle of operation, switching concepts, voltage gain, output voltage regulation, voltage stresses on switches,

TABLE 4. Comparison between the proposed converters and SC topologies derived from the series-parallel concept (only reported values of volume and efficiency are presented).

Case	Proposed (Fig.1)	Proposed extended (Fig. 5a)	Proposed extended (Fig. 5b)	Ref. [5]	Ref. [7]	Ref. [9]	Ref. [10]	Ref. [16]	Ref. [19]	Ref. [21]	Ref. [22]
Demonstrated case of a gain G	6	10	14	4	7	2 (extended to n)	G	2-13	8	6	2
Switch count n_s	4	6	6	6	7	2 (2)	4	≈1.2·13 (for G=13)	9-15 (with intersection transistors) 6-14 (with intersection diodes)	12	2
Diode count	6	7	8	4	5	2 ($2n$-2)	4+4G	0	3-7 (with intersection transistors) 6-8 (with intersection diodes)	0	2
Voltage stress across switches	min: U_{in} max: 2/3 U_{out}	min: U_{in} max: 2/3 U_{out}	min: U_{in} max: 2/3 U_{out}	min: U_{in} max:U_{out}	min: U_{in} max: 4/7 U_{out}	U_{in} (U_{in})	U_{in}	min: U_{in} max: ≈0.22·13 (for G=13)	min: U_{in} max:U_{out}	min: U_{in} max:2U_{in}	min: U_{in} max:U_{out}
Inductor count in a demonstrated setup	3x1.27µH, Energy stored: W=0.27 mJ (at P_{in}=300W)	3x 1.27µH	4x 1.27µH	3x 0.627µH	3x 2.97µH	1x1µH (1x1µH)	2	-	1, 2 or 3 higher energy input chokes, depending on the configuration	-	1x 0.83µH
Switched capacitor count	3	3	4	3	3	1 ($2n$-2)	2G	≈0.8·13 (for G=13	3-7 (in one case and two intermediate capacitors required)	4 (and 2 output capacitors)	1
Output voltage control	Possible	Possible	Possible	For G = 2 and adequate design	-	Possible	Possible	Possible	Possible	-	For the adequate design
Efficiency [%]	93.48	-	-	95	91.9	94.4	96.9 simulation result	98.4	-	96.5	97.1
Power value for peak efficiency [W]	104	-	-	200	305	49.6	50	200 for G = 5 300 for G = 6 and 7	-	200	540
Power density [W/dm3]	demonstrated: 468, current design limit: 4855	-	-	-	-	-	-	-	-	-	9330
Input/output common connection	No	No	No	Yes	No	Yes	Yes	Yes	Yes	No	Yes
Number of states in one switching cycle	7	10	7	2	4	2	4	2 (for G=5)	2	2	2
Output voltage ripple factor	2/7	Depends on control / for further research	2/7	1/2	2/4	1/2	1/2	1/2	1/2	2/6	1/2

power losses, efficiency, and temperature field distribution. Fig. 16 presents the photograph of the SCVMg6s4 laboratory experimental setup, and Table 5 contains important parameters of the converter and control modulation. The components are assembled on a PCB board with an area of approximately 162 × 89 mm. However, the setup is not optimized to demonstrate the maximum volume density, but to allow for obtaining credible results of operation.

The volume of the converter (assuming that the height of the MKP capacitor is 41.5 mm) is equal to V ≈ 0.59 dm^3 and the power density is P_D ≈ 468 W/dm^3. The power density of the tested setup deteriorates due to the large dimensions of the input and output capacitors. However, it can be significantly improved by selecting capacitors with low volume, e.g., CERA LINK (with a height of 4 mm). This would allow us to increase the converter's power density up to 10 times (P_D ≈ 4855 W/dm^3) using the existing PCB board. The gate driver circuits have been implemented with multiple bootstrap circuits. The topology and switching of the converter allow the high-side transistors (S_2, S_3, and S_4) to be supplied by bootstrap circuits with parameters presented in Table 5. Dual-channel and single-channel driver types were used in the converter.

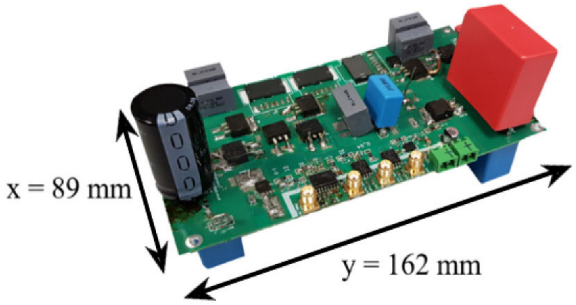

FIGURE 16. The experimental converter - SCVMg6s4.

B. OPERATION OF THE CONVERTER IN ZCS MODE

To verify the basic concept of the operation of the SCVMg6s4, the switching pattern SP1 (1) was used. The experimental waveforms presented in Figs. 17 and 18 confirm

TABLE 5. Parameters of the laboratory converter.

Parameter	Value
Input voltage	50 V
Input capacitor	100 µF ± 20% + 4.7 µF ± 5%
Output capacitor	2 x 4.7 µF ± 5%
Resonant and operating frequency	$f_0 = f_{osc}$ = 116.5 kHz, $f_S \approx$ 35 kHz (ZCS)
SC capacitance	1470 nF
Resonant inductances	Planar chokes: 3F36 Ferrite E18 Core 6 turns in PCB, (L = 1.27 µH and R_{ESR} = 84.11 mΩ at 120 kHz)
PCB: copper thickness	35 µm
PCB: laminate and prepreg	FR4 – ISOLA IS410 (TG 180° C)
Transistors	BSC160N15NS5 (V_{DS} = 150 V, I_D = 56 A, $R_{DS(on)}$ = 16 mΩ), RFS4229PbF (V_{DS} = 300 V, I_D = 45 A, $R_{DS(on)}$ = 42 mΩ)
Dual-channel driver for high and low sides	UCC21520ADWR - 4 A/6 A, dual-channel isolated gate driver
Single-channel driver for high side	1EDI60H12AH - 6.0 A high-side isolated gate driver
Bootstrap circuit capacitor	2 x 1 µF ± 5% + 100 nF ± 5% (1206)
Bootstrap resistor and diode	MURS160T3 diode 600V 1A with resistor $R_{Bootstrap}$ = 2 Ω (1206)
Diodes	VB60170G-E3 (I_F = 2x30 A, V_{RRM} = 170 V, V_F = 0.5 V at 5A, 125°C), STTH30L06 (I_F = 30 A, V_{RRM} = 600V, V_F = 1.0 V)
Controller	FPGA Control Board (Intel MAX10 10M16SAE144C8G)

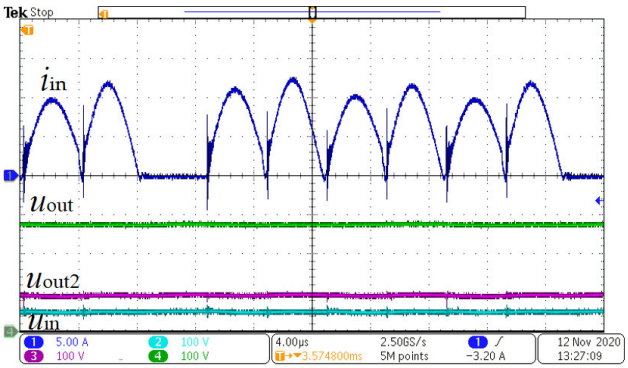

FIGURE 17. Experimental waveforms of SCVMg6s4 in ZCS mode. CH1: input current i_{in}, CH2: 50 V as input voltage, CH3: voltage u_{out2} and CH4: output voltage u_{out}. P_{in} = 300 W, $f_S \approx$ 35 kHz, and U_{in} = 50 V.

that the converter operates according to this pattern (its concept is described in Section II). Fig. 18 shows that the total voltage gain is close to the value $G \approx 6$. In Fig. 18, the switching operation is clearly seen as well. The voltage ripples on the switched capacitors are kept optimal, because each discharging state is followed by a charging one.

Fig. 19 presents the thermography result of the converter operating at P_{out} = 100 W (point of maximum efficiency). Table 6 presents the results of the temperature measurements of the switches, diodes, and planar chokes. From these results, it follows that the heat dissipation in the switches and diodes is not significant and that the surface-mounted semiconductors can be cooled by the PCB itself. However, a heat concentration near the resonant coils can be observed. The traces of the planar choke (~49.2°C) are the hottest points on the PCB.

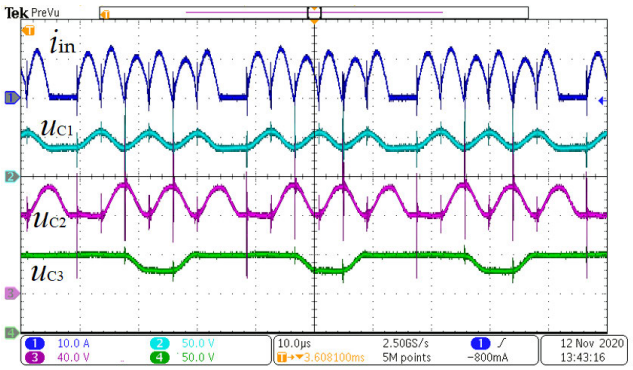

FIGURE 18. Experimental waveforms of SCVMg6s4 in ZCS mode. CH1: input current i_{in}, CH2: voltage across resonant capacitor C_1, CH3: voltage across resonant capacitor C_2, and CH4: voltage across resonant capacitor C_3. P_{in} = 300 W, f_S = 34 kHz, and U_{in} = 50 V.

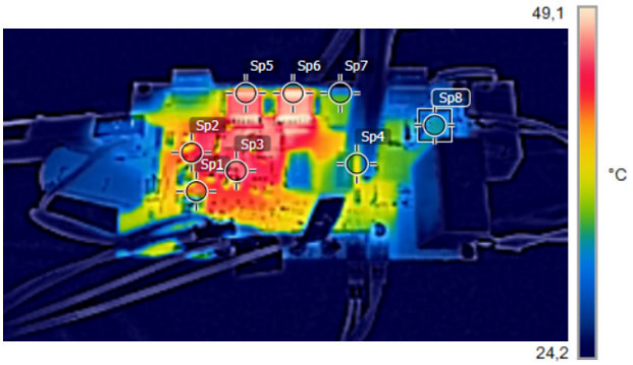

FIGURE 19. The steady-state temperature distribution – infrared photography of the converter. SCVMg6s4 operation with input power equal to 100 W without external airflow.

TABLE 6. Hot spots of the converter (Fig. 19).

Point name	Component	Temperature [°C]
Sp1	Transistor S_1	39.7
Sp2	Transistor S_2	40.9
Sp3	Transistor S_3	43.2
Sp4	Transistor S_4	34.8
Sp5	Inductor L_1	47.1
Sp6	Inductor L_2	49.2
Sp7	Inductor L_3	28.8
Sp8	Output Diode D_{out}	30.1

Fig. 20 presents the graph of voltage gain and efficiency versus input power. A series of measurements have been performed at a fixed switching frequency $f_S \approx$ 35 kHz. The efficiency has been precisely measured with the use of a Yokogawa WT 1500 Power Analyzer. The maximum efficiency of the converter in the ZCS mode was η = 93.43%. The result is rewarding, considering that the test setup has been designed as a low-cost unit (typical 35-micrometer copper thickness on the PCB, planar chokes, and MOSFET switches) and that parasitic resistances can cause overall efficiency deterioration.

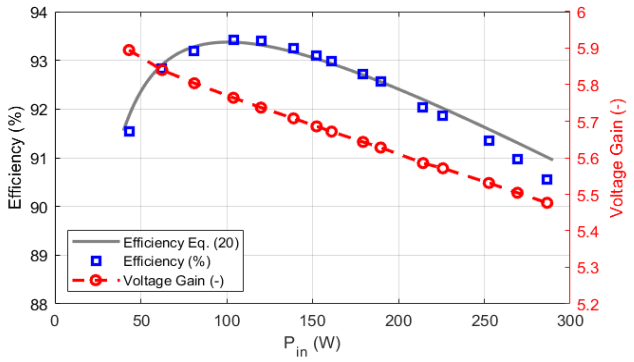

FIGURE 20. Measured voltage gain and efficiency (with theoretical efficiency – Fig. 6) of SCVMg6s4 versus input power at operating frequency $f_S \approx 35$ kHz without external airflow.

Fig. 21 presents the measurements of the drain-source voltages of the switches. From the results, a significant benefit of the proposed topology is seen. The SCVMg6s4 topology ensures lower voltage stresses compared to those of the converters presented in [5], [7], and [19]. The maximum measured voltage on three switches is 100 V at the approximately three times higher output voltage.

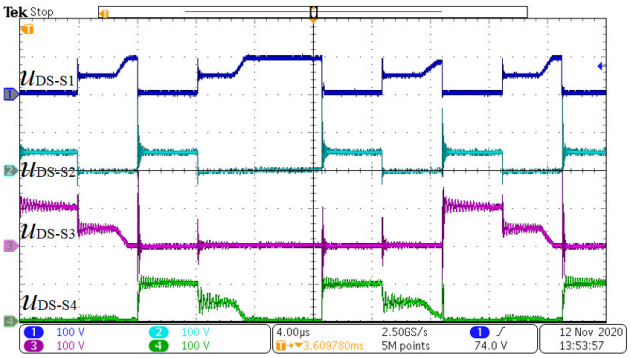

FIGURE 21. Voltage stresses on switches – plots from channels (CH) 1 to 4 denote voltages across transistors 1 to 4, respectively. The test was carried out at a low input power $P_{in} = 50$ W and operating frequency $f_S \approx 35$ kHz.

C. OUTPUT VOLTAGE CONTROL

According to the concept presented in Section II F, the output voltage can be controlled by varying the turn-on time of transistor S_1 (Figs. 9 and 10). Reducing the turn-on time of S_1 below the oscillation time (T_p) decreases the converter voltage gain. This method was verified by experiments, and the results obtained confirm its effectiveness.

Figs. 22–24 present the waveforms of the output voltages and the input current in the case of the operation with the maximum voltage gain (Fig. 22) and with the decreased turn-on time of transistor S_1 (Figs. 23 and 24).

From these results, it follows that decreasing the turn-on time of switch S_1 leads to a decrease in the converter voltage gain. Fig. 25 presents the graph with the output voltage versus output power results. From the results, it follows that the method allows for continuous voltage regulation over a wide

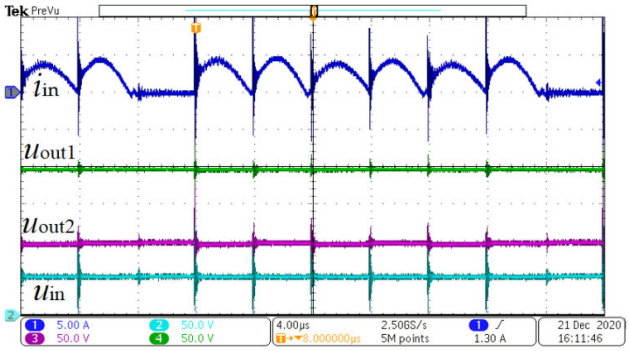

FIGURE 22. Experimental waveforms of SCVMg6s4. CH1: Input current, CH2: input voltage, CH3: output voltage u_{out2}, and CH4: output voltage u_{out1}. $P_{in} = 110$ W and $U_{out} = 287$ V.

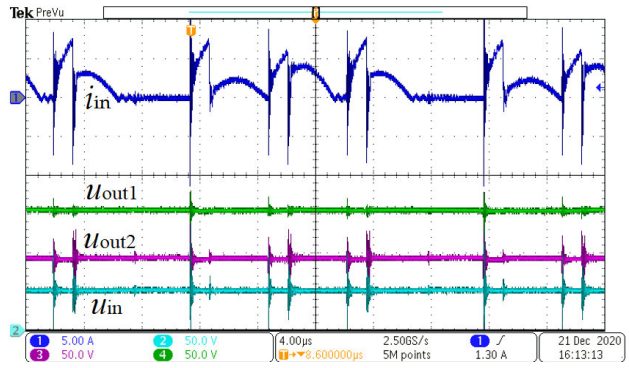

FIGURE 23. Experimental waveforms of SCVMg6s4. CH1: input current, CH2: input voltage, CH3: output voltage u_{out2}, and CH4: output voltage u_{out1}. $P_{in} = 61$ W and output voltage 190 V.

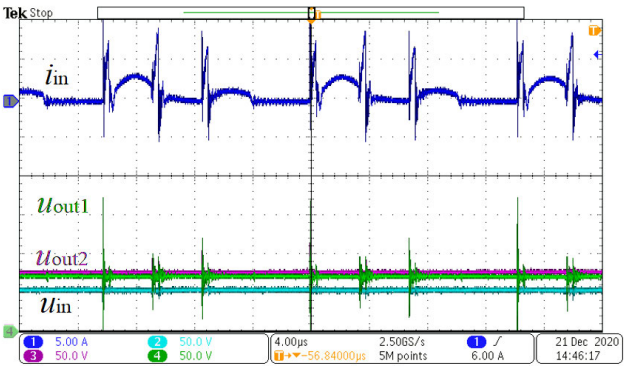

FIGURE 24. Experimental waveforms of SCVMg6s4. CH1: input current, CH2: input voltage, CH3: output voltage u_{out2}, and CH4: output voltage u_{out1}. $P_{in} = 38$ W and output voltage 138 V.

range. Switch S_1 does not operate in the ZCS mode, and additional switching losses may occur in this switch. However, the switch S_2 operates in the ZVS mode, which reduces its C_{oss} loss.

D. OPERATION WITH ZVS

In Section II H, the concept of the implementation of ZVS in switch S_2 was introduced. The method is based on discharging the output capacitance of transistor S_2 by the reverse

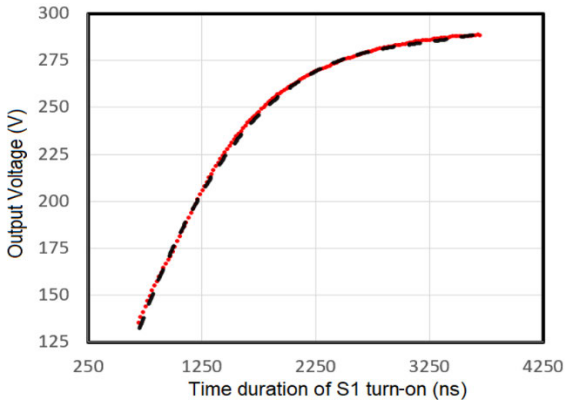

FIGURE 25. Converter output voltage vs. time duration of the S_1 turn-on interval – resistive load (variable values of f_S).

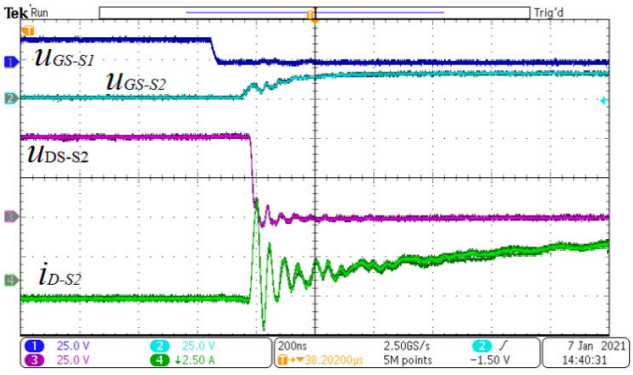

FIGURE 26. Switching of transistor S_1 – ZCS mode. CH1: gate-source voltage of transistor S_1, CH2: gate-source voltage of transistor S_2, CH3: drain-source voltage of transistor S_2 and drain current (S_2).

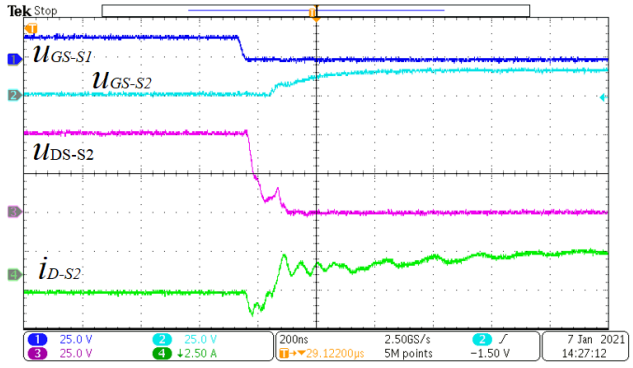

FIGURE 27. Switching of transistor S_2 – ZVS mode. CH1: Gate-source voltage of transistor S_1, CH2: Gate-source voltage of transistor S_2, CH3: drain-source voltage of transistor S_2, CH4: drain current of transistor S_2.

flow of the current in the resonant circuit. To achieve this, switch S_1 is turned off before the time when the current in the oscillatory circuit reaches zero. Figs. 26 and 27 present the experimental results that demonstrate the switching current and voltage when transistor S_1 is turned on. In the case of the ZCS mode (Fig. 26), the drain-source voltage varies from positive to zero, as a result of turning on switch S_2, which causes the C_{oss} loss. The visible rapid increase in drain current during the voltage transition can cause additional switching losses.

The charge stored in the output capacitance is dissipated in the transistor. Additionally, a rapid change in drain-source voltage triggers significant disturbances. In the case of the ZVS operation (Fig. 27), the drain-source voltage of the switch S_2 falls down when the switch S_1 is turned off. A small portion of the negative current is visible in the waveform of the S_2 drain current. Turning on switch S_2 occurs at zero drain-source voltage, which reduces C_{oss} loss and significantly decreases disturbances.

IV. CONCLUSION

This paper presents a novel concept of the topology and switching methods of a novel DC-DC converter. The research results presented in this paper confirm that the proposed converter contains various superior qualities, such as the following.

- High voltage gain. The theoretical maximum voltage gain of the converter can reach six.
- Low number of switches. The converter requires only four switches, which is favorable compared to the series-parallel SC converters.
- Quasi-inductiveless, low-volume design. The principle of operation assumes the transfer of energy through the capacitors. Low-volume chokes (based on planar PCBs) are used to achieve an oscillatory current in the circuits where the switched capacitors are charged and discharged.
- Low voltage stresses on switches. The converter can use switches with voltage stress three times lower than those required in a typical series-parallel converter.
- High efficiency. The efficiency achieved was 93.48%. Furthermore, it can be improved in design with a focus on minimizing parasitic resistances.
- Continuous output voltage regulation. This is an essential advantage in the SC-based converter family, where many converters operate with a fixed voltage gain.
- Fig. 25 also shows the nonlinear voltage change when we change the duration of the S_1 pulse. This characteristic may be important during the design process of the closed-loop control.
- Operation of one switch in the ZVS mode.

The outstanding characteristics of the converter were achieved by an original approach to a series-parallel SC converter, where the structure was extended in parallel rather than in series. When a voltage multiplier, such as that presented in [5], is extended by applying a larger number of switching cells connected in series, the output voltage gain increases, but the stresses of the switches also increase. Furthermore, in SCVM converters, the voltage stress of one switch is at the level of the output voltage [5]. This increases the cost of the converter and limits the application of SI MOSFET switches (e.g., in the case of the DC-link supply of 3-phase 3 × 400 V inverters). In the proposed approach

to converter optimization, the output voltage is extended in a parallel structure, which limits the voltage stresses of switches and gives many positive qualities of the converter. Note that parallel operation of the SCVM converters is not possible, as they do not operate as a dynamic current source to charge a common output capacitor. Therefore, the proposed idea of a parallel structure can be of special interest and useful for other concepts of converters based on SC circuits.

High-voltage-gain DC-DC converters can be applied in systems supplied from fuel cells [3], DC grids [4], automotive discharge headlamps [41], or in adequate topologies in PV systems.

REFERENCES

[1] A. Ioinovici, "Switched-capacitor power electronics circuits," *IEEE Circuits Syst. Mag.*, vol. 1, no. 3, pp. 37–42, Sep. 2001, doi: 10.1109/7384.963467.

[2] M. Forouzesh, P. Y. Siwakoti, A. S. Gorji, F. Blaabjerg, and B. Lehman, "Step-Up DC–DC Converters: A comprehensive review of voltage-boosting techniques, topologies, and applications," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9143–9178, Dec. 2017, doi: 10.1109/TPEL.2017.2652318.

[3] A. Emadi, S. S. Williamson, and A. Khaligh, "Power electronics intensive solutions for advanced electric, hybrid electric, and fuel cell vehicular power systems," *IEEE Trans. Power Electron.*, vol. 21, no. 3, pp. 567–577, May 2006, doi: 10.1109/TPEL.2006.872378.

[4] K. R. Kothapalli, M. R. Ramteke, H. M. Suryawanshi, N. K. Reddi, and R. B. Kalahasthi, "Soft-switched ultrahigh gain DC–DC converter with voltage multiplier cell for DC microgrid," *IEEE Trans. Ind. Electron.*, vol. 68, no. 11, pp. 11063–11075, Nov. 2021, doi: 10.1109/TIE.2020.3031453.

[5] Z. Waradzyn, R. Stala, A. Mondzik, A. Penczek, A. Skala, and S. Pirog, "Efficiency analysis of MOSFET-based air-choke resonant DC–DC step-up switched-capacitor voltage multipliers," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8728–8738, Nov. 2017, doi: 10.1109/TIE.2017.2698368.

[6] R. Stala, Z. Waradzyn, A. Penczek, A. Mondzik, and A. Skala, "A switched-capacitor DC–DC converter with variable number of voltage gains and fault-tolerant operation," *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 3435–3445, May 2019, doi: 10.1109/TIE.2018.2851962.

[7] R. Stala, Z. Waradzyn, A. Mondzik, A. Penczek, and A. Skala, "DC–DC high step-up converter with low count of switches based on resonant switched-capacitor topology," in *Proc. 21st Eur. Conf. Power Electron. Appl. (EPE ECCE Eur.)*, Sep. 2019, p. 10, doi: 10.23919/EPE.2019.8914785.

[8] G. D. Zulauf, J. Roig-Guitart, J. D. Plummer, and J. M. Rivas-Davila, "C_{OSS} measurements for superjunction MOSFETs: Limitations and opportunities," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 578–584, Jan. 2019, doi: 10.1109/TED.2018.2880952.

[9] K. K. Law, K. W. E. Cheng, and Y. P. B. Yeung, "Design and analysis of switched-capacitor-based step-up resonant converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 5, pp. 943–948, May 2005, doi: 10.1109/TCSI.2004.840482.

[10] A. Salehian, S. S. Hashemi, R. Beiranvand, and A. Yazdian, "Simulation of a step-up resonant switched-capacitor converter under the CCM operation mode," in *Proc. 10th Int. Power Electron., Drive Syst. Technol. Conf. (PEDSTC)*, Feb. 2019, pp. 230–235, doi: 10.1109/PEDSTC.2019.8697618.

[11] K.-C. Tseng and C.-C. Huang, "High step-up high-efficiency interleaved converter with voltage multiplier module for renewable energy system," *IEEE Trans. Power Electron.*, vol. 61, no. 3, pp. 1311–1319, Mar. 2014, doi: 10.1109/TIE.2013.2261036.

[12] M. Maalandish, S. H. Hosseini, and T. Jalilzadeh, "High step-up DC/DC converter using switch-capacitor techniques and lower losses for renewable energy applications," *IET Power Electron.*, vol. 11, no. 10, pp. 1718–1729, Aug. 2018.

[13] H. Choi, M. Jang, and J. Pou, "High-gain soft-switching interleaved switched-capacitor DC–DC converter with phase-shedding technique," *IET Power Electron.*, vol. 10, no. 9, pp. 1013–1022, Jul. 2017.

[14] V.-T. Tran, M.-K. Nguyen, Y.-O. Choi, and G.-B. Cho, "Switched-capacitor-based high boost DC–DC converter," *Energies*, vol. 11, no. 4, p. 987, Apr. 2018, doi: 10.3390/en11040987.

[15] H. Xie and R. Li, "A novel switched-capacitor converter with high voltage gain," *IEEE Access*, vol. 7, pp. 107831–107844, 2019, doi: 10.1109/ACCESS.2019.2931562.

[16] S. Xiong and S.-C. Tan, "Cascaded high-voltage-gain bidirectional switched-capacitor DC–DC converters for distributed energy resources applications," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1220–1231, Feb. 2017, doi: 10.1109/TPEL.2016.2552380.

[17] M. Chen, K. Li, J. Hu, and A. Ioinovici, "Generation of a family of very high DC gain power electronics circuits based on switched-capacitor-inductor cells starting from a simple graph," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 12, pp. 2381–2392, Dec. 2016, doi: 10.1109/TCSI.2016.2606124.

[18] L. He and Z. Zheng, "High step-up DC–DC converter with switched-capacitor and its zero-voltage switching realisation," *IET Power Electron.*, vol. 10, no. 6, pp. 630–636, May 2017.

[19] S. Pirog and R. Stala, "DC–DC boost converter with high voltage gain and a low number of switches in multisection switched capacitor topology," *Arch. Electr. Eng.*, vol. 67, no. 3, pp. 617–627, 2018, doi: 10.24425/123667.

[20] A. Kawa and R. Stala, "SiC-based bidirectional multilevel high-voltage gain switched-capacitor resonant converter with improved efficiency," *Energies*, vol. 13, no. 10, p. 2445, May 2020, doi: 10.3390/en13102445.

[21] W. Qian, D. Cao, J. G. Cintron-Rivera, M. Gebben, D. Wey, and F. Z. Peng, "A switched-capacitor DC–DC converter with high voltage gain and reduced component rating and count," *IEEE Trans. Ind. Appl.*, vol. 48, no. 4, pp. 1397–1406, Jul. 2012, doi: 10.1109/TIA.2012.2199731.

[22] M. Chojowski, R. Stala, A. Piłat, M. Skowron, and S. Folmer, "The design concept of low cost and volume switched-capacitor, DC–DC resonant converter," in *Proc. IEEE 19th Int. Power Electron. Motion Control Conf. (PEMC)*, Gliwice, Poland, Apr. 2021, pp. 200–206, doi: 10.1109/PEMC48073.2021.9432547.

[23] S. Li, N. Zhang, S. Zheng, W. Xie, and K. Smedley, "A Dickson resonant switched-capacitor converter with 'indirect' resonant core and continuous conversion ratio," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2019, pp. 2218–2222, doi: 10.1109/APEC.2019.8721994.

[24] K. Sano and H. Fujita, "Performance of a high-efficiency switched-capacitor-based resonant converter with phase-shift control," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 344–354, Feb. 2011, doi: 10.1109/TPEL.2010.2062537.

[25] Z. Waradzyn, R. Stala, A. Mondzik, A. Skała, and A. Penczek, "GaN-based DC–DC resonant boost converter with very high efficiency and voltage gain control," *Energies*, vol. 13, no. 23, p. 6403, Dec. 2020, doi: 10.3390/en13236403.

[26] M. Vasić, D. Serrano, V. Toral, P. Alou, J. A. Oliver, and J. A. Cobos, "Ultraefficient voltage doubler based on a GaN resonant switched-capacitor converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 622–635, Jun. 2019, doi: 10.1109/JESTPE.2019.2899180.

[27] S. Li, W. Xie, and K. M. Smedley, "A family of an automatic interleaved Dickson switched-capacitor converter and its ZVS resonant configuration," *IEEE Trans. Ind. Electron.*, vol. 66, no. 1, pp. 255–264, Jan. 2019, doi: 10.1109/TIE.2018.2829682.

[28] S. Li, Y. Zheng, B. Wu, and K. M. Smedley, "A family of resonant two-switch boosting switched-capacitor converter with ZVS operation and a wide line regulation range," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 448–459, Jan. 2018, doi: 10.1109/TPEL.2017.2669841.

[29] S. Li, K. Xiangli, Y. Zheng, and K. M. Smedley, "Analysis and design of the ladder resonant switched-capacitor converters for regulated output voltage applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 7769–7779, Oct. 2017, doi: 10.1109/TIE.2017.2694356.

[30] D. Gunasekaran, L. Qin, U. Karki, Y. Li, and F. Z. Peng, "A variable (n/m)X switched capacitor DC–DC converter," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6219–6235, Aug. 2017, doi: 10.1109/TPEL.2016.2621105.

[31] M. K. Alam and F. H. Khan, "A high-efficiency modular switched-capacitor converter with continuously variable conversion ratio," in *Proc. IEEE 13th Workshop Control Modeling Power Electron. (COMPEL)*, Jun. 2012, pp. 1–5, doi: 10.1109/COMPEL.2012.6251791.

[32] Y. Ye and K. W. E. Cheng, "A family of single-stage switched-capacitor–inductor PWM converters," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5196–5205, Nov. 2013, doi: 10.1109/TPEL.2013.2245918.

[33] G. Wu, X. Ruan, and Z. Ye, "Nonisolated high step-up DC–DC converters adopting switched-capacitor cell," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 383–393, Jan. 2015.
[34] Y. Tang, T. Wang, and D. Fu, "Multicell switched-inductor/switched-capacitor combined active-network converters," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2063–2072, Apr. 2015.
[35] J. Xu, L. Gu, and J. Rivas-Davila, "Effect of class 2 ceramic capacitor variations on switched-capacitor and resonant switched-capacitor converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 2268–2275, Sep. 2020, doi: 10.1109/JESTPE.2019.2951807.
[36] J. Xu, L. Gu, E. Hernandez, and J. Rivas-Davila, "Effect of class 2 ceramic capacitance variations on switched capacitor and resonant switched capacitor converters," in *Proc. IEEE 19th Workshop Control Modeling Power Electron*, Jun. 2018, pp. 1–7, doi: 10.1109/JESTPE.2019.2951807.
[37] R. Stala, Z. Waradzyn, A. Mondzik, A. Penczek, A. Skała, A. Kawa, and S. Piróg, "Resonance DC–DC converter and method of control of the resonance DC–DC converter," U.S. Patent, 231 870 B1, Apr. 30, 2019.
[38] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "ZVS of power MOSFETs revisited," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8063–8067, Dec. 2016, doi: 10.1109/TPEL.2016.2574998.
[39] M. Meneghini, G. Meneghesso, and E. Zanoni, *Power GaN Devices. Materials, Applications and Reliability*. Springer, 2017.
[40] M. K. Kazimierczuk and D. Czarkowski, *Resonant Power Converters*, 2nd ed. Hoboken, NJ, USA: Wiley, 2011.
[41] J. Wang, "Automotive headlamp HID ballast reference design using the dsPIC DSC device," Microchip Technol. Inc., Chandler, AZ, USA, Tech. Rep. AN1372, 2012.

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