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Current-Reused Current Feedback Instrumentation Amplifier for Low Power Leadless Pacemakers

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ABSTRACT This paper proposes a cardiac electrogram acquisition and stimulation integrated circuit (IC) for single-chamber leadless pacemaker applications. The proposed IC features self-determining pacing by acquiring an intracardiac electrogram without an external digital signal processor (DSP). A novel current-feedback instrumentation amplifier (CFIA) is proposed to achieve high noise-power efficiency and high input impedance. In this proposed CFIA, the current-reused cascode differential-difference input stage and class-AB biasing stage are merged. The electrocardiogram (ECG) sensing channel, equipped with a 60-Hz notch filter to relieve powerline interference (PLI), achieves a power supply rejection ratio (PSRR) of 80 dB, a common-mode rejection ratio (CMRR) of 174 dB, and an input-referred noise of 3.47 μVRMS, in a 350 Hz bandwidth. The ECG acquisition and cardiac pacing functionality of the IC are evaluated in a swine's right ventricle via a 4-electrode catheter.

INDEX TERMS Current-reused, current feedback instrumentation amplifier (CFIA), leadless pacemaker.

I. INTRODUCTION

Implantable cardiac pacemakers are widely used to treat bradyarrhythmias, which can result in a slow heart rate [1]. Along with the condition of bradycardia, various symptoms can occur, such as fatigue, weakness, and dizziness. An implantable pacemaker can improve the quality of life of the patient and give them near normal life capabilities [2]. A pacemaker continuously monitors the intracardiac electrogram and provides electrical stimulation when the heart, beats slower than the desired rate. The main design challenges, for pacemakers, include the necessity of a small form factor, low power consumption, and data transmission functionality.

Conventional pacemakers show complications primarily related to the transvenous lead and the subcutaneous generator pocket, such as insulation breaks, conductor fractures of the lead, skin erosion, pocket infection, and septicemia [3]. To address these lead and device pocket–related issues, leadless pacemaker systems were recently introduced to prevent post-transplant complications because leadless pacemakers with a catheter delivery do not need sensing and pacing

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leads, or a pocket on the top of the chest. Currently, two leadless pacing systems are clinically available: the Nanostim Leadless Cardiac Pacemaker from St. Jude Medical, and the Micra Transcatheter Pacing System from Medtronic [4], [5]. Both Nanostim and the Micra system provide single chamber sensing and pacing functionality of the right ventricle. Leadless pacemakers operate on batteries for almost 10 years while providing a precise bradycardia diagnosis and coordination. Therefore, the power consumption requirements become more stringent; thus, ultra-low power consumption and high-precision sensing and pacing circuits are necessary.

Leadless pacemakers provide VVI (ventricle pacing, ventricle sensing, inhibited by a ventricle event) or VVIR mode, inserted into the right ventricle and coordinating the ventricle. Here, the last ''R'' in VVIR implies that the desired heart rate is responsive to the body temperature or physical body activity [16]. The pacemaker measures the electrocardiogram (ECG) at the right ventricle and detects the QRS peak. Here, the QRS is a combination of three of the graphical deflections observed in a typical electrocardiogram, which consists of P-Q-R-S-T waveform components. Based on the detected QRS peak, the cardiac coordination algorithm is used to determine the presence or absence of cardiac coordination, and the pacing stimulation pulse, based on current injection or charge-transfer is performed. The sensing amplifier timing, control logic, and pacing stimulator are the key building blocks for pacemakers.

Many techniques for sensing amplifiers have been reported to improve the power-noise efficiency [6]–[9]. At the input stage, current-reused topologies with complimentary-input stages are widely used in ultralow power applications to achieve a high noise-power efficiency [6]–[8]. This current-reused topology can double the input transconductance with the same bias current. At the output stage, class-AB structures are commonly used, as these structures employ two transconductors with a single branch of bias current, and thus have a higher current efficiency and a faster transient response than that obtained with a class-A structure with the same quiescent current. The combination of the current-reused input stage and a class-AB output stage is a good solution to the noise-power requirement. As reported in [9], a two-stage amplifier was introduced. In the first stage, a current-reused input stage and class-AB biasing stage were merged; in the second stage, the class-AB output stage was implemented as shown in Fig. 1(a).

In Fig. 1(a), the current-reuse technique used in this circuit allows for a PMOS sourcing current to be reused as a NMOS sinking current. For higher power efficiency, the Monticelli-style floating class-AB biasing units [12], *M5–M8*, are merged with the complimentary input stages, *M1–M4*; thus, additional current is not required for the class-AB biasing units. This approach is an efficient way to use the supply current both at the input and output stages.

Based on [9], a 2-stage current-reused class-AB differential difference amplifier (DDA) was proposed, as shown in Fig. 1(b). In the proposed circuit, the two complementary current-reused input stages and class-AB biasing circuits are merged. The proposed DDA can be used for ultralow power and high input impedance instrumentation amplifiers (IAs). The DDA-style input stages can separate the input and feedback ports, which results in an increase in input impedance similar to the manner of the current-feedback instrument amplifier (CFIA).

Many research activities have been carried out to improve the performance of biopotential IAs in terms of power, noise, and linearity. The IAs are widely used for high precision biopotential measurements with high gain and high input impedance. The capacitively-coupled instrumentation amplifier (CCIA), shown in Fig. 2(a), is popular in electrocardiogram (ECG) measurements for its AC-coupling characteristics to eliminate the DC offset at the electrode-skin interface.

Assuming an input capacitance of 100 pF and an input signal frequency of 20 Hz, which is similar to the QRS frequency band, the input impedance of the CCIA is calculated to be 79.6 MΩ, and it decreases when a high frequency chopper is applied. The input impedance of the CCIA is determined by the CCIA's input capacitance, as expressed in (1).

$$Z_{IN(CCIA)} = \frac{2}{sC_i} \tag{1}$$

The transfer function of the CCIA can be expressed as

$$H(s)_{(CCIA)} = \frac{sC_iR_f}{1 + sC_fR_f} \tag{2}$$

The low input impedance can attenuate the signal amplitude and deteriorate the common mode rejection ratio (CMRR); thus, the signal can be contaminated by a common mode interference such as a 50/60 Hz power-line interference (PLI) and capacitive displacement currents.

As the impedance at the electrode-skin interfaces used for ECG measurements is in the range of tens of MΩ, a GΩ-level input impedance is needed to prevent signal distortion. To overcome this, it is reported that input impedance can be increased through the use of additional circuits, such as a positive feedback loop (PFL) [10]. However, the additional circuit complexity and the feedback stability are disadvantageous.

The CFIA topology, as shown in Fig. 2(b), is an efficient solution for high CMRR and high input impedance [11]. The input impedance of the CFIA is calculated as in (3).

$$Z_{IN(CFIA)} = 2\left(\frac{1}{sC_H} + R_B||\frac{1}{sC_g}\right) \tag{3}$$

The CFIA can achieve high input impedance because the input impedance of the CFIA is expressed as (3), where C_g is the gate input capacitance of input transconductor, G_{m2}. The DDA forms the CFIA with capacitive feedback. Thus, the DC offset can be attenuated by the high-pass transfer function, as expressed in (4).

$$H(s)_{(CFIA)} = \frac{sC_HR_B}{1 + sC_HR_B} \cdot \frac{1 + sR_f(C_f + 2C_1)}{1 + sC_fR_f} \tag{4}$$

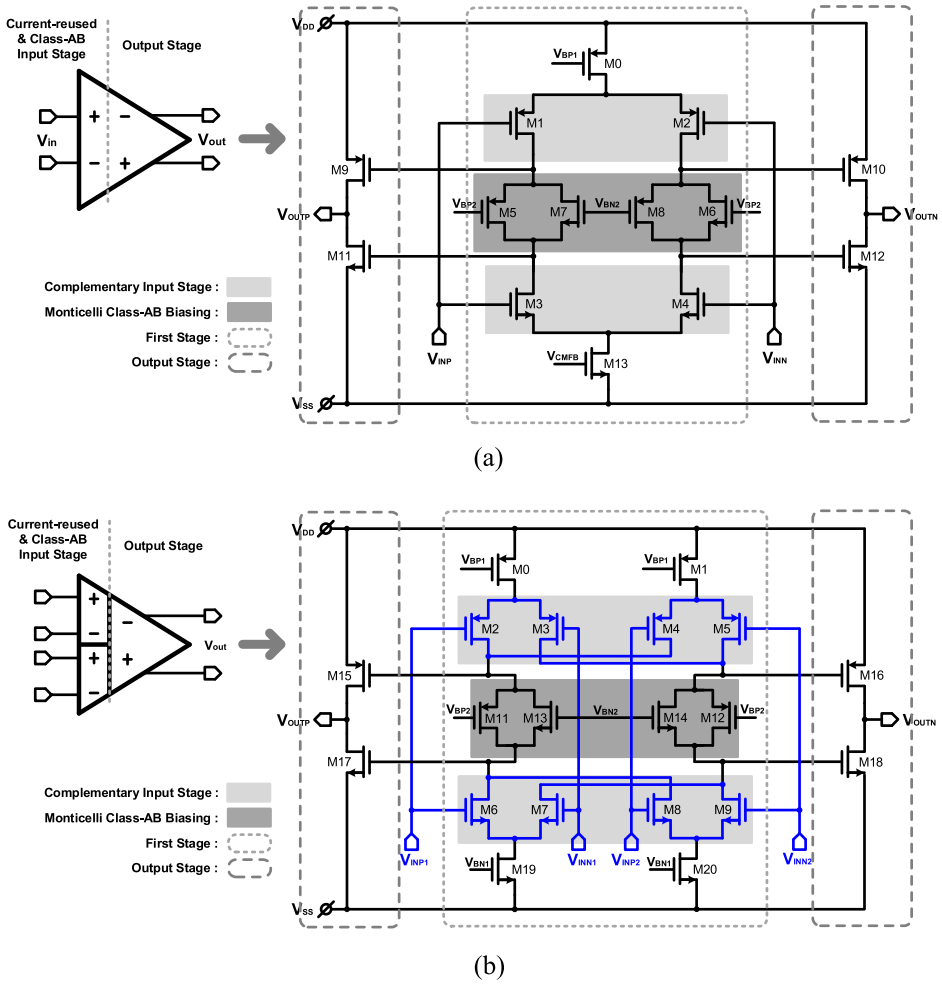

FIGURE 1. (a) Previous 2-stage current reused class-AB operational amplifier reported in [9]. (b) Proposed 2-stage current reused class-AB differential difference amplifier (DDA).

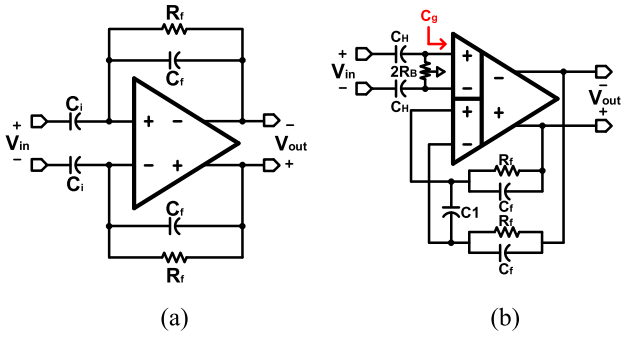

FIGURE 2. (a) Capacitive-coupled instrumentation amplifier (CCIA) (b) current feedback Instrumentation amplifier (CFIA) with input high pass filter.

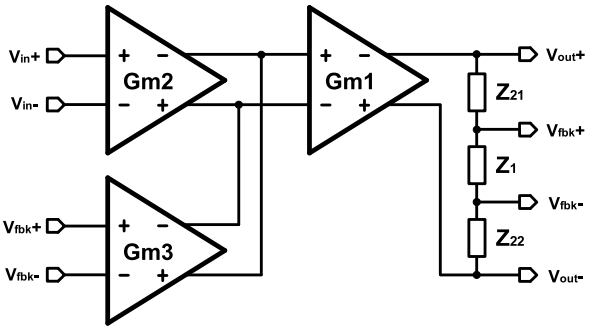

FIGURE 3. Typical CFIA topology.

As shown in Fig. 3, the input transconductor G_{m2} and feedback transconductor G_{m3} convert the input voltage and feedback voltage to the currents. The overall gain of the CFIA is calculated as in (5).

$$Gain = \frac{G_{m2}}{G_{m3}} \cdot \frac{Z_1 + Z_{21} + Z_{22}}{Z_1} \tag{5}$$

From the power consumption perspective, the CFIA is also power efficient because the input, and feedback transconductor share the current-summing and output stages.

In this paper, a low power current-reused class-AB CFIA is proposed. The basic idea of the proposed CFIA is based on [9]. In the first stage, the input, and feedback transconductor are implemented using complementary topology, and the Monticelli-style class-AB biasing units are also merged into

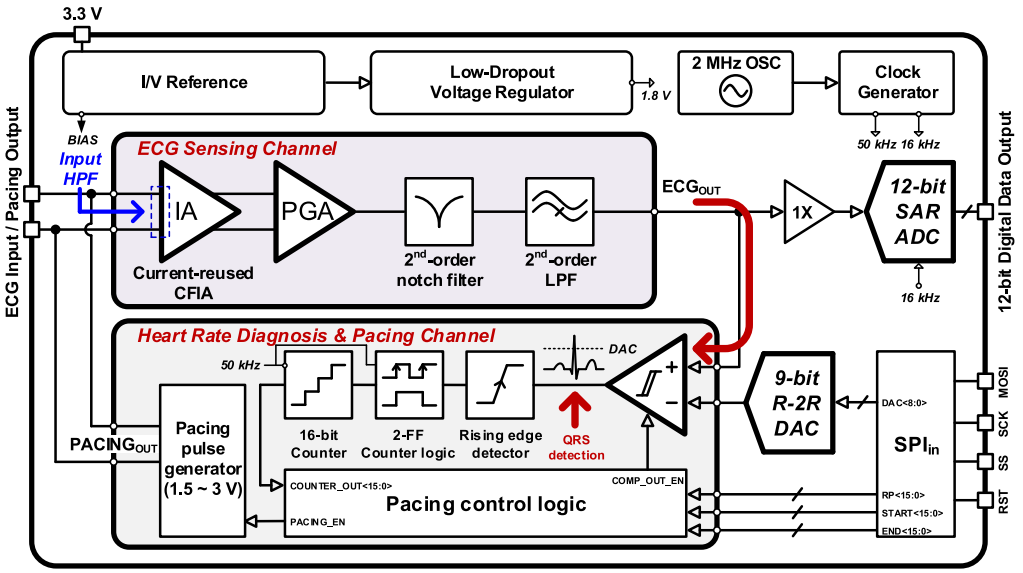

FIGURE 4. Proposed human inserted cardio diagnostic integrated circuit block diagram.

the first stage. The second stage operates as a class-AB output stage. The complete pacemaker chip prototype is implemented using a 180 nm CMOS fabrication process. The low power sensing channel based on the current-reused CFIA and the low power pacing channel based on the capacitive charge transfer are integrated on the presented IC. Sections II, III, and IV will discuss the design of the proposed pacemaker IC, the experimental results, and the conclusions, respectively.

II. PROPOSED PACEMAKER CIRCUIT

A. OVERALL CIRCUIT DESIGN

Fig. 4 shows a top-level block diagram of the presented IC for a leadless pacemaker. The proposed circuit consists of an ECG sensing channel and a pacing channel including a QRS detection circuit and cardiac stimulator. The proposed ECG channel consists of the current-reused CFIA, a programmable gain amplifier (PGA), a 60 Hz notch filter, a 500 Hz low-pass filter (LPF), and a 12-bit SAR analog to digital converter (ADC).

The current-reused CFIA and the PGA can amplify the ECG utilizing a 5-bit programmable gain. The input high pass filter (HPF) and AC-coupled capacitive feedback in the CFIA and PGA attenuate the low frequency components. The gate voltages of the pseudo-resistor are 4-bit controllable, for adjusting the high-pass cut-off frequency. The PLI components of the amplified ECG signal can be attenuated using the 60-Hz notch filter. The amplified ECG signal is converted to the digital signal via the 500 Hz LPF and the 12-bit SAR ADC.

The proposed pacemaker IC operates in VVI mode. The ECG amplifier channel provides the amplified ECG signal, and the QRS peak is extracted from the ECG signal by the hysteresis comparator and threshold voltage generator. The threshold voltage generator is implemented using a 9-bit R-2R digital to analog converter (DAC). The pacing control logic counts the duration between the QRS peaks, makes a comparison between the measured duration and the desired duration (normally 80 BPM). If the QRS peak is not detected within the desired duration, the pacing stimulator generates the pacing pulse. The internal status including gain, offset, pacing timing, and other variables are programmable using a serial peripheral interface (SPI). In the proposed circuit, the key building blocks include the ECG sensing chain, the pacing chain, the pacing control logic, the current and voltage reference, an on-chip oscillator, and a low drop-out regulator, all of which are fully integrated. The passive components for pacing capacitors and the optional input high pass filter are implemented in an off-chip.

B. PROPOSED CURRENT-REUSED CFIA

The block diagram of the input high pass filter (HPF) and the current-reused CFIA is shown in Fig. 5. Although the capacitive feedback provides the low-frequency attenuation

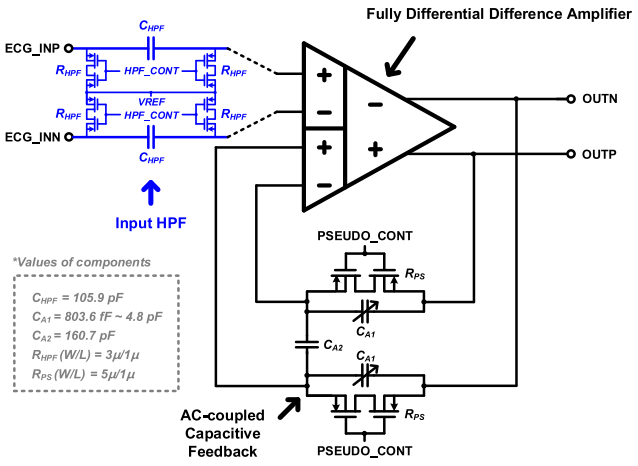

FIGURE 5. Proposed current-reused CFIA circuit.

characteristics, the input HPF is additionally implemented to reduce the slow varying baseline wander. As the baseline wander has a low-frequency noise of less than 1 Hz, the input HPF should be designed to have a cutoff frequency of several Hz [18], which requires a very large resistance. In consideration of the HPF design regarding size, a pseudo-resister is used in the input HPF, as it requires considerably less area when compared to a passive resistor with the same resistance value. In the in-vivo experiment, the peak amplitude and shape of waveforms have large variations. The main purpose of the sensing chain is to detect the QRS peak, and the different high-pass frequencies are required for proper QRS detection. To adjust the high-pass frequency, the resistance of the pseudo-resistor can be adjusted by utilizing the 4-bit programmable gate control voltage, HPF_CONT. Fig. 6 shows a control voltage generator that generates the gate control voltage, HPF_CONT. The pseudo-resistance value can be controlled by adjusting the gate voltage of the PMOS pseudo-resistor via the 4-bit control voltage generator. As the output voltage can be adjusted from 654.227 mV (DIN<3:0>= 1111) to 982.934 mV (DIN<3:0>= 0000), each pseudo-resistance varies from 640 MΩ to 28.7 TΩ, as shown in Fig. 7. The high-pass frequency variation according to the pseudo-resistance changes is shown in Fig. 8. The high-pass frequency varies from 6.343 mHz (DIN<3:0>= 0000) to 921.429 mHz (DIN<3:0>= 1111).

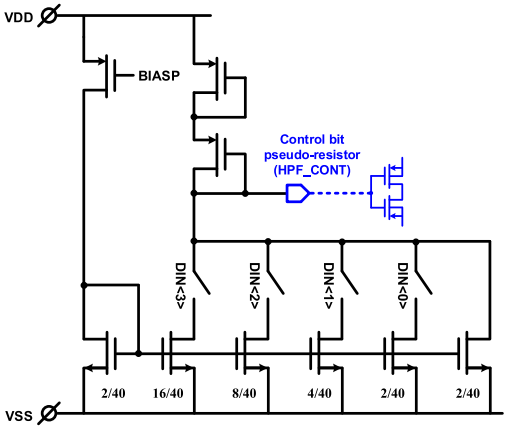

FIGURE 6. 4-bit control voltage generator.

The input HPF is implemented using a floating HPF topology for fast common mode response. The floating HPF bypasses the input common mode voltage to the output common mode voltage.

In the CCIA scheme, the input impedance at the input node of the amplifier is reduced owing to the shunt-shunt feedback. In the CFIA, however, the input node and the feedback node are separated; thus, the input impedance at the input node remains high as $1/sC_g$, where C_g is the gate capacitance of the amplifier input. With the proposed topology shown in Fig. 5(a), the high input impedance including HPF can be determined as expressed as in (3). At the DC operating point, C_g is simulated to 2.56 pF, which is the total gate

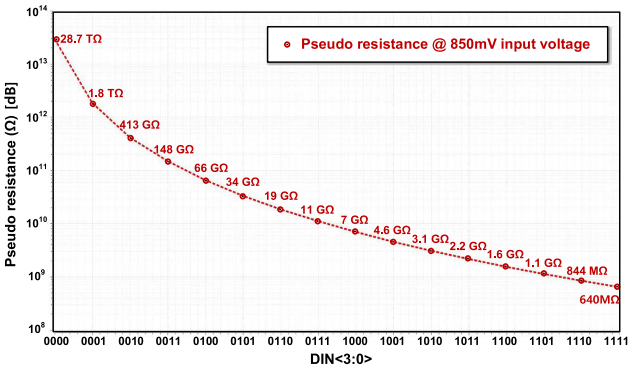

FIGURE 7. Pseudo-resistance variation according to 4-bit control voltage.

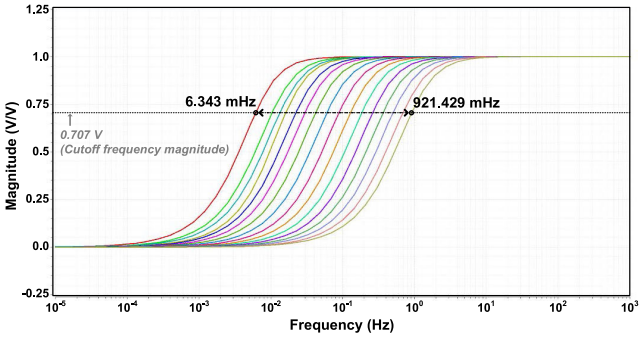

FIGURE 8. Programmable cutoff frequency simulation results of input HPF.

capacitance (cgg) of the input differential pair. Assuming the input signal frequency of 20 Hz, the impedance of 2.56 pF capacitance is 1.24 GΩ, which is of similar order to the pseudo-resistor R_B in (3). The proposed CFIA can achieve ten times higher input impedance (>1 GΩ) than conventional CCIA topologies. Owing to the very high input impedance, it is possible for the proposed CFIA to achieve a high CMRR and prevent signal distortion.

In the proposed CFIA, the AC-coupled capacitive feedback network with a parallel pseudo-resistor is adopted. The pseudo-resistor in the feedback, R_{PS}, is also controlled by the 4-bit programmable voltage, PSEUDO_CONT, in the same manner as input pseudo-resistor, R_{HPF}. As the AC-coupled capacitive feedback forms a high-pass transfer function, DC offset is almost not amplified, as shown in the Monte-Carlo simulation (Fig. 9). The standard deviation

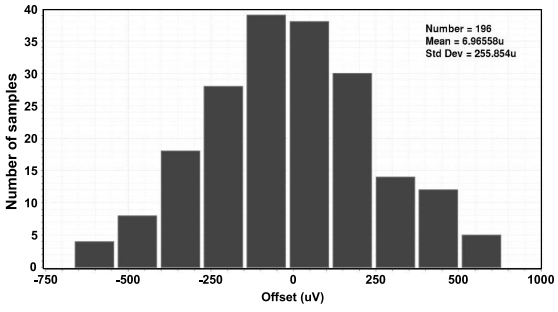

FIGURE 9. Offset variation through Monte-Carlo simulation.

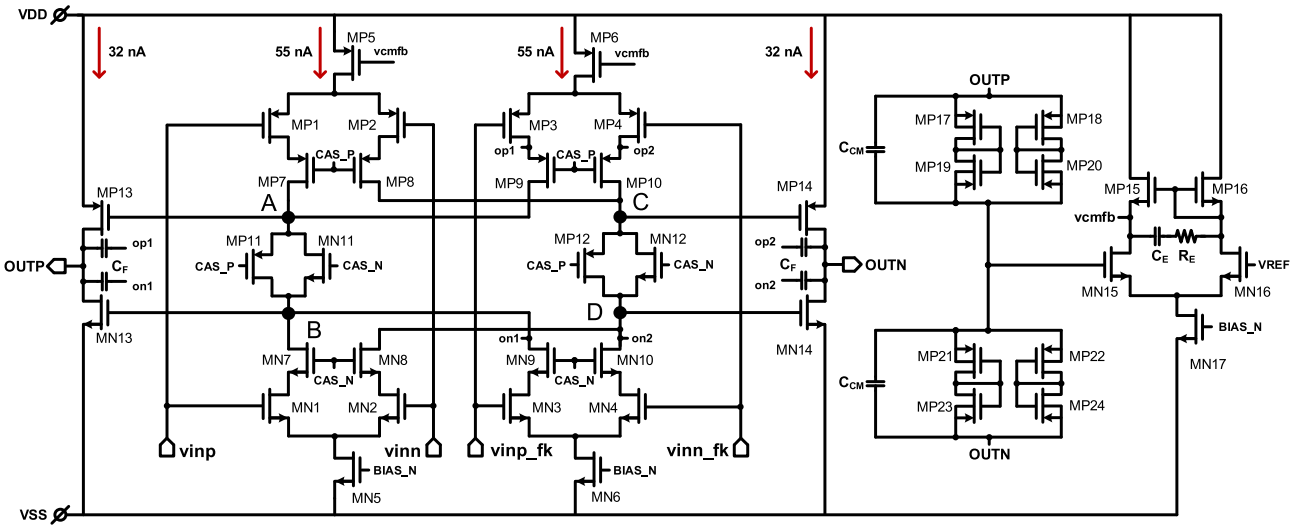

FIGURE 10. Proposed fully differential difference amplifier (FDDA) in current-reused CFIA.

of the offset variation of the instrumentation amplifier is 0.26 mV.

The transfer function of the input HPF and CFIA can be expressed as (6),

$$H(s) = \frac{sC_{HPF}R_{HPF}}{1+sC_{HPF}R_{HPF}} \cdot \frac{1+sR_{PS}(C_{A1}+2C_{A2})}{1+sC_{A1}R_{PS}} \simeq \frac{2C_{A2}}{C_{A1}} + 1 \quad (6)$$

and the passband gain of $|H(s)|$, can be approximated to $(2C_{A2}/C_{A1}+1)$ for high frequency. The passband gain is programmable using the 5-bit binary weighted capacitor array, C_{A1}.

The schematic of the proposed fully differential difference amplifier (FDDA) structure used in the CFIA is shown in Fig. 10. The PMOS differential pairs, *MP1* and *MP2*, and the NMOS differential pairs, *MN1* and *MN2*, form the current-reused input stage. Similarly, *MP3, MP4, MN3*, and *MN4* form the current-reused feedback input stage. These input transconductance stages convert the input and feedback voltages to currents. The common gate stages, namely, *MP7*, *MP8, MP9*, *MP10*, *MN7*, *MN8*, *MN9*, and *MN10*, are added to buffer these currents and increase the output impedances at A, B, C and D nodes. The open voltage loop gain from input voltage, $V_{IN} = V_{INP} - V_{INN}$, to output voltage, $V_{OUT} = V_{OUTP} - V_{OUTN}$, can be approximated as

$$\frac{V_{OUT}}{V_{IN}} \simeq (g_{mp1}+g_{mn1})(g_{mp7}r_{op7}r_{op1}||g_{mn7}r_{on7}r_{on1}) \times (g_{mp13}+g_{mn13})(r_{op13}||r_{on13}). \quad (7)$$

In [9], the current-reused class-AB amplifier obtains a 4-times larger open-loop gain than that of the traditional non-current-reused amplifiers under the same current consumption. In this amplifier, the open-loop gain is approximately $g_m r_o$ times larger than [9].

The Monticelli-style floating class-AB control units are implemented using *MP11*, *MN11*, *MP12*, and *MN12*. The class-AB control units are merged to the first stage, and then provide the gate voltage for the class-AB second stage without an additional bias current. The compensation capacitors, C_Fs, are connected between the output nodes and source of the common gate stages in a nested Miller compensation manner, to enhance the power supply rejection ratio (PSRR). The output common mode voltage is detected by the pseudo-resistors, *MP17-24*, and capacitors, C_{CM}s. The error amplifier for common mode feedback consists of *MP15*, *MP16*, *MN15*, *MN16*, and *MN17*, for generating the control voltage *vcmfb*, which controls the bias current of the input and feedback stages. The values of transistors and passive elements in FDDA are shown in Table 1. The pseudo-resistance has a typical value of few GΩ.

C. PGA, NOTCH FILTER, AND LPF

In the intracardiac electrogram acquisition, the peak QRS amplitude and the shape of the electrogram waveform have large person-to-person variations. To address these large variations, both the IA and PGA are designed with high programmability.

Fig. 11 is the AC-coupled PGA circuit with 5-bit programmable capacitor feedback combined with adjustable 4-bit pseudo-resistor. The gain is 5-bit adjustable, and the high-pass bandwidth is 4-bit adjustable. As the notch filter and LPF require large circuit area, using a single-ended PGA topology can reduce the chip area and power consumption. Further, the high input impedance of the DDA can reduce the driving burden of the IA.

The 5-bit programmable gain can be adjusted via serial peripheral interface (SPI) with 5-bit binary code. The gain changes as the 5-bit binary code adjusts the capacitor value by switching on and off each switch in the capacitor array.

TABLE 1. Values of transistors and passives in FDDA.

* Transistors	Size (μm)
MP1, MP2, MP3, MP4	40/8
MP5, MP6	16/8
MP7, MP8, MP9. MP10	300/40
MP11, MP12	1/20
MP13, MP14	0.5/80
MN1, MN2, MN3, MN4	12/160
MN5, MN6	2/80
MN7. MN8. MN9. MN10	1000/4
MN11, MN12	120/1
MN13, MN14	0.5/80
MP15, MP16	4/10
MN15, MN16	2/20
MN17	2/320
MP17–MP24 (pseudo resistor)	40/1
*** Passive elements**	**Values**
C_F	4.8 pF
C_{CM}	803 fF
C_E	80.36 pF
R_E	6.2 MΩ

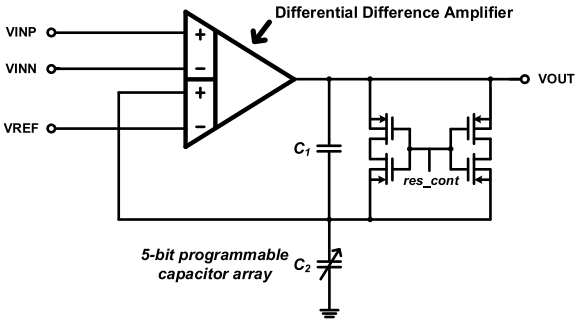

FIGURE 11. AC-coupled PGA circuit.

The closed loop gain of the PGA in shown Fig. 11 can be expressed as in (8).

$$Gain = \frac{C_1 + C_2}{C_1} \tag{8}$$

The transfer function of changing gain through a 5-bit binary code is shown in Fig. 12. As the frequencies of ECG QRS pulse often has values of 15–25 Hz, the gain value is specified at 20 Hz. The gain can be adjusted from 7.427 dB (00000) to 30.354 dB (11111).

The schematic of the proposed DDA structure used in the PGA is shown in Fig. 13. The DDA introduced a rail-to-rail input stage for wide input signal voltage range. The folded cascode structure was introduced to improve performance of the open loop DC gain and bandwidth. The class-AB outputs have high power efficiency and heavy load drive capability. The proposed AC-coupled PGA combines the folded cascode with the floating class-AB control unit, which is designed

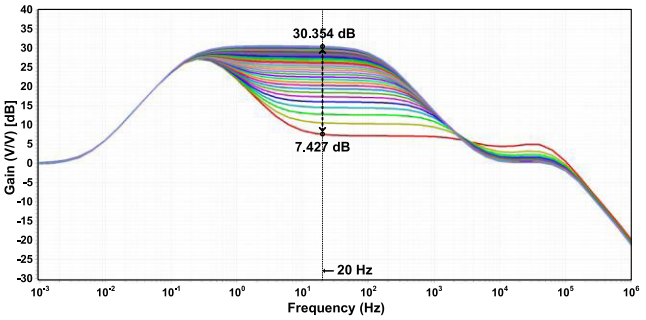

FIGURE 12. Programmable transfer function gain simulation results of PGA.

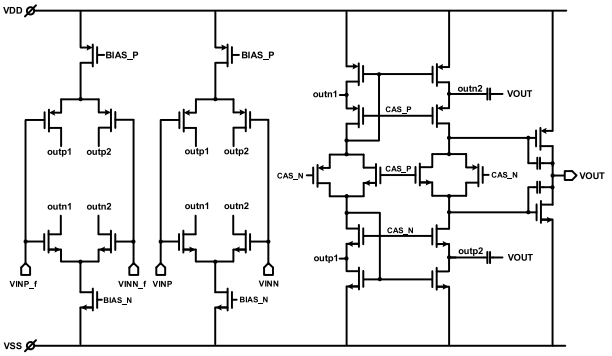

FIGURE 13. Schematic of DDA in PGA.

to drive the class-AB output stage without additional current consumption.

Figs. 14 and 15 show the 60 Hz notch filter and 500 Hz active LPF, respectively. The amplifiers utilized in both circuits used rail-to-rail input stage and class-AB output stage.

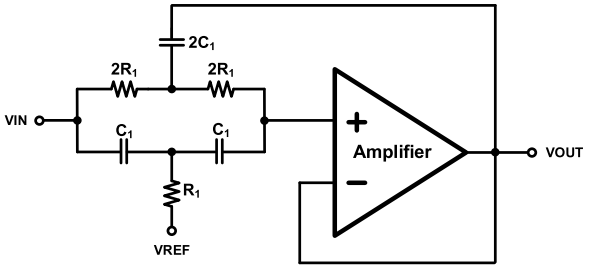

FIGURE 14. 60 Hz notch filter circuit.

D. PACING CHANNEL AND TIMING LOGIC

The operation of the pacing control logic is shown in Fig. 16. The main clock of the pacing control logic is 50 kHz. The amplified ECG signal from the sensing chain is compared with the threshold voltage by the hysteresis comparator. The rising edge detector detects the rising edge from the detected QRS peak and converts it to a fixed-width pulse. The converted pulse is synchronized with the main clock of the pacing logic.

The timing parameters, *VRP<0:15>*, *START<0:15>* and *END<0:15>* are programmable via a 16-bit SPI registers.

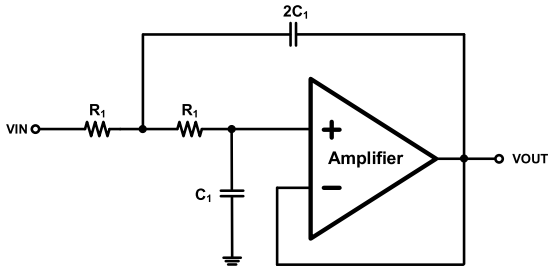

FIGURE 15. 500 Hz active LPF circuit.

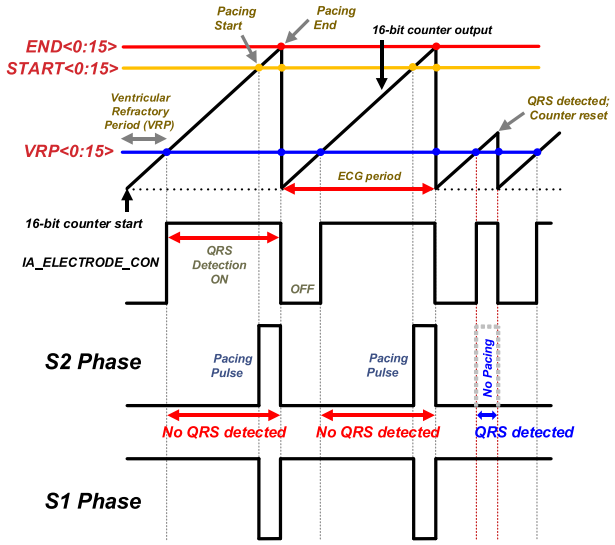

FIGURE 16. Pacing control logic operation.

The programming step and maximum range of timing parameters are 2 us and 1.31 s, respectively, at a 50 kHz clock. The main 16-bit counter tracks the main clocks, and compares the counted clocks to the timing parameters.

In Fig. 16, *VRP<0:15>* refers to a ventricular refractory period, which means a resting period of the electrocardiogram in which no QRS peak can be detected. Therefore, it does not detect any QRS peaks until the 16-bit counter matches the value in *VRP<0:15>*. The *START<0:15>* and *END<0:15>* are the start and end times of the pacing pulse, respectively. If the value of the 16-bit counter is greater than that of *VRP<0:15>* then the detection of the QRS peak is initiated. The QRS peak detection interval is defined from *VRP<0:15>* to *END<0:15>*. In this interval, the flag IA_ELECTRODE_CON is enabled. If no QRS peak is detected during the QRS peak detection interval, then the pacing pulse is generated from *START<0:15>* to *END<0:15>*. If a spontaneous QRS peak is detected during the QRS peak detection interval, the pacing pulse is not generated. The detected QRS peak pulse resets the 16-bit counter to zero, and then the counter restarts the counting.

The pacing pulse generator is shown in Fig. 17. The pacing pulse generator is based on [13]. The pacing amplitude can be adjusted in 32 steps from 1.5 V to 3 V. Prior to each pacing event, the analog switches *S1* is closed. In this phase,

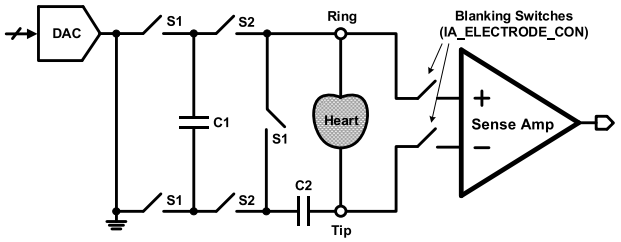

FIGURE 17. Capacitive pacing pulse generator.

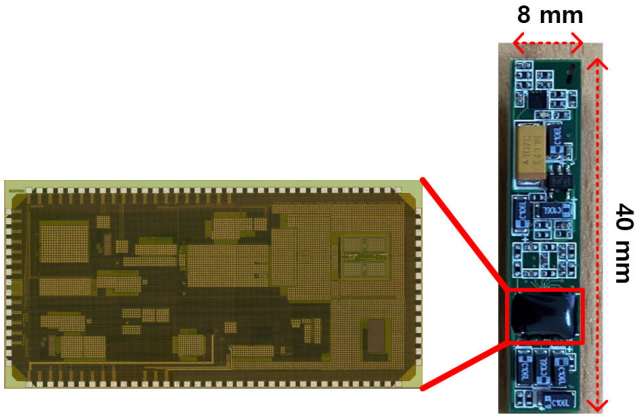

FIGURE 18. Die photograph and evaluation PCB for implantable leadless pacemaker.

the pacing storage capacitor *C1* is charged to the desired pacing voltage, and the blocking capacitor, *C2*, is negated. At the pacing phase, *S1* is opened, and S2, closed. In this phase, the charge stored in *C1* is transferred to *C2* via the heart tissue resistance, and then the pacing current flows between the heart and *C2*. The 10 μF off-chip capacitors are used for *C1* and *C2*, respectively.

III. EXPERIMENTAL RESULTS

Fig. 18 shows a die-photograph of the presented IC and the evaluation PCB for the implantable leadless pacemaker. The circuit is fabricated using a TSMC 180 nm CMOS process resulting in a chip size of 12.5 mm $\times$ 12.5 mm. The small-sized evaluation PCB with 8 mm $\times$ 40 mm was designed to evaluate the performance and the functionality of the proposed IC. Fig. 19 shows the input referred noise of the current-reused CFIA. The integrated input referred noise is 3.69 μVrms at a signal bandwidth from 1.7 Hz to 350 Hz with the noise floor measured as 180 nV/$\sqrt{}$Hz. Fig. 20 shows the measured transfer function of the current-reused CFIA. In this design, the muxed monitoring buffers for measuring the internal nodes are included. The buffers are enabled only in the monitoring operation and are disabled in the normal operation to reduce the power consumption. The operation scenario can lead to the variation in the total current consumption, as the building blocks in the sensing chain can be bypassed. The minimum current consumption of ECG sensing channel is 0.15 μA, where only IA is used, and if the PGA, Notch

TABLE 2. Amplifier performances and comparisons.

			This work	TBCAS'18[1]	TBCAS'14[14]	TBCAS'13[15]	TBCAS'11[19]	JSSC'21[20]
Technology			**0.18**	0.18	0.18	0.18	0.35	0.18
Supply Voltage			**1.8 / 3.3**	1/1.8	1.3-1.8	2.2-3.2/1.8	1.4-2.9	1.2
Total power consumption (μW)			**4.5~19.4 ***	4.2	-	-	48	24.8
ECG Sensing Channel	Input Impedance		**> 1 GΩ (simulated)**	-	> 0.4 GΩ	0.02 GΩ	-	-
	Current Consumption per Channel (μA)		**0.15 ~ 5.59**	0.5	0.68	3.24	0.49	10.25
	Bandwidth (Hz)		**1.7~352**	8-120	130	100	0~140	10 k
	Gain (dB)		**34.5**	14~44	43.2	26~53	21~31	40
	PSRR / CMRR (dB)		**80 / 174 (simulated)**	- / > 90	>80 / > 90	100 / 93	-	- / 66
	Input Referred RMS Noise (μV_{RMS})		**3.69**	2	4.9	2.2	1.1	1.67
	PLI cancellation		**Notch filter**	No	No	No	-	CMCP
	QRS extraction		**Yes**	No	Yes	Yes	Yes	No
	IA	Type	**CFIA**	CCIA	CCIA	CBIA	DDA	CBIA
		Current Consumption (nA)	**155**	-	150	660	28.5	3225
		NEF	**2.99**	-	-	6.87	-	-
Pacing Channel	Pacing Function / Programmability		**Yes**	Yes	Yes	No	Yes	-
	Current Consumption (μA)		**0.87 @ DC**	-	-	-	-	-
ADC	Resolution (bits)		**12**	10	7~10	10	8	-

* Min: IA + pacing + bias (4.5 μW), Max: IA + PGA + notch + LPF + ADC + pacing + bias (19.4 μW)

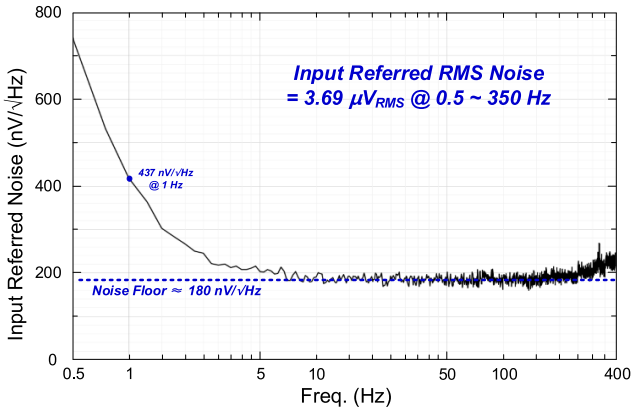

FIGURE 19. Input referred noise of current-reused CFIA.

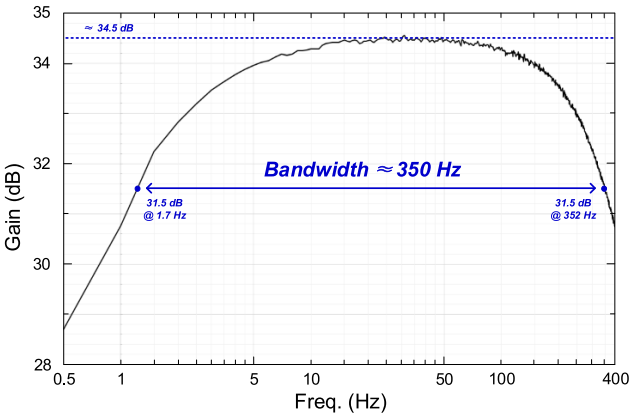

FIGURE 20. Transfer function of current-reused CFIA.

filter, and LPF are fully utilized, the power consumption is 4.21 μA. The power breakdown of the sensing channel is shown in Fig. 21.

The passband gain, high-pass cut-off frequency, and low-pass cut-off frequency are 34.5 dB, 1.7 Hz, and 352 Hz, respectively. The noise-efficiency-factor (NEF) is calculated to be 2.99. The performance comparisons of the circuit with the previous works are summarized in Table 2.

The in-vivo experimental setup for verifying the single-chamber VVI operation of the ECG sensing and the cardiac pacing coordination in the right ventricle (RV) of a swine is shown in Fig. 22. In this experiment, the pacemaker PCB is not implanted into the body, because the implantable hermetic packaging is still under development in our research group. Instead, the 4-lead electrode catheter is inserted to the RV of the swine, as shown in Fig. 23. The PCB with the

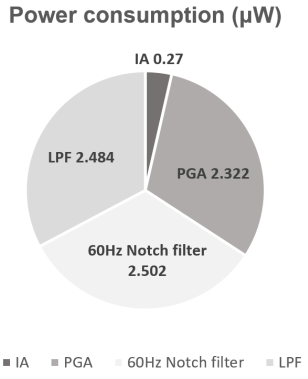

FIGURE 21. Power breakdown of the sensing channel.

proposed VVI pacemaker IC is outside of the swine's body. A 4-electrode catheter implements the electrical connection

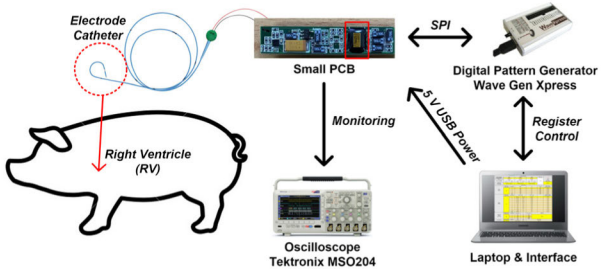

FIGURE 22. *In-vivo* **experimental setup for sensing and pacing in swine's right ventricle.**

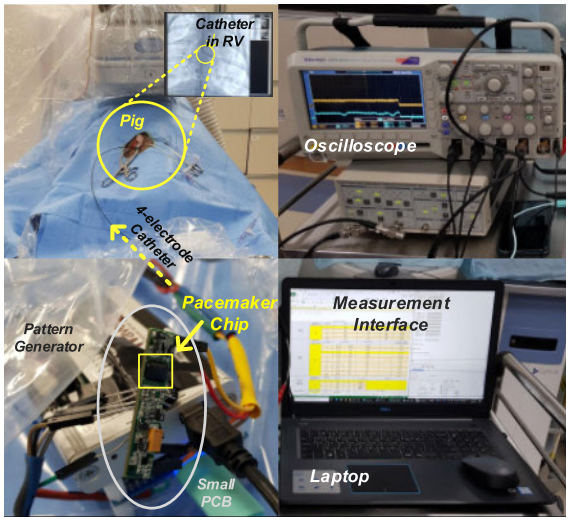

FIGURE 23. **Animal experiment measurement environment of human inserted cardio diagnostic integrated circuit.**

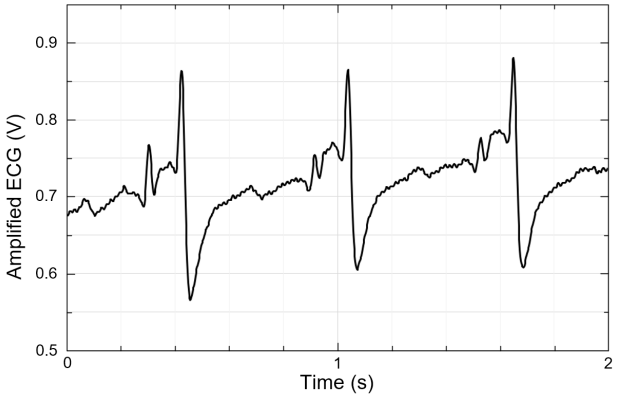

FIGURE 24. **ECG waveform measured in the right ventricle in swine's RV.**

between the swine's RV and the circuit. Two of the electrodes are used for sensing ECG, and the other two for sensing the pacing anode and cathode.

The acquired ECG signal from swine's RV is shown in Fig. 24. The sensing chain of the proposed circuit properly amplifies and acquires the ECG inside the RV.

The pacing experiment results are shown in Fig. 25. Before pacing, a normal heart rate of 89 BPM is measured. After pacing with 2.05 Hz pacing pulse frequency, the heart rate

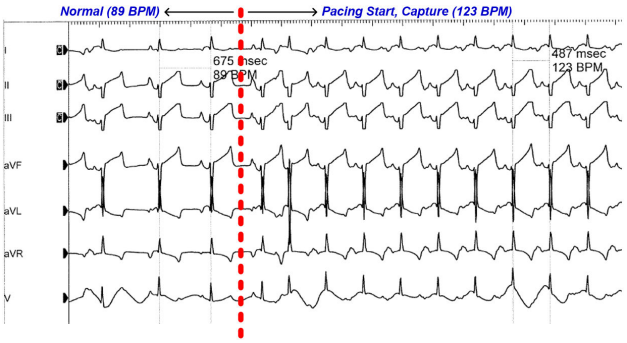

FIGURE 25. **Pacing experiment results: Before pacing, normal heart rate of 89 BPM is measured. After pacing, the heart rate is increased to 123 BPM.**

increased to 123 BPM. The amplitude and pulse width of the pacing pulse are 3 V and 0.3 ms, respectively.

IV. CONCLUSION

In this study, an integrated circuit for a single-chamber VVI leadless pacemaker is presented. To reduce the power consumption and to increase the input impedance, the current-reused CFIA is proposed. In the presented pacemaker circuit, the ECG sensing chain, including the proposed CFIA, the capacitive pacing pulse stimulator, and the pacing control logic are integrated.

In the sensing amplifier, the signal input stage and the feedback input stage are separated in a current-feedback configuration for high input impedance. The current-reused inverter-based cascode input stage and floating class-AB biasing circuit are merged in the first stage. The current-reused input stage and class-AB second output stage can result in an increase in power efficiency. The presented pacemaker IC is evaluated with an electrode catheter, and it properly acquires the electrogram and paces the heart rate to the desired rate inside the swine's RV.

V. DISCLOSURE

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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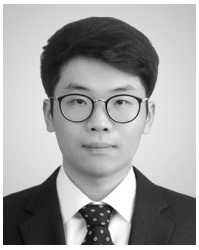

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