IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received July 4, 2021, accepted July 22, 2021, date of publication August 9, 2021, date of current version August 18, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3103752

A mHEMT Power-Reconfigurable Distributed Amplifier Using a Gain Cell Switching Technique

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This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea Government, Ministry of Science and ICT (MSIT) under Grant 2021R1G1A1010324.

ABSTRACT A power-reconfigurable distributed amplifier (DA) is implemented using a 130 nm metamorphic high-electron mobility transistor (mHEMT) process. Using a mHEMT process with excellent high-frequency characteristics, output power and efficiency at high frequencies are improved compared with the existing power-reconfigurable distributed amplifiers. In this article, a gain cell switching technique is proposed as the power reconfiguration method for the distributed amplifier. The gain cell switching technique expands the gain bandwidth and power reconfigurability more than the conventional bias control. The proposed power-reconfigurable DA obtains a measured linear gain of 10.0–13.6 dB from 0.5 to 62.5 GHz and a measured output power of 20.2–21.5 dBm from 10 to 40 GHz. A measured power added efficiency (PAE) is 11.6–20.0% from 10 to 40 GHz. Under a low power mode (LPM), it obtains a measured linear gain of 4.4–7.1 dB from 0.5 to 65 GHz and a measured output power of 14.7–15.9 dBm from 10 to 40 GHz. At 10 GHz, a drain efficiency (DE) is 11.4% at 5.6 dB power back-off. This is 6.5% higher than the conventional DA or more than twice as high.

INDEX TERMS Power back-off, distributed amplifier, gain cell switching, mHEMT, power reconfigurability.

I. INTRODUCTION

With the development of wireless communication, many new high-frequency bands have been allocated as 3G mobile communication has been upgraded to 4G long-term evolution (LTE). The recently commercialized 5G communication needs a transceiver system that can operate in the millimeter wave region [1]. In addition, short-range communications using ultra-wideband (UWB) technology have begun to be introduced into a variety of mobile applications [2]. Thus, mobile handsets used around the world require a number of transceiver systems capable of operating at various frequencies, from sub-GHz to over 30 GHz. This trend will add the burden of putting many radio frequency (RF) components into the handset's limited form factor.

Power amplifiers are essential components for RF transceiver systems, and they occupy a large portion of the handset's RF performance and form factor. A power- reconfigurable amplifier that covers multiple bands and multiple modes with one chip is an attractive research topic for solving this burden [3], [4]. In particular, a distributed amplifier (DA) shows the widest gain performance among amplifiers [5]–[13]. Among the existing amplifiers, a DA is the ultimate goal of reconfigurable power amplifiers because it is the only alternative that can cover LTE, UWB, and 5G communication bands with one chip.

To date, power-reconfigurable distributed amplifiers have been reported in some articles [5], [6]. They have been demonstrated using a commercial complementary metal oxide semiconductor (CMOS) process or a pseudomorphic high-electron mobility transistor (pHEMT) process. However, in the proposed scheme, gain bandwidth was reduced in low power mode (LPM) and power back-off was only 4 dB or less, so there was a limit to the use of LPM. In addition, they had the drawback that output power and efficiency dropped sharply above 30GHz, which belongs to one of the 5G bands.

In this study, we used an in-house metamorphic high-electron mobility transistor (mHEMT) process, which has an RF performance superior to a CMOS process or a pHEMT process that was used in previous works [5], [6]. Our mHEMT process was developed at Seoul National University [16]. This approach improves output power and efficiency above

The associate editor coordinating the review of this manuscript and approving it for publication was Vincenzo Conti.

30 GHz. In addition, a gain cell-switching technique is proposed as a method for power reconfiguration. The proposed gain cell switching technique improves the bandwidth reduction problem in LPM and expands the power back-off to 5.8 dB.

In section II, the power-reconfigurable methods on distributed amplifiers are analyzed and compared. First, in the previous power-reconfigurable method, which is called the ''double gate-bias control scheme,'' output power and gain bandwidth under LPM are calculated through a load line analysis and overall gain equations, including trans-conductance (G_m) in a gain cell. This analysis verifies that the previous method decreases gain bandwidth and limits power reconfigurability. Second, a gain cell-switching technique is proposed. In a similar way as before, the output power and gain bandwidth are analyzed. It is shown through analysis and simulations that the proposed method increases power reconfigurability and provides gain bandwidth equal to high power mode (HPM). In section III, the power-reconfigurable distributed amplifier is designed and simulated. In section IV, the proposed DA has been fabricated using the in-house mHEMT process, and measurement results are presented to verify the proposed method.

II. ANALYSIS OF POWER-RECONFIGURABLE METHODS ON DISTRIBUTED AMPLIFIERS

A. DOUBLE GATE-BIAS CONTROL SCHEME

The previous power-reconfigurable DAs used the double gate-bias control scheme [5], [6]. As shown in Figure 1, the gate bias of the middle transistor (V_{gg2}) and the gate bias of the bottom transistor (V_{gg1}) among the stacked transistors of each gain cell are lowered at the same time. This is the method of improving the back-off efficiency in LPM by prematurely saturating the entire load line of the gain cell. In [5], this method is called the ''double gate-bias control scheme.'' The biases of each transistor constituting the stacked gain cell are obtained as follows. Under HPM, to obtain the maximum output power, the same drain-source (V_{ds}) and gate-source voltage (V_{gs}) must be applied to each transistor. Therefore, when the total drain voltage is V_{dd} and the gate-source voltage of the bottom transistor is V_{gg1}, V_{gg3} becomes $2/3V_{dd} + V_{gg1}$, and V_{gg2} becomes $1/3V_{dd} + V_{gg1}$. If V_{gg2} and V_{gg1} are lowered to V'_{gg2} and V'_{gg1}, respectively, in LPM, the stacked gain cell should still share the same drain current, so each transistor must have the same gate-source bias, that is, V'_{gg1}. Accordingly, in Figure 1, the voltage of node A becomes $2/3V_{dd} + V_{gg1} - V'_{gg1}$ and that of node B $V'_{gg2} - V'_{gg1}$. As a result, the biases of each transistor in HPM and LPM are shown in Figures 2 (a) and (b), respectively. Because of $V'_{gg1} < V_{gg1}$ and $V'_{gg2} < V_{gg2}$, the drain-source voltage of M3 in LPM becomes smaller by $V_{gg1} - V'_{gg1}$, that of M2 becomes larger by $V_{gg2} - V'_{gg2}$, and that of M1 becomes smaller than $V_{gg2} - V_{gg1} = 1/3V_{dd}$. As an example, referring to Figures 2 (a) and (b), the bias voltages applied to each transistor of the stacked gain cell during HPM and LPM operations are as shown in Table 1. The LPM bias-setting criterion is set as the gate-source voltage in which the g_m of mHEMT decreases by about 60%. The reason is to obtain a power back-off of more than 3 dB from the low frequency band, as can be seen from the simulation results later.

TABLE 1. Example of the bias scheme during HPM and LPM operations.

	HPM	LPM
V_{dd} (V)	6.0	6.0
V_{gg3} (V)	3.6	3.6
V_{gg2} (V)	1.6	1.0
V_{gg1} (V)	−0.4	−0.6
V_{ds} (M3) (V)	2.0	1.8
V_{ds} (M2) (V)	2.0	2.6
V_{ds} (M1) (V)	2.0	1.6
V_{gs} (M1,2,3) (V)	−0.4	−0.6

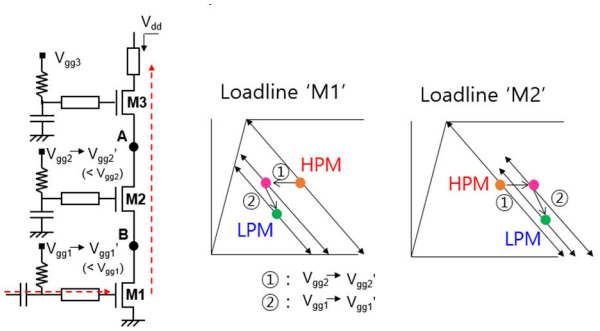

FIGURE 1. Load line variation of the stacked gain cell according to double gate-bias control scheme.

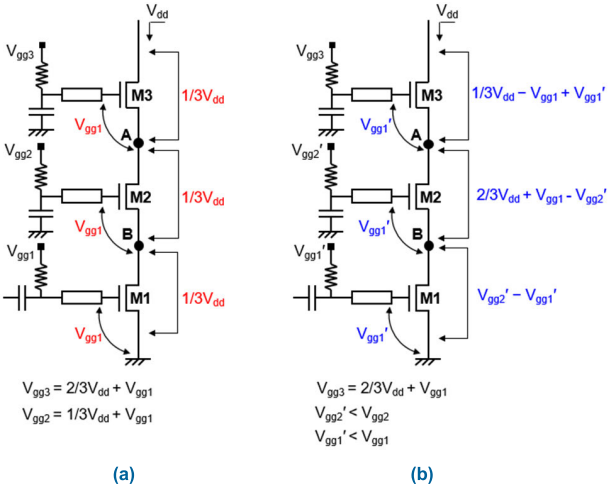

FIGURE 2. Biases of each transistor in (a) HPM and (b) LPM.

At this time, to analyze the gain bandwidth in HPM and LPM, the total transconductance (G_m) of the single stacked gain cell is calculated using an equivalent circuit. The G_m equation using the equivalent circuit of the triple-stacked transistor in Figure 3 can be expressed as follows.

$$G_m = \frac{g_m\left(g_m - sC_{gd}\right)}{\frac{g_m+s(C_{gd}+C_{gs}+C_{ds})}{g_m+sC_{ds}}\left(g_m+s\left(C_{gd}+C_{gs}+2C_{ds}\right)\right)-sC_{ds}} \quad (1)$$

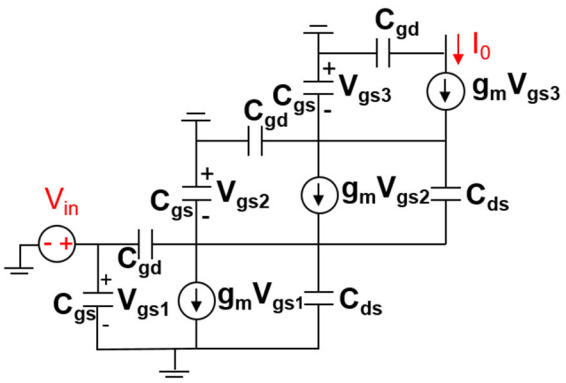

FIGURE 3. Equivalent circuit of the triple-stacked transistors.

where g_m is the transconductance, C_{gs} is the gate-source capacitance, C_{gd} is the gate-drain capacitance, C_{ds} is the drain-source capacitance, $s = j \times \omega$, and $\omega = 2 \times \pi \times$ frequency. Equation (1) consists of small-signal parameters and expresses G_m at a specific bias. Therefore, G_m is bias-dependent.

To simplify the analysis, we assume that the size of each field effect transistor (FET) is equal, the top transistor's C_{gd} and C_{ds} are absorbed by the drain line, and external gate bias circuits are omitted. On the other hand, when the G_m of the gain cell is known, the total gain (G) of DA can be expressed by the following equation, as is well known [17].

$$G = \frac{G_m^2 Z_0^2 \left(e^{-\alpha_g l_g n} - e^{-\alpha_d l_d n}\right)^2}{4\left(\alpha_g l_g - \alpha_d l_d\right)^2} \tag{2}$$

$$\alpha_g = \frac{1}{2}\frac{r_i \omega^2 C_{gs}^2}{l_g} Z_{gl} \tag{3}$$

$$\alpha_d = \frac{1}{2}\frac{G_{ds}}{l_g} Z_{dl} \tag{4}$$

where n is the number of stages in the DA, r_i is the channel resistance, G_{ds} is the output conductance, l_g/l_d are a gate/drain line length and Z_{gl}/Z_{dl} are a gate/drain line termination load, respectively. To simplify the analysis, we assume that the reverse gain is cancelled and the line phase between gate lines and drain lines is equal. Using Equations (1) – (4), the total gain of the triple-stacked DA can be calculated. In the double gate-bias control scheme, the gate bias of each transistor changes depending on the operation mode (HPM or LPM), and accordingly, the small signal parameters also change. Therefore, by comparing the overall gain according to the change of each small signal parameter, the effect on gain bandwidth according to the mode can be analyzed. In the case of LPM, since the drain-source voltage applied to each transistor is different, the small signal parameters of each transistor may also be different because they are bias dependent. However, the bias region dealt with here is a saturation region in which the V_{ds} is 1 V or more. As shown in Figures 4 (a) – (d), it can be seen that in the saturation region, when the V_{gs} is constant, there is little change in

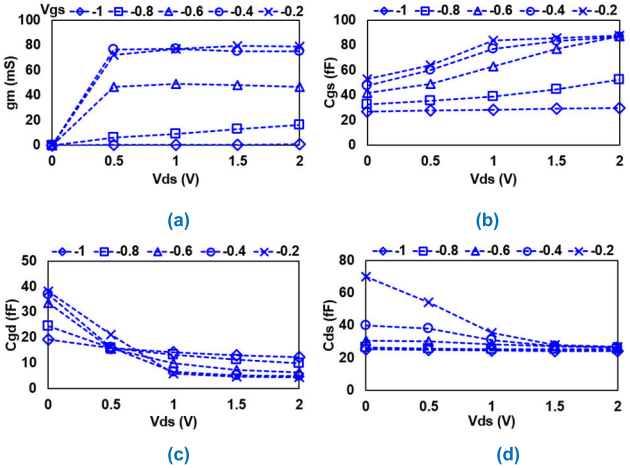

FIGURE 4. Small signal model parameters according to biases ((a) g_m (b) C_{gs} (c) C_{gd} (d) C_{ds}).

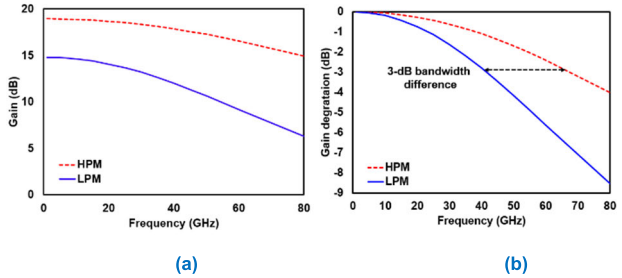

FIGURE 5. Calculated DA gain performance (a) Gain (b) Gain degradation according to frequency.

the small signal parameters according to the V_{ds}. Therefore, even if the V_{ds} of each transistor constituting the stack cell is different, if the V_{gs} is constant, the small signal parameters of each transistor may be assumed to have the same value. Using this assumption, Equation (1) can be used again when calculating the gain of LPM. For gain calculation, small signal model parameters are extracted from our in-house mHEMT's s-parameter measurement [18].

Figures 4 (a) – (d) show small signal model parameters according to biases. The gate length of mHEMT is 130 nm, and the size of that is $2 \times 50\ \mu$m. We assume that both Z_{gl} and Z_{dl} are 50 Ω-terminated and the n is 8. When the DA operates according to the bias scheme shown in Table 1, the total gain can be calculated and compared as shown in Figures 5 (a) and (b). G_{ds} is fixed as 3.3 mS. As shown in Figure 5 (a), the gain difference from HPM in LPM operation starts at about 3 dB, and the difference increases as the frequency increases. Thus, it can be seen that 3-dB bandwidth decreases by more than 20 GHz during LPM operation, as shown in Figure 5 (b).

The cause of the decrease in 3-dB gain bandwidth in LPM can be found through Equation (1) for G_m and the change of small signal parameters according to biases shown in Figures 4 (a) – (d). Under the bias condition of LPM, the g_m reduction of the transistors constituting the stacked gain cell is the most remarkable, and the C_{gd} is also slightly increased. In Equation (1), the decrease of g_m in the

numerator makes the magnitude of G_m smaller from the low frequency, and the increase of C_{gd} further decreases it as the frequency increases. The decrease of g_m in the denominator cancels out the g_m of the numerator and does not have a significant effect. Rather, as the frequency increases, the terms of capacitances have more influence and increase the magnitude of the denominator, thereby reducing the magnitude of G_m faster in Equation (1).

Therefore, to minimize the decrease in 3-dB gain bandwidth in LPM, the decrease in g_m and the increase in C_{gd} by continuously lowering V_{gs} should no longer be allowed, which in turn limits power back-off, or power reconfigurability. In previous papers that adopted the double gate-bias control scheme, LPM operation showed only about 3–4 dB power back-off characteristics, and even they showed power reconfigurability less than 2 dBm at 5 GHz or less depending on frequencies [5]–[6]. However, in commercial communication systems, power back-off of 5–6 dB or more is required during an LPM operation [19]. In conclusion, a new power reconfiguration method is needed to extend the gain bandwidth and power back-off in LPM.

B. GAIN CELL SWITCHING TECHNIQUE

As mentioned above, to overcome the drawbacks of the double-gate bias control scheme, this study proposes a new power reconfiguration method. Figure 6 shows the block diagram of a newly proposed gain cell switching technique. This is a method of turning off some of the gain cells that make up the DA during an LPM operation. That is, the operation of the gain cells is divided into ''ON'' and ''OFF'' modes. In HPM, all gain cells are operated in the ''ON'' mode, and in LPM, some of the gain cells are operated in the ''OFF'' mode to implement power reconfiguration. As shown in Figure 7 (a), in the ''ON'' mode, the gain cell is biased in the same way as HPM in Figure 2 (a). In the ''OFF'' mode, the supplied V'_{gg2} makes it fall below the pinch-off voltage ($V_{gg\_pinch-off}$). In this case, the bias of each transistor should be determined so that no current flows throughout the gain cell. As shown in Figure 7 (b), since V_{gg1} and V_{gg3} are fixed values, the voltage of node B is close to 0 V so that no current flows in the M1 transistor, and the voltage of node A is V_{gg3}-V'_{gg2} so that the M3 transistor also has the same pinch-off voltage as the M2 transistor. As an example, referring to Figures 7 (a) and (b), the bias voltages applied to each transistor of the triple-stacked FET gain cell during the ''ON'' and ''OFF'' modes are as shown in Table 2. From the bias configuration of each transistor shown in Table 2, in the ''OFF'' mode, the M1 transistor acts like a kind of capacitor. The gate-source voltages of M2 and M3 are given in a pinch-off state in which the drain current does not flow, and the drain voltage is divided according to V'_{gg2}. Therefore, it is possible to implement power reconfiguration while reducing the driving current of the entire DA by operating some of the gain cells in the ''OFF'' mode in LPM. Plus, compared with the conventional method, the control biases can be reduced from two to one, making the operation easier.

TABLE 2. Example of the bias scheme during the ''ON'' and ''OFF'' modes.

	ON	OFF
V_{dd} (V)	6.0	6.0
V_{gg3} (V)	3.6	3.6
V_{gg2} (V)	1.6	-1.0
V_{gg1} (V)	-0.4	-0.4
V_{ds} (M3) (V)	2.0	1.4
V_{ds} (M2) (V)	2.0	4.6
V_{ds} (M1) (V)	2.0	0.0
V_{gs} (M3) (V)	-0.4	-1.0
V_{gs} (M2) (V)	-0.4	-1.0
V_{gs} (M1) (V)	-0.4	-0.4

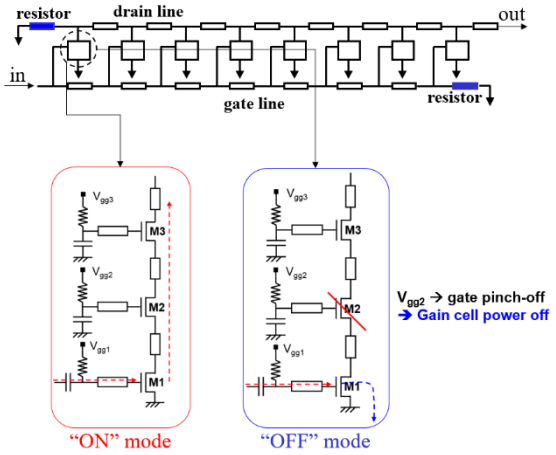

FIGURE 6. Block diagram of a newly proposed gain cell switching technique for LPM operation.

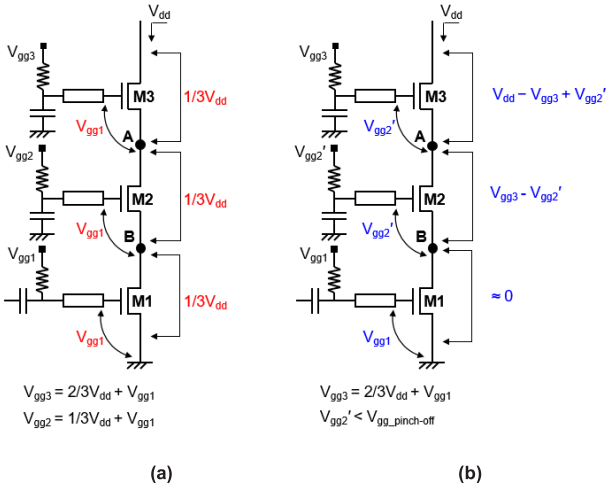

FIGURE 7. Biases of each transistor in (a) ''ON'' mode and (b) ''OFF'' mode.

Next, gain bandwidth can be calculated under the gain cell switching technique. First, when the gain cell operates in ''ON,'' since it is the same method as the previous HPM, the gain of the gain cell uses Equations (1) and (2) as it is. When operating in the ''OFF'' mode, since the g_m is close to zero from the bias configuration in Table 2, the equivalent circuit of the gain cell is changed as shown in Figure 8. In the ''OFF'' mode, the gain cell acts as a general transmission line to which small series capacitors are connected.

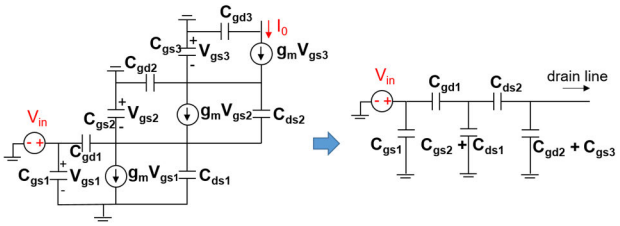

FIGURE 8. Equivalent circuit of the triple-stacked transistor in the "OFF" mode.

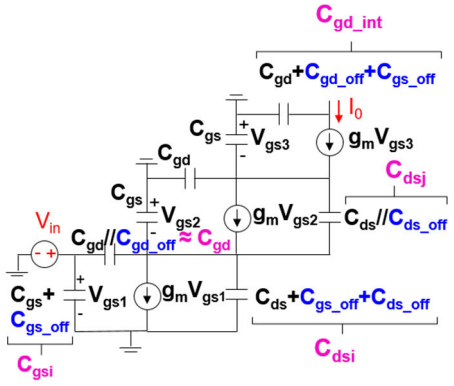

FIGURE 9. Circuit schematic of the "OFF" mode gain cell absorbed in the "ON" mode (black color parameters: "ON" mode; blue color parameters: "OFF" mode).

If we roughly put the capacitance values found from Figures 4 (a) – (d) and Table 2 into the above equivalent circuit, the gain cell in the "OFF" mode can be composed of capacitances between 10 fF and 150 fF. Since the value of the capacitance is small, the series capacitances pass only high frequencies and the parallel capacitances pass only low frequencies. Therefore, ideally, the input signal cannot pass through this circuit in the entire frequency band. Theoretically, if half of the gain cells are operated in the "OFF" mode in LPM, the n becomes half in Equation (2), the gain decreases by 6 dB, and the gain bandwidth does not differ from that of HPM.

To prove this, when implementing LPM with the gain cell switching technique, the total gain of DA can be calculated. To simplify the calculation, it is assumed that the eight gain cells of DA operate in the "ON" and "OFF" modes, respectively, in order from the front. Since the equivalent circuit in the "OFF" mode is a passive circuit, the total G_m can be recalculated by absorbing it into the "ON" mode. In this case, the G_m of the integrated gain cell (G_{m_int}) is calculated as Equation (3), and the circuit schematic of the "OFF" mode gain cell absorbed in the "ON" mode is shown in Figure 9. For convenience, the gate/drain line's inductance is ignored, and the C_{gs}, C_{gd}, and C_{ds} of transistors M1, M2, and M3 in

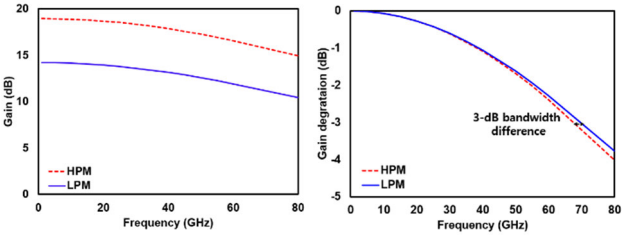

FIGURE 10. New calculated DA gain performance (a) Gain (b) Gain degradation according to frequency.

the "OFF" mode are unified as C_{gs_off}, C_{gd_off}, and C_{ds_off}, respectively. (5), as shown at the bottom of the page, where $C_{dsi} = C_{ds} + C_{gs\_off} + C_{ds\_off}$ and $C_{dsj} = C_{ds} \cdot C_{ds\_off}/(C_{ds} + C_{ds\_off})$.

Similar to section II−A, when the DA operates according to the bias scheme shown in Table 2, the total gain can be calculated and compared as shown in Figures 10 (a) and (b).

As expected from the analysis, the gain difference from HPM in LPM operation starts at about 6 dB, and the difference remains almost the same as the frequency rises.

In terms of power, the gain of DA can be expressed as Equation (4) as well as Equation (2) as is well known [20].

$$G = \frac{P_L}{P_{avs}} \tag{6}$$

where P_L is the power delivered to the load, and P_{avs} is the power available from the source. Since the other conditions are the same in LPM and HPM, the difference in gain can be considered to be similar to the difference in output power. Of course, if the input power increases and the output power is strongly saturated, the transistors in the "OFF" mode can operate in a class B or C type, and the assumption mentioned earlier can be changed. In general, input power is divided into each gain cell when the n of DA is large, so it can be said that the back-off power follows the gain difference unless it is in a deep saturation region.

Therefore, the proposed gain cell switching technique can provide greater power back-off than the conventional method with gain bandwidth equal to that of HPM. However, the LPM gain is reduced by more than 6 dB compared with HPM, and if the capacitances of the transistors in the "OFF" mode gain cell are large, they may have a negative effect on RF performance in LPM. To effectively utilize this method for power-reconfigurable DA, a semiconductor process with a high maximum oscillation frequency (f_{MAX}) and cut-off frequency (f_T) is advantageous.

$$G_{m\_int} = \frac{g_m\left(g_m - sC_{gd}\right)}{\frac{g_m + s\left(C_{gs}+C_{gd}+C_{dsj}\right)}{g_m + sC_{dsj}}\left(g_m + s\left(C_{gd} + C_{gs} + C_{dsi} + C_{dsj}\right)\right) - sC_{dsj}} \tag{5}$$

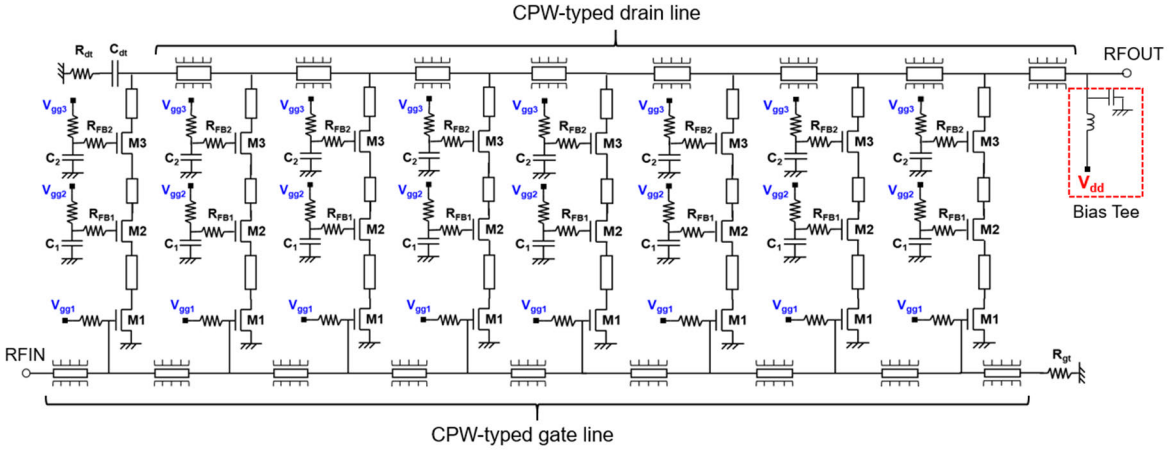

FIGURE 11. Circuit schematic of the proposed power-reconfigurable DA.

III. DESIGN OF POWER-RECONFIGURABLE DISTRIBUTED AMPLIFIER

To confirm the analysis performed earlier, a power-reconfigurable DA is designed using a 130 nm mHEMT process that has good RF performance. Figure 11 represents the circuit schematic of the proposed DA. It consists of eight gain cells. The size of the used mHEMT is commonly $2 \times 50\ \mu m^2$. Each gain cell is composed of triple-stacked FETs to overcome the low breakdown voltage of mHEMT and increase output power. The triple-stacked FET structure also facilitates LPM operation by the gain cell switching technique. According to the theory of stacked FET PA, the shunt capacitors C_1 and C_2 values are initially set to match the voltage swing of each transistor to the maximum, but the tuned values 60 fF and 20 fF are finally used in consideration of the bandwidth performance and prevention of oscillation [21]. In addition, 10 Ω series feedback resistors R_{FB1} and R_{FB2} are added in front of the shunt gate capacitances C_1 and C_2 of M2 and M3 transistors to prevent high-frequency oscillations that are likely to occur in the stacked FET structure. The drain/gate lines are implemented with coplanar waveguide (CPW) transmission lines that are easy to process and have low loss at high frequencies [22]. The gate CPW line has a line width of 10 μm, a ground spacing of 30 μm, and a line length of 240 μm. The drain CPW line has a line width of 10 μm, a ground spacing of 20 μm, and a line length of 280 μm. For absorbing the waves reflected at the gate/drain lines, 40 Ω of R_{gt} and R_{dt}, which are gate/drain termination resistors, are connected to the end of the gate/drain lines, respectively. In addition, 5.65 pF C_{dt} is connected in series with R_{dt} to protect R_{dt} from drain current. To reduce the chip size, the drain voltage is designed to be supplied through an external bias tee.

Figure 12 shows the simulated S_{21} of the proposed power-reconfigurable mHEMT DA. In HPM, all eight gain cells are operated in the "ON" mode, and in LPM, the 2nd, 4th, 6th, and 8th gain cells are operated in the "OFF" mode. An LPM operation with the double gate control bias scheme

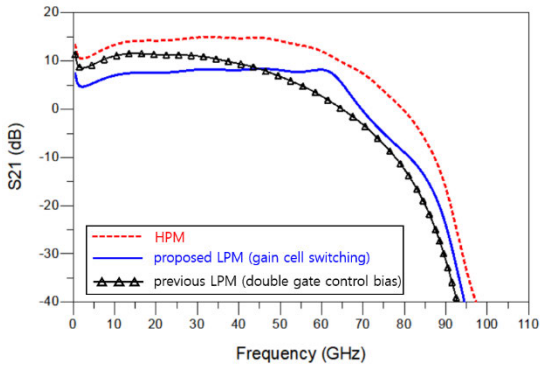

FIGURE 12. Simulated S21 of the proposed power-reconfigurable mHEMT DA.

is simulated for comparison. All parameters are consistent except for bias conditions and the double gate control bias is selected under the optimal state considering both the power reconfigurability and the gain bandwidth.

As analyzed in section II, the gain of the previous LPM method decreases as the frequency increases. 3-dB gain bandwidth decreases by more than 20 GHz compared with HPM, whereas the newly proposed LPM method has a flat gain slope and 3-dB gain bandwidth similar to HPM. In the calculation, the resistive components of the transistor are not included in the equivalent circuit for simplicity. At high frequencies, the gate-drain resistance (R_{gd}) of the transistor increases the loss, and the feedback resistors added to prevent oscillation also degrade the gain by reducing the G_m of stacked FET cell. This is why the simulated gain is reduced from the calculated value.

Figures 13 (a) and (b) show the simulated output power (P_{out}) and drain efficiency (DE) according to the frequencies in the power-reconfigurable mHEMT DA. To compare the reconfigurable power characteristics, both HPM and LPM operations are compared at the same input power according to frequencies. The input power is determined based on the 4−5-dB compression point in HPM. As shown

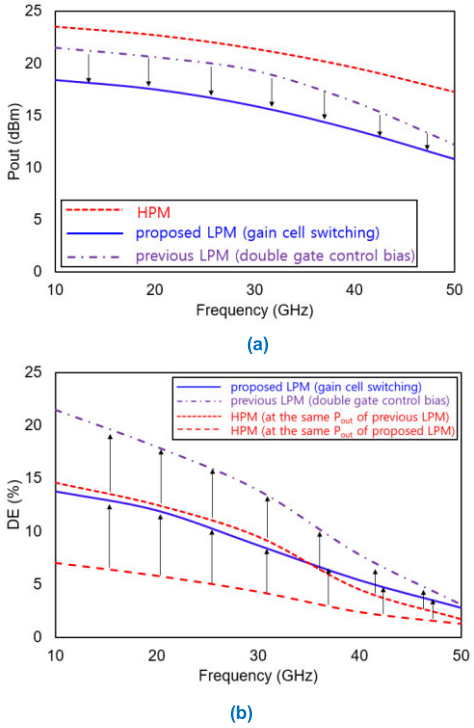

FIGURE 13. Simulated (a) output power and (b) drain efficiency in HPM and LPM with the same input power.

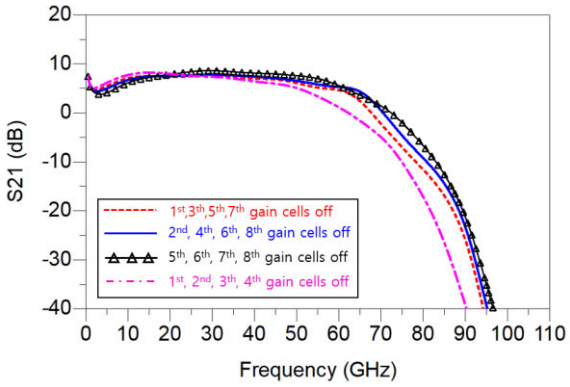

FIGURE 14. Simulated S21 according to the position of turning off the gain cells under LPM.

in Figure 13 (a), the newly proposed LPM shows higher power reconfigurability compared with the previous one for the same input power. In addition, unlike the previous method, it shows uniform power reconfigurability at 30 GHz or more. As shown in Figure 13(b), it brings about twice as high back-off drain efficiency at the same output power compared with HPM.

Through the above simulations, it is shown that the proposed DA shows more improved 3-dB gain bandwidth and power reconfigurability performance than the previous method by applying the gain cell switching technique to LPM.

Additionally, we investigated the effect of the position of turning off the gain cells through simulation. Figure 14 shows

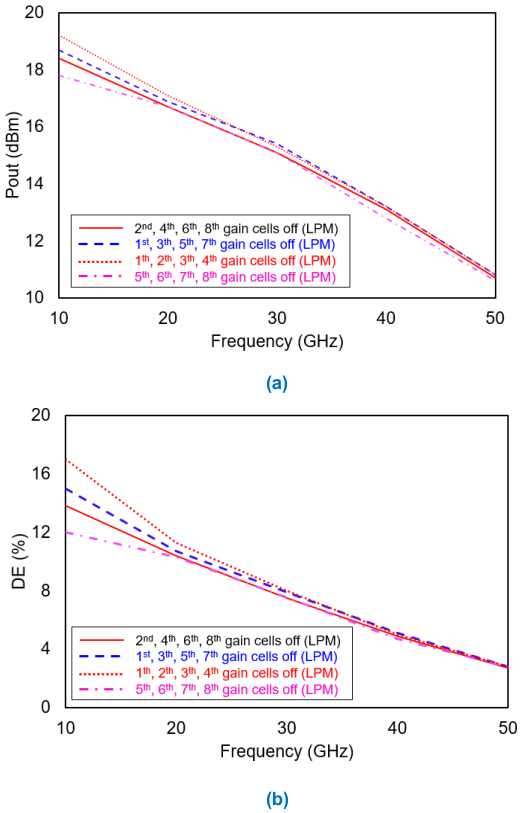

FIGURE 15. Simulated (a) output power and (b) drain efficiency according to the position of turning off the gain cells.

the simulated S21 result. As can be seen in Figure 14, there is no significant difference in the influence of S21 characteristics depending on the positions where the gain cells are turned off, except that the bandwidth of S21 is reduced in the case that the 1st, 2nd, 3th, 4th gain cells are off. As the bandwidth is reduced when the front gain cells are turned off, it can be expected that the increase of the parasitic components at the front end have a greater effect on the overall gain reduction at high frequencies. Figures 15 (a) and (b) show the simulated P_{out} and DE according to the positions where the gain cells are turned off. As shown in Figures 15 (a) and (b), when the front gain cells are turned off, the P_{out} and DE are slightly improved. The reason is thought to be that the parasitic components added when the gain cells close to the DA output are turned off directly affect power loss. In conclusion, it can be seen that even with the same number of cells turned off, the gain bandwidth and output power are slightly affected depending on the position where they are turned off, and there is a trade-off relationship.

IV. FABRICATION AND MEASUREMENT

The power-reconfigurable DA proposed in this study was fabricated using the in-house mHEMT process developed at Seoul National University [16]. $In_{0.8}GaP/In_{0.4}AlAs/In_{0.35}GaAs$ mHEMTs layers were grown by molecular beam epitaxy (MBE) on GaAs substrate. The metamorphic buffer consisted of a 1 μm-thick linearly graded InAlAs layer with

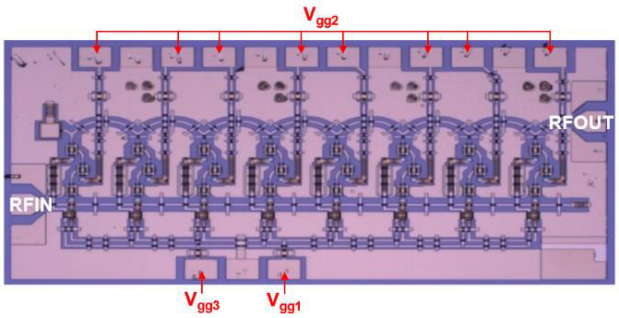

FIGURE 16. Chip photograph of the fabricated mHEMT DA (size = 2.16 mm × 1.16 mm).

a final indium content of 45%. Our previous works have been successfully fabricated by this process, which is a 130 nm $In_{0.8}GaP/In_{0.4}AlAs/In_{0.35}GaAs$ mHEMTs technology [14], [15]. The mHEMT exhibits a maximum extrinsic g_m of 750 mS/mm. The gate-drain breakdown voltage of 8 V, on-state breakdown voltage of over 4 V, and forward turn-on voltage of 0.9 V, respectively, are measured at a gate current density of 1 mA/mm. The fabricated $2 \times 50\ \mu m^2$ mHEMT achieves a f_T of 133 GHz and f_{MAX} of 291 GHz, respectively.

Figure 16 is the chip photograph of the mHEMT DA. The chip size is 2.16 mm × 1.16 mm. Capacitors are implemented with metal-insulator-metal (MIM) capacitors, and resistors are implemented with thin film resistors (TFR). The ground planes of the CPW are connected to several air bridges so that RF signals are stably transmitted through the transmission line. The measured S-parameters are shown in Figures 17 (a) and (b). The bias conditions in the "ON" mode are $V_{dd} = 4.3$V, $V_{gg3} = 2.4$ V, $V_{gg2} = 1.6$ V, and $V_{gg1} = -0.3$ V, and in the "OFF" mode, it is $V_{gg2} = -1$ V. The total quiescent drain currents under HPM and LPM were 256 and 130 mA, respectively. In actual measurements, the original bias is fine-tuned to obtain the best small signal S-parameter characteristics. The measured results are largely consistent with the simulation results. In HPM, the fabricated mHEMT DA represents return loss at which S_{11} is below −13 dB from 0.5 to 65 GHz and S_{22} is below −7.5 dB from 0.5 to 64 GHz. The measured S_{21} is greater than 10 dB from 0.5 to 62.5 GHz, the peak value of which is 13.6 dB at 16.5 GHz. In LPM, it represents return loss at which S_{11} is below −12.5 dB from 0.5 to 74 GHz and S_{22} is below −12 dB from 2.5 to 66 GHz. The measured S_{21} is greater than 4.4 dB from 0.5 to 65 GHz, the peak value of which is 7.1 dB at 13 GHz. From the S-parameter measurement, it can be seen that the mHEMT DA maintains a trend similar to that of HPM in both gain bandwidth and return loss when operating in LPM by the proposed gain cell switching technique.

Next, to test the output power performance of the proposed DA, output power (P_{out}) and efficiency were measured at several frequencies (10, 20, 30, and 40 GHz) in HPM. Figure 18 shows the output power and power added efficiency (PAE) in HPM. The fabricated mHEMT DA obtains a saturated output power (P_{sat}) of 20.2 – 21.5 dBm with a

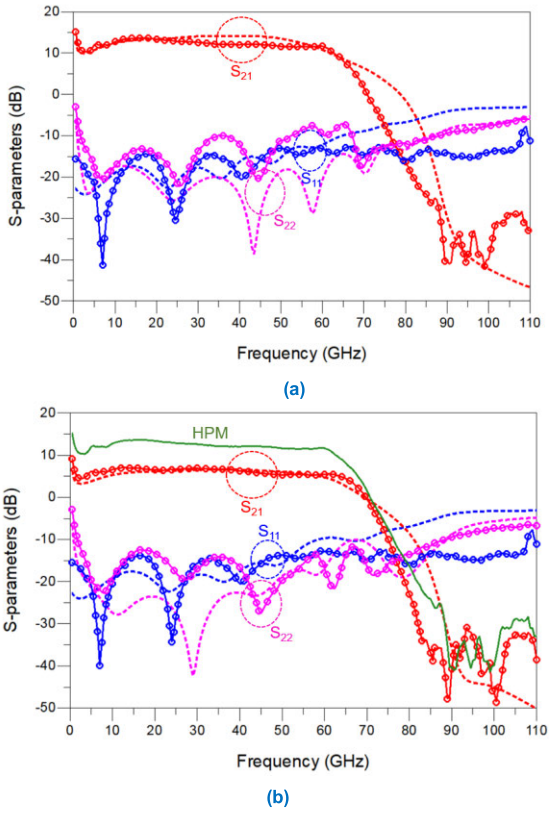

FIGURE 17. S-parameters of the DA under (a) HPM (b) LPM (simulation: dashed lines, measurement: solid lines with circle shapes, "ON" mode: $V_{dd} = 4.3$ V, $V_{gg3} = 2.4$ V, $V_{gg2} = 1.6$ V, and $V_{gg1} = -0.3$ V, "OFF" mode: $V_{dd} = 4.3$ V, $V_{gg3} = 2.4$ V, $V_{gg2} = -1$ V, and $V_{gg1} = -0.3$ V).

PAE of 11.6% – 20.0%. The P_{out} and PAE at 1-dB compression point (P_{-1dB}) is 17.1 – 19.6 dBm and 5.5 – 10.1% from 10 to 40 GHz, respectively. Unlike the previous power-reconfigurable DAs, it is noteworthy that output power maintains 20 dBm or more, even at 30 GHz or more, corresponding to the 5G frequency band. Unfortunately, the output power was not measurable beyond 40 GHz because our power source cannot support enough input power beyond 40 GHz. However, compared with the simulation result in Figure 13 (a), the output power up to 40 GHz shows similar results with less than 2 dBm error and power reconfigurability with 1 dB error, so even at 50 GHz, the measurement results are expected to be similar to the simulation.

To test the power- reconfigurable characteristics of the proposed DA, the P_{out} and DE in LPM are measured according to frequencies. The same input power is supplied in both modes for comparison. Figure 19 represents the power-reconfigurable characteristics of the proposed mHEMT DA. It obtains a saturated output of 14.7 – 15.9 dBm with a DE of 8.3 – 11.4%. As expected from the simulation, the newly applied method provides 5.5 to 5.8 dB of power back-off, which is higher than the previous method, from 10 to 40 GHz, and the higher than the previous method, from 10 to 40 GHz, and the power back-off deviation according to frequency is within only 0.3 dB. It provides uniform power back-off

TABLE 3. Performance comparison of power-reconfigurable DAs/Conventional DAs operating beyond 30 GHz.

Ref	Technology	Topology	BW[5] (GHz)	Linear Gain (dB)	P_{sat} (dBm)	P_{-1dB} (dBm)	PAE (%)	LPM BW[5] (GHz)	LPM power back-off (dB)	LPM DE (%)	Chip Size (mm^2)
[7]	0.15 μm pHEMT	Conventional DA	0.1–40	16	–	18–25 @2-4 0 GHz	—	—	—	—	2.64
[8]	40 nm GaN HFET	Conventional DA	1–57	14.5	26 @20 GHz	22.5 @ 20 GHz	13 @10 GHz	–	–	–	–
[9]	InP HBT	Conventional DA	1–160	10.5	14.6–17.8 @1-110 GHz	13.5–17 @1-110 GHz	12.5 @110 GHz	–	–	–	1.28
[10]	130 nm SiGe	Conventional DA	14-105	6-12	4–17 @14-105 GHz	4–14.9 @14-105 GHz	1–12.6[1] @14-105 GHz	–	–	–	1.51
[11]	22 nm FD SOI CMOS	Conventional DA	0.4–31.6	11.6	14.5–16.4 @0.4-35 GHz	10.6–12.9 @ 0.4-35 GHz	10–17.2[1] @ 0.4-35 GHz	–	–	–	1.50
[12]	45 nm SOI PMOS	Conventional DA	1.5–103	16	19–22 @20-60 GHz	17–21 @20-60 GHz	10–19.5[1] @20-60 GHz	–	–	–	0.73
[5]	0.15 μm pHEMT	PRDA[2] (DGBC[3])	DC–53	10.0–14.8	18.3–24.0[1] @1-40 GHz	–	4.9–18.5[1] (DE) @1-40 GHz	DC–44	2.2–4.1[1]	4.4–18[1]	3.92
[6]	65 nm CMOS	PRDA (DGBC)	0.5–38	11.0–15.7	12.8–20[1] @1-38 GHz	7.5–16.6[1] @1-38 GHz	2–18[1] (DE) @1-38GHz	–	1.5–4.8	6.1–16	3.3
This work	0.13 μm mHEMT	PRDA (GCST[4])	0.5–62.5	10.0–13.6	20.2–21.5 @10-40 GHz	17.1–19.6 @10-40 GHz	11.6–20 @10-40 GHz	0.5–65	5.5–5.8	8.3–11.3	2.5

[1]Estimated data from the reported paper [2]Power-reconfigurable distributed amplifier [3]Double gate bias control scheme [4]Gate cell switching technique [5]small-signal gain bandwidth

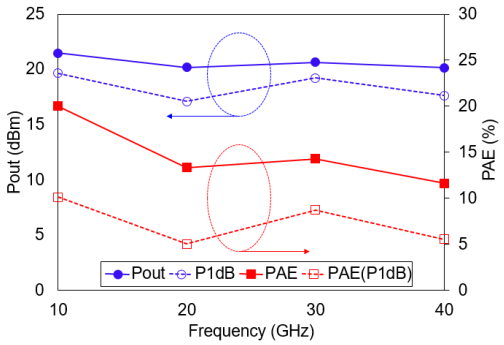

FIGURE 18. Measured output power and PAE of the DA in HPM (V_{dd} = 4.3 V, V_{gg3} = 2.4 V, V_{gg2} = 1.6 V, and V_{gg1} = −0.3 V, input power = 10–13 dBm).

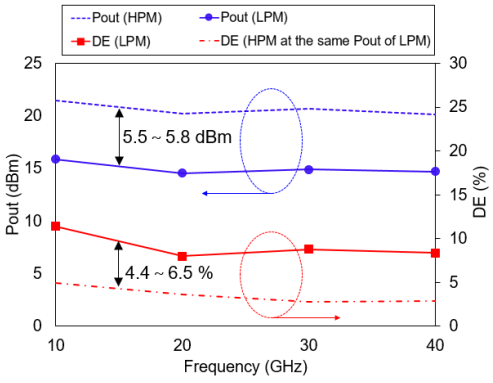

FIGURE 19. Measured output power and DE of the DA in LPM with the same input power (V_{dd} = 4.3 V, V_{gg3} = 2.4 V, V_{gg2} = −1 V, and V_{gg1} = −0.3 V, input power = 10–13 dBm).

regardless of frequencies. In addition, when LPM is applied to the DA, it obtains the advantage of back-off power DE by 4.4 – 6.5% compared with conventional DA (HPM). Figure 20 shows the measured output power versus PAE, DE in HPM, and LPM at 10 GHz. As shown in Figure 20, when LPM is applied at 10 GHz, the efficiency curves according to output power sweep are shifted to the left, and accordingly, the efficiency at the low power region can be improved. Similar graphs are obtained at other frequencies. Through the above measurements, the improved reconfigurable power performance of DA is verified.

Table 3 summarizes the performance of the reported power- reconfigurable DAs and conventional DAs operating beyond 30 GHz. For fair comparison, P_{sat}, P_{-1dB}, PAE, and LPM DE over 10 GHz are summarized. Compared with conventional DAs, the proposed DA shows competitive performance in the overall specifications. In particular, among the reported DAs, it is the only one that consistently shows an output power of 20 dBm or more and a PAE of 10% or more up to 40 GHz. The advantages of the proposed DA appear better when compared with the other power-reconfigurable DAs. Compared with [5], the 3-dB gain bandwidth is increased in LPM, and LPM power back-off is increased compared with [5] and [6]. Plus, it appears uniformly in broadband. Although power back-off is increased, DE is also maintained at a level that does not deteriorate significantly compared to previous works.

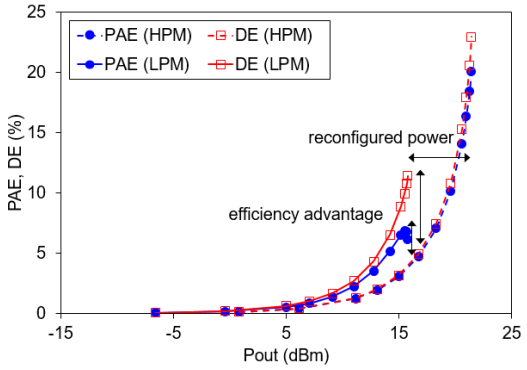

FIGURE 20. Measured output power versus PAE, DE in HPM and LPM at 10 GHz.

V. CONCLUSION

A power-reconfigurable DA is implemented using a 130 nm mHEMT process. Our in-house mHEMT process can provide a transistor with a higher f_T and f_{MAX} than the conventional GaAs pHEMT process. As a result, by improving the RF power performance of the triple-stacked FETs constituting the DA, the fabricated DA shows an output power of 20 dBm or more and a PAE of 10% or more up to 40 GHz. In addition, the gain cell switching technique is proposed to increase 3-dB gain bandwidth in LPM, and power reconfigurability is improved by increasing power back-off. The proposed power-reconfigurable DA is expected to be used as a multi-function power amplifier supporting multi-bands and multi-modes in various RF applications ranging from DC to millimeter wave bands in the future.

ACKNOWLEDGMENT

The author would like to thank Prof. Jinho Jeong of Sogang University for proposing a circuit design that applies power reconfigurable operation to a DA for the first time, and Prof. Kwangseok Seo of Seoul National University for making a chip through the advanced mHEMT process through a national project.

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