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Fast Near-Interface Traps in 4H-SiC MOS Capacitors Measured by an Integrated-Charge Method

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ABSTRACT Oxide traps existing in 4H-SiC MOS capacitors with fast response times that are active in the strong accumulation and depletion regions were characterized by an integrated-charge method. The method is based on the measurement of charging and discharging voltages across MOS capacitors in response to high-frequency voltage pulses. This method can identify traps with response times in the order of hundreds of nanoseconds. The results reveal an increasing density of near-interface traps with energy levels above the bottom of the conduction band, which are the active defects reducing the channel-carrier mobility in 4H-SiC MOSFETs.

INDEX TERMS 4H-SiC MOS capacitor, MOSFET, near-interface traps (NITs), near-interface trap density (DNIT), trap response time.

I. INTRODUCTION

In recent times, significant progress has been made in the development of 4H silicon carbide (4H-SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs) [1]–[3]. In spite of being commercialized and delivering higher performance compared to their silicon counterparts, 4H-SiC MOSFETs continue to suffer from low channel-carrier mobility [4], [5]. The low channel-carrier mobility is attributed to both interface [6], [7] and near-interface traps (NITs) [8], [9]. The most critical impact of these defects is at the operating gate voltage (V_G), when the MOSFETs are biased in strong inversion. At this bias level, owing to the quantum confinement effect, the Fermi level (E_F) is above the bottom of the conduction band (E_C) at the SiC surface [10]–[12]. Consequently, near-interface traps with energy levels aligned to the conduction band can trap electrons from the channel by tunneling [13]–[15]. A trapped electron is immobile for the fraction of time that it is trapped, which is observed as a reduction of the average mobility below the electron mobility in the absence of trapping. This tunneling of electrons to the near-interface traps is an important reason for the low channel-carrier mobility in 4H-SiC MOSFETs.

Typically, MOS capacitors are used to investigate interface and near-interface traps as they are much easier to fabricate in comparison to MOSFETs. In this paper, MOS capacitors on N-type SiC, biased in accumulation, have been used to represent the biasing of a MOSFET in strong inversion [3], [11].

Numerous characterization techniques based on MOS capacitors on N-type SiC have been used, but most of these techniques are applicable only to the depletion region [16]–[18]. There are some recently developed techniques that are capable of characterizing MOS capacitors in strong accumulation. Current-transient techniques were used by Amini Moghadam *et al.* to characterize MOS capacitors biased in accumulation, but the response times of the traps measured were longer than 20 ms because of the limitation of the instruments for current measurements [6].

Recently, Pande *et al.* published a direct current-measurement technique that could detect near-interface traps with specific response times in the order of hundred nanoseconds [19]. In this technique, a high-frequency sinusoidal

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voltage was applied across a series connection of a resistor and the MOS capacitor under test. By measuring the voltage across the MOS capacitor, Pande *et al.* showed that the voltage across the capacitor was distorted from the expected sinusoidal waveform. This effect was attributed to the near-interface traps with response times in the order of hundred nanoseconds. However, direct measurement technique cannot detect NITs with response times longer than 100 ns. This is because the direct measurement technique utilizes distortions in the measured sinusoidal signals, which are very small when the frequency is reduced below 5 MHz. Consequently, this technique is not sufficiently sensitive to detect traps with response times longer than hundreds of nanoseconds.

The observed distortion in the expected sinusoidal waveform is the key issue with all characterization techniques based on the AC measurements of accumulation capacitance [16], [20].

A standard method successfully used in silicon technology, which can characterize traps with response times ranging from nanoseconds to milliseconds, requires capacitance measurements from high to low frequencies [21]. According to this method, the trapped electrons with longer response times do not respond to high-frequency signals, whereas they do respond to the low-frequency signals. In the case of SiC-based MOS capacitors, the quasi-static measurement technique can be used for the low-frequency measurements, but there is no reliable high-frequency measurement technique. The AC measurements based on the sinusoidal signal at frequencies above 1 MHz are not reliable due to the above-mentioned distortion of the sinusoidal waveform (particularly in accumulation).

Capacitance can be measured by stepping input voltage and measuring charge using commercial instruments like Agilent and Keithley, but these instruments have the limitation of integrating the charge for at least 100 ms.

To overcome these limitations, we propose in this paper an integrated-charge technique suitable for measurements of fast-response times. This technique enables the detection of traps with response times from hundreds of nanoseconds up to hundreds of milliseconds and can be applied in accumulation as well as in depletion.

II. THE INTEGRATED-CHARGE MEASUREMENT TECHNIQUE

The integrated-charge measurement technique utilizes a series *RC* circuit, where an external resistor, *R* is connected in series with the MOS capacitor as shown in Fig. 1.

The measurement is then performed by applying $v_{IN}(t)$ voltage consisting of a DC-bias voltage (V_G) and a superimposed rectangular waveform with precise height and set frequency. In this paper, we used rectangular waveform with duty cycle of 50%, and frequencies of 10 kHz, 100 kHz, 1 MHz, and 2 MHz. Both the applied voltage, $v_{IN}(t)$, and the voltage across the capacitor, $v_C(t)$, are measured over multiple periods. To reduce noise, the digital storage oscilloscope automatically averages thousands of cycles, which

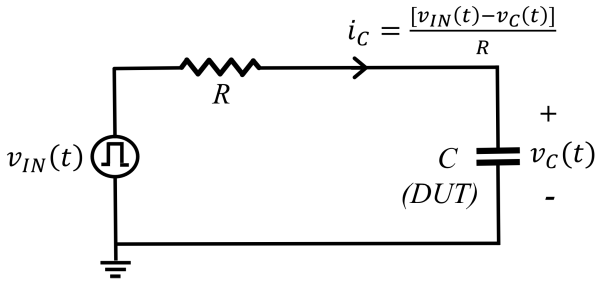

FIGURE 1. Measurement circuit with the MOS capacitor (*C*) as the device under test (DUT) and an external series resistor *R*.

the instrument delivers as a clear trace over a single period. Then we download the data for both input, $v_{IN}(t)$, and output, $v_C(t)$, voltages and for a single period to obtain the charging and discharging currents as $[v_{IN}(t) - v_C(t)]/R$.

Once the measurement at a set DC-bias voltage is completed, the DC-bias voltage is stepped down with the selected voltage step in order to take measurements from accumulation to depletion (gate voltages from 15 to −5 V). In this paper, the range of 15 V to +5 V was measured with the step of 500 mV and the range from +5 V to −5V was measured with the step of 100 mV. The voltage steps are sufficiently small so that the resulting changes in electric field and band bending are negligible and do not significantly impact the response time. This is different from the fact that a change in applied bias from $V_G = 5$ V to $V_G = 15$ V does change the electric field significantly, reducing the distance of an individual trap from the SiC surface and shortening the time response. Given the time it takes to perform the measurement and download the data at a single DC point, and given the number of DC points measured in accumulation, it takes 1-2 hours of gate biasing in accumulation ($0 < V_G < 15$V). It takes about the same time to perform the measurements with $V_G < 0$V.

In response to the rising edge of the pulse, the electron density per unit area on the capacitor plates is changed by ΔN_{el}. This change corresponds to a charge flow through the resistor and the capacitor, which is equal to $Aq\Delta N_{el}$, where A is the area of the capacitor and q is the electron charge. This charge can be obtained by integrating the current through the resistor and the capacitor. The available commercial instruments do not enable precise measurements of fast current transients. Therefore, we used the resistor in the circuit shown in Fig. 1 to obtain the current from the measured $v_{IN}(t)$ and $v_C(t)$ voltages. Then, we integrated this current to obtain the change in electron density in response to the rising edge of the applied pulse:

$$\Delta N_{el} = \frac{1}{qAR}\int_0^{T/2}(v_{IN} - v_C)\,dt \tag{1}$$

The integration is performed over the half period of the applied pulses ($T/2$) because this corresponds to the rising edge of the pulse.

Analogous integration is applied for the falling edge, which gives the change of electrons on the capacitor plates in

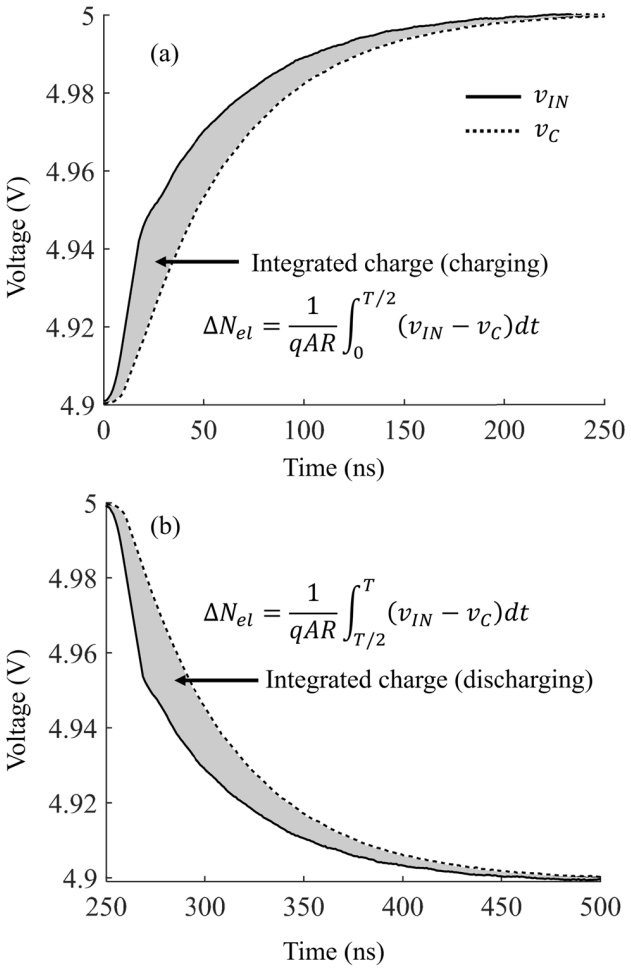

FIGURE 2. Illustrative voltage transients: (a) rising edge for charging, (b) falling edge for discharging. The voltage transients consist of real data measured at $V_G = 4.95$V with 2 MHz rectangular waveform (the digital storage oscilloscope automatically averages thousands of periods to deliver these traces over a single period).

response to the falling edge. In principle, the total value of this change of electrons has to be the same as for the rising edge. Hence, to reduce the noise, the average value was used as the final result for ΔN_{el}.

Figure 2 illustrates the voltage transients of $v_{IN}(t)$ and $v_C(t)$ for the case of DC-bias voltage $V_G = 4.95$ V, which means the applied 100-mV pulse changes $v_{IN}(t)$ and $v_C(t)$ voltages between 4.90∼V and 5.00∼V. The shaded area between $v_{IN}(t)$ and $v_C(t)$ is the integrated charge corresponding to the rising and falling edges of the applied pulse. It is important to note that the integrated charge does not depend on the actual shape of the applied pulse $v_{IN}(t)$, for as long as both $v_{IN}(t)$ and $v_C(t)$ reach the maximum level during the rising edge and the minimum level during the falling edge (these levels are 5.00∼V and 4.90∼V in Fig. 2). This feature enables measurements of fast transients that are not sensitive to pulse distortions by the function generator and by the parasitic capacitances and inductances in the measurement probes.

The direct result of this measurement technique—the change of electron density at the capacitor plate (ΔN_{el})—can be used to calculate the corresponding capacitance per unit area by the following fundamental equation:

$$C = \frac{q\Delta N_{el}}{\Delta v_{IN}} \tag{2}$$

III. EXPERIMENTAL DETAILS

In this paper, MOS capacitors were used as the device under test (DUT) in the *RC* circuit shown in Fig. 1. The samples were fabricated on N-type, silicon-faced 4H-SiC wafers with a 10^{16}cm^{-3} nitrogen-doped epitaxial layer. Before the oxidation, cleaning of the samples was performed by standard Radio Corporation of America (RCA) procedure. Oxidation in dry O_2 for 60 min and subsequent annealing in nitric oxide for an additional 60 min were performed in a horizontal-tube furnace at 1250°C and atmospheric pressure. The thickness of the grown oxide was 51 nm. To form square MOS capacitors with the area of 500×500 μm^2, aluminum was sputtered and patterned by photolithography after the oxidation. Aluminum was also deposited on the back of samples to form Ohmic contact. It is worth noting that, before performing any further measurements, the leakage currents of the MOS structures were measured. The maximum leakage current through the gate oxide was found to be in the order of nA.

It is a well-established phenomenon that gate oxides on SiC trap electrons when the gate is biased at positive voltages and that these electrons remain trapped for days. If the first Capacitance–voltage (C–V) measurement of a virgin sample is performed by sweeping the voltage from depletion to accumulation and then swept back from accumulation to depletion, the C–V curve measured from accumulation to depletion will exhibit shift to positive voltages due to the electron trapping. These electrons remain trapped for a very long time and repeated C–V measurements by sweeping in either direction will match the accumulation-to-depletion measurement. That is why standard C–V measurements on SiC MOS capacitors are performed from accumulation to depletion [9], [22]. However, the amount of this electron trapping depends on the value of positive voltage and the duration of positive-voltage biasing [23]. To avoid the adverse impact of this voltage- and time-dependent drift, we held the sample at 15 V for 10 min, before starting the measurement from accumulation to depletion.

AC measurements were performed by Agilent B1505A Power Device Analyzer and the measured capacitance and conductance are shown in Figs. 3 (a) and (b), respectively. It should be noted that the overlapping C–V curves at both low and high frequencies, shown in Fig. 3 (a), were obtained when separate calibration (open circuit, short circuit and phase compensation) at each frequency was performed for the AC measurements by Agilent B1505A. However, even with the separate calibrations, which resulted in overlapping C–V curves, the corresponding values of the conductance were negative. This has no physical meaning and is an effect of the best-achieved fitting of assumed perfect sinusoidal

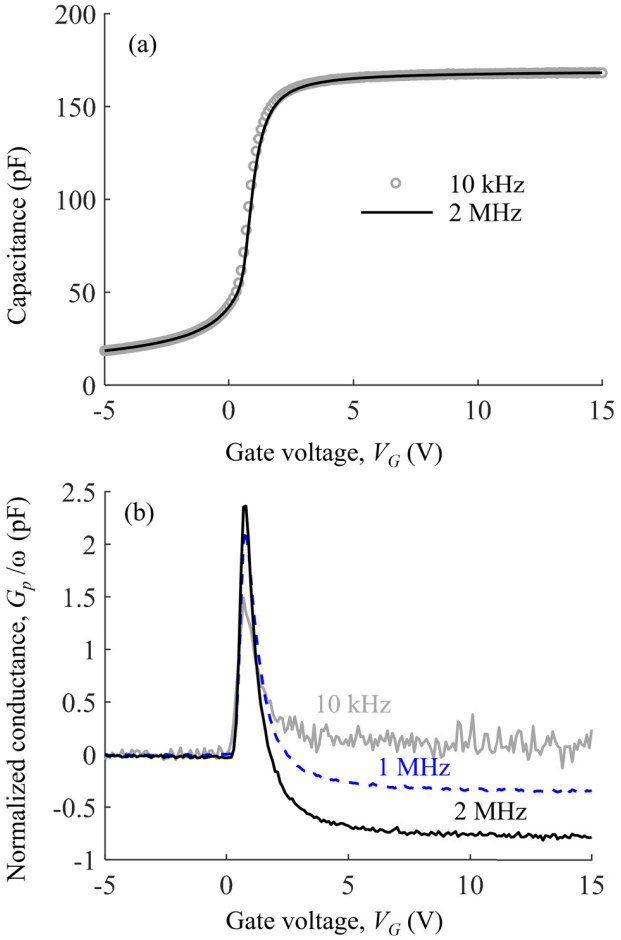

FIGURE 3. (a) Capacitance-voltage curves of the measured MOS capacitors. For better clarity the lowest and highest frequency C–V curves are shown. There was no observable difference in the C–V measurement at the following frequencies: 10 kHz, 100 kHz, 1 MHz, and 2 MHz. (b) Normalized conductance-voltage curves of the measured MOS capacitors for 10 kHz, 1 MHz, and 2 MHz.

voltages to the actual distorted sinusoids at higher frequencies [19]. The implication of this result is that the high-frequency measurements by the AC method cannot be trusted, because of its dependence on specific calibration process. The Agilent B1505A was also used to perform quasi-static C–V measurements. A voltage pulse of 100 mV was used in this method to calculate the capacitance.

For the integrated-charge measurements, square pulses with the frequencies of 10 kHz, 100 kHz, 1 MHz, and 2 MHz were applied as input voltage by a Tektronix AFG1022 function generator, through 60 kΩ 5.5 kΩ, 360 Ω, and 100 Ω resistors, respectively. The response times (half period) were 50 μs, 5 μs, 500 ns, and 250 ns for 10 kHz, 100 kHz, 1 MHz, and 2 MHz frequencies, respectively. A Tektronix DPO 7104 oscilloscope with Tektronix P6139B voltage probes was used to measure the input voltage and the voltage across the capacitor. The measurements were performed in a dark box at room temperature. The effect of parasitic capacitance due to the oscilloscope probes and connecting wires was eliminated when calculating the integrated charge.

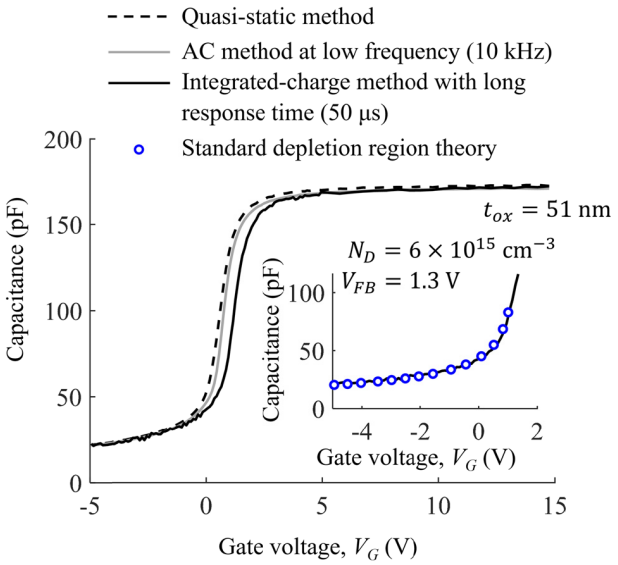

FIGURE 4. Comparison of C–V curves obtained using quasi-static, AC, and the proposed integrated-charge method. The inset shows the matching of the curve obtained from standard depletion region theory with the depletion curve measured by the integrated-charge method, which was used to determine the donor doping density (N_D), and the flat-band voltage (V_{FB}). The capacitance at V_{FB} = 1.3 V is 111 pF. The capacitance corresponding to mid-gap voltage, $V_{MG} = -1.07$ V is 32.6 pF.

The C–V curve obtained from integrated-charge method with the long response-time (50μs) was used to determine the donor doping density (N_D), and the flat-band voltage (V_{FB}) (see Fig. 4).

IV. RESULTS AND DISCUSSION

A. COMPARISON TO QUASI-STATIC AND AC METHODS

Figure 4 shows the comparison of C–V curves obtained by three methods: (1) the integrated-charge method with long response time (50 μs), (2) the quasi-static method, and (3) the AC method at low frequency (10 kHz). The measurements shown in Fig. 4 using the two available standard techniques (the quasi-static and AC methods) followed the standard measurement procedures, which is gate-voltage sweeping from accumulation to depletion, but without a long exposure at the highest positive value of the gate voltage. The results obtained by all three methods agree in accumulation and depletion. However, there is a voltage shift, which reflects different densities of electrons trapped far from the interface (deep trapping) due to different times of exposure to high positive gate voltages [23]. In the quasi-static and the AC methods, the sample is exposed to the positive voltages for several seconds only, when the measurements are performed from accumulation to depletion. However, the integrated-charge method keeps the MOS capacitor under positive gate voltage for 1-2 hrs. This long exposure to positive voltage enabled the slow traps, positioned further from the interface, to be filled by electrons, resulting in the positive shift of flat-band voltage.

This effect of shifting C–V curves due to the exposure to positive gate voltages is well established [23] and it represents

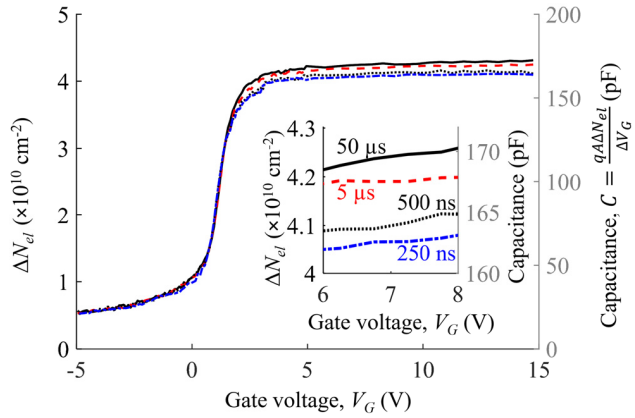

FIGURE 5. Electron-density change (ΔN_{el}) and capacitance corresponding to gate-voltage steps $\Delta V_G = 100$mV. In the inset, the solid, the dashed, the dotted, and the dash-dot lines correspond to the electrons responding the gate-voltage steps within time intervals of 50 μs, 5 μs, 500 ns, and 250 ns, respectively.

a significant problem for the application of the standard high/low frequency method for trap characterization. The commonly observed differences in capacitance at a given voltage can be misinterpreted as interface traps, whereas they could be to a large extent C–V shifts due to different density of electrons at the slow near-interface traps. For example, the split between the quasi-static and the AC C–V curves in Fig. 4, which is also called ''frequency dispersion'', could be interpreted as a capacitance reduction at a certain voltage, rather than a flat-band voltage shift. If the interpretation is a capacitance reduction at a given voltage, the application of high–low frequency method would convert the capacitance reduction into trapped electrons that are unable to respond to the high frequency (in Fig. 4, these would be electrons that respond to the quasi-static measurements but cannot respond to the 10 kHz AC signal applied by the AC measurement). However, the quasi-static and the AC measurements expose the sample to high positive gate voltages for different time intervals, which may cause the deep trapping and the shift in flat-band voltage. To remove the shift of C–V curves due to difference in the density of electrons trapped at slow traps (the slow traps are not filled when the long exposure to high V_G is not applied), it is recommended to apply a high positive gate voltage for a long time before performing the C–V measurements.

In contrast, the integrated-charge method enables measurements with very short and with long response times and with almost identical exposure to positive gate voltages. This enables the characterization of traps without the undesirable impact of flat-band voltage shift. Therefore, we used the results obtained by the integrated-charge method with long response time (50 μs) as the reference level for comparisons to measurements with faster response times.

B. CHARGE MEASUREMENTS

The measurement results for ΔN_{el} and the corresponding capacitance are shown in Fig. 5 (ΔN_{el} is shown on the left-hand y-axis and capacitance on the right-hand y-axis). The solid line is obtained by integrating the responding charge up to 50 μs (half-period of the applied 10-kHz pulses as described in the previous section). Similarly, other curves have been obtained by integrating the responding charge up to 5 μs (the dashed line), 500 ns (the dotted line), and 250 ns (the dash-dot line).

Theoretically, it should be possible to use the current measured with the smallest resistor of 100 Ω, corresponding to the shortest time constant, and to profile the time response of the traps by integrating the current from $t = 0$ to $t = t_e$. Theoretically, the profiling would be achieved by changing from 250 ns to as long as 1 s. However, the shortest time constant with the smallest resistance corresponds to the highest value of measured current, which drops to noise levels after several time constants. Accordingly, we used larger resistors and longer time constants to reduce the current range and to measure the smaller currents corresponding to traps with longer response times. The largest resistor that we used was 60 kΩ, corresponding to the time constant $\tau = 60\,\text{k}\Omega \times 172.49\,\text{pF} = 10.34\ \mu$s. With this time constant, we used a rectangular waveform with frequency of 10 kHz and half-period of 50 μs. This means that the fraction of the integrated charge for the case of trap-free current is $1 - e^{(-50/10.34)} = 0.9921$. When we integrate the measured current up to 50 μs, this fraction is somewhat smaller because any trapped charge with response times longer than 50 μs is not detected. The integrated charge from the measured current, ΔN_{el}, corresponds to capacitance $C = q\Delta N_{el}/\Delta v_{IN} = 172.49$ pF at $V_G = 15$ V. For the measurement with 5 μs pulse (time constant of 0.94 μs), the trapped charge with response times longer than 5 μs is not detected. Because more trapped charge is not detected, a smaller value of integrated charge ΔN_{el} is measured, and in this case, it corresponds to a smaller apparent capacitance, $C = 169.95$ pF. For the shortest pulse of 250 ns (time constant of 17 ns), trapped charge with response times longer than 250 ns is not detected, corresponding to the smallest value of integrated charge ΔN_{el} and the smallest apparent capacitance, $C = 163.89$ pF.

Therefore, the differences in ΔN_{el} in the accumulation region ($V_G > V_{FB} = 1.3$V) show the existence of electrons with response times between 250 ns and 50 μs. The trapped electrons do not respond to pulses with short periods [24], however, they do respond to the pulse that integrates all responding charge up to 50 μs.

In the depletion region ($V_G < V_{FB} = 1.3$V), the measurements with long and short integration times show the same results. This means that (1) the density of trapped electrons responding between 250 ns and 50 μs is negligible and (2) the absence of flat-band voltage shifts is consistent with the equal exposures to positive gate voltages (equal deep-trapping effect).

This absence of detected traps for $V_G < V_{FB} = 1.3$V is different from the results published in studies of threshold-voltage instabilities in SiC MOSFETs. The reason is that the thermal emission of electrons from traps with energy

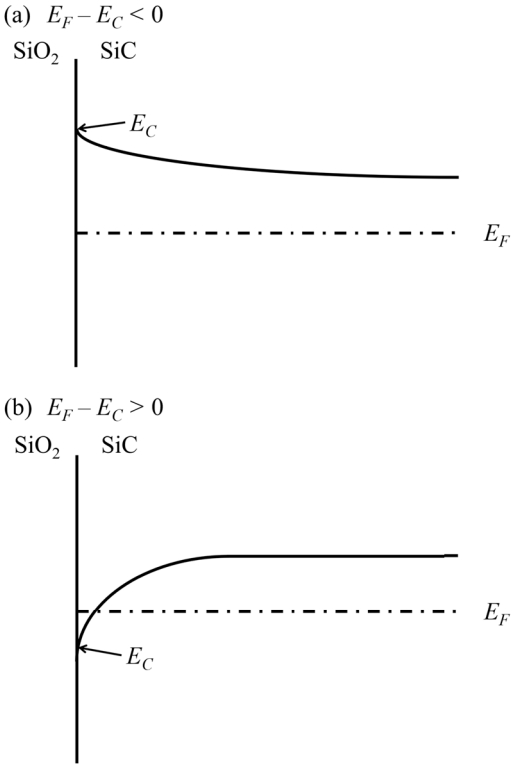

FIGURE 6. Illustration of the position of the bottom of conduction band (E_C) at the SiC surface with respect to fermi level (E_F) in (a) depletion, (b) accumulation.

levels toward the midgap (deep traps) takes much longer than 50 μsnnnn, and in fact extend to days, months, and years. This is different from the case of P-type body of N Channel MOSFETs, where the trapped electrons at deep traps are neutralized by capturing holes. When the P-type body of MOSFET is biased in strong inversion, electrons are supplied from the drain and the source, and the traps re-capture electrons.

C. CONVERSION OF V_G INTO $E_F - E_C$ AT SIC SURFACE

The applied V_G, from the deep depletion to accumulation, should be converted into the corresponding position of the Fermi level at the SiC surface with respect to the bottom of the conduction band ($E_F - E_C$), as illustrated in Fig. 6.

Standard depletion region theory is applied in the depletion region, to convert V_G to $E_F - E_C$ [25] which is represented by the solid line in Fig. 7.

For the accumulation region, the quantum-mechanical theory is needed to account for the quantum confinement and the resulting effect of the Fermi level appearing above the bottom of the conduction band at the SiC surface [26], [27]. Pennington *et al.* considered the quantum confinement effect to determine the areal density of electrons in strong inversion (N_{inv}) as a function of $E_F - E_C$ [27]. The energy bands of P-type SiC in strong inversion are analogous to the energy bands of N-type SiC in accumulation [11], [19]. Hence,

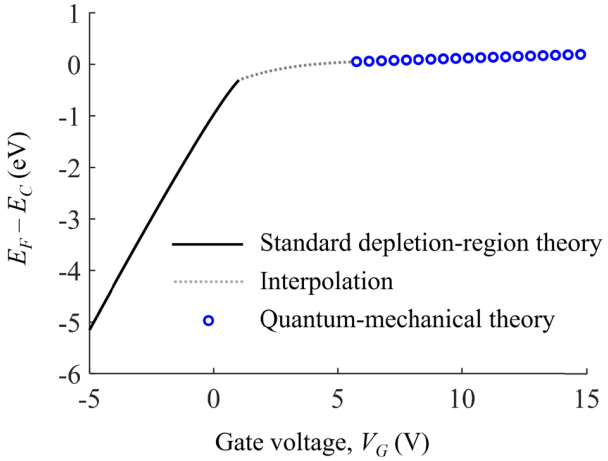

FIGURE 7. Energy positions with respect to the gate voltage.

by replacing N_{inv} with areal density of electrons in accumulation (N_{acc}),

$$N_{acc} = \frac{(V_G - V_{FB})\, C_{ox}}{q} \tag{3}$$

The results obtained in [27] for N_{inv} versus $E_F - E_C$ can be used to relate the Fermi level ($E_F - E_C$) to the applied V_G. The results are shown by the symbols in Fig. 7.

As can be seen in Fig. 7, there is a gap between the quantum-mechanical results in the accumulation and the standard theory in depletion. To make the conversion of gate voltage continuous, a spline interpolation has been performed (the dashed line in Fig. 7).

D. DENSITY OF TRAPPED ELECTRONS AT NEAR-INTERFACE TRAPS

As shown in Fig. 5, ΔN_{el} and the corresponding capacitance are different for different response times in the accumulation region ($V_G > 1.3$V). These differences between faster response-time measurements (250 ns, 500 ns, and 5 μs) and the longest response time (50 μs), are equal to the density of trapped electrons that are too slow to respond to the faster pulses. Dividing this density of trapped electrons per unit area by the energy-band bending, ΔE_C, that corresponds to the applied voltage pulses, we obtain the following equation for the density of trapped electrons per unit area and unit energy:

$$D_{NIT} = \frac{\Delta N_{el_{SLOW}} - \Delta N_{el_{FAST}}}{\Delta E_C} \tag{4}$$

where $\Delta N_{el_{FAST}}$ is the change of electron density at the capacitor plate for shorter response time measurements and $\Delta N_{el_{SLOW}}$ is the change of electron density at the capacitor plate for the longest response-time measurement (50 μs). Therefore, D_{NIT} in (4) is equal to the density of *active* near-interface traps—the traps that capture and release electrons—which is different from the absolute or total density of defects near the interface.

The obtained result for the density of active near-interface traps (D_{NIT}) with energy levels E_{NIT} aligned to E_F, which

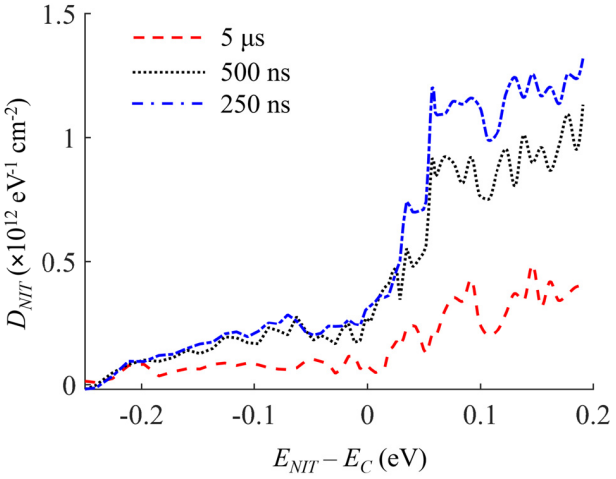

FIGURE 8. Density of active near-interface traps (D_{NIT}) obtained from the proposed integrated-charge method. The dashed line represents the density of trapped electrons with response times between 5 μs and 50 μs. Similarly, the dotted line and the dash-dot line show the densities of trapped electrons with response times from 500 ns to 50 μs and from 250 ns to 50 μs, respectively.

means $E_{NIT} - E_C = E_F - E_C$, is shown in Fig. 8. It reveals that the highest trap density is observed for the shortest response time. Also, the density increases with energy and the majority of traps have energies aligned to the conduction band ($E_F - E_C > 0$), which corresponds to the accumulation region. This also implies that tunneling of electrons to and from the near-interface traps is the responsible mechanism for electron trapping in the accumulation region [28]–[30]. It is worth noting that there are interface traps that are active in the energy gap ($E_F - E_C < 0$) and, as can be seen in Fig. 8, the density of interface traps with shorter response time is higher. However, the density of these interface traps is 4 to 5 times lower in comparison to the density of near-interface traps that are active at $E_F - E_C > 0$.

E. DISCUSSION

AC measurements are typically used to characterize MOS capacitors. The C–V curves for the N-type, 4-H SiC MOS capacitors used in the present study are shown in Fig. 3(a). With careful calibration, we could match the C–V curves at various frequencies, but the normalized conductance becomes negative for frequencies above 1 MHz [Fig. 3(b)], which has no physical meaning. CV measurement techniques, based on sinusoidal modulation, are sensitive on the distortions of the sinusoidal waveform due to the impact of capture and release of electrons from near-interface traps and with time constants in the order of the signal period [19]. This distortion is the reason for physically impossible results, such as the negative conductance shown in Fig. 3(b). The meaningless negative conductance in the accumulation region appears for as low frequency as 1 MHz, which means that the density of near-interface traps with the time constant in the order 1 μs is sufficiently high to distort the sinusoidal waveform. The key advantage of the integrated-charge method is that the integration of current through the capacitor—performed to obtain the charge in response to a voltage step—does not depend on the distorted shape of the current.

It should also be noted that the equation used in the standard high–low frequency method cannot be applied in accumulation, because the accumulation capacitance at low frequency is equal to the oxide capacitance ($C_{LF} = C_{ox}$) resulting in the division by $C_{ox} - C_{LF} = 0$. However, the direct measurement of ΔN_{el} at faster response times by the integrated-charge method enabled us to use Eq. (4) to calculate trap densities (D_{NIT}) when the MOS capacitor is biased in the accumulation also, as shown in Fig. 8.

Another advantage is that the integrated-charge technique is able to detect traps with response times in the order of hundred nanoseconds (Fig. 2), in comparison to other techniques that detect traps with response times in the order of microseconds [3], [6], [16], [31]. The integrated-charge technique does not have any measurement delay, because it is directly measuring the electrons captured during the half-period of high voltage level and released during the half-period of low-voltage level of the rectangular waveform.

The results in Fig. 8 show an increase in D_{NIT} above the bottom of E_C. These NITs are located near the SiO_2/SiC interface and trap electrons from the conduction band by tunneling [3], [6], [8], [25].

Integrating the trapped carriers per unit area and unit energy, shown in Fig. 8, we obtain the trapped carrier density of 6.9×10^{10} cm^{-2} for the case of charge integration up to 5 μs. This means that the response times of these trapped carriers are longer than 5 μs. Because the total carrier density at $V_G = 15$ V is about 6.3×10^{12} cm^{-2}, only 1.1% of carriers with response times longer than 5 μs are trapped. However, the density of trapped carriers with response times longer than 500 ns increases to 1.8×10^{11} cm^{-2}, which is about 2.9% of the total carrier density. The density of trapped carriers with response times longer than 250 ns is 2.3×10^{11} cm^{-2}, corresponding to 3.6% of the total carrier density. The fraction of trapped carriers will continue to increase if trapped charge with faster response times than 250 ns is included.

The measured data show that 1.1%, 2.9%, and 3.6% of carriers with response times longer than 5 μs, 500 ns, and 250 ns, respectively, are trapped. These data can be fitted by the following equation, with the coefficient of determination $R^2 = 0.995$:

$$f_{trapped} = a\tau^b \tag{5}$$

where a = 0.01055, b = −0.3847, $f_{trapped}$ is the fraction of trapped electrons in percent, and τ is the response time in seconds. This equation shows that the fraction of trapped channel electrons increases to 74% when traps with response times longer than 0.1 ns are included.

V. CONCLUSION

In this paper, an integrated-charge method has been proposed to characterize active near-interface traps in N-type 4H-SiC MOS capacitors biased in both depletion and accumulation

regions. The main advantage of this method is its ability to detect active NITs with energy levels aligned to the conduction band and with response times in the order of hundred nanoseconds to hundred milliseconds. This was enabled by utilizing an *RC* circuit to measure fast current transients and also by the fact that the integrated charge is insensitive to any distortions in the applied voltage pulses. The measurement results show an increase in the density of active NITs with increasing energy levels above the bottom of the conduction band.

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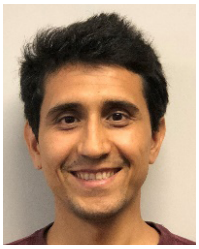

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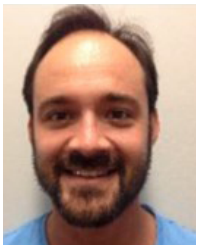

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