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MicroSTARLING: A Millimeter Scale Self-Organizing Optical Communication Processor for Embedded Multihop Sensor and Computational Networks

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ABSTRACT In the development of small scale, networked nodes, design inspiration can be found in the decentralized and simplistic communication used by starlings in flight. Here, we present a novel node processor based on simple nearest neighbor connections to yield a self-organized linear optical sensor network. We present the processor state machine design and evaluation of the Verilog code. Each node, termed a MicroSTARLING, contains a processor fabricated using 180nm CMOS technology. The chips are 1.2mm $\times$ 1.2mm and the digital processor occupies 0.063 mm^2 of the chip. We assemble three test bench nodes to evaluate the processor function in wired, wireless communication and fully wireless circuits. When nodes are directly wired, the MicroSTARLING processor functions with a 25MHz input clock enabling a linear multihop network readout of 8 devices in 1.8ms. With a 20μW, 524KHz input clock, the processor requires 12μW at 1.2V. We evaluate the processor function under optical communication obtaining 6-hops between 7 nodes with little noticeable reduction in communication quality. Our fully wireless node required 3mW of power harvested via a 940nm light emitting diode (LED) and communicated via separate LEDs. To our knowledge this is the first demonstration of more than 3 hops of linear wireless communication with a mm scale self-organizing node processor. The processor size and power make possible the concept of smart dust networks with multihop communication between nodes for an embedded wireless sensor network in biological tissue structures or as the foundation of an optical neural network for edge computing.

INDEX TERMS Wireless sensor networks, optical communications, smartdust, computational networks.

I. INTRODUCTION

There exist many structures comprised of individual units in communication. The internet and the brain are two of significance that exist at different ends of the size scale. Other examples include sensor network arrays, insect swarms, and starling murmurations. For smaller and simpler units, the communication methods are simpler and efficient. For example, with starlings in flight network communication seems to involve only the 6 or 7 closest birds, yet the entire murmuration moves as if a single living entity [1].

Our interest is in miniature versions of embedded networks and murmuration networks. Embedded networks we classify as networks that are interspersed into an active functional environment. The goal is to have the units sample data and/or stimulate the environment. This is conceptually similar to a miniature sensor network used to measure temperature across the surface of the human hand [2] instead of across a rain forest [3]. The network only reads out the temperatures, it does not know what to do in response to the data. Murmuration networks we consider as networks that exist

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in a generally passive environment and are concerned with processing data from outside of the network as with a neural network. In nature a murmuration is a group of starlings which fly as a large group and change the group form and flight direction in response to external threats or food sources.

In either network type, we are concerned with network technology for currently impractical applications. Currently, there are no readout systems based on submillimeter-scale nodes for embedded sensor arrays such as distributed neuronal recording arrays [4] or embedded computational networks, such as artificial neural networks embedded in 3D printed smart materials [5]. Other applications include underwater optical networks, motion tracking or biomarker monitoring in 3D printed tissue and microrobot swarm linkages. Our size goal is 1mm scale in a first generation, 180nm CMOS node processor and 200 micrometer scale in a future, 45nm CMOS processor. We therefore call the nodes ''micro'' starlings and the entire network a ''micro'' murmuration or micromurmer.

What then can one learn from nature when developing small scale communication units? Nature seems to teach a few lessons: to avoid complexity, to embrace simplicity, to interact with the units closest, to develop fast low latency approaches and to avoid centralization of the interactions. The work presented herein is an attempt to apply these lessons to a practical communication network. We will avoid complexity with a single purpose, small size processor that is not required to maintain knowledge of the entire network. We will embrace simplicity by communicating small data packets. We designed the nodes to interact with only the neighboring nodes and respond to loss of neighbors with network repair latencies of tens of milliseconds.

Our goal for the work presented in this report is to develop the essential part of the node, the data link control layer or processor. It will be a single function processor using hundreds of fast parallel logic gates not thousands as in a standard serial microprocessor. However, we add analog physical layer circuits to demonstrate a complete system that can be wirelessly powered and controlled. Optical communication is the focus of the paper but communication via resistive or capacitive coupling when the nodes are embedded in a conductive media could be used as well. There are several networks which can inform the design of an embedded network. Several are presented in the next section.

II. RELATED WORK

A. WIRELESS SENSOR NETWORKS

Wireless sensor networks are used to take data samples from an environment such as the side of a volcano, a vineyard, or the rooms in an office building. Typically, individual units or nodes are formed into a network which leverages neighboring units to relay a data message to the external observer. Several commercial devices exist and even more research devices. A comprehensive review of radio frequency (RF) wireless sensor networks can be found in a paper by Amutha [6]. Most wireless sensor systems rely on some form of radio frequency transmission as the physical communication means. The physical signals are interpreted by the data link control systems to allow transmission and reception of data packets.

Of the many existing network types and protocols, each can be categorized as either single-path or multi-hop. Single-path protocols such as the star network and one-to-one network have no data packet relays. In tree, mesh and linear networks the data may hop across more than one link as it is transmitted and thus can undergo a multihop path. An advantage of multi hop pathways is that transmission power can be greatly reduce for the wireless sensor network (WSN) [7]. Wireless sensor networks have been used in crop management [8], geological studies [9], structural health monitoring [10] and other areas. The algorithms and protocols to optimize WSNs are well suited for use in a complex microprocessor handling cluster heads or for systems with significant centralized control of the network. However, for a dumb terminal or ultra-simplistic node many of the proposed algorithms are too complex. In addition, current WSNs based on RF signals are too large to meet our desired demonstration unit's mm scale size specifications. There are single chip processors that are hundreds of micrometers in scale, but these usually require an RF antenna that makes the entire chip larger [11]. In addition, for a multihop network that requires several links to operate simultaneously, the RF crosstalk is likely to be significant [12]. A solution to avoid prohibitively large antennae and crosstalk for large networks is to use a light emitting diode (LED) chip based optical physical layer. In addition, the use of optical communication may allow for multiple links to communicate in the same optical band since the signals cannot propagate as far across the network as RF.

B. OPTICAL COMMUNICATION SYSTEMS

Free space optical (FSO) communications became common in the 1970's [13], [14]. While free space optical communication could be used to describe any non-fiberoptic based optical communication system, in practice it refers to complex systems capable of laser-based point to point communication with high data rates. Often the laser is steered towards a target with mechanical or other means. These systems can be made mobile [15] but are usually fixed to tall structures or satellites [16]. The large size of these systems precludes them from easy modification for use in miniature embedded networks.

A more size appropriate optical approach can be found in visual light communication (VLC) systems. The term VLC could be used to describe any free space optical systems but typically describes LED and non-coherent, small-scale systems for use over meters as opposed to kilometers [17]. Since these systems tend to use visible light, they are well suited to underwater as well as terrestrial use [18]. VLC systems tend to use LED transceivers controlled by compact single board computers such as the Arduino series, focal plane gated arrays or BeagleBones [19]–[23]. The key advantage over other

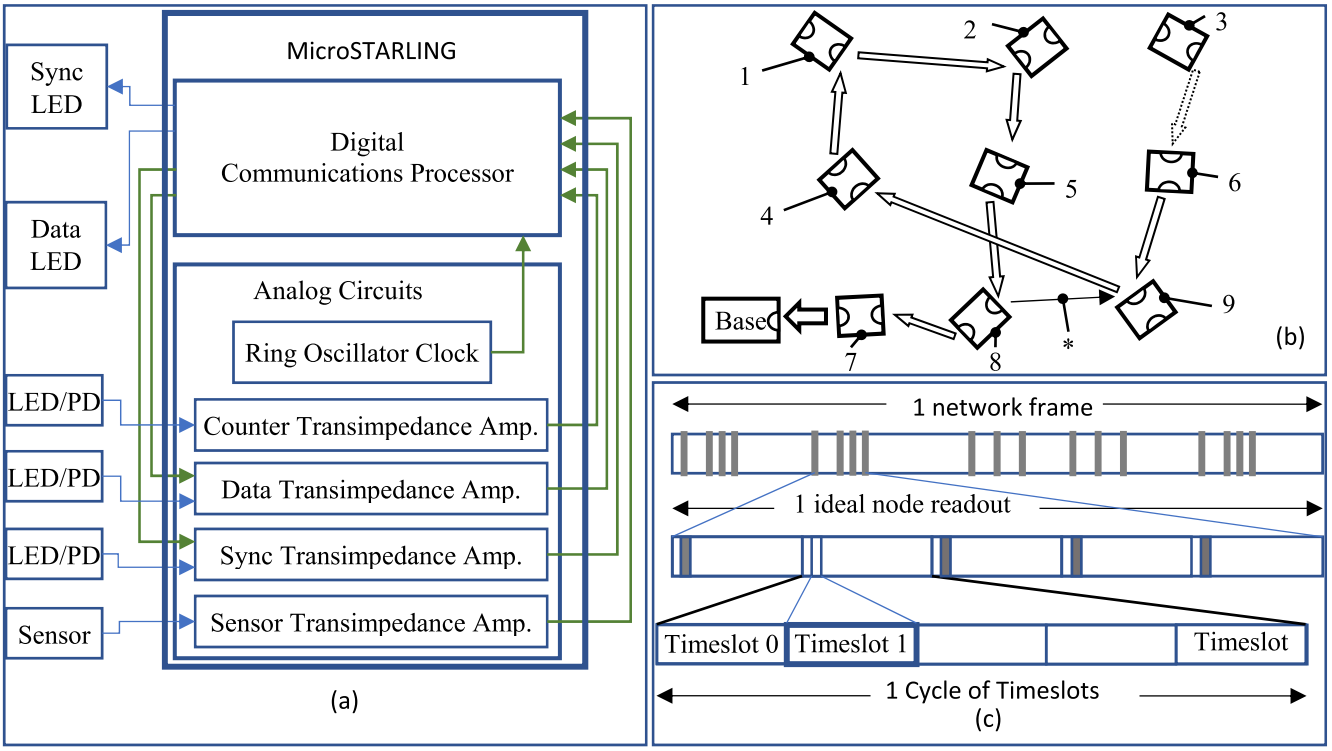

FIGURE 1. (a) The node is designed to be compact and comprised of MicroSTARLING chip, external photoactive devices, and sensor. The digital communications processor controls the interpretation of input signals from other nodes and sends appropriate sync and data signals. The processor periodically samples the sensor amplifier and packages the data value into the data signal. The processor also clock divides the input clock as part of a counter alignment process. The MicroSTARLING chip has analog interface circuits including a ring oscillator clock and four transimpedance amplifiers. The Data and Sync transimpedance amplifiers are gated and others are always on. (b) The nodes are designed to be placed into aligned or random orientation forming a network based upon the processor algorithm and physical orientation. The base node acts as a drain to readout the nearest node (7) and can be placed anywhere near the network or it can be remote using fiber optics for communication with the embedded array. Some nodes (3) may not find partners so redundant coverage is required for random orientation arrays. The algorithm is designed to avoid and recover from collisions due to light flashes (∗) from non-partner nodes. (c) The entire network array is readout in a *network frame* (with 5 nodes in this case). Each frame is made of a preset number of ideal *node readouts*. The node readouts are comprised of a set number of *timeslots*, 16 for the current fabricated processor.

optical communication methods are the many demonstrations of multihop optical networks while using incoherent LEDs for both signal detection and generation. These credit card sized systems are still too large for use in miniature embedded networks. In addition, many of the systems utilize network layer methods which transmit large data packets suitable for file or image transfers. This is a desirable feature for room scale systems but for an embedded network the data transfers will be much smaller and thus allow for lower complexity, smaller processors, lower power, and faster transfers.

C. SMART DUST DEVICES

For a miniature network we envision submillimeter units small enough to be embedded in the brain to study neural function, embedded in a bioprinted cornea to detect surgical motion or form a learning network in a cubic centimeter of transparent conductive polymer. Smart dust nodes are mm scale devices that use optics [11], [24], [25], ultrasound [26] or radio frequency [11], [27] to communicate data to an outside control unit. The promise of smart dust is a miniature multihop wireless sensor network. However, such a network has not yet appeared in published work. Typically, the smart dust wireless nodes only interact with the base station and not other nodes. To our knowledge multihop networks using mm scale units have yet to be presented. A possible reason for the lack of multihop devices is the use of optical, RF and ultrasound-based devices that require a link to a large base unit to function. Another consideration is the complexity of the processors required to meet specifications such as IEEE 802.15.4 or transmit kilobits of data per second.

The term smart dust indicates why the miniaturization of smart dust has not continued to 100um scale true dust size or been used in large networks of 3 or more nodes. The goal is often to make a smart node, rather than a collection of not-so-smart nodes. The device complexity seems restrictive to size.

III. NODE AND NETWORK DESIGN

A. NODE OVERVIEW

The nodes presented in this report are designed to be 1-mm scale in size. To that end we sought to design a system requiring a minimal number of external components. Fig. 1 shows the ideal organization of a node. The primary component being the MicroSTARLING chip designed and presented herein. Ancillary components include light emitting diodes (LED), photodiodes (PD) and a sensor. The MicroSTARLING chip has analog and digital circuits which are wire bonded (Fig. 1, green lines) to fully connect each

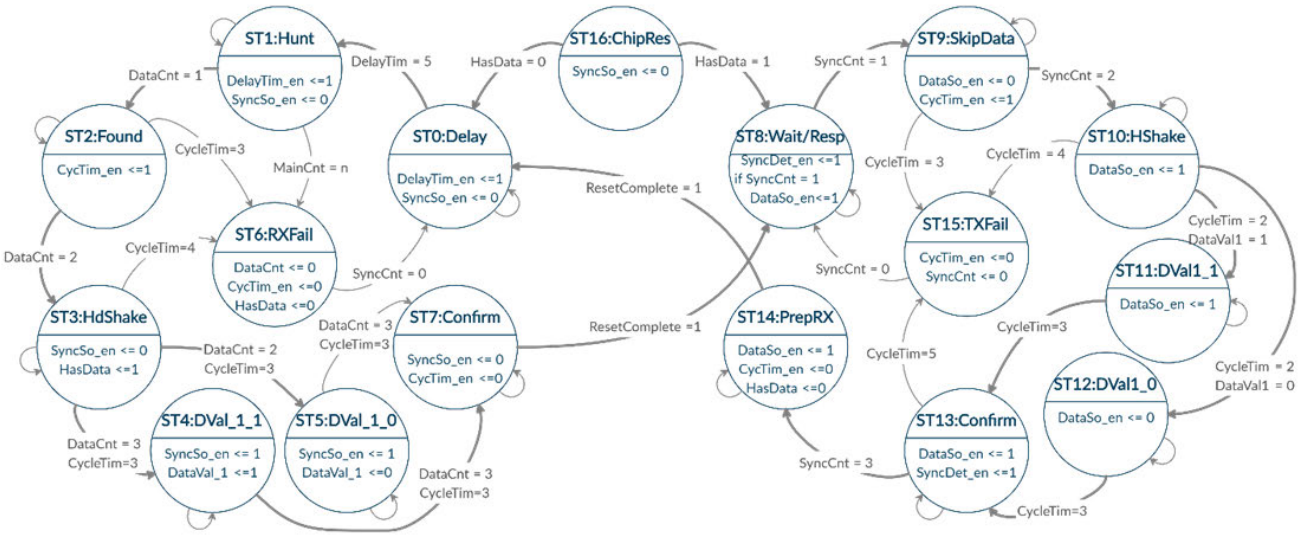

FIGURE 2. Simplified state machine diagram for MicroSTARLING processor. See text for description.

circuit. This allows us to test the digital circuit, our primary focus, without analog circuits. The on chip analog circuits are based on standard amplifier and clock designs that have not been optimized for power consumption or stability. The clock is a differential ring oscillator comprised of 7 differential delay stages and a bias control circuit [28]. The amplifiers are transimpedance amplifiers staged with a comparator. The nodes can be placed onto a surface or embedded into a material. The network is formed based on the preset transmission timeslots of available nodes adjacent to a data free node looking for a transmitting partner. The details of the processor function are found in the state machine diagram of Fig. 2.

B. DIGITAL PROCESSOR

1) COMMUNICATION STUCTURE

The MicroSTARLING nodes communicate with a form of the time division multiple access (TDMA) communication protocol. Unlike standard TDMA the time a given node has to communicate is not fixed. The smallest unit of communication is the *timeslot*, Fig. 1C. A node will use a masterclock to advance through each timeslot during the communication process. The nodes have several timeslots, 16 in this report, and a counter is used to cycle through these continuously. The group of 16 timeslots is thus referred to as a *cycle*. Each device has a timeslot within the cycle to send a single communication pulse. The node is readout using an unspecified number of cycles. The *node readout*, Fig. 1C, is the time it takes to readout an individual node. As many node readouts as possible will occur during the frame time. Ideally, a node readout is 4 + d cycles long, where d is the number of data bits. In this report the MicroSTARLING chip has 1 data bit and thus the ideal node readout is 5 cycles long. For several cases, including if the network is not initialized (i.e. nodes have not found partners) the time for a node to be read out can be significantly longer than the ideal (see Fig. 6). The entire array of nodes is readout as a *network frame* (Fig. 1C) analogous to a single image readout from a camera chip. The network frame time limit is controlled by a frame counter limit for each node in the array and is set to 3900 masterclocks in the fabricated MicroSTARLING chips. It is possible for the FrameCounter to stop readout before an entire array is readout if communication errors occur.

2) STATE MACHINE SUMMARY

The processor was developed in the hardware descriptive language Verilog from a state machine description. The state machine is diagramed in Fig. 2. Each of the 17 states can be classified as either a reset state or one of two modes of operation: transmit or receive. Several registers: HasData, DataValue and counters: CycleTimer, MainCounter, DataCounter, SyncCounter and DelayTimer are used to control the decision to move between states. The receive mode on the left of Fig. 2 has 8 states and begins when the processor registers that it is without data (HasData = 0) or the processor is reset (Reset = 1). In receive mode the processor sends pulse signals termed sync pulses and counts received data pulses (DataCounter). Receive mode states work to identify a transmitting partner and receive data from the partner. Once identified, the processor retains the successful receiving timeslot for future communications. The receive mode states handle errors from extraneous pulses, missing data pulses and timeouts by entering a receive failure state (State 6) which clears state registers, increments the receive timeslot and retries communication. The 8 transmit mode states, right of Fig. 2, work to transmit data held in the processor register. In transmit mode the processor sends data signals termed data pulses and counts sync pulses (SyncCounter). The processor has a preset transmission timeslot which, unlike the receive timeslot, is fixed. The transmit mode states handle errors from extraneous pulses, missing sync pulses and timeouts by

entering a transmit failure state (State 15) which clears state registers and retries communication.

3) STATE MACHINE DETAILS

For an array of nodes which are not yet networked, each node must obtain a transmit partner and a receive partner. A node without data in state 1 or ST1, Hunt, is hunting for a partner at a starting receive timeslot. Hunting consists of sending sync flashes at timeslots which decrement after each failed communication attempt. The node sends sync pulses by setting SyncSourceEnable to 1. The potential partner transmit node is waiting in ST8, Wait and Respond, to detect a pulse on its preset transmit timeslot. If the transmit node detects a sync flash it will count it by incrementing the register SyncCounter, send the first data pulse by setting the DataSourceEnable to 1 to flash the data pulse and move to ST9, Skip Data, where it advances the cycletime but withholds a data flash until the next cycle. The receive node detects the first data pulse, counts it by incrementing DataCounter and moves to ST2, found device, where it sends a second sync pulse as part of the handshake portion of a node readout. If the transmit (TX) node, in ST9, counts a second sync pulse it moves to ST10, TX Handshake End, and sends a second data pulse. This second data pulse causes the receive (RX) node to move to ST3, RX Handshake End, and changes the HasData register to 1 since the receive node now has data and is waiting for further communication to determine the data value.

The transmit node will now send the data value of either 1 via ST11, DataValue11 or 0 via ST12, DataValue10. If the receive node counts a data pulse in the next timeslot cycle it will move to ST4, DataValue_11, and set the DataValue_1 register to 1. If it does not receive a data pulse it will move to ST5, DataValue_10 and set the DataValue_1 register to 0. As fabricated in this report, there is only 1 bit of data. Additional data bits would result in additional transmit and receive DataValue states such as DataValue_20, DataValue_21, DataValue_30, DataValue_31 etc. The transmit node moves from a DataValue state to ST7, confirmation send, sends a confirming sync pulse to acknowledge it has received the data with no errors, clears registers and moves to ST8 as a newly transmitting node. Meanwhile, the transmit node waits in ST13, RX Confirmation, until it receives the confirmation sync pulse. The transmit node then moves to ST14, Preparation for Receive, clears registers and moves to ST0, Delay. In ST0 the newly receiving node delays moving to ST1, Hunt, for a preset number of cycles to avoid receiving its own data from the newly transmitting node.

4) CODE SIMULATION

The processor code was simulated in ModelSim (Mentor-Graphics, Inc). Fig. 3 shows the digital timing diagram for two simulated chips communicating data. The signal traces follow the behavior detailed above in the state machine description. In Fig. 3 there are four notable events during the node readout. The first event is hunting. Node 1 varies the timeslot for the SyncSourceSwitch (SSS) as it hunts

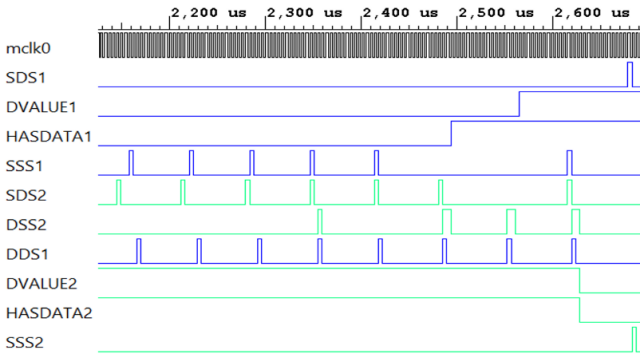

FIGURE 3. Vivado™ digital timing diagram for two simulated processors communicating. Chip 1 is the receive mode chip shown with blue traces. Chip 2 is the transmit mode chip shown with green traces. The traces identify internal registers (DataValue, HasData), output source switch values (SSS, DSS) and detector TIA switches (SDS, DDS). When the sync source switch, SSS1, aligns with the sync detector, SDS2, communication begins. Data source and sync source signals are active as designed in the state machine description.

for a transmitting partner. Only when SSS1 matches the SyncDetectorSwitch timeslot of node 2 does the data communication start. The DataSourceSwitch (DSS) of node 2 initiates communication at 2360μs. SSS1 responds by retaining the found timeslot and signaling a response flash during the next cycle at 2410μs. The second event is a handshake. The handshake is comprised of the transmitting node sending a data pulse and the receiving node responding in the next cycle. As part of the handshake the receiving node must not detect a data pulse during the second cycle of the node readout. The third event is the data transmission. During the third and fourth cycles the sync pulses are off, and one or two data pulses occur. The first data pulse sets the HasData1 register to 1 within the receiving node. The second data pulse sets the DataValue1 register to 1. If the second data pulse were not sent the DataValue1 register would be set to 0.

The final event is the confirmation of data received via the final SSS1 pulse and confirmation received via the responding final DSS2 pulse. After the confirmation of data received, the transmit node changes to a receiving node as evidenced by the node 2 SSS2 pulse at 2685μs. Likewise, node 1 changes to transmit mode observed as the initial SDS1 pulse at 2680μs. Not shown in Fig. 3 is that for subsequent data communications between nodes 1 and 2, node 1 will not hunt for a partner timeslot. Rather, it will continue to send its sync pulse, SSS1, at the successful timeslot of node 2 until no data is received for a configurable number of masterclocks.

C. MATERIALS AND METHODS

The MicroSTARLING analog and digital components were designed and fabricated in 180nm low voltage CMOS technology. The chip layout and die micrograph are presented in Fig. 4. The total chip size is 1250μm $\times$ 1250μm. The chips were packaged in 40 pin chip carriers for testing in breadboards. Digital timing diagrams from fabricated chips were recorded with a Digital Discovery logic analyzer and function generator (Digilent Inc., Pullman, WA). The same

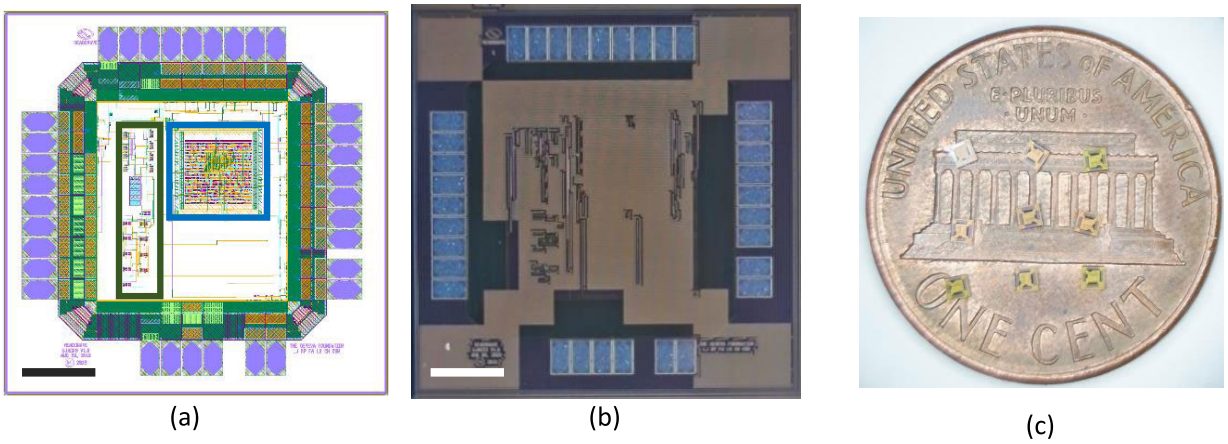

FIGURE 4. The MicroSTARLING chip as a layout (a), as fabricated in 180nm CMOS (b) and as a chip array on a US penny for scale (c). The Scale bars in a and b are 200 microns. The active area analog components (green box) cover an area 100 μm × 450 μm and the active area of the digital processor (blue box) covers 250 μm × 250 μm.

unit provided chip power, LED control and the chip clock. The analog voltage traces were recorded with an Analog Discovery 2 oscilloscope and power supply (Digilent Inc., Pullman WA). A fully wireless node was powered via a 3.2V, 1A, 940nm, Luxeon IR (Lumileds Inc., San Jose, CA) energy harvesting LED, which was illuminated with a M940D2 board mounted 940nm LED and LEDD1B LED driver (all Thorlabs, Newton, NJ). LEDs for communication between wireless data nodes were 2.2V, 20mA, 605nm, 30° Field of View, WP710A10SEC/J4 LEDs (Kingbright, Taiwan). The wireless data and power node used bare die chip LEDs for communication. The source LEDs were 215μm chips, 625nm, LAUR09HP1 and the detector LEDs were 270μm, 659nm LADR11HP1 (Light Avenue, Germany).

We assembled three different nodes to measure the device performance. Each node was arrayed to create three testbenches to examine data rates and device component function. The first node was fully wired to allow evaluation of the MicroSTARLING processor without regard for the function of on-chip analog components. Fig. 5a presents a schematic of the wired circuit. The central symbol in the schematic is the MicroSTARLING chip with corresponding pinout, see Fig. 5 for acronyms used in this section. The six key connections are: the external clock, main counter trigger input, nominal 2.5V power, ground, data source switch output, sync source switch output, data input and sync input. The three inputs are directly connected to the digital processor (DPDDI, SPDDI, MCTDI, see Fig. 5 acronyms) and not connected to the corresponding analog amplifiers. Of note are the two diodes (D7, D8) added to prevent any damage to the sync and data source switch outputs from external sources. The external clock for the wired circuit can be a common clock directly wired to inputs of adjacent nodes. We used a pulse signal from the Digilent Digital Discovery function generator for all data except the power requirements characterization. There we used a MEMS-based oscillator, SiT8021, from SiTime, Inc.

It is possible to connect a given output, such as sync source output to a common wire that connects to the inputs and outputs of adjacent nodes. This we term a pooled connection and can evaluate the ability of nodes to select amongst potential nodes. The sensor digital input is left floating or connected to a power voltage to simulate data value.

The second node is a partially wireless node designed to test the analog transimpedance amplifier and comparator. 7 of these nodes were connected in an array with an additional wired base node for readout. The power, ground and main counter trigger remain wired. The data and sync outputs are connected to LED D2 and LED D4, respectively, to send optical flashes to an adjacent node. To detect these flashes, the data and sync inputs (DPDDI, SPDDI) are now connected to the corresponding amplifier outputs DPDAO and SPDAO, see Fig. 5 acronyms. The inputs to those amplifiers (SPDAI, DPDAI) are LEDs connected across the transimpedance amplifier input terminals. Resistors R1 and R2 are connected in parallel as current shunts to discharge capacitive charge built up on the LEDs. The voltage bias, VBS, terminal of the amplifier is voltage biased via the R3, R5 voltage divider. Finally, a photodiode biased to the power supply voltage is connected to the sensor digital input to be sampled by the digital processor as the data value.

The third node is fully wireless, (Fig. 5c) and was used to interface to two wireless data nodes (Fig. 5b) creating a three-node testbench array. The fully wireless node was used to test the internal clock, wireless power, and wireless main counter trigger. On the chip, the MainCounterTrigger amplifier amplifies the internal clock to a voltage usable by the digital processor. A frequency tuning capacitor is used to connect the MainCounterTrigger analog output (MCTAO) to the digital clock input pin. The power voltage and ground are replaced with a 1A, 940nm LED which is powered with an external 940nm LED. The external 940nm LED is pulsed to 0V periodically to send a MainCounter alignment trigger. The processor resets the masterclock signal to the trigger edge.

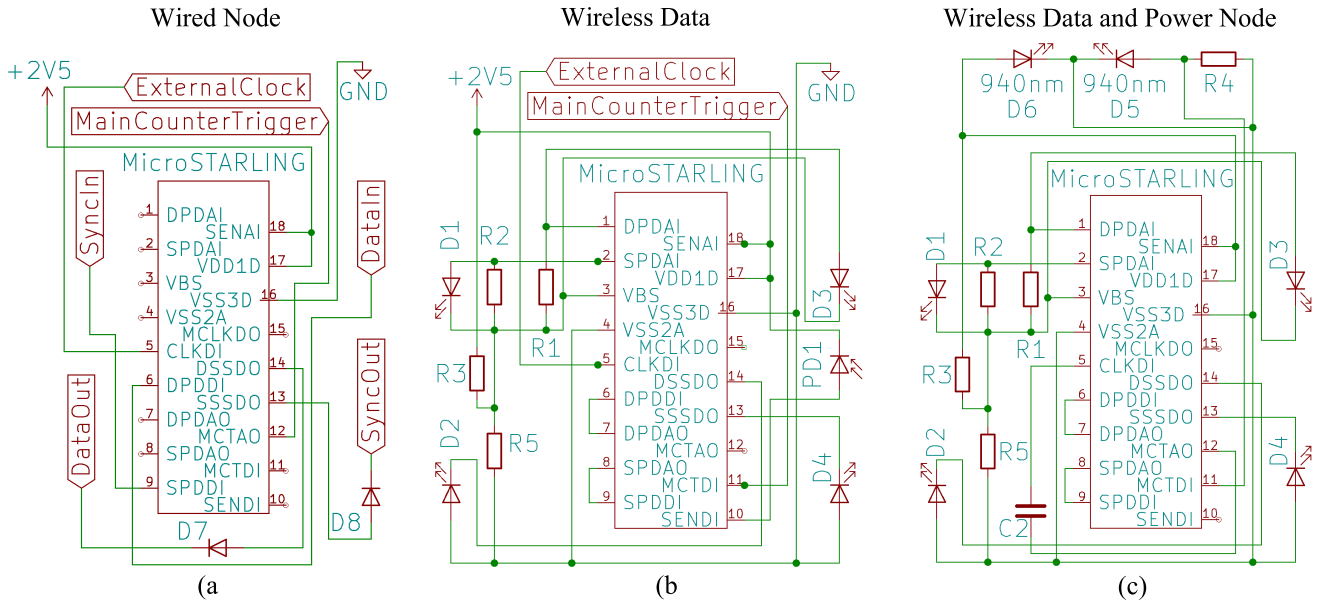

FIGURE 5. MicroSTARLING nodes in the three testbench formats used to evaluate the components of the system. The first (a) is a wired version with wired connections to for communication between nodes, power supply, clock source and MainCounter trigger. The second testbench node (b) uses the on-chip amplifiers and LEDs to allow for wireless data communication and wired connections otherwise. The last testbench circuit (c) details connections for a wireless node using two 940nm LEDs for power and a synchronization trigger and 604nm LEDs for data communication. This testbench uses the on-chip clock. The circuit symbol for the MicroSTARLING only shows the 18 pins used for these testbenches. The chip pin labels are abbreviated as follows: DPDAI-data photodiode analog in, SPDAI-sync photodiode analog in, VBS- voltage bias, CLKDI-clock digital in, DPDDI-data photodiode digital in, DPDAO-data photodiode analog out, SPDAO-sync photodiode analog out, SPDDI-sync photodiode digital in, SENAI-sensor analog out, VDD1D-digital source input, VSS3D-digital ground input, MCLKDO-masterclock digital output, DSSDO-DataSourceSwitch digital output, SSSDO-SyncSourceSwitch digital output, MCTAO-maincounter trigger analog input, MCTDI-maincounter trigger digital input and SENDI- sensor digital input.

This aligns each chips masterclock pulses. This testbench node uses D3-D2 and D1-D4 pairs of the bare die LEDs wire bonded to a DIP package for the communication with the base node and dual 604nm, 3mm dome LEDs to communicate with the upstream node to form a three-node array. The sensor digital input is left floating or connected to power voltage to create the data value.

IV. EVALUATION RESULTS

A. WIRED PROCESSOR TESTING

1) DATA READOUT

The wired node presented in Fig. 5a is used in a network of 8 nodes. The first node (node 0) is the base node. The external clock is 25MHz. The processor clock divides the input clock to create the masterclock. The hunting phase, green box, is seen in Fig. 6a. The sync source switch (SSS0) timeslot is reduced each cycle (16 masterclocks) until it matches the timeslot of the sync detector switch (SDS1) of node 1. It remains at this timeslot, as seen in the match between SSS0 and SDS1, for future pulses (Fig. 6a). The handshake event occurs (blue oval, Fig. 6a) as described in the state machine description detailed in the previous section. Of note is the change in pulse duration of the last 3 data pulses compared to the first data pulse. Normal data and sync pulses are 1 masterclock (1.68μs at 525.2KHz). The longer 2 masterclock pulses are to improve data pulse detection by node 0. The data value (green arrow, Fig. 6a) is 1 for this data transfer. The last confirming data pulse (red arrow, Fig. 6a) ends the transfer and node 1 sets the DataValue1 and HasData1 registers to 0. Node 1 changes from data transmit mode to data receive mode. The base readout node, node 0, is designed to auto reset to receive mode without transferring its data after data collection, HasData0 changes from 1 to 0. Notice that the base node DataValue0 register remains at the last set value, 1 in the case presented in Fig. 6a.

The data communication for three chips is shown in Fig. 6b. The data registers of the base, node 0, and the data and sync source outputs are shown for nodes 1 and 2. The data value at each transfer is seen in the 4th cycle (green arrow, Fig. 6b). The data value of 1 from node 1 is first sent to node 0 freeing node 1 to pass another bit of data, the data value of 0 from chip 2, to chip 1. In this case, unlike Fig. 6a, there is no SSS hunting period. The data transfer is immediate as the nodes have previously found transmitting partners. The input clock is divided 42:1 to create the 592.5KHz masterclock (MCLK, Fig. 6a). The MicroSTARLING chip functions in the same manner as the Verilog simulation.

The effect of the hunting period can be seen to a greater extent in Fig. 6c, where the initial readout of the 8-node array from 0 to 5.4ms has several periods of hunting and is stopped by the framereset timer before the last data bit from node 7 is finished being readout (red arrow, Fig. 6c). The data from node 7 (red circle) gets as far as node 5 at 5.4ms, DSS5. The second readout has only one hunting period from SSS3 and takes 1.8ms to readout all 7 non-base nodes versus the over 5.4ms of the initial readout. Once the nodes have all found partners the wired array is readout without error consistently, Fig. 6d.

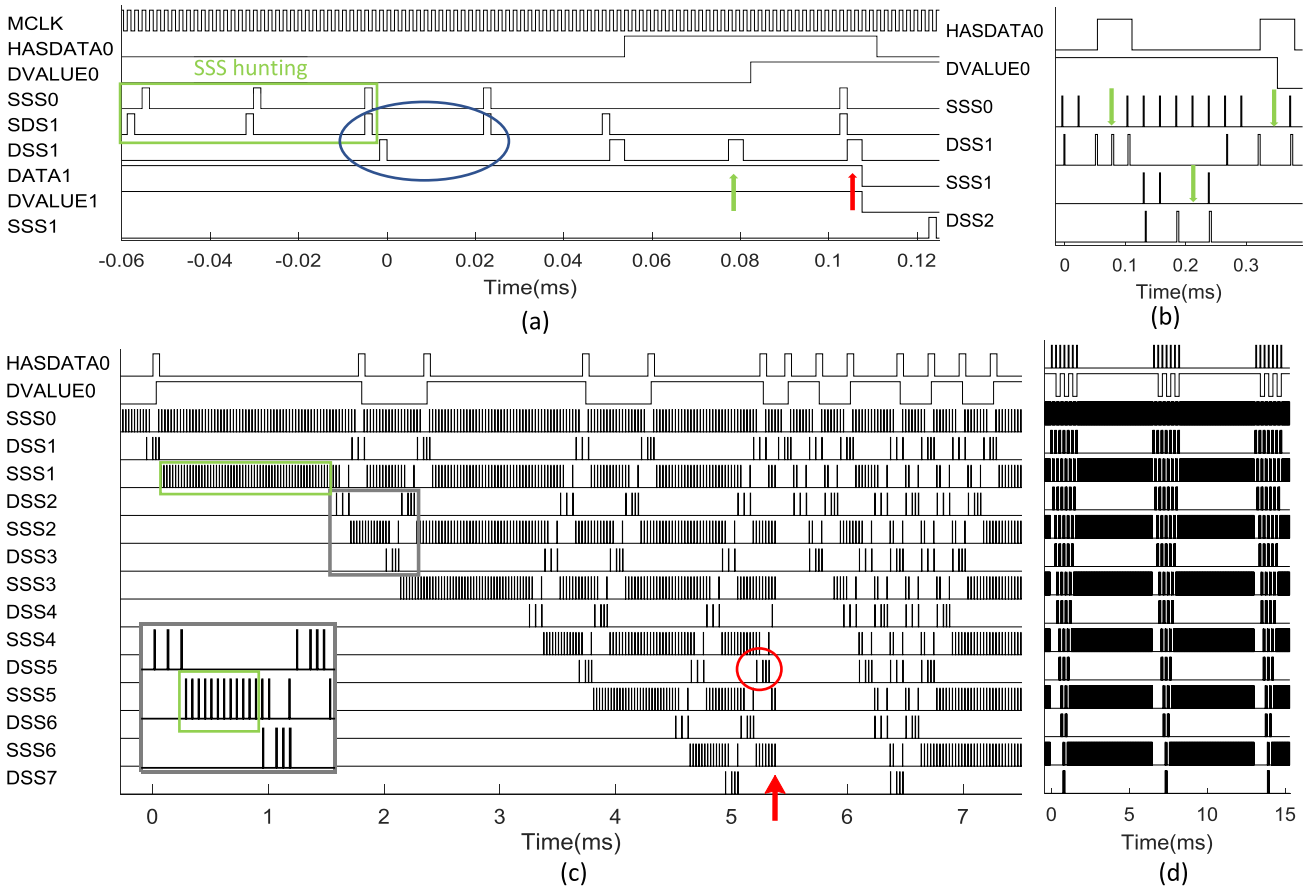

FIGURE 6. Digital communications processor functions at up to 155Hz framerate with an external 25MHz clock. A single data communication is shown in (a). The sync source (SSS0) timeslot change can be seen in the green box. The blue oval indicates the successful handshake between nodes. The green and red arrows indicate the data value and confirmation signals from the data source switch (DSS1). The node 1 requires 5 cycles (134.4μs) to transfer its data to node 1. (b) Nodes 0, 1 and 2 transfer data in numerical order. For the first transfer the data from the sensor of node 1 has a value of is 1 as indicated by the pulse at the 4th cycle of the transfer (green arrow). The second transfer, of node 2's sensor data, has a value of 0 as evidenced by the lack of a pulse at the middle green arrow. The third transfer is also of node 2's sensor data and has the same 0 value as the second transfer (last green arrow). (c) Full readout of the 8-node array. Inset shows a 3-chip readout similar (b). The initial frame readout ends prematurely at 5.4ms due to the many hunting phases (green boxes). The red arrow indicates the framereset moment and the red circle shows the last full data transfer on DSS5. The next full frame readout takes only 1.8ms and all 7 nodes are readout. (d) Three frame readouts with frame reset period of 6.6ms. No readout errors occur.

The processor itself requires only 10μA of current at 1.2 volts (12μW). Additional power is drawn by any clock used and we have demonstrated function with a low power 524KHz clock source which draws only 20μW at 1.2V. The total draw for an always on device is 32μW using wired or conductive gel communication. This power was provided by a standard 3mm, 30mA, 536nm LED at a distance of 8mm from an energy harvesting LED. Separately, we generated 60μA from a 340μm $\times$ 340μm bare die LED chip (Light Avenue, LANI14HP1), suggesting that a small package of a few mm^2 is possible if several chip LEDs are used for energy harvesting.

2) SELF-ORGANIZING DECISION PROCESS

The design concept of the MicroSTARLING chips assumes that in a dense array of nodes the processor will need to handle optical inputs from more than one potential partner node and select between them. The added density will likely reduce performance unless the processor can handle multiple inputs or collisions. To evaluate the efficacy of the self-directed network organization in a non-optical, or a wired network, several inputs and outputs are connected to a single wire. Multiple outputs connected can cause damage if one is grounded and the others held high for the case of push-pull drivers. Our design is optically based and thus uses push-pull output circuits. For this report, we utilize diodes which prevent low/ground outputs from one source from shorting another output with a high value. The wired array shown in Fig. 5a has 2 diodes (D7, D8) which only allow current to flow away from an output source preventing sinking of current. These wired nodes were formed into small networks (Fig. 7b) that included both directly paired nodes and nodes which interact in a "pool". In a pool of nodes each node in the pool has sync and data detectors and sources wired together.

Unlike the directly wired nodes of Fig. 6 where each node has only one possible transmitting partner and one possible receiving partner, this arrangement requires a node to decide which node to connect to. The decision is mainly based on

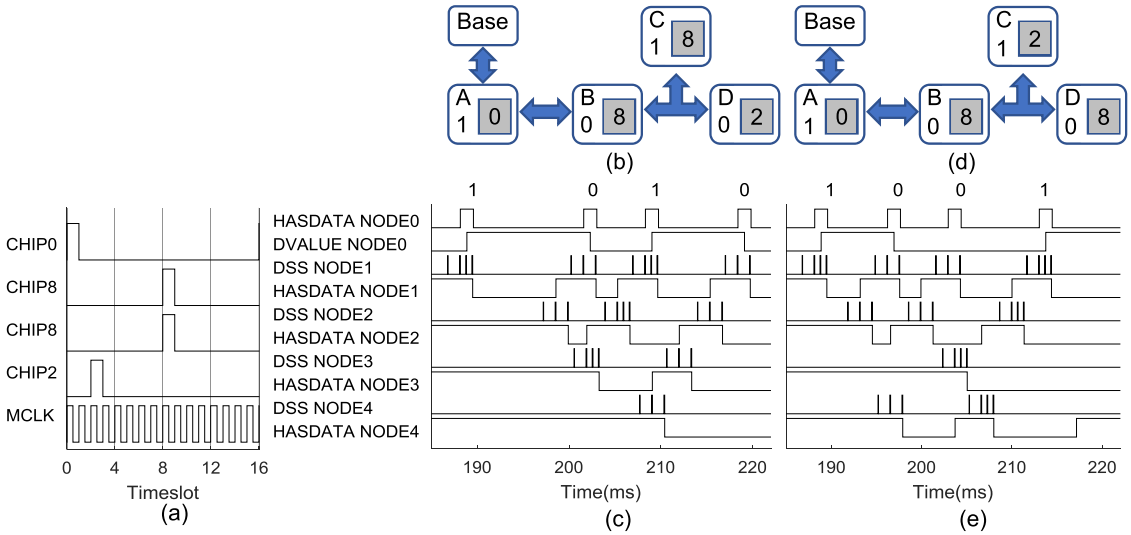

FIGURE 7. Self-organizing network decisions are based on chip IDs of potential partner nodes. (a) The sync detector traces from 4 chips used in this experiment with chip IDs as indicated on the y axis. There are 16 possible IDs for the chips fabricated and the ID determines on which of the cycle timeslots the chip detects sync pulses and transmits data pulses (TX). Also shown in (b) and (d) are the two 5 node networks tested. In both networks, the base node and nodes A and B are linked in series while nodes B, C and D are in a fully connected pool. In a pool, each node can partner with the others. The digital scope traces in (c) show the tested network of (b) formed a path in the order: base, A, B, C, D and the traces in (d) show the tested network formed a path in the order: base, A, B, D, C. In the (b), node B selects node C to pair with since node C contains a chip with a TX timeslot of 8 and node D contains a chip with a TX timeslot of 2. In the test network (d), the chips were physically swapped. Now node B selects node D to pair with since node D contains a chip with a TX timeslot of 8 and node C contains a chip with a TX timeslot of 2. See previous Figs. for details on voltage trace interpretation.

the timeslot of the transmitting node. The transmit timeslot of each node is fixed. The receive timeslot is changed after each unsuccessful attempt during hunting. The receiving node's timeslot cycles from the highest numbered timeslot to the lowest. When a chip processor is in transmit mode, the processor waits for a pulse to be detected by the sync detector which is on for only one timeslot during the cycle of timeslots, Fig. 1c. Fig. 7a shows the sync detector timeslot of each processor chip used to form the array in Fig.7. Two chips have the same timeslot of 8 and the others have timeslots 0 and 1. The effect of the sync detector timeslot is seen in the timing diagrams of Fig. 7c and 7e. The timing diagrams shows the data registers of node 0, the base node. Also shown are the data source switch output pulses and the data presence register, HasData, for each of the other 4 nodes.

In the first array nodes A, B, C and D have chips with timeslots 0, 8, 8 and 2, respectively. The timing diagram in Fig.7c shows that data is first read from node A, then node B, then node C and lastly node D. For example, the data value of 0 passes from node D to node C to node B to node A. The DataValue register of node 0 indicates the data value from each readout node and can be seen to cycle through values in a chain of 1 0 1 0. The order of node readout was the result of the chip sync detector timeslot of the pooled nodes. Node B transmits its data to node A since node A is the first node emptied of data and in receive mode. This results in node B looking for a transmitting partner. It has a connection via a common wire to node C and node D. As node B changes its sync source timeslot from 15 down to 0, the first node it affects is node C since node C has a chip with a transmit timeslot of 8 whereas node D has a transmit timeslot of 2. After sending its data to node B, node C looks for a partner with data. Node B and D both have data at time 203ms (red arrow, Fig. 7c) and are potential transmit partners for node C. However, node C has a delay (Fig. 2, state 0/delay) before it hunts for a partner, which prevents it from receiving data from node B before it transmits the data to node A. Thus, when it is ready to hunt for a partner, node C only finds node D with data and partners with node D to readout the last data value.

In the second array, we swapped the chips between nodes C and D, while keeping all the connections and data values the same. Now when node B looks for a transmit partner it connects with node D as node D has a higher numbered transmit timeslot than node C. This is observed in Fig. 7e where node D sends data and node B is the next node to transmit in the timing diagram at 200ms. Later at 203ms, node C transmits a data value of 1 which is seen to be transmitted by node D then nodes B and A. The node readout order is now A, B, D, C. The order of readout is also observed in the change in the register DataValue readout chain from the previous 1 0 1 0 (Fig. 7c) to 1 0 0 1 (Fig. 7e).

B. WIRELESS COMMUNICATION TESTING

1) TRANSIMPEDANCE AMPLIFIER FUNCTION

Having presented the chip processor function without potential limitations of the on-chip amplifiers, we present in this section the ability of the MicroSTARLING processor to communicate wirelessly. This section covers the as fabricated Physical Layer of the network nodes. Wireless optical communication can introduce errors due to time delay and gain of the analog circuits. Fig. 8 presents data

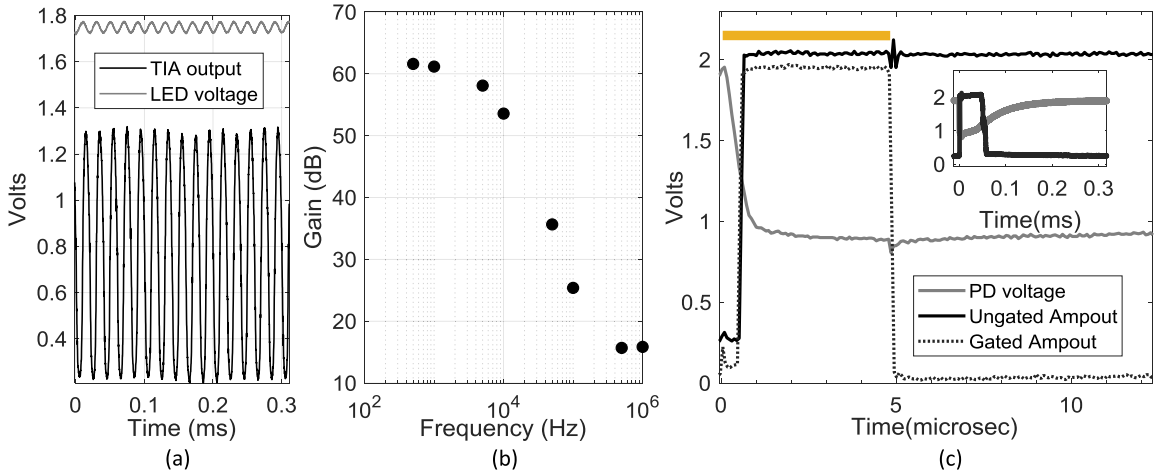

FIGURE 8. The analog transimpedance amplifier (TIA) provides amplification of sinewaves as observed in (a). The TIA functions above unity gain for up to 100KHz sinewaves (b). The amplifier is designed to pair with a comparator to respond to pulse inputs. In (c) a 605nm, 20mW LED across the TIA inputs, creates a response with a rise time of 500ns for photodiode detection of 605nm 20mW LED source flash at 1mm distance.

characterizing frequency response and pulse response of the transimpedance (TIA) amplifier and comparator circuit. A 605nm LED is driven with a 50KHz sinewave. 1 mm distant a second 605nm LED (D1, Fig. 2b) is placed across the data photodiode analog input and voltage bias input of a transimpedance amplifier (DPDAI and VBS, Fig. 2b). A small voltage can be detected across the LED D1 and is plotted in Fig. 8a as an LED voltage. The bias voltage creates a non-zero voltage baseline. The current generated results in the TIA output voltage of Fig. 8a. Fig. 8b shows the gain in dB for frequencies ranging from 500Hz to 1MHz. The node design is for pulsed data and sync signals. We applied a test pulse of 5μs duration and were able to obtain a functional response from the amplifier.

Fig. 8c details the function and limitations of the amplifier circuit. The LED pulse was for the duration indicated by the yellow bar. The voltage across the detecting LED, acting as a photodiode (PD), is shown in gray. The diode cathode voltage falls relative to the anode/bias terminal. The signal fall time is $\sim$1μs. The TIA/Comparator circuit results in an output pulse with a $<$140ns rise time, solid black line, and an effective delay of 600ns from the LED on time and the output pulse leading edge. The fast rise is due to the comparator which follows the TIA on-chip. The delay is due to the time it takes the TIA output to cross the comparator threshold. The LED has an inherent capacitance that prevents a rapid decay of the pulse. The amplifier output continues past the end of the LED flash and inset plot shows that the total TIA/Comparator output pulse is expanded to 50μs from the original 5μs flash. The PD voltage does not settle to baseline until 300μs. Fig. 8c also indicates the gating turn on response of the amplifier. When gated with the data detector switch, the amplifier turns on at time 0 and off at time 5μs with sub-200ns switching (dotted line, Fig. 8c). The amplifier delay (500ns) and frequency response suggest a limit of a 100KHz, 5μs masterclock for the on-chip amplifier. The 42:1 clock divider would indicate a maximum 4.2MHz input clock. This is less than the 25MHz input clock that successfully operated the array of 8 wired devices in Fig. 6. We selected a 4MHz input clock for the evaluation of the wireless optical testbench.

2) OPTICAL COMMUNICATION RESULTS

Seven wireless communications nodes as in Fig. 5b are assembled into an array seen in Fig. 9. Node 1 is the base readout node. The nodes are described in the Materials and Methods section above. A 4Mhz clock and 2.5V power supply drive the arrayed nodes. The MainCounter trigger was wired to each breadboard node to align the masterclock edges. 610nm LEDs were connected to the inputs of the gated data and sync amplifiers. Additional 605nm LEDs were used to send data and sync light pulses. The image of the array of nodes shows the linear arrangement between nodes. The spacing between the LEDs of each node varied between 2mm and 50mm. MicroSTARLING chips are mounted in the 40 pin chip carriers. Fig. 9a shows the timing diagram for the array with the data registers HasData1 and DataValue1 shown for node 1. The LED drivers (SSSn, DSSn) are shown for each node. As in previous Figs. the inverted triangle pattern of data transfers shows 5 stable, full frame readouts with a 4MHz input clock. For the 4MHz input clock, the time to readout a frame of data from all 7 devices is 11ms and the time between full frame readouts is 41ms. The framerate is nominally 24 frames per second. The addition of light communication did not prevent stable data transmission. However, the maximum stable input clock frequency with the ad-hoc on-chip amplifiers was 5 MHz versus the 25MHz of the wired communication nodes (data not shown). Of note are the 3 data values of 1 that where readout each frame. They represent the stable readout of data without any errors or dropped frames. In Fig. 9a, the sensor digital inputs were wired to the positive voltage for nodes 1, 3 and 7. However, in Fig. 9b the sensor inputs of nodes 2 through 6 were connected to photodiodes biased to the positive power supply, 2.5V. A flashlight was directed at the photodiode of node 5

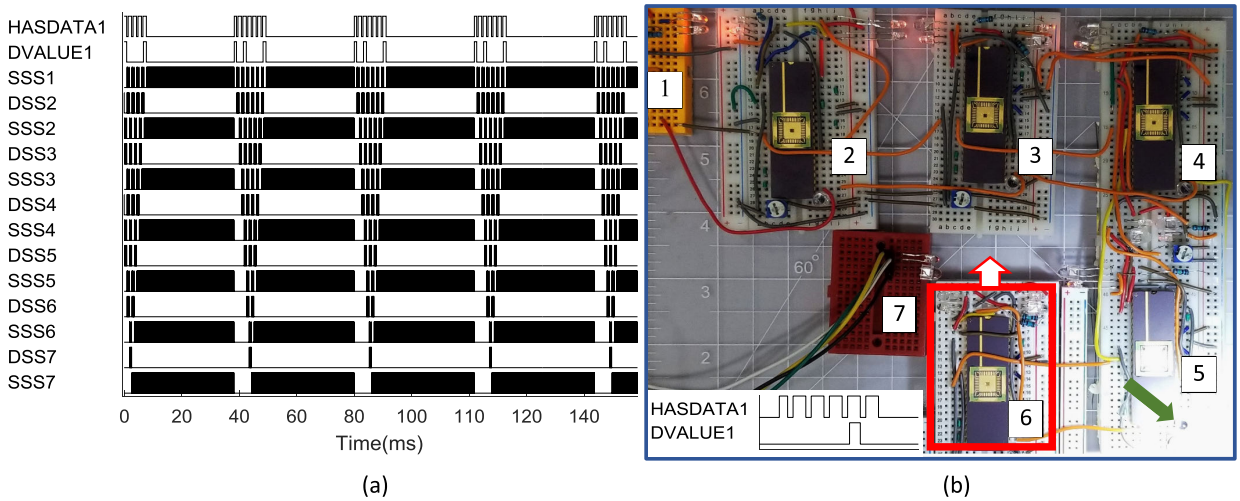

FIGURE 9. Sensor readout with optical communication using on chip transimpedance amplifiers with LEDs and photodiodes. (a) The timing diagram of a 7 node array with a 4MHz input clock and readout of static data values of 1 on nodes 1, 3 and 7. The actual breadboard nodes are shown in (b) with the 6th node (red box) pulled out of the array. The photodiode sensor of node 5 (green arrow) is illuminated and results in a readout of DataValue1 = 1 in the inset timing diagram.

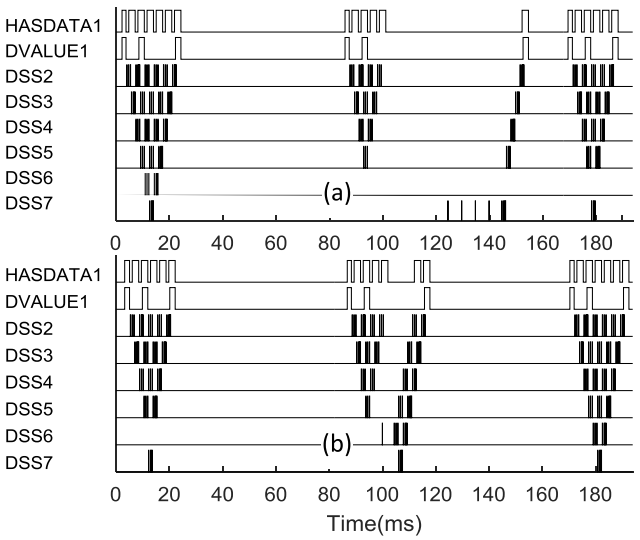

FIGURE 10. Removal and insertion of a node results in self organized network repair in less than 180ms, representing 2 readout frames for a 2MHz input clock.

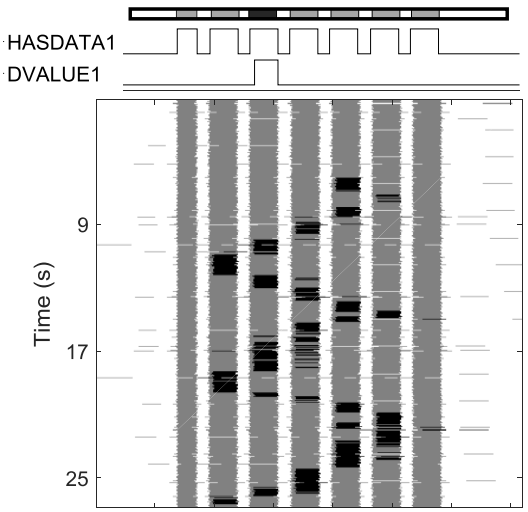

FIGURE 11. Image of a 25 second readout of an array with 5 photo sensing nodes (2-6), optically communicating, while presented with a moving spot of light. At the top, the timing diagram from one frame is shown indicating the data status (HasData1) and data value (DataValue1) for each node. The bars above the traces relate the three shades used in the image to indicate trace voltages. White is both traces off; gray is HasData on and DataValue off; and black is Hasdata on and DataValue on. The optical sensor controls the data value for each node. In the image the y axis is time in seconds and the x axis is the time during a single frame readout in arbitrary units. The meandering black pixels indicate the motion of the light as it is manually scanned across the node photosensors.

(green arrow) and resulted in a DataValue of 1 aligned with the fifth HasData pulse (Fig. 9b, inset timing diagram).

A central use case for the MicroSTARLING arrays is a miniature embedded network in flexible materials such as polymer sheets in surgical simulators or bioprinted corneas [29]. For example, sufficiently small versions could track damage in a flexible material by monitoring the change in the network readout path. The use of optically communicating nodes makes it possible to insert and remove nodes to evaluate the timing of the formation and repair of the self-organized network. In Fig. 9b the red box identifies node 6 which is withdrawn from the network resulting in only 6 HASADATA1 readout pulses for the nodes 1, 2, 3, 4, 5 and 7. If node 6 is inserted between the nodes 5 and 7 with the LEDs aligned, a new network may be formed with all 7 nodes and 7 HasData1 pulses.

Fig. 10b shows the effect of such an insertion procedure for an input clock of 2MHz. The first readout frame in the timing diagram has 6 HasData1 pulses and node 6 is not sending data on DSS6. When node 6 is inserted between nodes 5 and 7, the second readout frame is disrupted as node 6 attempts to send data to node 5 (single pulse at 100ms). After a few milliseconds nodes 5 and 6 form a new partnership and node 6 readily receives data from node 7 (node readout at 108ms). In the third frame readout all 7 nodes are stably readout. The time to repair the network is less than 80ms, the duration between the last stable readout and

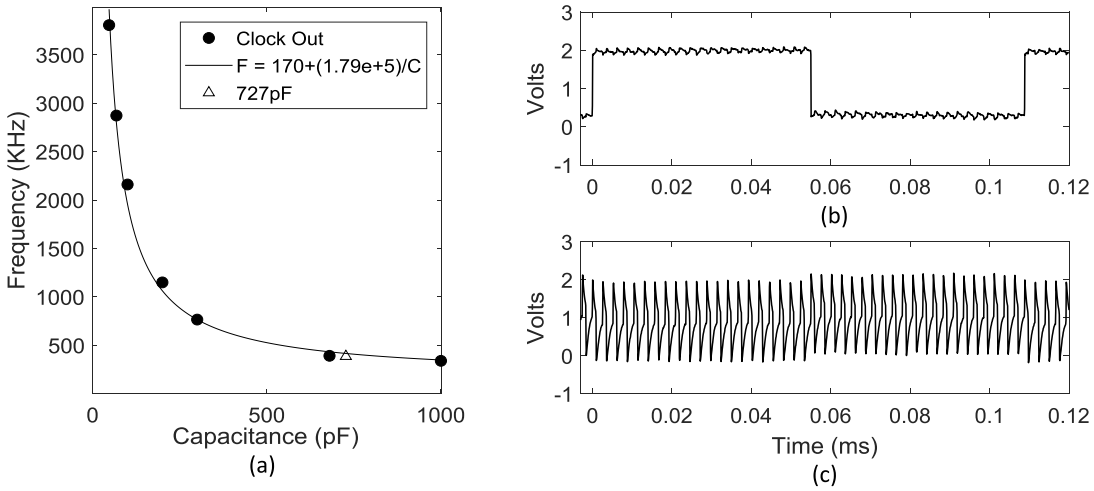

FIGURE 12. The on-chip ring oscillator clock output is controlled via the input capacitor (a). The clock frequency increases for lower capacitance values from 400Hz to 3.8MHz. The triangle (a) indicates the 420Hz frequency for a 727pF capacitor and the 420Hz clock signal is shown in (c). Data in (b) presents the resulting clock divided masterclock signal.

the reformed readout of node 7. Fig. 10a presents network repair after node removal. In this case there are 4 attempts at data transmission by node 7 (124ms – 140ms) before a successful transmission to node 5. The maximum repair time in this example is 140ms. The third frame readout is stable with 6 nodes.

The key function of a wireless sensor network is to readout data from the environment. For a mesh network, multihop readout leverages the energy savings of short distance data transmission. The array presented in this report offers an opportunity to readout real-time data from a multihop optical sensor network. We passed a flashlight over the node photodiodes in the array and recorded the output from the readout node only for 100 seconds. The timing diagram data for HasData1 and DataValue1 were reshaped into a matrix with each row holding a full array frame readout. The input clock is 4MHz and there are 2431 potential frames in the matrix. An image of the first 26s of a data collection is shown in Fig. 11. The time between frames is approximately 41ms. The DataValues of 1 resulting from light exposure during the flashlight sweep are shown as black pixels. The gray pixels show the presence of DataValues of 0.

The readout performance of this array can be assessed in part by examining the throughput. The throughput is calculated from the 100s run of the 7-node array with a 4MHz clock. The errors are taken as any readout signals on the HasData1 output trace that occur outside of the expected window of each frame. In the 7-node, 4MHz clock case the expected time window is 12ms from the start of the 7 pulses on HasData trace the end. In Fig. 11 some of the errors are visible as gray lines outside of the expected window. There are also white lines within the gray expected window indicating the possibility of a complete failure of readout rather than a shifting of the readout. We also looked for such errors caused by a complete failure of any readout value on trace HasData and did not find any. In our representative run we found 175 shift errors for 2431 frames resulting in error rate of 0.072 errors per frame. We understand that evaluation of the physical layer is often aided by examining the bit error rate or BER. We and others [22] prefer to use throughput for analyzing performance of multi-hop networks. However, as it may aid in comparison, we present the BER as follows. The masterclock for the data in figure 11 is 95.2KHz. While a time shift of the data does not prevent correct data transmission it does result from an incorrect physical layer bit transferred. So each time shift can be viewed as an incorrect physical data bit (light pulse) transferred. The 100s of data captured results in 9.52×10^6 bits transfers per hop and the 7 devices require 6 hops yielding 5.7×10^7 bit transfers. The 175 shift errors suggest a BER of slightly better than 1×10^{-5}. This is consistent with the physical layer frequency response of limit of 100KHz described in section B1 above.

C. WIRELESS POWER AND COMMUNICATION TESTING

1) ON CHIP CLOCK GENERATOR

The function of the fully wireless node shown in Fig. 5c requires that each node provides its own clock. This can be from an external clock chip or the on-chip ad-hoc clock. In this section we characterize the basic output from the on-chip clock. Fig. 12 shows the range of frequencies that can be generated with the given capacitors. The capacitor is placed between the output source of the clock and the digital circuit input (Fig. 5c, C2). For higher capacitor values the frequency settles at 170Hz.

2) FULLY WIRELESS NODE TESTING

A fully wireless node, node 1, was placed between two wireless communication nodes, node 0 and node 2. For communication between node 0 and node 1 the LEDs used were bare die led chips (Fig. 13a). The LEDs between node 1 and node 2 are standard 3mm packaged LEDs. The bare die LEDs are less than 270μm in extent and used to evaluate the lower limits of node size. The devices (a-d) in Fig. 13 were used to

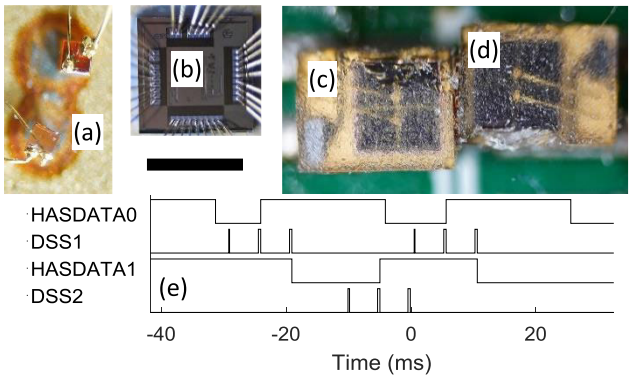

FIGURE 13. Devices used to create the fully wireless node. The communication chip LEDs with wire bonds (a), the MicroSTARLING chip (b), the energy harvesting LED (c) and main counter trigger LED (d) are shown at the same scale with a 1mm scale bar. The timing diagram (e) shows wireless transmission of data from node 2 to node 1 and then to node 0.

collect the data demonstrating wireless communication from node 2 to node 1 to node 0. The current drawn from the fully wireless device, node 1, was measured to be 1.5 mA at 2 volts during active communication between the three nodes, Fig. 13e. The power was provided by a single energy harvesting 1mm, 940nm LED (Fig. 13c, Fig. 5c, D4) that was exposed to a 940nm, 2W LED at 1mm distance. The previous nodes (Fig. 5a, 5b) had wired MainCounter trigger signals to align the masterclock edges of each node. For the fully wireless node in the MainCounter trigger signal was delivered via the wireless signal LED D5, Fig. 13d. The 2W power LED signal was dropped to 0W for 1 masterclock duration (90μs). This signal did not interrupt power harvested by LED D4 due to LED intrinsic capacitance. However, the drop to 0W does interrupt the signal detected in LED D5 since it is shorted with a resistor, R6 (Fig. 5c), to overcome the capacitance and reduce the time constant of the LED. The signal is applied to MainCounter trigger input of the digital processor as a trigger to align the masterclock edges of all nodes.

V. DISCUSSION AND CONCLUSION

In this report we present data detailing a low power, small area processor capable of controlling self-organized communication with partner nodes in a decentralized manner. The processor and clock can require as little as 32μW. The required power increases significantly when the ad-hoc analog components are used. Power consumption for the fully wireless node is 3mW. This is primarily due to our unrefined analog amplifier and clock circuits which consume higher power than even commercially available units such as the SiT8021 clock used for wired connections. In future devices, we would replace a current consuming voltage divider on the present MicroSTARLING chip and gate the sensor and MainCounter trigger amplifiers. This would reduce our current consumption from 1.5 mA to approximately 100uA.

The second goal was to develop a processor that occupies a small area when fabricated. We fabricated the processor with 180nm CMOS technology. This first version of the device has 33 bond pads, most of which are for diagnostics and data collection. Although the total chip area is 1.56mm^2, the active area of the processor is only 0.063 mm^2 and the active area of the analog components is only 0.045mm^2. Fabricating the same processor design in 45nm CMOS technology would further reduce the processor area to approximately 70μm $\times$ 70μm (0.0049mm^2).

TABLE 1. Comparison between the MicroSTARLING and other general classes of wireless networks. There are systems that cover more than one class. VLC—Visual light communication, RFWSN—Radio frequency wireless sensor network.

	MicroSTARLING	VLC	Smartdust	RFWSN
1mm scale	*		*	
<3mW	*		*	
Multihop ≥6	*			*
Self-Organizing	*	*		*
Optical	*	*	*	
>1m spacing		*	*	*
>2 Kbps		*	*	*

Comparing the MicroSTARLING type nodes to similar devices is challenging given our design goals of a miniature, embeddable, multihop, small data packet wireless network. Demonstrated versions of wireless sensor networks, visual light communication networks and smart dust nodes have been reviewed extensively. Table 1 distinguishes between the general classes of demonstrated wireless communication devices that are similar to developed MicroSTARLING arrays. Individual systems may cover more than one class.

A. NODE SIZE

MicroSTARLING nodes based on the fully wireless device components in Fig. 13 could fit within a 3mm $\times$ 2mm package. These would be comparable to the original approximately 3mm $\times$ 5mm corner cube, retro-reflecting node by Warneke and Pister [25], the 2.2mm $\times$ 1.1 mm stacked chip mote by Lee [30], the 3mm $\times$ 1mm ultrasound based node by Seo [26], the 5mm $\times$ 5mm laser modulating node by Liu [24], and the single chip 3mm $\times$ 2mm optical and BLE beacon chip by Maksimovic [27].

B. NODE POWER

Lower power is always an important attribute for wireless networks and even more so for small energy harvesting devices. Only a few devices can function on less than 3mW of power. The MicroSTARLING fully wireless node requires 3mW of continuous power, while other smart dust nodes require mW of power [27], μW of power [25], [26], [30] or even nW of power [23]. The μW and nW power nodes generally employ modulating reflectors rather than use power for their own optical source, preventing them from multihop data transmission.

C. MULTIHOP PERFORMANCE

A key requirement for small, embedded arrays which transmit over short distances is the ability to transmit data through a high number of multihop transfers. Without stable multihop

transitions the power required to reach the base station will increase beyond the ability of the small package devices to harvest sufficient energy. In general, VLC nodes attempting larger data transfers have not demonstrated more than 1 or 2 hop transfers except for a report of 3 hops by Matheus [22] with significant loss of throughput for each additional hop. MicroSTARLING nodes have produced 6 hops with no noticeable change in throughput for our small data transfers. We are the first group to our knowledge with successful data transmission of 6 or more hops using optical communication. To our knowledge, no multihop smart dust nodes exist as most have been demonstrated as one-to-one or require direct communication with a base station for all communications. The larger and higher power RFWSN nodes using RF for data transmission have demonstrated multihop communication of up to 7 hops. Two RF studies with PC based 802.11b networks have resulted in 6 hops [31] and 7 hops [32].

D. OPTICAL COMMUNICATION

Optical communication is not a requirement for small, embedded nodes but when the density of nodes is high the optical signals from small LEDs have a low probability of traveling more than a few cm due to scattering and absorption. The short signal range reduces the likelihood of crosstalk across the full span of a network on tens of nodes. Radio frequency or ultrasound-based nodes have a higher likelihood of interference given the distance their signals can travel.

E. DATA RATE

In general VLC and RFWSN can transmit Kbps to Mbps of data over meters of distance. Smart dust systems also transmit over meters of distance. Although, the breadboard version of the MicroSTARLING nodes (Fig. 9) can transmit up to 50mm, the nodes are designed for use in an embedded array of 0.5 mm nodes with 5 mm node spacing. Therefore, the communication distance will be significantly lower than a meter unless external amplifiers are used. With respect to data rate our device can transmit data out from the last node at a rate of 192bps for an input clock of 4MHz. Our demonstration chip has an extremely low data rate and a future device with up to 16bits per node readout would only improve to 3Kbps. This fits with our design plan of a small sensor or weighted learning network. The exact data rate for smart dust transfers is not always clearly reported. We identified three reports of data rates from the node to the base station of possibly more than 1Kbps. Seo *et al.* report sampling of neurons at 10K samples per second. Lee *et al.* report occasional readout of stored data at ∼7Kbps. Maksimovic *et al.* report transmitting BLE beacons of 128 bits at an unspecified number of beacons per second.

F. SELF-ORGANIZATION

Self-organization is essential for nodes which may be placed randomly into an environment or experience movement during data collection. We have demonstrated self-organization using our MicroSTARLING nodes. Additionally, these devices can repair the network during the loss or insertion of another node within 140ms. The MicroSTARLING processor can also select between nodes when more than one is within range. The selection process is important as a wider field of view will affect the hunting phase in that partners are easier to find and collisions are more likely. The RFWSN nodes and VLC nodes we cited above are self-organizing however, none of them are suitable for fabricating a mW and mm scale multihop embedded network node.

G. APPLICATIONS

The MicroSTARLING nodes presented in this report will be most useful for sensor networks within structures or tissues. For instance, a key application would be a 3D printed tissue model in which data on local changes in position are desired for surgical simulation training. The cuts into the tissue model would result in reorganization of the network and repairs to the tissue would reform the original network. Another application is for brain machine interfaces. In this case transimpedance amplifiers in the nodes could be used to detect neuronal field potentials and wirelessly transmit the data to a base node. This would result in a distributed recording array more compact and wider spread than current cortical surface arrays. Another application would be to embed the MicroSTARLING nodes in a transparent material as a novel neuromorphic computing system. Here the nodes would be modified to have variable strength connections which mimic the weights between ''neurons'' of standard software neural networks. One advantage being the ability to connect with many nodes optically removing the need for wired connection between the neural network elements. Another advantage would be the independent function of each node which is more like the way neurons in the animal brain work.

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