IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received June 29, 2021, accepted July 19, 2021, date of publication July 26, 2021, date of current version August 11, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3100129

A Ka-Band Balanced Four-Beam Phased-Array Receiver With Symmetrical Beam-Distribution Network in 65-nm CMOS

NA PENG, (Graduate Student Member, IEEE), PENG GU, (Graduate Student Member, IEEE), AND DIXIAN ZHAO, (Senior Member, IEEE)

National Mobile Communication Research Laboratory, School of Information Science and Engineering, Southeast University, Nanjing 210096, China
Purple Mountain Laboratories, Nanjing 211100, China

Corresponding author: Dixian Zhao (dixian.zhao@seu.edu.cn)

This work was supported by the National Key Research and Development Program of China under Grant 2019YFB1803000.

ABSTRACT This paper demonstrates a Ka-band CMOS phased-array receiver capable of generating four balanced beams from two inputs. A passive four-beam symmetrical differential network is proposed to distribute two input signals to eight channels and facilitate beam generation at the outputs in the receiver. The detailed design and optimization of the passive four-beam differential network are presented. Using a 6-bit passive vector-modulated phase shifter and a 5-bit switched-type attenuator in each channel, we implement a phase control of 360° with <4° RMS phase error and a gain control of 17 dB with <0.35 dB RMS gain error from 27 to 31 GHz. The receiver consumes a current of only 40 mA under 1 V supply voltage. Eight channels of the four-beam phased-array receiver were measured and a gain mismatch of less than 0.3 dB has been achieved. Beam to beam couplings are investigated by measurements and beam-to-beam isolation are better than 32 dB from 27 to 31 GHz. The chip size is 2.6×4 mm^2 including all digital control circuitry and pads.

INDEX TERMS Symmetrical beam-distribution network, CMOS, integrated circuits, millimeter wave, phase shifter, phased array, receiver, Wilkinson power combiner, satellite communications.

I. INTRODUCTION

High-throughput satellites (HTS) and low earth orbit (LEO) satellites are future directions in broadband satellite communications (SATCOM). Millimeter-wave (mm-Wave) SATCOM is a frequency-division duplexing system using the Ka band (i.e., 27.5-30 GHz), which is exclusively allocated for communication between the transmitters at the ground terminal and the receivers at the satellite side. Phased-array based approaches are a favored solution for future mm-Wave SATCOM [1]–[7] both at ground and satellite sides. To improve system reliability, a large-scale array with thousands of channels is usually required for space use, so that communication quality can still be ensured in extreme cases where some of the chips are temporarily damaged due to single event effects caused by energetic particles in the space.

The associate editor coordinating the review of this manuscript and approving it for publication was Dušan Grujić.

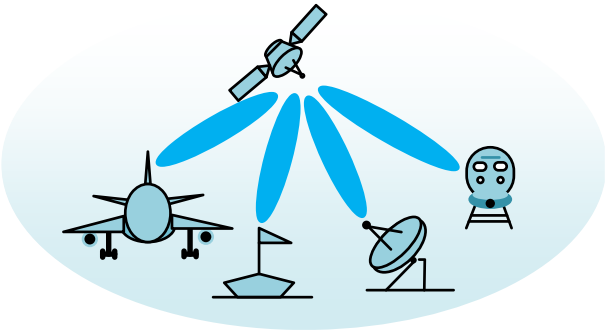


FIGURE 1. Satellite communication scenario equipped with multi-beam phased-array systems.

Increasing communication capacity is required in SATCOM systems. To this end, the state-of-art solution is to use multi-beam phased arrays to support concurrent communications (see Figure 1). To implement a concurrent multi-beam communication system, an intuitive method is to

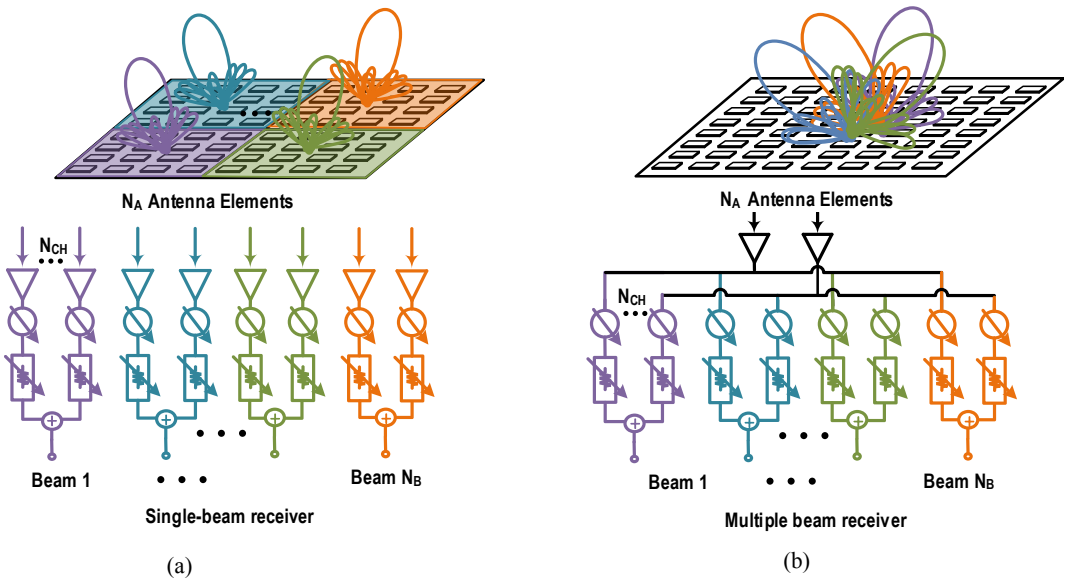


FIGURE 2. Large-scale antenna arrays based on (a) single-beam phased array receiver front-ends and (b) multi-beam phased array receiver chips.

assemble multiple single-beam phased arrays in one board as show in Figure 2(a). However, this solution leads to a bulky, expensive and energy inefficient design for multi-beam generation, with $N_B \times N_A$ chips needed to generate N_B beams with N_A-element phased arrays. The other solution is shown in Figure 2(b), where multiple concurrent beams can be received by a single phased array using multi-beam receiver front-ends. For N_{CH} channels of each beam at the same antenna aperture size, the solution in Figure 2(b) has higher gain than that in Figure 2(a). In fact, for a total of N_A antenna elements to support N_B beams, the gain of the phased array in Figure 2(a) is only from N_A/N_B antennas while the gain of the multi-beam phased array in Figure 2(b) is from N_A antenna elements. In other words, the solution in Figure 2(b) can reduce the system size of a multi-beam phased array by using the high-integration multi-beam chip. As an example, to realize four beams with each beam drawing from the same number of antennas, the integrated four-beam chip can help save about 75% physical size.

Multi-beam phased-array transceivers have been proposed in [8]–[12] to improve system integration and reduce cost. In [9], a hybrid beamforming phased array is proposed, with two baseband streams generated from eight antennas. Also, the work in [8] proposed a dual-band four-beam receiver. Although the designs could be employed for a large-scale phased array, a high power consumption would be introduced by the large number of mixers and the LOs. Active combining networks are used in the eight-beam receiver [10] and four-beam receiver [11], introducing extra power consumption. Besides, imbalance is caused in [11] by the different length of transmission lines at the beam outputs. Therefore, the multi-beam chip design has special challenges to properly design the signal distribution networks

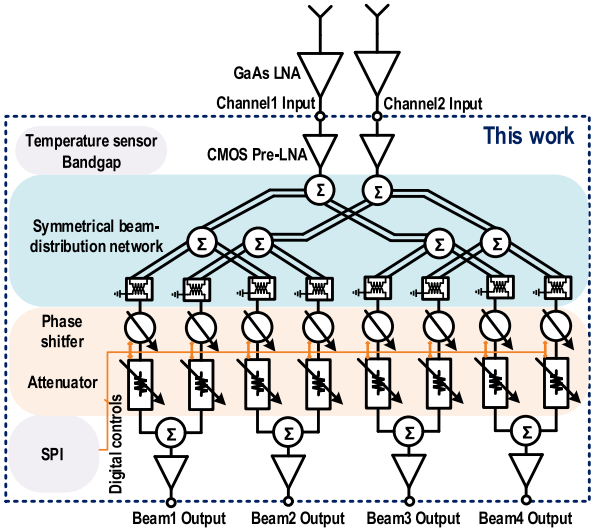
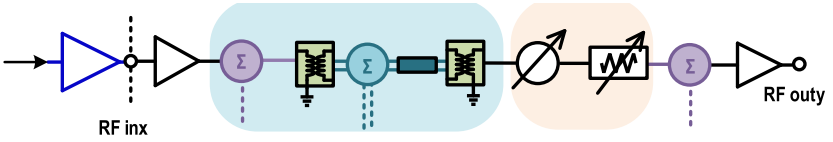


FIGURE 3. Block diagram of the two-element four-beam phased array receiver.

and to reduce the couplings between different beams. Furthermore, the power consumption needs to be reduced for space use.

This paper presents a Ka-band four-beam phased-array receiver based on [13] for SATCOM application, featuring balanced and beam generation, accurate gain/phase control and ultra-low power consumption. A passive symmetrical beam-distribution network (SBDN) is proposed for generating four balanced beams with high isolation. Accurate phase and gain controls of each channel are achieved by a vector-modulated phase shifter (VMPS) and a switched-type attenuator (STA). The fully-passive SBDN, gain and phase tuning blocks, along with the low-power low noise



	GaAs-LNA [19]	Pre -LNA	SE-PD	Balun 1	Diff.-PD + T-line	Balun 2	PS	ATT	SE-PD	Amplifier	Total
Gain(dB)	+17	+20	-3.7	-1	-4.3	-1	-10	-4	-3.7	+10	2.3/ 19.3
NF(dB)	1.2	4	3.7	1	4	1	10	4	0.7	4	12.3/ 2.1
DC Power (mW)	24	10	0							5	5/ 11

FIGURE 4. Channel gain, NF and power calculations.

amplifiers (LNAs) contribute to an extremely low power consumption. In consequence, the complete two-element four-beam phased-array receiver only consumes a total of 40 mW DC power, which satisfies the low-power requirement of space use.

The rest of this paper is organized as follows. Section II presents the overall architecture of the proposed two-element four-beam phased array. Section III demonstrates the detailed circuit implementation of the building blocks, including the SBDN, the pre-LNA, the phase shifter and the attenuator. In section IV, single-channel measurement and beam coupling characterization through measurement results are presented. Section V concludes this paper.

II. SYSTEM ARCHITECTURE

For the large-scale phased arrays, low power consumption is of great importance. While the multiple-beam receiver chip can help reduce the system size, the large number of phase/amplitude tuning blocks, required for multiple-beam operation, would still cause high power consumption. To tackle this challenge, a two-element four-beam receiver chip consuming extremely low power is proposed.

Figure 3 shows the block diagram of the proposed two-element four-beam receiver chip. The two pre-LNAs are employed to suppress the noise of the subsequent circuit stages and improve the noise figure of the system. Then, the two outputs from the pre-LNAs are each divided into four signal paths, which forms two elements for each beam. The elements for the same beam are placed adjacently. A passive SBDN featuring perfect balance and high isolation is proposed to perform the aforementioned two-to-eight signal division. After the SBDN, each of the eight channels incorporates the phase and gain control blocks, which are independently controlled. The phase tuning is implemented by a 6-bit fully-passive VMPS and the gain tuning is implemented by a 5-bit STA, both introducing zero DC power consumption. After the phase and gain tuning blocks, four combiners are adopted to sum up the signals from element 1 and element 2, which generate four output beams. Finally, an amplifier is added after the combiner to increase the gain of each beam.

To take advantage of the low-noise GaAs technology, external GaAs LNA will be added before the pre-LNA, which can suppress the noise of the CMOS chip and reduce the system noise figure. GaAs LNAs with good performance have been reported in [14]–[20]. In particular, broadband LNAs with 1-2 dB noise figure (NF) and 20 dB gain have been achieved in [14]–[16]. In Figure 4, the calculation of the gain and noise performance with and without the GaAs LNA is summarized. As indicated, a 2.3 dB gain and 12.3 dB NF can be achieved by the CMOS chip, without GaAs LNA. By adding a GaAs LNA with 17 dB gain and 1.2 NF in [19], the gain of the whole system can be increased to 19.3 dB and the NF can be reduced to 2.1 dB. Therefore, the complete system can achieve low power consumption and low NF at the same time.

III. CIRCUIT IMPLEMENTATIONS

A. SYMMETRICAL BEAM-DISTRIBUTION NETWORK

In this work, a two-to-eight SBDN is required to distribute the signals from the two inputs. Since the passive distribution networks have the advantage of high linearity and zero dc power consumption, the SBDN in this work is implemented by a symmetrical two-stage Wilkinson power divider (WPD). The main design target of this network includes: 1) high isolation between different beam branches; 2) identical transmission performance for each branch; 3) low loss and compact area; 4) facilitation of beam synthesis.

The circuit diagram of the proposed SBDN is shown in Figure 5, which consists of single-ended and differential WPDs, differential interconnection lines and transformer-based baluns. The eight outputs (i.e., OUT A_1-OUT A_4 and OUT B_1-OUT B_4) distributed from the two inputs (i.e., IN A and IN B) are arranged in a way that facilitates beam synthesis.

At the first stage of the network, a single-ended WPD is employed. To reduce the large area of the $\lambda/4$ transmission line (TL) in the WPD, lumped-element WPDs have been

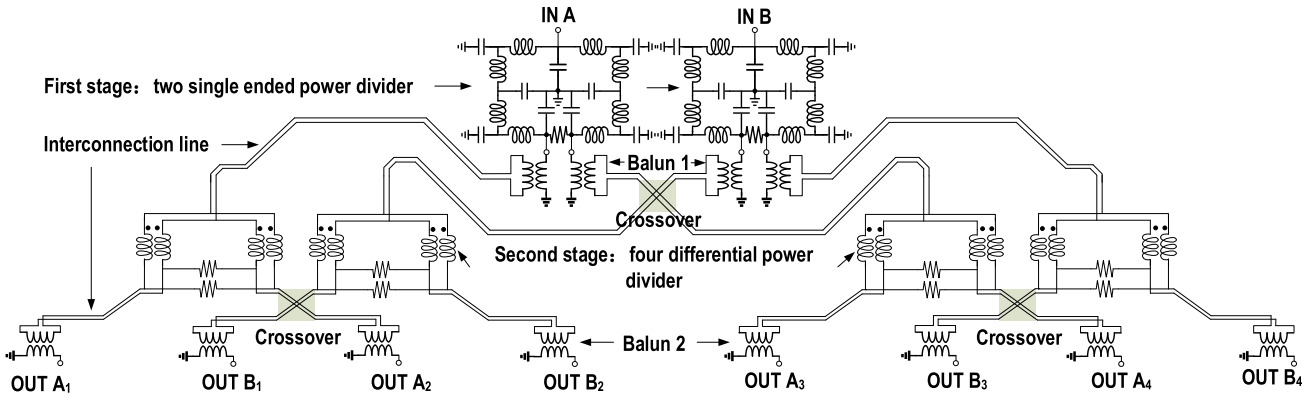


FIGURE 5. Circuit diagram of the symmetrical beam-distribution network.

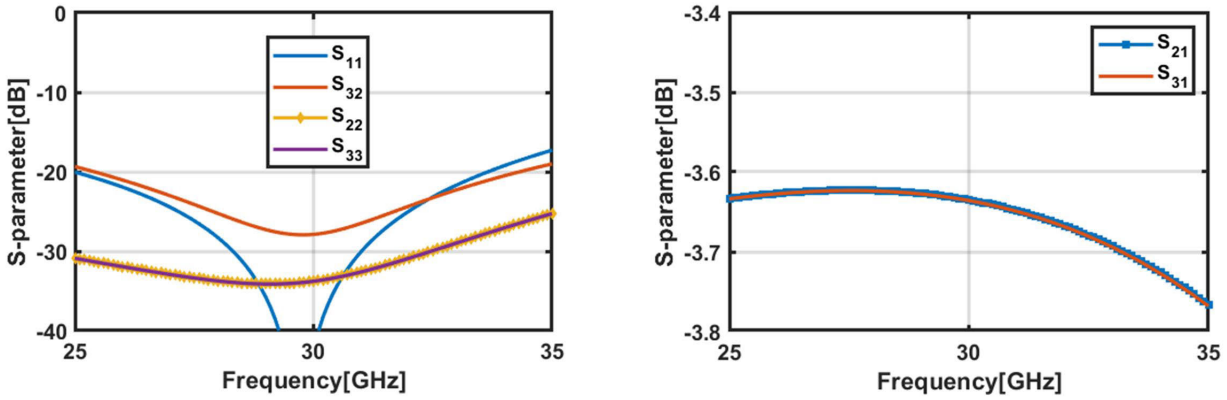


FIGURE 6. Simulated (a) $S_{11}/S_{22}/S_{33}$ /S_{23} and (b) S_{12}/S_{13} of the multi-tap technique based single-ended WPD.

employed [21]. In this design, the λ/4 TL is implemented by a five-tap inductor to ensure compact size and broad bandwidth simultaneously. The simulated S-parameter of the compact WPD are shown in Figure 6. The isolation and return loss are better than 25 dB and the insertion loss is less than 0.64 dB across the 27-31 GHz band.

The differential WPDs are required at the second stage. A low-loss, broadband and compact differential λ/4 TL is the key to implement a high-performance differential WPD. To reduce chip area, transformer-based [22] and inductor-capacitor-based [23] differential WPD have been proposed. However, the former introduces phase and magnitude imbalance and the latter suffers from narrow bandwidth. In this design, a capacitor-free differential λ/4 TL with compact area is proposed, as shown in Figure 7(a), where L_p and L_n represent the inductors in the positive and negative paths, respectively. The parasitic capacitance between L_p and L_n inherently forms the capacitance of a λ/4 TL, which avoids the use of extra capacitors and thus improves the bandwidth. Besides, benefiting from the electromagnetic enhancement between L_p and L_n, the insertion loss of the λ/4 TL is greatly

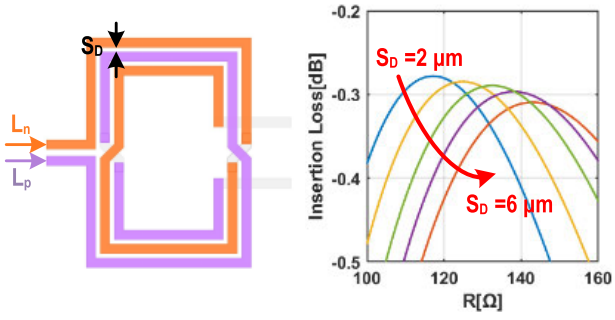


FIGURE 7. (a) Layout of the compact capacitor-free λ/4 transmission line, (b) simulated insertion loss and of coupling-inductor quarter wavelength differential transmission lines with various line space (S_D) settings by sweeping the port impedance at 29 GHz.

reduced with shorter line length. Further, the characteristic impedance of the λ/4 TL can be tuned by employing different line space and width. For example, Figure 7(b) depicts the simulated insertion loss of the transmission line versus the

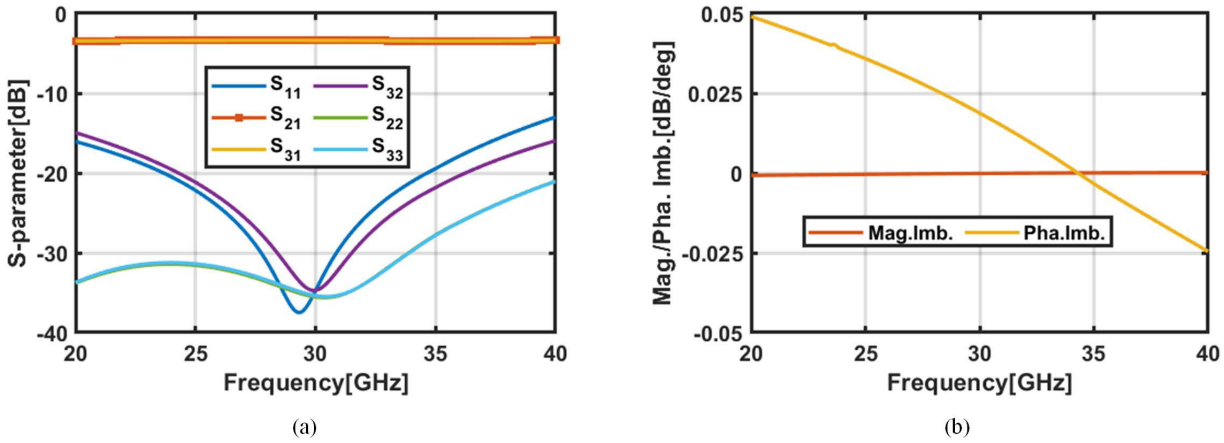


FIGURE 8. Simulated (a) S-parameter and (b) phase and magnitude imbalances of the coupling-inductor based differential WPD.

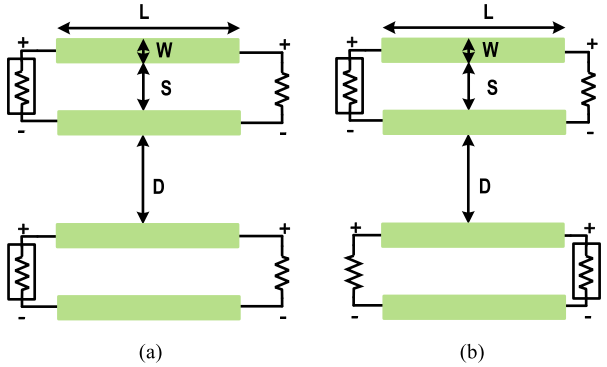


FIGURE 9. (a) Forward and (b) reverse coupling simulation setups of two differential lines.

port impedance at 29 GHz, while the line space (S_D) is varied. As expected, the characteristic impedance will increase with larger line space, due to the decreased parasitic capacitance between the metal lines. Nonetheless, it should be noted that there is a lower bound of the characteristic impedance of the differential λ/4 TL due to physical limitation of the technology. In this work, line space of 2 μm and line width of 4 μm are chosen for the λ/4 TL, which exhibits a simulated characteristic impedance of 113 Ω. Thus, the characteristic impedance of the differential WPD is 80 Ω. Figure 8 shows the simulated S-parameters and magnitude/phase imbalance between the two output ports. As indicated, the differential WPD achieves a simulated 0.36 dB loss and 25 dB isolation from 27 to 31 GHz. The phase and magnitude imbalances are less than 0.05° and 0.001dB, respectively.

To reduce the coupling between the interconnects for different beams, differential lines are preferred for the outstanding anti-interference ability [24]. Considering the pair of differential lines shown in Figure 9, the line distance (D), line length (L), line width (W) and line space (S) will affect the coupling between the two differential lines. The coupling factor of the differential lines under various D and L is compared in [24], which indicates that large D and small L contribute to lower coupling. For further improvement of isolation and also to reduce insertion loss, the optimization of W and S is necessary. Figure 9(a) and (b) depict the forward and reverse coupling simulation setup for the pair of differential lines, where Z_o represents the characteristic impedance of the differential line. Based on the settings in Figure 9, electro-magnetic (EM) simulations are performed to calculate TL insertion loss versus isolation and TL characteristic impedance versus S, with various W and S settings. Figure 10(a) suggests that a low S contributes to high isolation between the two differential lines, mainly because that much less electromagnetic energy is leaked to the outside of the differential lines. However, setting the S for optimal isolation will cause several problems. First, the low S for high isolation will cause high loss, as revealed by Figure 10(a). Second, a low S will reduce the characteristic impedance Z_o to <60 Ω, as presented in Figure 10(b). This will cause impedance mismatch at the differential WPD input ports, since there is a low bound of the characteristic impedance of the differential WPD, as mentioned. In consequence, a line space of 6 μm and line width of 5 μm contributing to 80 Ω Z_o is chosen for the differential interconnection lines, which ensures low loss and relatively high isolation. The routing of the differential interconnection lines is carefully designed for symmetry, in order to achieve balanced outputs. Finally, the transformer-based baluns (i.e., balun 1 and balun 2) are employed to perform the single-ended to differential conversion signal and also provide impedance matching.

The performance of the proposed SBDN is simulated by the ADS Momentum simulator. The simulations indicate the return loss of the input and output ports are 15-27 dB from 27 to 31 GHz. The insertion losses are less than 10 dB across the 27-31 GHz band including the 6 dB intrinsic loss as shown in Figure 11(a). The loss differences among the eight distribution branches (i.e., from IN A to OUT A_x and from

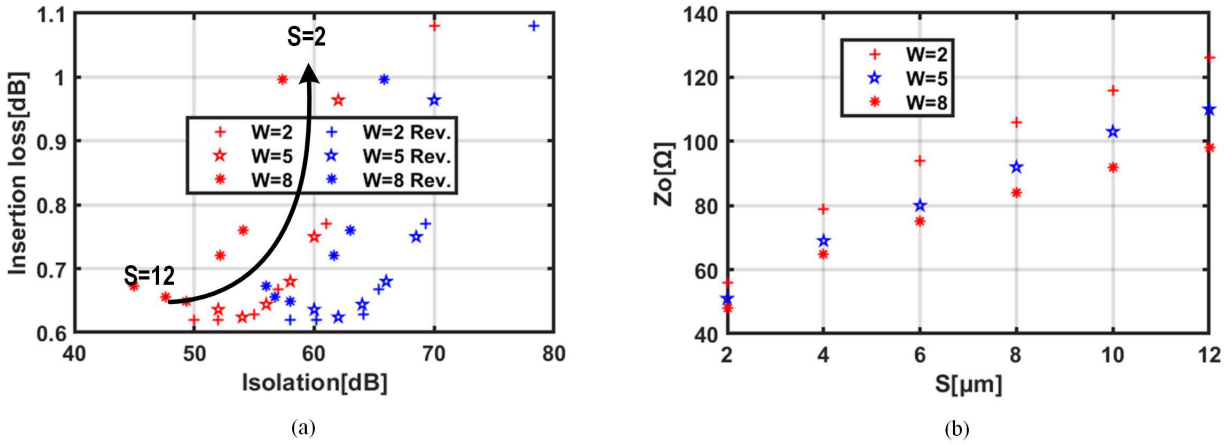


FIGURE 10. Simulated (a) isolation and insertion loss, (b) characteristic impedance with different line width (*W*) and line space (*S*) settings of quarter wavelength differential transmission lines at 29 GHz.

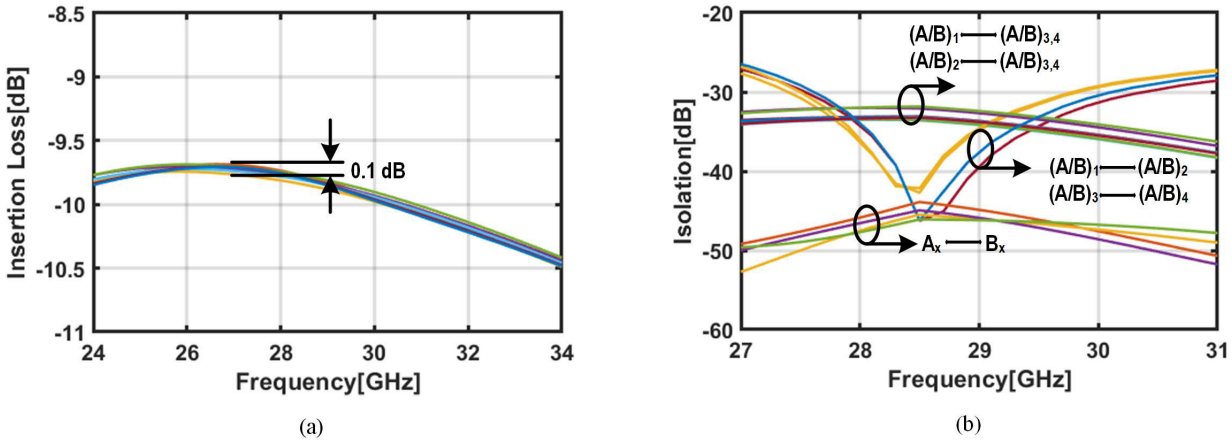


FIGURE 11. Simulated insertion loss (a) insertion loss and (b) isolation of the SBDN.

IN B to OUT B_x) are less than 0.1 dB, which is mainly caused by the implementation of the lower metal lines in the three crossovers (see the shadow in Figure 5). The output ports isolations are shown in Figure 11(b). As can be seen, the isolations between different beams (i.e., between OUT A_x and OUT B_x) are higher than 46 dB. The isolations between the signal branches of a same power divider from individual input A or B(i.e., between OUT $(A/B)_1$ and OUT $(A/B)_2$ or OUT $(A/B)_3$ and OUT $(A/B)_4$) are higher than 28 dB at 27-31 GHz. The peak values are higher than 42 dB at 28.5 GHz. The isolations between signal branches of different power divider (i.e., between OUT $(A/B)_1$ and OUT $(A/B)_{3,4}$ or OUT $(A/B)_2$ and OUT $(A/B)_{3,4}$) are 32-38 dB at 27-31 GHz. The amplitude balance and beam to beam isolation of the SBDN will be verified in the measurement section.

B. PRE-LNA

The pre-LNA is intended to suppress the noise of the CMOS phased-array and improve the noise figure of the system. As shown in Figure 12, the first stage employs a small source-degenerated inductor of 55 pH to achieve input impedance and noise matchings simultaneously. To achieve low noise figure and broadband impedance matching with low power dissipation, the total gate width of 2×32 μm is chosen for all transistors. The L-C-L network at the interstage can provide two frequency peaks to realize broadband matching while minimizing the insertion loss. The spiral inductors are widely used for saving the chip area and the capacitors are adopted between stages for independent biasings which are generated by the bandgap reference circuit. Furthermore, design iterations are required to fine tune matching circuits for optimal performance. The simulated results are plotted in Figure 13, it shows that the gain of the pre-LNA is 20 dB. The gain variation is less than 1 dB from 26 to 32 GHz. The two peak gains are 21 dB and 20.85 at 26.3 GHz and 31 GHz, respectively. The noise figure is less than 4.3 dB across 26-32 GHz. The minimum noise figure is 4 dB at 29-31 GHz. From 27 to 31 GHz, the simulated S_{11} and S_{22} are less than -11 dB and -8 dB, respectively. The simulated input P_{1dB} is -27 dBm.

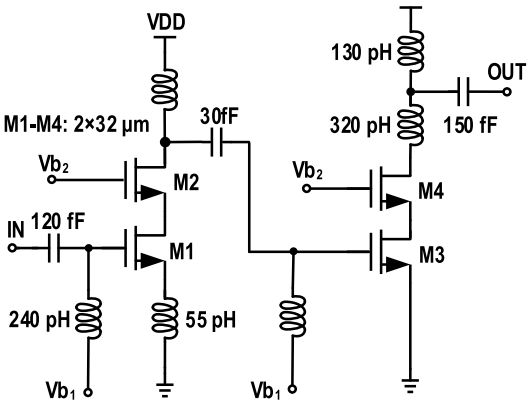


FIGURE 12. Schematic of the single-ended LNA.

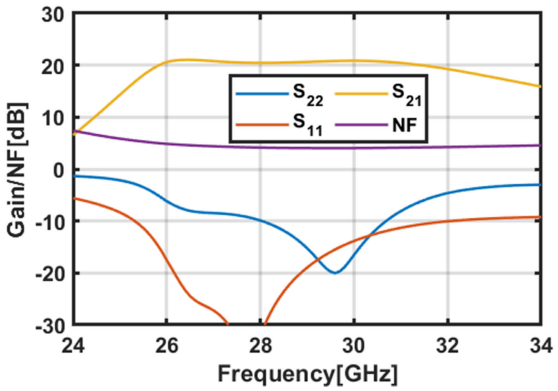


FIGURE 13. Simulated results of the single-ended LNA.

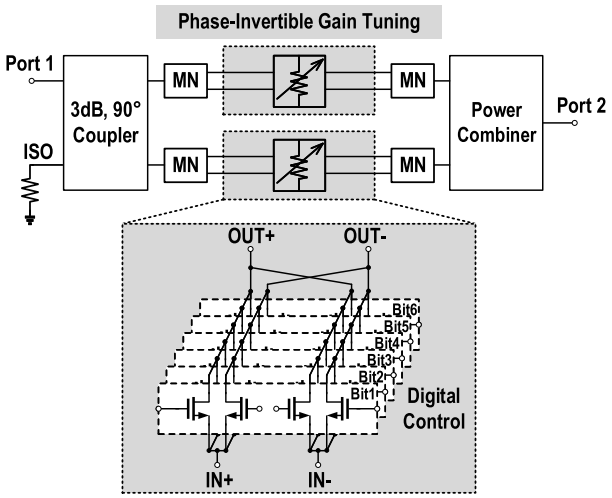


FIGURE 14. Block diagram of the phase shifter.

C. VECTOR-MODULATED PHASE SHIFTER

Figure 14 shows the block diagram of a fully-passive vector-modulated phase shifter (VMPS). It consists of a 3-dB quadrature coupler, two fully-passive phase-invertible gain tuning blocks, a power combiner and the matching networks (MN). The design is similar to [25]. The 3-dB quadrature coupler is implemented by vertically coupled microstrip lines using the top two metal layers, as shown in Figure 15. The microstrip lines are folded to reduce chip area. The simulated amplitude and phase responses of the coupler is depicted in Figure 16. The IQ gain and phase errors are less than 0.2 dB and 2.1° within the 26 – 32 GHz band, implying good IQ balance. Then, the two generated quadrature signals are weighted by the switch-array-based gain tuning blocks. The gain tuning block contains a total of six cross-connected

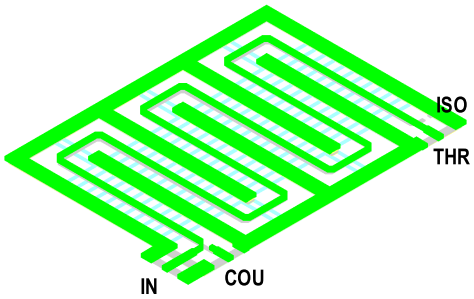
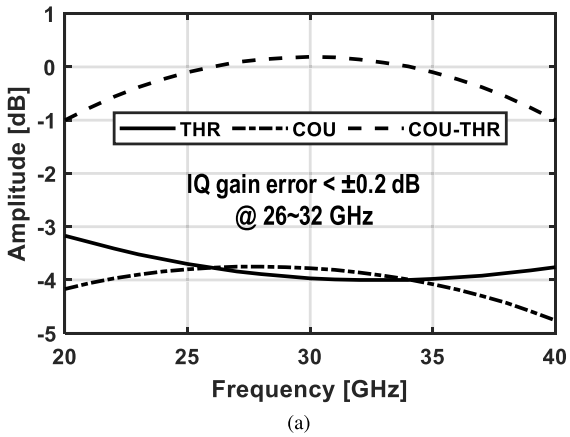
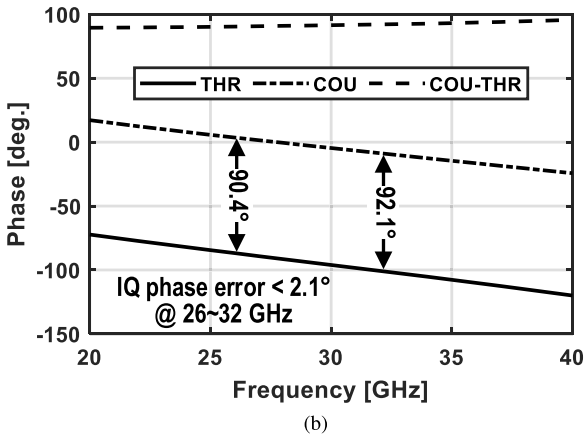


FIGURE 15. 3-D electromagnetic (EM) model of the 3 dB quadrature coupler.



(a)



(b)

FIGURE 16. (a) Simulated amplitude responses of the through and coupled ports and the IQ gain error. (b) Simulated phase responses of the through and coupled ports and the IQ phase error.

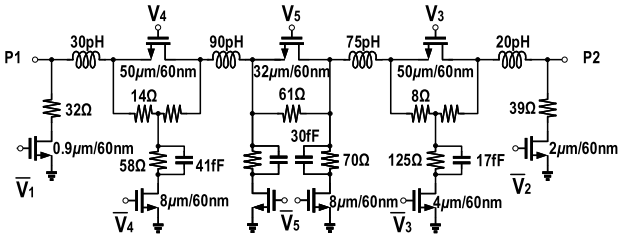


FIGURE 17. Schematic of the 5-bit attenuator.

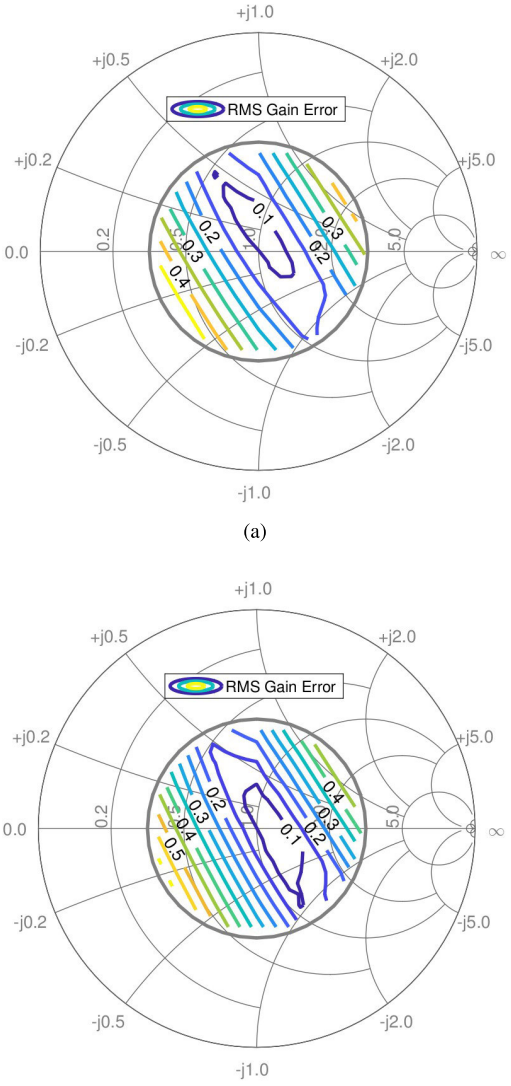


FIGURE 18. Simulated contour lines of RMS amplitude error under various (a) source and (b) load impedances at 30 GHz.

transistor-array units (i.e., Bit1 to Bit6). The transistors in the units have the width of 0.7 μm per finger and the finger number scales up from 1 (i.e., Bit1) to 32 (i.e., Bit6). All the transistors operate in the deep triode region, where the drain and source are biased with 0 V. The transistor gates are biased with 0 or 1 V, which enables direct-digital control for the gain tuning block. The cross-connected structure of

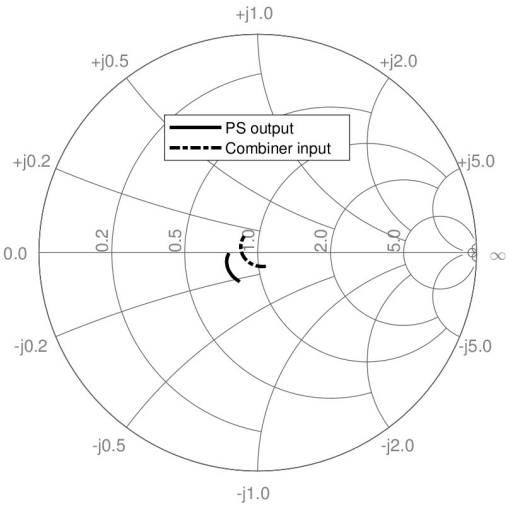


FIGURE 19. Simulated phase shifter output and combiner input impedances in the Smith chart across the 27 – 31 GHz band.

the transistor array provides phase inverting operation for the passive gain tuning block and thus ensures phase shifting in all four quadrants which covers full 360° phase-shift range. The transformer-based MNs are employed for the input and output impedance matching of the gain tuning blocks, which also provide the conversions between the single-ended and differential signals. Then, the I- and Q-path signals are summed up by the Wilkinson-like power combiner. Lumped inductors and capacitors are adopted to implement the $\lambda/4$ transmission line, based on its lumped L-C model, in order to reduce chip area. The passive VMPS are digitally controlled by a total of 12 bits (i.e., 6 bits for each of I and Q paths), which provides 4096 possible phase shifting states. A sub-selection of the 4096 states ensuring both accurate phase shifting and low gain error are determined based on the simulated phase responses. The corresponding controls are stored in a look-up table (LUT) and can be refreshed according to the measured results, if changes are necessary.

D. SWITCHED-TYPE ATTENUATOR

A switched-type attenuator (STA) is employed to achieve the linear-in-dB gain tuning. The schematic of the 5-bit STA is shown in Figure 17. Accurate gain tuning and good impedance matching can be ensured by optimizing the resistance values of each attenuation cell. Capacitive compensation technique is used to enhance the attenuator performance over a wide operation bandwidth. According to the simulation, the stand-alone 5-bit STA has an RMS amplitude error of less than 0.1 dB from 27 to 31 GHz. This design is similar to [26] while the source and load impedance of the attenuator are further optimized to ensure wide band amplitude tuning performance. Noted that the attenuation performance would deteriorate if the attenuator is connected to poorly matched source or load impedances. To evaluate this effect, the RMS amplitude errors of the STA under different source and load impedances at 30 GHz are simulated and

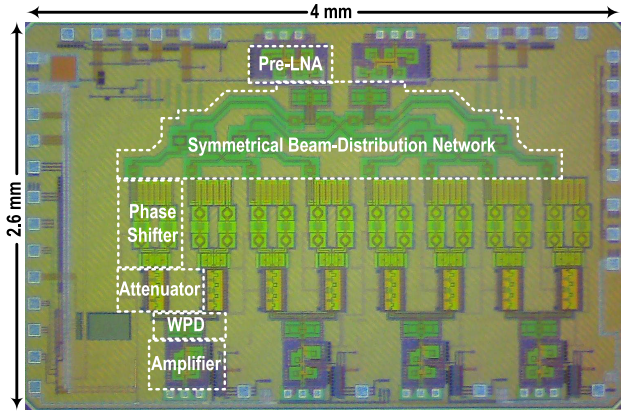


FIGURE 20. Chip micrograph of the 4-beam phased array receiver.

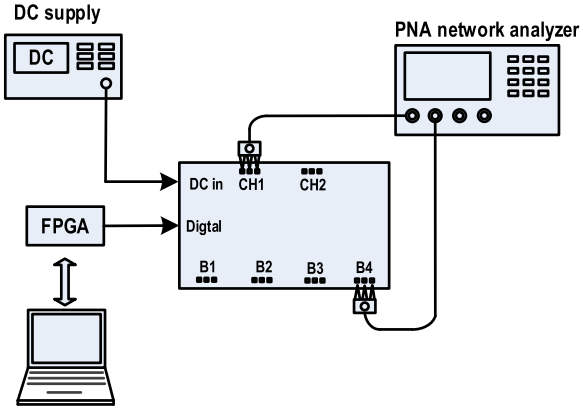


FIGURE 21. Measurement setup.

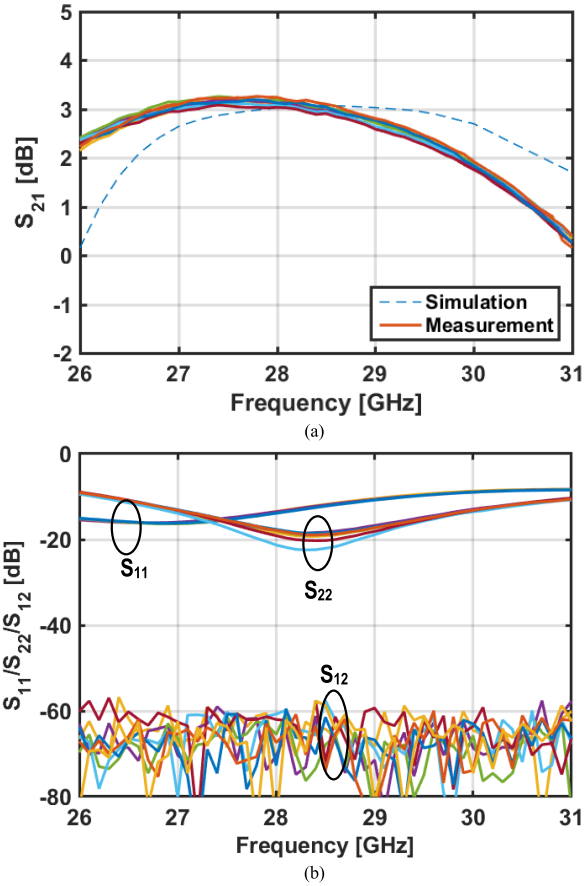


FIGURE 22. Measured and simulated (a) S_{21} and measured (b) S_{11}, S_{22} and S_{12} of the eight channels.

depicted in the Smith chart (see Figure 18). As revealed, the RMS amplitude error exhibits degradation when the source or the load impedance deviates from the perfect 50 Ω. Thus, the source and load impedances connected to the STA should be carefully designed to avoid possible performance degradation. In this work, this is accomplished by a proper arrangement of the circuit stages as shown in Figure 3. This configuration takes advantage of the inherently good matching at the phase shifter output and the combiner input. As shown in Figure 19), the impedances at the output of the phase shifter and the input of the combiner are located in low amplitude error area and thus ensures high attenuation accuracy.

IV. MEASUREMENT RESULTS

The four-beam phased-array receiver is implemented in 65-nm CMOS technology. Figure 20 shows the die micrograph of the receiver chip that occupying 2.6×4 mm^2 including all pads. A block diagram of the measurement setup is shown in Figure 21. The SPI is controlled by the field programmable gate array (FPGA). The RF measurements are done using GSG probes on a high-frequency probe station. Note that the measurements can only be performed by probing one input and one output (i.e., one of the two channel inputs and one of the four beam outputs).

A. SINGLE-BEAM MEASUREMENTS

The balance of the SBDN is verified by measuring the S-parameter of each channel (i.e., from two inputs to four outputs). As shown in Figure 22, the return loss (S_{11} and S_{22}) and reverse isolation (S_{12}) are < -10 dB and < -60 dB, respectively. The magnitude and phase errors of S_{21} are shown in Figure 23. As can be seen, owing to the symmetrical design of the SBDN, the gain and phase mismatches of the eight channels remain less than 0.3 dB and 2°, respectively. Figure 24 depicts the measured relative gain and relative phase, indicating that the phased array has achieved approximately 17 dB gain tuning range with 0.53 dB tuning step and 360° phase shift range with 5.625° phase step. The corresponding RMS gain and phase errors are shown in Figure 25, which are less than 0.35 dB and 4°, respectively. The measured and simulated NF are shown in Figure 26. As can be seen, the measured NF is 10.8-11.7 dB at 26-31 GHz. It is slightly less than the value of 12.3 dB calculated in Figure 4. This is because of the measured gain is increased to 3 dB. It should be noted that in order to reduce power consumption, the gain of each channel is low, so the noise figure of the channel is relatively high and it will be reduced to about 2 dB by adding a external GaAs LNA. The measured input P_{1dB} is -22 dBm at 29 GHz.

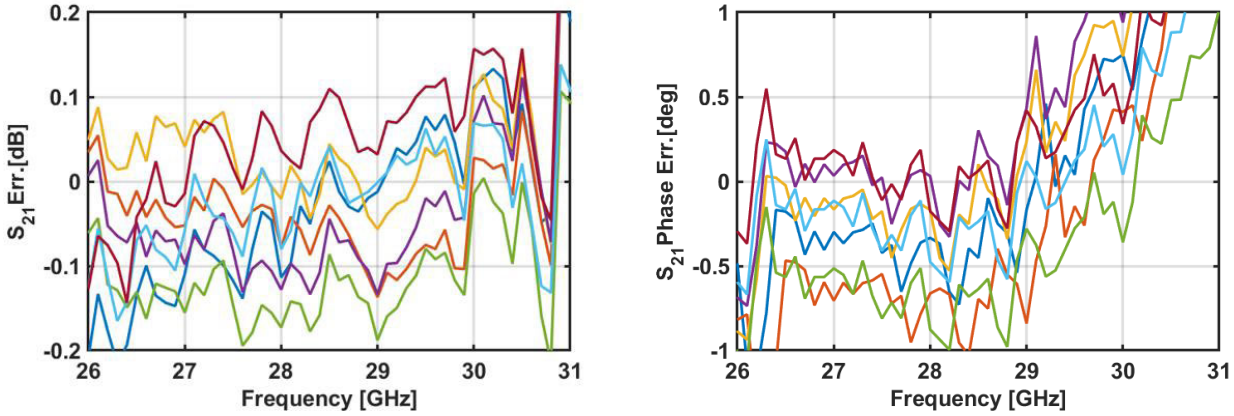


FIGURE 23. Measured S_{21} (a) gain and (b) phase errors of the eight channels.

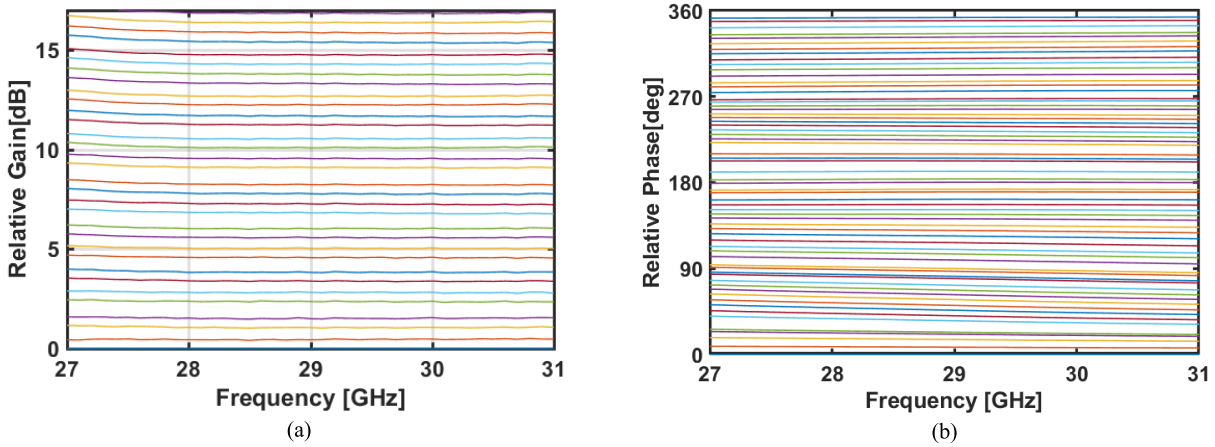


FIGURE 24. Measured (a) relative gain and (b) relative phase.

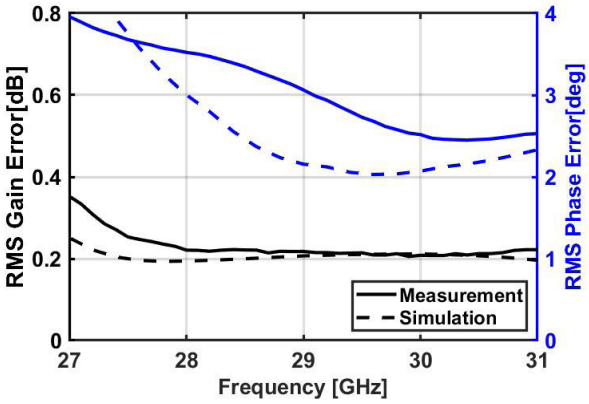


FIGURE 25. Measured and simulated RMS gain and phase error.

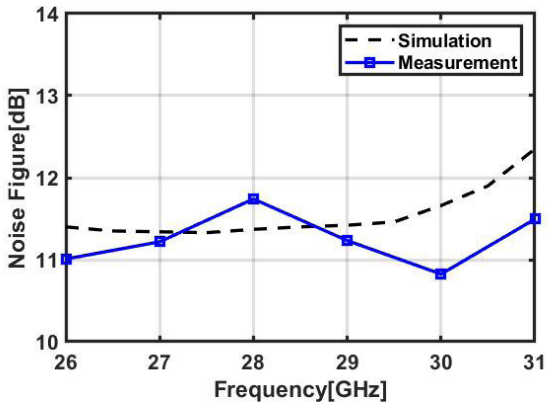


FIGURE 26. Measured and simulated NF.

B. BEAM-COUPLING MEASUREMENTS

Figure 27 depicts the measurement setup and vectorial representation beam coupling of the 4-beam phased array. It is shown that beam 4 (B4) is under test with the input signal fed to channel 2 (CH2). Due to the limitations of the probe-station test, both the input port of CH1 and the output ports of B1, B2, B3 are left open circuited. Note that when these four ports are terminated by 50 Ω, as in the real application, the measured beam couplings would be further reduced. The couplings from beams 1 , 2 and 3 to beam 4 can be obtained

TABLE 1. Performance summary and comparison.

Reference	This work	[10]	[27]	[28]	[29]	[30]
Technology	65-nm CMOS	65-nm CMOS	130-nm COMS	45-nm CMOS SOI	130-nm SiGe	130-nm CMOS
Frequency (GHz)	27-31	7.5-9	24-27	54-64	28-32	22-24
Phase Resolution	5.625° (6-bit)	5.625° (6-bit)	Continuous (0-360°)	11.25° (5-bit)	22.5° (4-bit)	Continuous (0-360°)
Gain Resolution	0.53 dB (5-bit)	18 dB Coarse Control +15.75 dB, 6 bit	Continuous (0-20 dB)	0.43 dB (5-bit)	NA	Continuous (0-20 dB)
RMS Phase Error (°)	<4	<2	<6	3-8	<5.4	6
RMS Gain Error (dB)	<0.35	NA	<0.5	0.6-0.8	<0.6	NA
No. of Beams × No. of Elements	4×2	8×4	1×4	1×4	1×4	1×4
Power (mW)	40	860	920	150	546	115
Power per Element per Beam (mW)	5	27	230	37.5	136	28.75
Area (mm^2)	10.4	19.6[a]	3.96	6	7.2	3.02

[a] Excluding pads area.

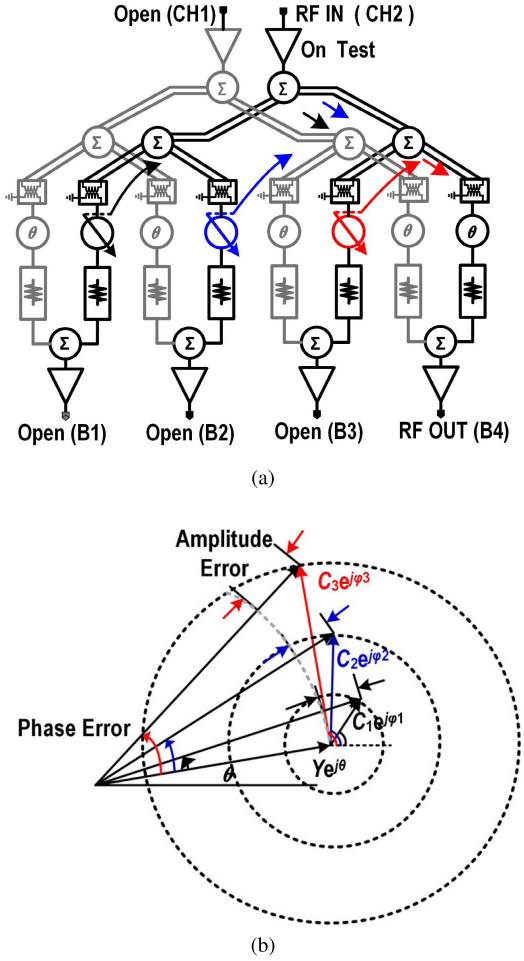


FIGURE 27. Measurement setup and (b) vectorial representation of beam coupling of the four beam phased array.

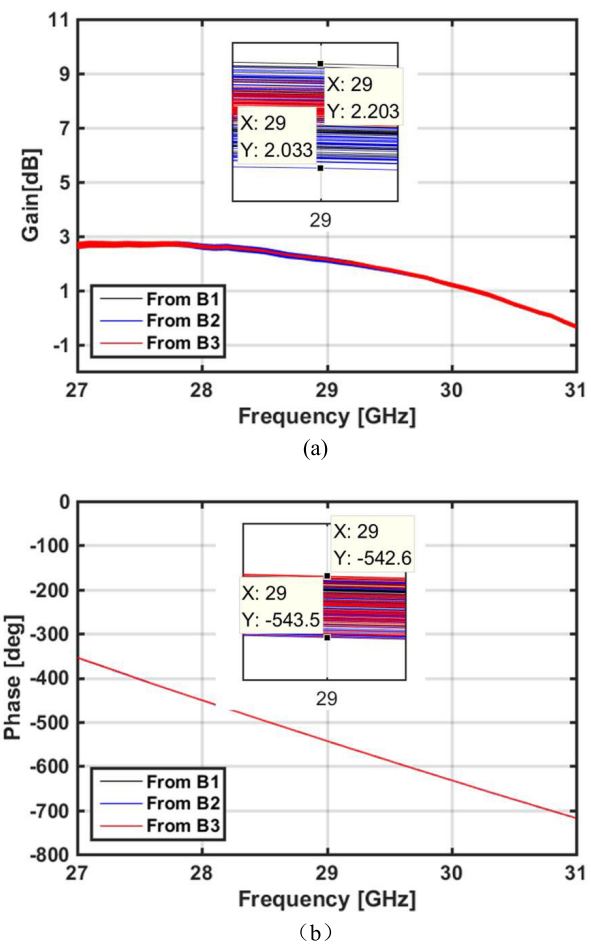


FIGURE 28. Channel coupling characterization: measured (a) gain and (b) phase.

by measuring beam 4 at a constant phase setting and sweeping the phases of beams 1 , 2 and 3 all over 360° . Amplitude and phase of the output B4 will be affected by the couplings from beams 1 , 2 and 3 . They can be characterized as vector $C_1e^{j\varphi_1}$, $C_2e^{j\varphi_2}$ and $C_3e^{j\varphi_3}$ [30] (see Figure 27), respectively. Suppose the unaffected output signal of B4 is $Ye^{j\vartheta}$. The magnitude of

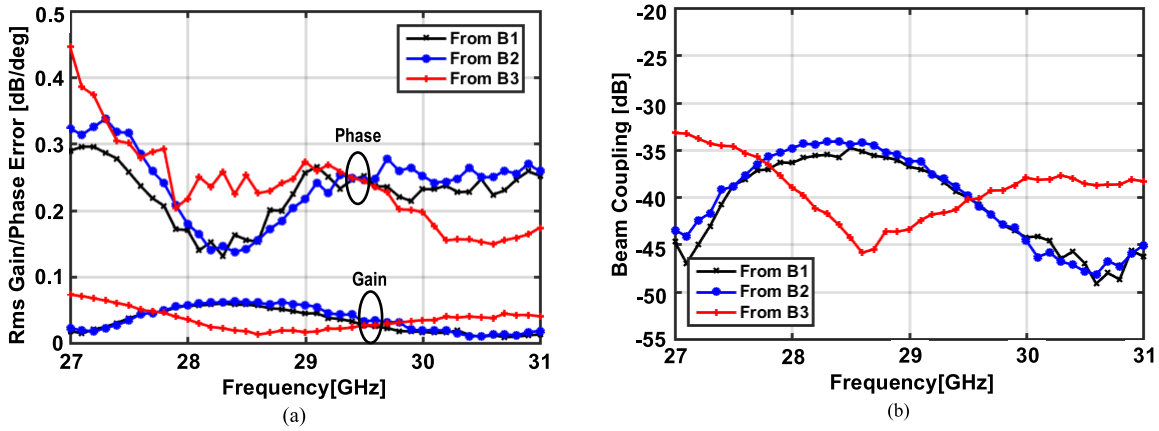


FIGURE 29. Channel coupling characterization: (a) RMS gain and phase errors; (b) beam coupling.

the coupling vector C can be calculated by

$$C = \sqrt{Y^2 + (Y + E_{amp})^2 - 2Y(Y + E_{amp})\cos E_{pha}} \quad (1)$$

where E_{amp} and E_{pha} represent amplitude error and phase error. Then the coupling coefficient described as $C_{coe} = C/Y$ can be obtained from the measured data. Figure 28(a) and (b) shows the measured gain and phase deviation caused by the couplings from beams 1, 2 and 3. Among these three beams, the gain and phase deviations are 0.17 dB and 0.9° at 29 GHz, respectively. The corresponding RMS gain error and phase error are presented in Figure 29 (a), which are less than 0.1 dB and 0.5° respectively. The coupling coefficients are calculated in dB, as shown in Figure 29 (b). As can be seen, the coupling from beam 1 , 2 and 3 are better than −32 dB. Thanks to the symmetrical structure of the beam distribution network. Note that coupling curves of beam 1 and 2 has a similar shape. As indicated in the simulated isolation of the SBDN, the coupling curve of beam 3 is different because of the signal of beam 3 and beam 4 are divided from the same power divider. Similar measurements were performed with beams 1, 2 and 3 and similar results were obtained.

Table 1 summarizes the performance of the phased-array receivers, which shows that this work has achieved four beams generation with competitive phase shifting and gain tuning accuracy under ultra-low power consumption.

V. CONCLUSION

A Ka-band four-beams phased-array receiver is presented in this paper. A symmetrical beam-distribution network is used to achieve four balanced beam generation and high beam isolation in a compact area. From single channel measurements, the phased array has achieved an RMS gain error of less than 0.35 dB and phase error of less than 4° from 27 to 31 GHz. The beam imbalance and beam to beam coupling are first reported, and are less than 0.3 dB and −32 dB, respectively. While the NF is 12.3 dB, this can be improved to 1.9 dB by the external GaAs LNA. The beam couplings of the phased array have investigated, excellent beam isolation is achieved. The passive beam distribution network, the passive phase shifter and STA of each channel contribute to the extremely low power consumption (only 40 mW) of the proposed four-beam receiver. All these made the design appropriate for large-scale space use.

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NA PENG (Graduate Student Member, IEEE) received the M.S. degree in communication and information system from Chengdu University of Information Technology, Chengdu, China, in 2017. She is currently pursuing the Ph.D. degree in information science and engineering with Southeast University, Nanjing, China.

Her current research interests include RF and millimeter-wave integrated circuits for wireless communications and phased-array systems.

PENG GU (Graduate Student Member, IEEE) received the B.Sc. degree in information science and engineering from Southeast University, Nanjing, China, in 2017, where he is currently pursuing the Ph.D. degree.

His current research interests include RF and millimeter-wave integrated circuits for wireless communications and phased-array systems.

DIXIAN ZHAO (Senior Member, IEEE) received the B.Sc. degree in microelectronics from Fudan University, Shanghai, China, in 2006, the M.Sc. degree in microelectronics from Delft University of Technology (TU Delft), The Netherlands, in 2009, and the Ph.D. degree in electrical engineering from the University of Leuven (KU Leuven), Belgium, in 2015.

From 2005 to 2007, he was with the Auto-ID Laboratory, Shanghai, where he developed the non-volatile memory for passive RFID tags. From 2008 to 2009, he was with Philips Research, Eindhoven, where he designed the 60-GHz beamforming transmitter for presence detection radar. From 2009 to 2010, he was a Research Assistant with TU Delft, working on the 94-GHz wideband receiver for imaging radar. From 2010 to 2015, he was a Research Associate with KU Leuven, where he developed several world-class 60-GHz and E-band transmitters and power amplifiers. Since April 2015, he has been with Southeast University, China, where he is currently a Full Professor. He has authored or coauthored more than 50 peer-reviewed journals and conference papers, one book, and two book chapters. His current research interests include millimeter-wave integrated circuits, transceivers and phased-array systems for 5G, satellite, radar, and wireless power transfer applications. He serves as a Technical Program Committee (TPC) Member or the Sub-Committee Chair for several conferences, including the IEEE European Solid-State Circuits Conference (ESSCIRC), IEEE Asian Solid-State Circuits Conference (A-SSCC), and IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA). He was a recipient of the Top-Talent Scholarship from TU Delft, in 2007 and 2008, the Chinese Government Award for Outstanding Students Abroad, in 2013, the IEEE Solid-State Circuits Society Predoctoral Achievement Award, in 2014, and the Innovative and Entrepreneurial Talent of Jiangsu Province, in 2016. He serves as an Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS.