IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received July 11, 2021, accepted July 22, 2021, date of publication July 26, 2021, date of current version August 13, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3100111

Development of Frequency Fixed Sliding Discrete Fourier Transform Filter Based Single-Phase Phase-Locked Loop

GUOJUN TAN, (Member, IEEE), QIWEN FU, (Graduate Student Member, IEEE), TAO XIA, AND XU ZHANG, (Graduate Student Member, IEEE)
School of Electrical and Power Engineering, China University of Mining and Technology, Xuzhou 221116, China

Corresponding author: Guojun Tan (gjtan_cumt@163.com)

This work was supported in part by the National Key Research and Development Program of China under Grant 2016YFC0600804.

ABSTRACT The single-phase phase-locked loop (PLL) is essential for the stable operation and control of single-phase grid-connected converters. However, in practical applications, the grid voltage is usually affected by harmonics and dc offset, which will cause errors in the output of the PLL. Therefore, using sliding discrete Fourier transform filter (SDFT) as a prefilter, this paper proposes an improved single-phase synchronous reference frame PLL with a fixed sampling frequency, which can accurately and quickly obtain the grid parameters under distorted grid conditions. Most importantly, the paper theoretically analyzes phase and amplitude errors generated by SDFT for the first time and a quantitative compensation method is proposed, which is straightforward to be used by a reader. Finally, the proposed PLL is compared with other PLLs through simulation and experiments. The experimental results show the effectiveness and practicability of the proposed method.

INDEX TERMS Sliding discrete fourier transform filter (SDFT), phase-locked loop (PLL), dc offset, harmonic.

I. INTRODUCTION

In recent years, single-phase grid-connected power conditioning systems such as pulse width modulation (PWM) rectifier [1], active power filters, distributed generation, uninterruptible power supplies (UPS), etc. have attracted more and more attention [2]. Therefore, obtaining the grid voltage phase accurately and quickly is the key factor to ensure the stable operation of these systems.

At present, phase-locked loop (PLL) is a widely used method to obtain grid synchronization signals. The block diagram of the single-phase PLL is shown in Fig. 1, which consists of three parts: 1) phase detector (PD), 2) loop filter (LF), 3) voltage controlled oscillator (VCO). According to the design of PD, single-phase PLLs can be divided into power-based PLLs (pPLLs) and quadrature signal generation-based PLLs (QSG-PLLs) [3].

The pPLLs generate the phase error signal V_e by multiplying the output voltage signal and the input voltage signal, which is easy to implement. However, this method causes double-frequency oscillatory errors. To solve this problem, notch filter-based PLL (NF-PLL) [4] and programmable cascaded low-pass filter-based PLL (PCLPF-PLL) [5] are proposed. But the dynamic response speed of the system is sacrificed due to the introduction of filters.

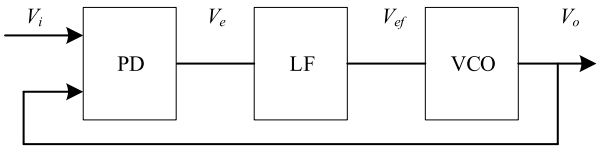

FIGURE 1. Block diagram of a typical single-phase PLL.

On the other hand, the QSG-PLL has attracted wide attention due to its effectiveness and reliability. The QSG-PLL is derived from the synchronous reference frame PLL (SRF-PLL) in the three-phase system. The key point of QSG-PLL is how to accurately and quickly generate virtual orthogonal component. There are various QSG methods such as transfer delay-based PLL (TD-PLL) [3], linear Kalman filter-based PLL (LKF-PLL) [6], inverse Park transformation-based PLL (IPT-PLL), Hilbert transformer-based PLL (HT-PLL) [7],

The associate editor coordinating the review of this manuscript and approving it for publication was Shihong Ding.

second-order generalized integrator-based PLL (SOGI-PLL) [8], all pass filter-based PLL (APF-PLL) [9], etc. The above methods work well under ideal conditions but these PLLs will suffer a large phase error under grid voltage disturbances such as harmonics, dc offset. Therefore, they will not meet the requirements of the grid-connected system.

In recent years, many advanced PLLs have been proposed. [10] proposes a PLL based on the differential elements (DE-PLL). It generates orthogonal component through differential method and has a fast response speed. When the grid frequency changes, the out of the TD-PLL will contain a double frequency term, which will cause offset errors. Therefore, [11] proposes the nonfrequency-dependent TD-PLL (NTD-PLL) to correct the offset error of the PLL output, but it still cannot remove the double-frequency oscillation term. The extended Kalman filter-based PLL is complicated to design and requires constant adjustment of parameters, which is difficult to achieve in practice. [12] proposes an advanced design version of Kalman filter-based PLL, which has a simple structure and uses a fixed gain. The performance of traditional SOGI-PLL algorithm will be seriously affected when the input signal contains dc offset. Therefore, [13] proposes *dq*-frame delayed signal cancellation based PLL ($dq\text{DSC}_2$-PLL). However, it has a low response speed and a large estimated phase error when the grid distortion is serious. [14] proposes a method for detecting frequency and phase through an adaptive sliding mode observer, which has a simple structure and high real-time performance. However, this method does not perform well when the grid input signal is distorted. A novel PLL based on a circular limit cycle oscillator (CLO) is proposed in [15], but it cannot suppress the influence of harmonics and dc offset on the PLL. The improved scheme of this PLL can be found in [16]. [17] proposes a single-phase PLL by using multiple complex band-pass filters as pre-filters, which shows good performance in the case of distorted grid conditions. However, when the sampling frequency is low, the estimated frequency will produce errors [18]. Recently, [19], [20] proposes an advanced frequency-fixed SOGI-based PLL (FFSOGI-PLL) to improve dc-offset rejection ability of the traditional SOGI-PLL. By adding a fractional gain parameter, [21] proposes an adaptive FFSOGI-PLL, to improve the anti-frequency interference ability of FFSOGI-PLL. However, the above improved versions of the SOGI-PLL cannot obtain the estimated phase without steady error under harmonic interference. The multiple SOGIs-based PLL (MSOGI-PLL) effectively solves this problem, but the system response time requires at least two fundamental periods [22].

Discrete Fourier transform (DFT) is popular in power systems for signal spectrum analysis and harmonic detection. Recently, a sliding discrete Fourier transform filter (SDFT) is proposed. In [24], a method for acquiring the synchronous fundamental signal based on SDFT is proposed, which can suppress the dc offset and harmonic. However, the estimated phase will produce large deviations in the case of asynchronous sampling.

In this case, [25] presents a method, which multiplies the quadrature signal obtained from the SDFT and the input signal to produce the phase error signal, V_e. In addition, it realizes the frequency adaptation by feeding back the estimated frequency to a numerically controlled oscillator (NCO). However, all the above methods need to change the sampling frequency. For the single-phase grid-connected systems, each subsystem such as current controller and grid synchronization control must adopt a consistent sampling frequency. Therefore, the method of implementing the SDFT-based PLL frequency adaptation by feedback of the estimated frequency is not suitable for these applications.

An improved SDFT-based SRF-PLL with fixed sampling frequency is proposed in this paper. By using SDFT as the prefilter, the pure fundamental component of the input voltage can be accurately obtained when the input voltage signal contains harmonics and dc offset. Then, the phase can be detected by SRF-PLL without generating fictitious quadrature component and introducing additional filters. Most importantly, this paper analyzes the phase and amplitude offset errors generated by SDFT during asynchronous sampling for the first time, and proposes a quantitative compensation algorithm based on this analysis to improve the performance of the PLL under frequency changes. Finally, through experiment and simulation comparison with the other two PLL methods, the superiority of the proposed algorithm is proved.

Our contribution is as follows.

1. In the case of asynchronous sampling, this article theoretically analyzes the phase and amplitude errors generated by SDFT for the first time, and proposes a compensation algorithm that is easy for readers to follow.

2. A single-phase phase-locked loop based on a fixed frequency sliding discrete Fourier transform filter is proposed. Even in the case of grid distortion, the estimated phase can be obtained accurately and quickly.

3. In this paper, by improving the traditional SRF-PLL, the effort of generating quadrature component is eliminated. In addition, the double-frequency term in the u_q is eliminated by the feedback decoupling method, which avoids using additional filters and improves the dynamic performance.

The rest of the paper is organized as follows. Section I introduces the SDFT algorithm in detail. In Section II, the output error of SDFT during asynchronous sampling is analyzed in depth and the compensation method is proposed. Section III presents the proposed PLL based on fixed frequency SDFT. Simulation and experimental verification are carried out in Section IV. Finally, Section V concludes this paper.

II. SDFT

DFT is widely used in signal processing, harmonic analysis and other occasions, but the traditional DFT algorithm is computationally intensive. This paper uses the SDFT method as the prefilter of the input voltage signal.

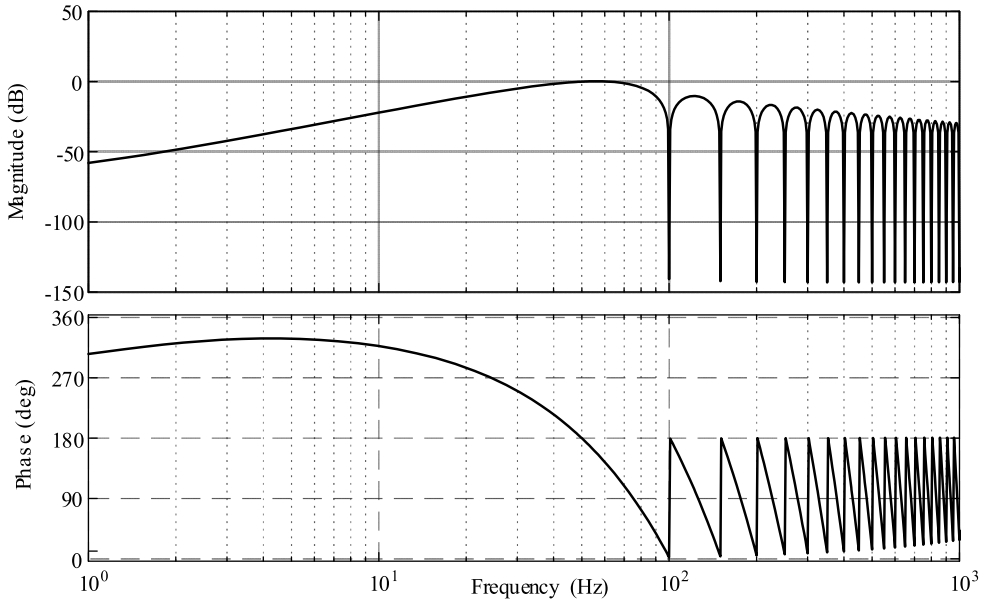

FIGURE 2. Frequency response diagram of the SDFT, $N = 128$; $T_0 = 20$ms.

Assuming that the time domain signal is $x(t)$, $x\{k\}$ is generated by sampling at the rate of N/T_w (N is the number of samples, T_w is the time window for the DFT, usually $T_w = T_0$, T_0 is the fundamental period of the input voltage). The mth harmonic $X_m(k\text{-}1)$ at the k-1 moment is expressed as follows.

$$X_m(k-1) = \sum_{n=k-N}^{k-1} x_n e^{\frac{-j2\pi(k-1)m}{N}} \tag{1}$$

One time step later, the mth harmonic $X_m(k)$ at the k moment can be obtained as follows.

$$X_m(k) = \sum_{n=k-N+1}^{k} x_n e^{\frac{-j2\pi(k-1)m}{N}} \tag{2}$$

Subtracting (1) from (2) yields

$$X_m(k) = X_m(k-1) + [x_k - x_{k-N}]\, e^{\frac{-j2\pi(k-1)m}{N}} \tag{3}$$

We can be obtained (4) by inverse DFT transformation.

$$x_m(k) = G_m X_m(k)\, e^{\frac{j2\pi(k-1)m}{N}} \tag{4}$$

where

$$G_m = \begin{cases} N^{-1} & m = 0,\ \dfrac{N}{2} \\ 2N^{-1} & otherwise \end{cases} \tag{5}$$

From (3) and (4), we can obtain the z-domain transfer function of SDFT.

$$H(z) = \frac{1}{N}\left[\frac{1-z^{-N}}{1-e^{\frac{j2\pi}{N}}z^{-1}} + \frac{1-z^{-N}}{1-e^{-\frac{j2\pi}{N}}z^{-1}}\right] \tag{6}$$

where

$$1 - z^{-N} = \prod_{k=0}^{N-1}\left(1 - e^{\frac{j2\pi k}{N}}z^{-1}\right) \tag{7}$$

It can be seen from (6) and (7) that the two poles cancel with the zeros corresponding to the fundamental frequency.

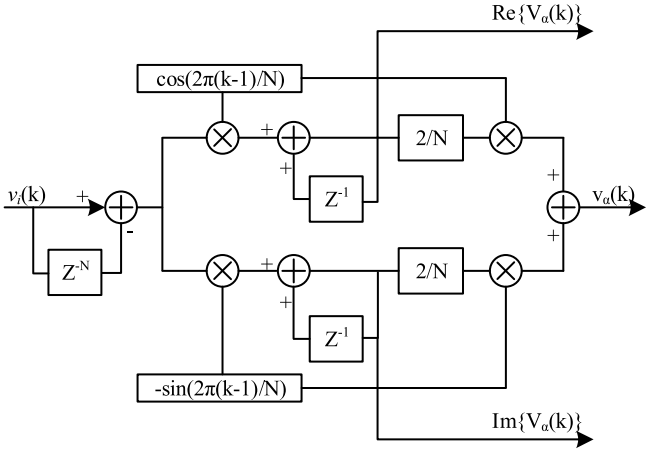

FIGURE 3. Block diagram for the SDFT.

Thus, the gain of the SDFT transfer function at other integer harmonic frequencies (including dc) is $-\infty$ and the gain at the fundamental frequency is 0 dB. This conclusion can also be proved by the frequency response diagram of the SDFT shown in Fig. 2.

Finally, as shown in Fig. 3, by setting m to 1, the pure fundamental component of the input voltage signal can be obtained by (4). In addition, the amplitude of the fundamental voltage can be calculated by $V_\alpha(k)$:

$$A_1 = \frac{2}{N}\sqrt{[\mathrm{Re}\{V_\alpha(k)\}]^2 + [\mathrm{Im}\{V_\alpha(k)\}]^2} \tag{8}$$

Since the pole of the SDFT is located on the unit circle in the z-domain, the system is in a critical steady state. In [27], the stability of the system is improved by adding the stability factor $r < 1$ and r is chosen to be 0.99999 in this paper.

III. FREQUECNY FIXED SDFT

When the frequency of the input signal changes, the SDFT time window length is inconsistent with input signal period, that is, $T_w \neq T_0$. At this time, the output of the SDFT and the input signal obviously have a large phase and amplitude deviation. Therefore, in the case of sudden changes in frequency, quantitative compensation must be made.

The time domain signal $x[k]$ obtained in the case of asynchronous sampling is shown in (9).

$$x[k] = Acos(\frac{2\pi kT_w}{NT_0} + \varphi) \tag{9}$$

where φ is the initial phase for the time sequence. We can get (10) after a sampling period

$$X_{m=1} = A\sum_{k=0}^{N-1} cos(\frac{2\pi kT_w}{NT_0} + \varphi)e^{\frac{-j2\pi k}{N}} \tag{10}$$

which is equal to

$$X_{m=1} = \frac{A}{2}\sum_{k=0}^{N-1}\begin{pmatrix} e^{j\left(\frac{2\pi}{T_0}\frac{kT_w}{N}+\varphi-\frac{2\pi k}{N}\right)} \\ +e^{-j(\frac{2\pi}{T_0}\frac{kT_w}{N}+\varphi+\frac{2\pi k}{N})} \end{pmatrix} \tag{11}$$

solving (11) gives

$$X_{m=1} = \frac{A}{2}\left(\frac{e^{j\varphi\left[1-\exp\left(\frac{j2\pi T_w}{T_0}\right)\right]}}{1-e^{j\frac{2\pi}{N}\left(\frac{T_w}{T_0}-1\right)}} + \frac{e^{-j\varphi\left[1-\exp\left(-\frac{j2\pi T_w}{T_0}\right)\right]}}{1-e^{-j\frac{2\pi}{N}\left(\frac{T_w}{T_0}+1\right)}}\right) \tag{12}$$

For the sake of analysis, define λ as follows

$$\lambda = 2\pi(T_w - T_0)/T_0 \tag{13}$$

Therefore, (12) can be further written as

$$X_{m=1} = \frac{A}{2}\left[\frac{e^{j\varphi}\left[1-e^{j\lambda}\right]}{1-e^{j\frac{\lambda}{N}}} + \frac{e^{-j\varphi}\left[1-e^{-j\lambda}\right]}{1-e^{-j(\frac{\lambda}{N}+\frac{4\pi}{N})}}\right] \tag{14}$$

Simplify (14), we can get (15), as shown at the bottom of the page.

Considering that λ is actually small, the phase after SDFT can be expressed as

$$\theta = \tan^{-1}\left(\frac{Im_{X_m(k=N)}}{Re_{X_m(k=N)}}\right) = \varphi + \frac{\lambda}{2} = \varphi + \pi(\frac{T_w}{T_0} - 1) \tag{16}$$

By further simplification, we can obtain (17)

$$\varphi = \theta + \frac{\pi}{f}\Delta f \tag{17}$$

Here, f_0 is nominal grid frequency, f is the actual grid frequency and $\Delta f = f - f_0$. Combining (8) and (15) we can get

$$A_1 = \frac{A}{N}sin\left(\frac{\lambda}{2}\right)\frac{\sin(2\pi/N)}{(\sin(\lambda/2N)\sin(\lambda/2N + 2\pi/N))} \tag{18}$$

By further simplification we can obtain (19)

$$A_1 = \frac{A}{N}tan\left(\frac{2\pi}{N}\right)\frac{sin\left(\frac{\pi}{f}\Delta f\right)}{sin\left(\frac{\pi}{Nf}\Delta f\right)} \tag{19}$$

(17) and (19) show that the phase and amplitude errors are both functions of frequency deviation Δf under grid frequency drift. The following variables are defined to compensate the SDFT output error during asynchronous sampling.

$$K = \frac{A}{A_1}; \quad \theta_d = \varphi - \hat{\theta} \tag{20}$$

In practical applications, the grid voltage frequency fluctuations are in a very small range. Therefore, in this paper, the value of f in (17) and (19) takes the nominal frequency of the grid (50Hz). Due to the fixed sampling frequency, N is a fixed value, we can get

$$K = \frac{Nsin\,(0.000491(\Delta f))}{tan(2\pi/N)sin\,(0.062832(\Delta f))} \tag{21}$$

$$\theta_d = 0.062832\,(\Delta f) \tag{22}$$

When the grid frequency changes, the frequency of the SDFT output is equal to the actual grid frequency [25], [26].

By the feedback decoupling network proposed in this paper we can obtain accurate and instantaneous estimated frequency ($f = \hat{\omega}/2\pi$), i.e., the actual grid frequency, through the PLL without additional filters. Then Δf is calculated.

Finally, a phase compensator is used in the output of the SDFT-PLL, which is rather straightforward to implement and does not introduce additional control loops.

$$\theta^+ = \hat{\theta} + \theta_d; \quad A = KA_1 \tag{23}$$

IV. PROPOSED SRF-PLL BASED ON SDFT

A. PRINCIPLE OF THE PROPOSED SRF-PLL

The improved SRF-PLL algorithm proposed in this paper is shown in Fig. 4. Through SDFT module, the fundamental signal v_α synchronized with the input voltage v_i is obtained from the distortion grid. In this study, for the convenience of system design, the β-axis signal is directly set to zero.

$$X_{m=1} = \frac{A}{2}\sin\left(\frac{\lambda}{2}\right) \times \left[\frac{jsin\left(\frac{2\pi}{N}\right)sin\left(\varphi+\frac{\lambda}{2}\right) + cos\left(\frac{2\pi}{N}\right)sin\left(\varphi+\frac{\lambda}{2}\right) - \sin\left(\varphi+\frac{\lambda}{2}-\frac{\lambda}{N}-\frac{2\pi}{N}\right)}{\sin\left(\frac{\lambda}{2N}\right)\sin\left(\frac{\lambda}{2N}+\frac{2\pi}{N}\right)}\right] \tag{15}$$

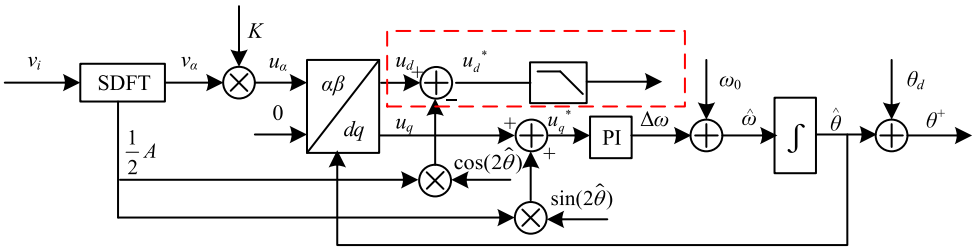

FIGURE 4. Schematic diagram of the proposed improved SRF-PLL.

Besides, the double-frequency term in the u_q is limited by the feedback decoupling method. No additional filters are used and the dynamic performance of the PLL is improved.

The input single-phase voltage signal v_i is shown in (24).

$$v_i(t) = A\cos(\omega t) + \sum_{h=2}^{n} A_h \cos(\omega_h t) \tag{24}$$

where A_h, ω_h are the amplitude and angular frequency of h-order voltage component, respectively. When v_i passed into the SDFT, we can obtain the fundamental component, v_α.

$$v_\alpha(t) = A_\alpha \cos(\omega t) \tag{25}$$

The quadrature signals required for the $\alpha\beta/dq$ coordinate transformation are shown in (26) and (27).

$$u_\alpha = A\cos(\omega t) = \frac{1}{2}[A\cos(\omega t) + A\cos(-\omega t)] \tag{26}$$

$$u_\beta = 0 = \frac{1}{2}[A\sin(\omega t) + A\sin(-\omega t)] \tag{27}$$

Then the transformed u_d, u_q can be expressed as

$$\begin{pmatrix} u_d \\ u_q \end{pmatrix} = \frac{1}{2}A\begin{pmatrix} \cos(\omega t - \hat{\theta}) \\ \sin(\omega t - \hat{\theta}) \end{pmatrix} + \frac{1}{2}A\begin{pmatrix} \cos\left(-\omega t - \hat{\theta}\right) \\ \sin\left(-\omega t - \hat{\theta}\right) \end{pmatrix} \tag{28}$$

where, $\hat{\theta}$ is the estimated phase, By further simplification, we can get (29).

$$\begin{aligned} \begin{pmatrix} u_d \\ u_q \end{pmatrix} &\approx \frac{1}{2}A\begin{pmatrix} 1 \\ \omega t - \hat{\theta} \end{pmatrix} + \frac{1}{2}A\begin{pmatrix} \cos(-2\omega t) \\ \sin(-2\omega t) \end{pmatrix} \\ &= \begin{pmatrix} u_d^* \\ u_q^* \end{pmatrix} + \frac{1}{2}A\begin{pmatrix} \cos(-2\omega t) \\ \sin(-2\omega t) \end{pmatrix} \end{aligned} \tag{29}$$

When the system reaches stability, $\hat{\theta} = \omega t$, we can know from (29) that the amplitude information of the fundamental voltage component can be obtained from $u_d{}^*$, and its phase error information can be obtained from $u_q{}^*$. As shown in the red line box in Fig. 2, a low-pass filter is often needed to obtain the amplitude information, which will greatly reduce the dynamic response of the system. In this paper, the amplitude A is obtained by (8).

B. TUNING PROCEDURES

When the system is stable, it can be seen from (14) that $u_q{}^* = A/2(\omega t - \hat{\theta}) = 1/2A\Delta\theta$. According to Fig. 2, the phase angle small signal model is established and shown in Fig. 5. Based on the linear model, we can obtain the system closed-loop transfer function.

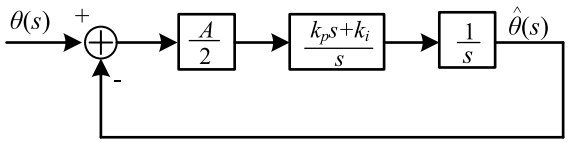

FIGURE 5. Linearized model of the proposed PLL.

$$f(s) = \frac{\hat{\theta}(s)}{\theta(s)} = \frac{Mk_p s + Mk_i}{s^2 + Mk_p s + Mk_i} \tag{30}$$

Here, $M = A/2$. (30) shows a typical second-order system with a damping ratio of $\xi = \frac{k_p}{2}\sqrt{\frac{M}{k_i}}$ and an undamped natural frequency of $\omega_n = \sqrt{Mk_i}$. When designing the system, the damping coefficient ξ is usually designed to be $\sqrt{2}/2$, and the undamped natural frequency ω_n is designed to be 20π rad/s. In this way, the system response speed and anti-high frequency interference can be optimized.

V. SIMULATION AND EXPERIMENTAL VALIDATION

A. SIMULATION RESULTS

In [8] and [28], The SOGI-PLL and the adaptive MAF-PLL (AMAF-PLL) are widely used methods to achieve grid synchronization and they show satisfactory performance. In order to compare the performance of the proposed SDFT-based SRF-PLL, SOGI-PLL and AMAF-PLL, we have tested these three PLLs under various conditions in the Matlab/Simulink environment. For a fair comparison, the three PLL algorithms use the same design parameters.

To compare the transient response of the proposed method SOGI-PLL, and AMAF-PLL for amplitude change, a voltage sag of 0.3 p.u. is considered. From Fig. 6, it can be observed that the settling time for the proposed SDFT-based PLL is one cycle. The settling time for SOGI-PLL and AMAF-PLL are almost three cycles and two cycles, separately.

Next, Fig. 7 shows the results of the estimated frequency and the estimation phase error when the grid is subjected to 40° phase-angle jump. We can know that the proposed method has the fastest setting time (one cycle).

In Fig. 8, the simulation results of the estimated frequency and phase estimation error when the grid voltage frequency

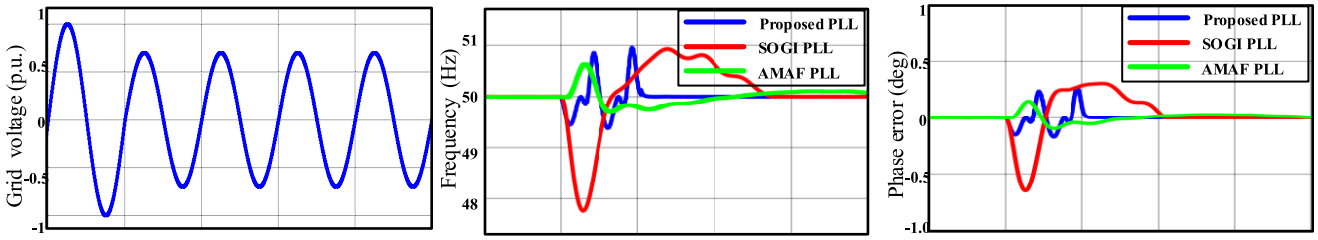

FIGURE 6. Simulation results for a voltage sag. Time scale: 20ms/div.

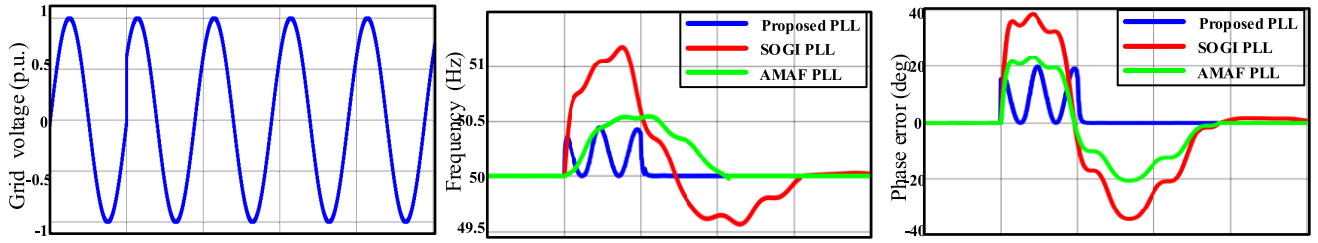

FIGURE 7. Simulation results for a phase step. Time scale: 20ms/div.

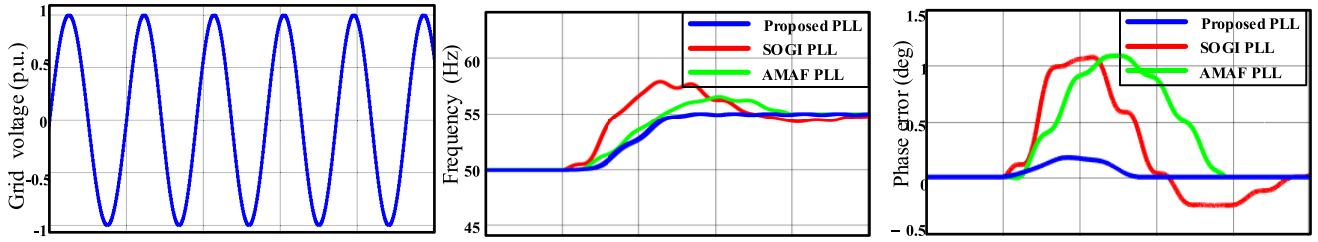

FIGURE 8. Simulation results for a frequency change. Time scale: 20ms/div.

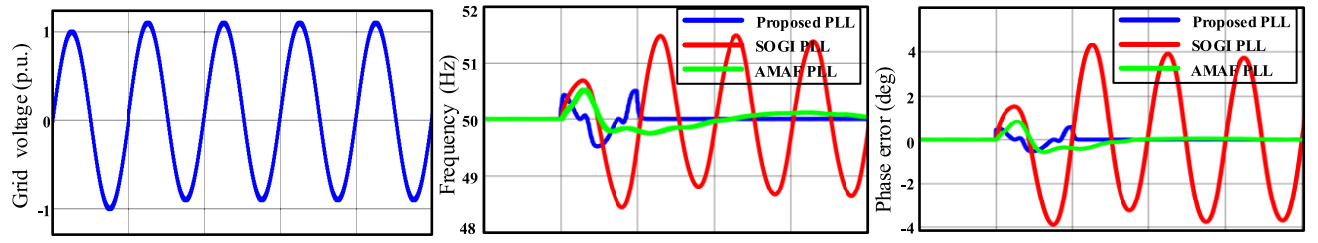

FIGURE 9. Simulation results when grid voltage is distorted (10% dc offset). Time scale: 20ms/div.

is increased by 5 Hz can be obtained. The proposed method has the fastest setting time, 0.024 s. Because the SOGI-PLL and AMAF-PLL adopt frequency feedback, they also have the feature of frequency adaption. Note that without any overshoot, the frequency of the proposed method converges to its new steady-state. In addition, it can be seen that the output frequency of SOGI-PLL will fluctuate.

Fig. 9 shows the waveform for the input voltage when it is distorted with 10% dc offset. We can know that the proposed method can reach a new steady in one cycle, and the AMAF needs two cycles to reach steady state. But the SOGI-PLL will generate a large oscillation.

In the case where the grid is distorted by harmonics (10% third harmonics and 10% fifth harmonics), the simulation results are shown in Fig. 10. The estimated frequency of SOGI-PLL and AMAF-PLL show noticeable oscillations. From Figs. 9 and 10, we can find that the proposed PLL can reach a new steady state in one cycle, and is not affected by harmonics and dc offset.

In order to compare the noise immunity of the PLLs, it is assumed that the grid voltage is polluted by a zero-mean white Gaussian noise with variance $\sigma^2 = 0.05$. The signal-to-noise ratio (SNR) in the PLL input is $SNR = 10\log\left(1/2\sigma^2\right) = 10$ dB. The relevant specific noise selection and processing

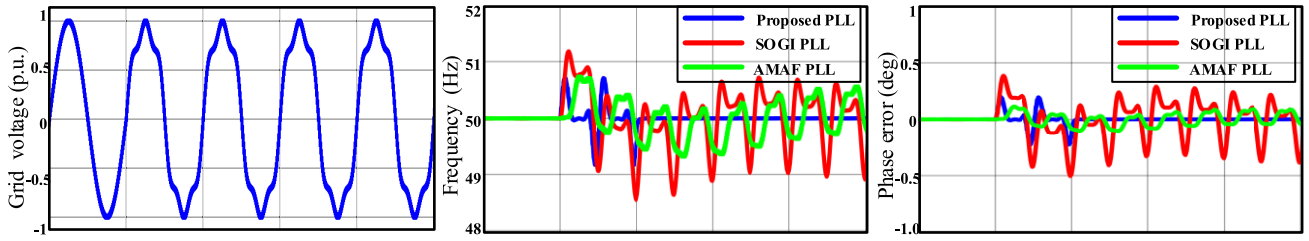

FIGURE 10. Simulation results when grid voltage is distorted (10% third, 10% fifth harmonics). Time scale: 20ms/div.

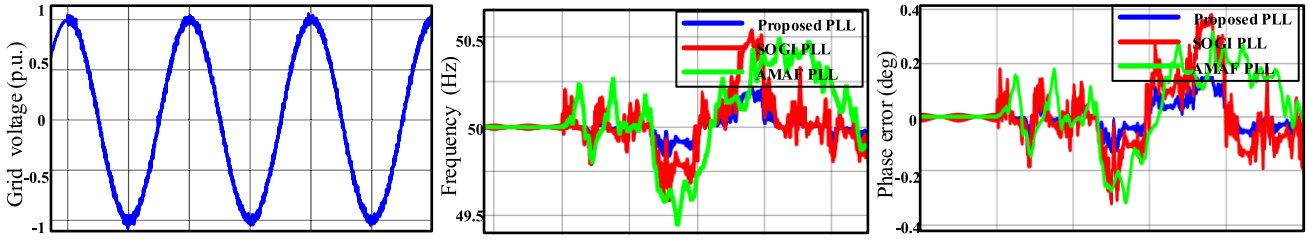

FIGURE 11. Simulation results when the input signal is polluted by a zero mean white gaussian noise. Time scale: 20ms/div.

can be found in [18]. The simulation results are shown in Fig. 11. It can be seen that the estimated frequency of AMAF-PLL and SOGI-PLL will produce a large oscillation. The proposed method has the smallest steady-state oscillation of 0.23 Hz.

B. EXPERIMENTAL RESULTS

In this paper, we established an experimental platform based on the floating-point digital signal processor TMS320C28346, and the desired input voltage is generated by a programmable AC power supply. In the experiment, the sampling frequency is 6.4 kHz, and the nominal grid frequency is 50 Hz. The experimental results of SOGI-PLL and AMAF-PLL are also presented here.

1) Test A: The input grid voltage is reduced by 0.3 p.u.
2) Test B: The grid voltage is increased by 5 Hz.
3) Test C: A 40° phase jump occurs in the grid voltage.
4) Test D: The grid voltage is polluted with 10% third harmonics, 10% fifth harmonics and 10% dc offset.

Fig. 12 shows the experimental results of the proposed PLL in Test A. From the figure, we can know that the estimated amplitude can reach a new steady state in a short time (about one fundamental period) without overshoot in the adjustment process. In addition, the estimated frequency is also stabilized in one cycle with a deviation of 0.8 Hz.

The experimental results under frequency drifts can be observed in Fig. 13. The estimated frequency converges to the new steady state without any overshoot. It is verified that the proposed feedback decoupling network and compensation algorithm effectively improve the system response speed.

Next, the grid voltage has a 40° phase angle jump in Fig. 14. The estimated frequency of the proposed PLL can

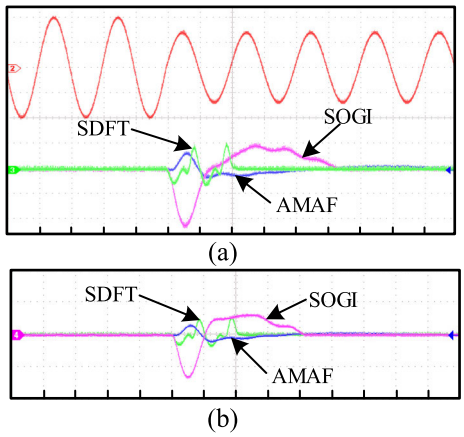

FIGURE 12. Experimental results for a voltage sag. (a) Frequency estimation (1 Hz/div). the input voltage (0.5 p.u./div). (b) Estimation error of phase angle (0.5 deg/div). Time scale: 10ms/div.

be stabilized within 20 ms. We can know that the proposed method has the fastest setting time.

The experimental results in the case where the grid voltage is polluted by harmonics and dc offset are shown in Fig. 15. The proposed PLL has the fastest dynamic response, 20 ms. But the SOGI-PLL and AMAF-PLL will generate the large oscillation.

In summary, compared with SOGI-PLL and AMAF-PLL, the proposed PLL shows the best response, especially when the input signal is distorted due to harmonics and dc offset.

C. PERFORMANCE COMPARISON

In order to further verify the superiority of the proposed method, it is compared with several other advanced PLLs. The comparison results are shown in Table 1, where

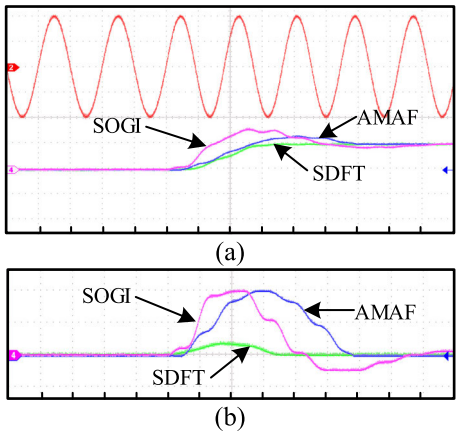

FIGURE 13. Experimental results for a frequency step. (a) Frequency estimation (5 Hz/div). the input voltage (0.5 p.u./div). (b) Estimation error of phase angle (0.5 deg/div). Time scale: 10ms/div.

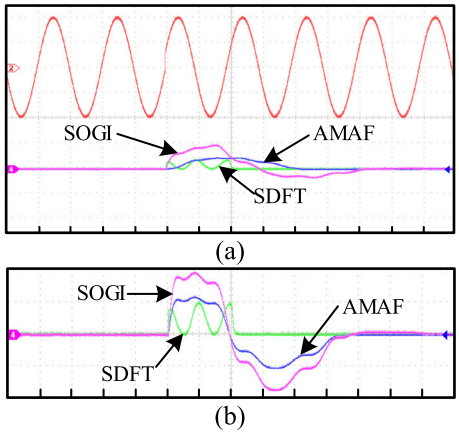

FIGURE 14. Experimental results for a phase step. (a) Frequency estimation (1 Hz/div). the input voltage (0.5 p.u./div). (b) Estimation error of phase angle (20 deg/div). Time scale: 10ms/div.

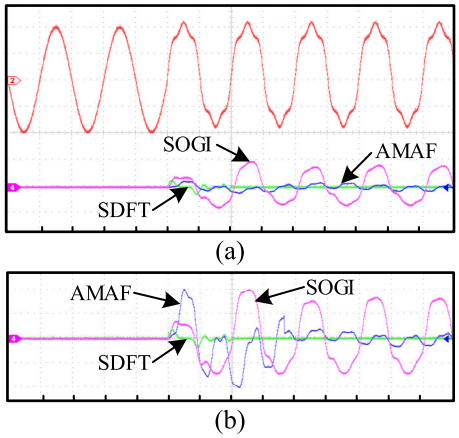

FIGURE 15. Experimental results when the input voltage is polluted. (a) Frequency estimation (1 Hz/div). the input voltage (0.5 p.u./div). (b) Estimation error of phase angle (2 deg/div). Time scale: 10ms/div.

f_m represents the frequency peak error, θ_m represents the phase peak error and t_s is the settling time. The experimental data of DE-PLL and the adaptive cascaded delayed signal cancelation operators-based PLL (CDSC-PLL) come from the literature [8], [10], and [23], respectively.

TABLE 1. Performance comparison.

Disturbance	AMAF-PLL	DE-PLL	Adaptive CDSC-PLL	Proposed -PLL
Voltage sag of 0.3pu				
t_s (cycle)	2.5	3.5	2	1
Frequency step of +5Hz				
t_s (cycle)	2.5	1.8	2	1.5
f_m	1.5 Hz	0.05 Hz	0	0
θ_m	1.01°	14.3°	5.8°	0.14°
Phase-angle jump of 40°				
t_s (cycle)	2.1	3.4	2.4	1
f_m	0.51 Hz	0.8 Hz	6Hz	0.46 Hz
θ_m	25.0°	58°	40°	21.6°
Harmonics and dc-offset				
t_s (cycle)	–	1.5	2	1

It can be seen from Table 1 that the settling time of the proposed PLL is minimum under all test conditions. When the phase of the power grid changes, compared with other PLLs, the frequency and phase overshoot of the proposed method is smaller. Therefore, the proposed PLL effectively improves the dynamic response speed of the system and is more suitable for the synchronization control of grid-connected converters.

VI. CONCLUSION

This paper presents an improved SRF-PLL based on SDFT with a fixed sampling frequency. By using SDFT as a pre-filter, we can get the fundamental voltage component from the grid where harmonics and dc offset exist. But when the frequency changes, the output of the SDFT will produce errors. For the first time, this paper analyzes the errors and proposes a quantitative compensation method. In addition, by improving the traditional SRF-PLL, the proposed algorithm uses a feedback decoupling network, which can greatly improve the response speed of the PLL.

Finally, through simulation and experimental results, the proposed algorithm is compared with several other PLLs. The results show that the proposed PLL has the fastest dynamic response and the best performance, especially when the input signal is polluted by harmonics and dc offset. Therefore, in a single-phase grid-connected converter, the proposed algorithm will be a good grid synchronization scheme.

REFERENCES

[1] L. Hadjidemetriou, E. Kyriakides, and F. Blaabjerg, "A robust synchronization to enhance the power quality of renewable energy systems," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 4858–4868, Aug. 2015.
[2] R. M. S. Filho, P. F. Seixas, P. C. Cortizo, L. A. B. Torres, and A. F. Souza, "Comparison of three single-phase PLL algorithms for UPS applications," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2923–2932, Aug. 2008.
[3] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Single-phase PLLs: A review of recent advances," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9013–9030, Dec. 2017.

[4] F. D. Freijedo, J. Doval-Gandoy, O. Lopez, and J. Cabaleiro, "Robust phase locked loops optimized for DSP implementation in power quality applications," in *Proc. 34th Annu. Conf. IEEE Ind. Electron.*, Orlando, FL, USA, Nov. 2008, pp. 3052–3057.
[5] A. M. Mnider, D. J. Atkinson, M. Dahidah, Y. B. Zbede, and M. Armstrong, "A programmable cascaded LPF based PLL scheme for single-phase grid-connected inverters," in *Proc. 7th Int. Renew. Energy Congr. (IREC)*, Mar. 2016, pp. 1–6.
[6] S. Reza, M. Ciobotaru, and V. G. Agelidis, "Accurate estimation of single-phase grid voltage fundamental amplitude and frequency by using a frequency adaptive linear Kalman filter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 4, pp. 1226–1235, Dec. 2016.
[7] P. Hao, W. Zanji, and C. Jianye, "A measuring method of the single-phase AC frequency, phase, and reactive power based on the Hilbert filtering," *IEEE Trans. Instrum. Meas.*, vol. 56, no. 3, pp. 918–923, Jun. 2007.
[8] Y. Han, M. Luo, X. Zhao, J. M. Guerrero, and L. Xu, "Comparative performance evaluation of orthogonal-signal-generators-based single-phase PLL algorithms—A survey," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3932–3944, May 2016.
[9] S. Golestan, J. M. Guerrero, J. C. Vasquez, A. M. Abusorrah, and Y. Al-Turki, "All-pass-filter-based PLL systems: Linear modeling, analysis, and comparative evaluation," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3558–3572, Apr. 2020.
[10] Q. Guan, Y. Zhang, Y. Kang, and J. M. Guerrero, "Single-phase phase-locked loop based on derivative elements," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4411–4420, Jun. 2017.
[11] S. Golestan, J. M. Guerrero, A. Vidal, A. G. Yepes, J. Doval-Gandoy, and F. D. Freijedo, "Small-signal modeling, stability analysis and design optimization of single-phase delay-based PLLs," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3517–3527, May 2016.
[12] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Steady-state linear Kalman filter-based PLLs for power applications: A second look," *IEEE Trans. Ind. Electron.*, vol. 65, no. 12, pp. 9795–9800, Dec. 2018.
[13] M. Xie, H. Wen, C. Zhu, and Y. Yang, "DC offset rejection improvement in single-phase SOGI-PLL algorithms: Methods review and experimental evaluation," *IEEE Access*, vol. 5, pp. 12810–12819, 2017.
[14] H. Ahmed, S.-A. Amamra, and I. Salgado, "Fast estimation of phase and frequency for single-phase grid signal," *IEEE Trans. Ind. Electron.*, vol. 66, no. 8, pp. 6408–6411, Aug. 2019.
[15] H. Ahmed, S.-A. Amamra, and M. Bierhoff, "Frequency-locked loop-based estimation of single-phase grid voltage parameters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 11, pp. 8856–8859, Nov. 2019.
[16] M. L. Pay and H. Ahmed, "Modeling and tuning of circular limit cycle oscillator fll with preloop filter," *IEEE Trans. Ind. Electron.*, vol. 66, no. 12, pp. 9632–9635, Dec. 2019.
[17] K. Liu, W. Cao, J. Zhao, and J. You, "Unified digital phase-locked loop with multiple complex resonators for both single- and three-phase grid synchronization," *IEEE Access*, vol. 5, pp. 24810–24818, 2017.
[18] S. Golestan, M. Ramezani, J. M. Guerrero, F. D. Freijedo, and M. Monfared, "Moving average filter based phase-locked loops: Performance analysis and design guidelines," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2750–2763, Jun. 2014.
[19] F. Xiao, L. Dong, L. Li, and X. Liao, "A frequency-fixed SOGI-based PLL for single-phase grid-connected converters," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1713–1719, Mar. 2017.
[20] S. Golestan, S. Y. Mousazadeh, J. M. Guerrero, and J. C. Vasquez, "A critical examination of frequency-fixed second-order generalized integrator-based phase-locked loops," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6666–6672, Sep. 2017.
[21] M. A. Akhtar and S. Saha, "An adaptive frequency-fixed second-order generalized integrator-quadrature signal generator using fractional-order conformal mapping based approach," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5548–5552, Jun. 2020.
[22] P. Rodriguez, A. Luna, I. Candela, R. Mujal, R. Teodorescu, and F. Blaabjerg, "Multiresonant frequency-locked loop for grid synchronization of power converters under distorted grid conditions," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 127–138, Jan. 2011.
[23] S. Golestan, J. M. Guerrero, J. C. Vasquez, A. M. Abusorrah, and Y. Al-Turki, "Advanced single-phase DSC-based PLLs," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3226–3238, Apr. 2019.
[24] B. P. McGrath, D. G. Holmes, and J. J. H. Galloway, "Power converter line synchronization using a discrete Fourier transform (DFT) based on a variable sample rate," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 877–884, Jul. 2005.
[25] P. Sumathi and P. A. Janakiraman, "Phase locking scheme based on look-up-table-assisted sliding discrete Fourier transform for low-frequency power and acoustic signals," *IET Circuits, Devices Syst.*, vol. 5, no. 6, pp. 494–504, Nov. 2011.
[26] H. Liu, Y. Sun, H. Hu, and Y. Xing, "A new single-phase PLL based on discrete Fourier transform," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2015, pp. 521–526.
[27] C. Subramanian and R. Kanagaraj, "Single-phase grid voltage attributes tracking for the control of grid power converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 4, pp. 1041–1048, Dec. 2014.
[28] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "A nonadaptive window-based PLL for single-phase applications," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 24–31, Jan. 2018.

GUOJUN TAN (Member, IEEE) was born in Zunyi, Guizhou, China, in 1962. He received the Ph.D. degree in motor driver and its automation from the China University of Mining and Technology, Xuzhou, China, in 1992. Since 2000, he has been a Professor with the School of Information and Electrical Engineering, China University of Mining and Technology, where he has been the Chief Professor with the National Key Discipline on Power Electronics and Motor Driver, since 2003. His main research interests include electrical drive, intelligent algorithm, and system optimization.

QIWEN FU (Graduate Student Member, IEEE) was born in Chongqing, China, in 1995. She received the B.S. degree in electrical engineering from the China University of Mining and Technology, Xuzhou, China, in 2017, where she is currently pursuing the M.S. degree in electrical engineering with the School of Electrical and Power Engineering. Her current research interests include reliability in power electronics and systems, including reliable assessment and multi-physics modeling of power electronic devices and converters.

TAO XIA was born in Gansu, China. He received the B.S. degree in electrical engineering and automation from Jilin University, Jilin, China, in 2014. He is currently pursuing the M.S. degree in electrical engineering with the School of Electrical and Power Engineering, China University of Mining and Technology. His research interests include grid synchronization technology and power converter control.

XU ZHANG (Graduate Student Member, IEEE) was born in Liaoning, China, in 1990. He received the B.S. and M.S degrees in electrical engineering and automation from the China University of Mining and Technology, Xuzhou, China, in 2014 and 2017, respectively, where he is currently pursuing the Ph.D. degree in electrical engineering with the School of Electrical and Power Engineering. His main research interests include power electronics, multilevel converter, data drive control, intelligent algorithm, and system optimization.