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A Four-Phase Interleaved Buck-Boost Converter With Changed Load Connection for the Fuel Cell Activation

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ABSTRACT When the fuel cell (FC) is being activated before used in industrial applications, a power conditioner is needed to interface the FC with the load. Due to low current ripples, high output power, and simple structure, the multi-phase interleaved non-isolated DC-DC converter is most suitable for the power conditioner. This paper proposed, analyzed and designed a four-phase interleaved buck-boost converter with changed load connection (CLC-FIBC) for the FC activation with characteristics as simple structure, wide input current, high current, and low current ripples. The operating principle and mathematical model of the CLC-FIBC were firstly analyzed, derived and presented, and then mathematical equations of transistor voltage stress and inductor current ripple are derived respectively. Besides, this CLC-FIBC was compared with several DC-DC converters to prove the superiority. The simulation and experimental prototype was built to validate the theoretical analysis after presenting some design considerations. Simulation and experimental results show that the CLC-FIBC has characteristics of both step up/down function, high power, wide input current range, and low current ripples.

INDEX TERMS Multiphase interleaved, buck-boost converter, changed load connection, fuel cell.

I. INTRODUCTION

The fuel cell (FC) is usually used in microgrid, fuel cell vehicles (FCVs), and aerospace [1]–[4]. Before being officially put into use, the FC must be activated to release more performance. However the FC has the soft volt-ampere characteristic, which means that the output voltage will decrease with the increase of the load current. In order to perform FC activations and obtain a controlled input current, a DC-DC converter is usually required to interface the FC with the load as a power conditioner [5], which can provide constant current input mode for the FC. The main challenge of DC-DC converters for the FC power conditioner is to achieve both wide input currents and non-pulsating low ripple input currents.

In order to meet the demand of the FC power conditioner, the DC-DC converter must feature as low current ripple, high power, good dynamic response, and adapting to wide input current ranges. Benefiting from simple structure, easy to control, and high efficiency, traditional non-isolated DC-DC converters such as boost, inverting buck-boost, and two/four-switch buck-boost converters (TBC/FBC) are widely used in the FC activation test applications [6]–[8]. However, traditional non-isolated DC-DC converters are confronted with many drawbacks such as poor performance in the wide input current range, large input ripple, slow dynamic response, etc., and cannot satisfy the needs of the FC activation. In general high step-up DC-DC converters are proposed to improve the voltage transmission ratio [1], [9]–[13]. Literature [12] proposed a high step-up boost converter, which employs charge-pump and voltage multiplier cells to obtain high voltage ratio. Literatures [13] adopt two switched-capacitor cells and one energy storage cell to construct the high voltage gain DC-DC converter. However the introduction of auxiliary devices will bring extra losses, and increase the cost. Adopting multiphase interleaved

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technology can increase the input power, reduce the input current ripple and the current stress of the switching devices [8], [14]–[19]. S. Somkun, P. Mungporn, and Y. Huangfu respectively proposed various control methods for interleaved boost converters used in the FC power conditioner [16]–[18]. These control method try to improve the dynamic performance, the robustness and convergence problems of interleaved boost converters. V. Samavatian *et al.* proposed the input/output magnetically coupled interleaved buck-boost converter for the FC power conditioner to obtain a high efficiency and nonplusing I/O currents [19]. Combining multiphase interleaved technology and the high step-up technology, the high step-up interleaved DC-DC converters could be obtained [20]–[25]. H. Xiao et.al proposed a fix phase shifts extended-duty-ratio boost converter with a variable phase-shift control strategy to expand current sharing range [20]. L. Zhang proposed an alternating phase shift control strategy for the interleaved boost converter with the voltage multiplier for the FC power conditioner [24]. As a result, the voltage stress of switches in light load is reduced. H. Moradisizkoohi proposed interleaved DC-DC converter using coupled inductors and switched capacitor [25]. This DC-DC converter has an ultra-high voltage gain and reduced voltage stress. However the existence of a large number of auxiliary devices in high step-up interleaved DC-DC converters increases volume, mass and cost, reduces the reliability.

In order to solve abovementioned problems and satisfy the needs of FC activation, this paper proposed a four-phase interleaved buck-boost converter with changed load connection (CLC-FIBC) for the FC activation. The new CLC-FIBC uses four-phase interleaved strategy to increase the input power. Besides, this CLC-FIBC changes the connection location of the load to obtain wide input current range, both step-up and step-down functions, and transistor common ground configuration, which will simplify drive design of power transistor in the multi-phase parallel application. Meanwhile CLC-FIBCs obtain characteristics of simple structure, and low power electronic components.

This paper presents the theoretical analysis and experimental verification for the CLC-FIBC. The rest of this paper is organized as follows. In Section II, the mathematical model of the single phase buck-boost converter with changed load connection (CLC-SBC) and the CLC-FIBC is given by the analysis of operating modes and waveforms. Features and design considerations are presented in section III. The construction of the simulation and experimental platform, the analysis of results are given in Section IV. Finally conclusions and discuss are presented in Section V.

II. MATHEMATICAL MODEL OF THE CLC-FIBC

A. OPERATING PRINCIPLE AND VOLTAGE GAIN

Figure 1 shows the topology derived process of the CLC-FIBC. A traditional boost converter (Figure 1(a)) is composed of a power transistor (S), a power diode (D), a freewheeling inductor, and two filter capacitors (C_1 and C_2). V_{in} is the input

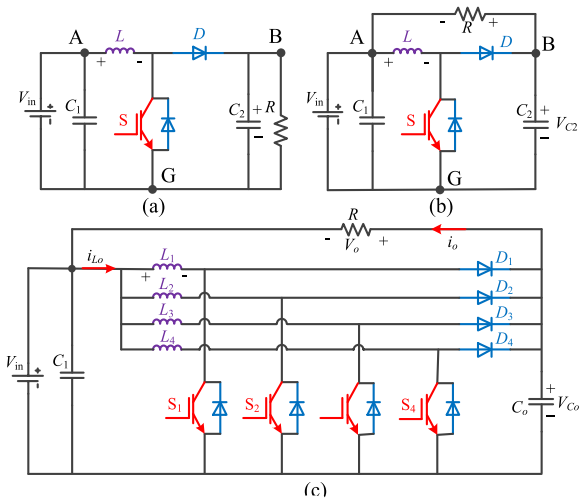

FIGURE 1. Topology derived process of the CLC-FIBC. (a) Traditional boost converter. (b) Single phase buck-boost converter with changed load connection (CLC-SBC). (c) Four-phase boost converter with changed load connection (CLC-FIBC).

voltage, and the load (R) is connected with C_2 in parallel. In this configuration, the boost converter can only step up the input voltage. In order to extend voltage conversion range, we changed the load connection from BG to BA. Then the CLC-SBC is obtained as shown in Figure 1(b) [26]–[28]. The so-called changed load connection is defined as: the negative pole of the load is not the grounded (G) of the input power supply, but connected to the input positive pole (A). The positive pole is still connected to the output positive pole as B. This new configuration is the buck-boost converter with changed load connection, but the filter capacitor C_2 is still connected between B and G. Then this buck-boost converter can be treated as a boost converter from structure and control characteristic. Replacing D as a transistor S_2, a synchronous rectification (SR) CLC-SBC can be obtained to reduce the conductive loss. Considering the peripheral resource limitation of micro-controller and the implementation complexity of control strategy, we proposed the CLC-FIBC consisted of four CLC-SBCs in this paper to increase the input power, reduce the current ripple on the input side, reduce the volume of the filter inductor and capacitor, and expand the input current range. The main circuit topology of the CLC-FIBC (Figure 1(c)) follows four identical parallel connections of the CLC-SBC to feed power to the load and reduce the input current ripple. These CLC-SBCs share the output filter capacitor C_o, which has a capacity value four times than that of the CLC-SBC filter capacitor C_2. In Figure 1(c), V_{Co} is the high side voltage across Co, V_o is the output voltage.

Comparing to the traditional boost converter, the proposed CLC-FIBC has two advantages. The first one is that the CLC-FIBC has low input current ripples, which will reduce the damage on the FC. The second one is that the CLC-FIBC has both step-up and step-down functions, which will provide a wide input current range from 0 to maximum input current

with a constant load resistor. The boost converter cannot obtain this function.

Because CLC-SBCs in the CLC-FIBC are all the same, the analysis of the CLC-FIBC can be divided into two steps: the operating principle of the CLC-SBC and the interleaved principle of the CLC-FIBC. The equivalent circuit of the CLC-SBC in the inductance continuous current mode (CCM) is shown in Figure 2 and the related waveforms of some key devices are shown in Figure 3. The filter of the load R is completed by C_1 and C_2. The specific operating principle is described as follows:

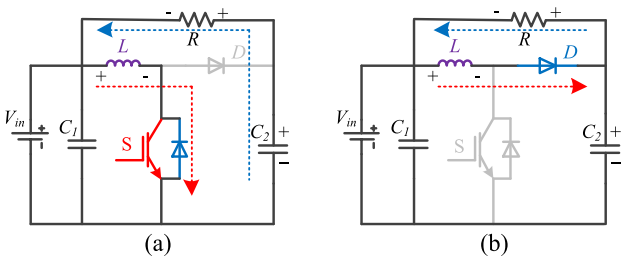

FIGURE 2. Operating modes. (a) Mode I: equivalent circuit when the S is turned on. (b) Mode II: equivalent circuit when the S is turned off.

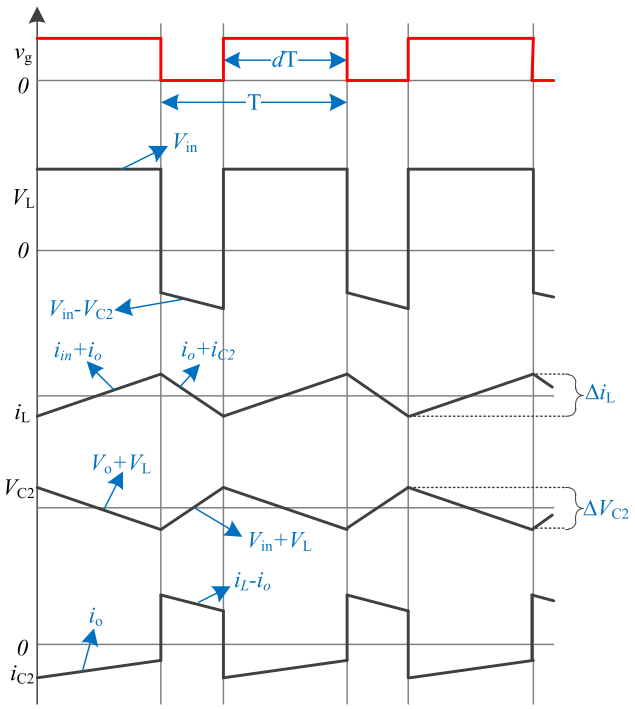

FIGURE 3. Voltage and current waveforms of several key devices.

Mode I (Figure 2(a)): At mode I the transistor S is turned on, the inductor stores the power energy through the path of $V_{\text{in}} \rightarrow L \rightarrow S$ (the red dotted line). At the same time the voltage of the filter capacitor C_2 reverses cutoff the diode D, and then the load R is powered by C_2 through the path of $C_2 \rightarrow R \rightarrow L \rightarrow S$ (the blue dotted line).

Mode II (Figure 2(b)): At mode II the transistor S is turned off, since the inductor L is connected to the anode of the diode D, the inductor discharges power energy to the C_2 through the path of $V_{\text{in}} \rightarrow L \rightarrow D \rightarrow C_2$ (the red dotted line), and the C_2 is in a charging state. The load R is powered by L through the path of $L \rightarrow D \rightarrow R$ (the blue dotted line).

According to the principle of inductance volt-second and capacitance ampere-second balance, the average voltage across the inductor under CCM can be expressed as:

$$V_{\text{L}} = dV_{\text{in}} + (1-d)(V_{\text{in}} - V_{\text{C2}}) \tag{1}$$

where in, V_{in} is the input DC power, V_{C2} is the voltage across the high side capacitor, and d is the duty cycle of the power transistor S.

The average voltage across the inductor is zero throughout the switching period T (the switching frequency $f = 1/T$), then the voltage transfer ratio between V_{in} and V_{C2} is:

$$V_{\text{C2}} = \frac{1}{1-d} \cdot V_{\text{in}} \tag{2}$$

It can be seen from equation (2) that the voltage ratio between the V_{C2} across the capacitor C_2 and the input voltage V_{in} is same as that of the traditional boost converter. Based on (2), the output voltage V_{o} of the CLC-SBC and the CLC-FIBC will be:

$$V_{\text{o}} = \frac{d}{1-d} \cdot V_{\text{in}} \tag{3}$$

Based on (3), when the duty cycle is equal to 0.5, the output voltage is equal to the input voltage. When the duty cycle is less than 0.5, the output voltage is less than the input voltage to realize the buck function. When the duty cycle is greater than 0.5, the output voltage is greater than the input voltage to realize the boost function. Therefore the CLC-FIBC can automatically switch between boost function and buck function according to the duty cycle.

The CLC-SBC and the CLC-FIBC will be the buck-boost converter with changed load connection and filter capacitors. According to the small ripple approximation analysis method, the average current through the capacitor C_2 under the CCM of the CLC-SBC is derived as:

$$i_{\text{C2}} = (1-d) \cdot i_{\text{L}} - \frac{V_{\text{C2}} - V_{\text{in}}}{R} \tag{4}$$

where i_{L} is the current through the L, and R is the load resistance.

The average current through the capacitor during the whole switching period is zero, and then the equation of the i_L will be:

$$i_{\text{L}} = \frac{V_{\text{C2}} - V_{\text{in}}}{(1-d)R} \tag{5}$$

Substituting equation (2) in equation (5), the equation of the i_L under CCM throughout the switching period is:

$$i_{\text{L}} = \frac{dV_{\text{in}}}{(1-d)^2 R} \tag{6}$$

The small ripple approximation analysis method can also be used to calculate voltage and current stresses in power transistors S and diodes D. When the S is turned on, the D is turned off instead, the inductor current i_{L} is equal to the power transistor current I_{S}, and the D withstands the voltage V_{C2}. When the S is turned off, the D is turned on, the current through the D is equal to i_{L}, and the S is subjected to the voltage V_{C2}. Related equations will be:

$$\langle V_{\mathrm{S}}\rangle = \langle V_{\mathrm{D}}\rangle = \langle V_{\mathrm{C2}}\rangle = \frac{V_{\mathrm{in}}}{1-d} \tag{7}$$

$$\langle I_{\mathrm{S}}\rangle = dI_{\mathrm{L}} = \frac{d^2 V_{\mathrm{in}}}{(1-d)^2 \cdot R} \tag{8}$$

$$\langle I_{\mathrm{D}}\rangle = (1-d)I_{\mathrm{L}} = \frac{V_{\mathrm{in}}}{(1-d)\cdot R} \tag{9}$$

B. FOUR-PHASE INTERLEAVED PRINCIPLE

The CLC-FIBC has four CLC-SBCs connected in parallel as shown in Figure 1(c). The simplest control strategy is synchronous control strategy, where four transistors have the same switching behavior. However the current ripple of the CLC-FIBC will be four time than that of the CLC-SBC in synchronous control strategy. In order to solve this problem, this paper adopts the interleaved control strategy: set one phase (a CLC-SBC) of the CLC-FIBC as the main converter, and the control PWM signals of other phases lag 90 degrees in sequence. Based on the method of [19], [21], we suppose that the equivalent series resistance of all inductors in the CLC-FIBC is neglected, all semiconductor components are in ideal switching state (on-state impedance is zero, and off-state impedance is infinite). And the CLC-FIBC operates in CCM. Through analysis, one period of the CLC-FIBC can be divided into four segments based on the size of the duty cycle d [22]–[24]. In the whole period, T/4, T/2, and 3T/4 are used as segmentation points. The power transistor (IGBT) driving signal, inductor current ripple and the conduction mode of each phase under the different duty cycle are shown in Figure 4, where 1 represents the power transistor turn-on and 0 represents turn-off. Detailed analysis of each mode is presented as follows:

Segment 1 [Figure 4(a)]: $0 < d\mathrm{T} \le \mathrm{T}/4$. If the i_{Ln} ($\mathrm{n} = 1, 2, 3, 4$) is the current across L_1, L_2, L_3, L_4 respectively, the i_{Ln} rises between the turn-on time and the turn-off time of S_{n} ($\mathrm{n} = 1, 2, 3, 4$), and reaches the maximum value at the turn-off time of S_{n}. On other time, the i_{Ln} will decrease, and reaches the maximum value at the turn-on time of S_{n}. Besides, because the behavior of i_{Ln} is not the same, the synthetic current i_{Lo} will have lower ripples than single phase current attributed to the phase shift control strategy. The inductor current ripple will be:

$$\frac{\mathrm{d}i_{\mathrm{Lo}}}{\mathrm{d}t} = \frac{V_{\mathrm{in}}}{L_1} + \frac{V_{\mathrm{in}}-V_{\mathrm{Co}}}{L_2} + \frac{V_{\mathrm{in}}-V_{\mathrm{Co}}}{L_3} + \frac{V_{\mathrm{in}}-V_{\mathrm{Co}}}{L_4} \tag{10}$$

$$\Delta i_{\mathrm{Lo}} = \frac{V_{\mathrm{Co}}}{Lf}(1-4d)d \tag{11}$$

where: V_{Co} is the voltage of C_o (the high side voltage), and is equal to the input voltage V_{in} plus the output voltage V_o.

Segment 2 [Figure 4(b)]: $\mathrm{T}/4 < d\mathrm{T} \le \mathrm{T}/2$. This segment has similar current waveforms and conclusion to Segment 1. The inductor current ripple expression is as follows:

$$\frac{\mathrm{d}i_{\mathrm{Lo}}}{\mathrm{d}t} = \frac{V_{\mathrm{in}}}{L_1} + \frac{V_{\mathrm{in}}-V_{\mathrm{Co}}}{L_2} + \frac{V_{\mathrm{in}}-V_{\mathrm{Co}}}{L_3} + \frac{V_{\mathrm{in}}}{L_4} \tag{12}$$

$$\Delta i_{\mathrm{Lo}} = \frac{V_{\mathrm{Co}}}{Lf}(2-4d)(d-\frac{1}{4}) \tag{13}$$

Segment 3 [Figure 4(c)]: $\mathrm{T}/2 < d\mathrm{T} \le 3\mathrm{T}/4$. This segment also has similar current waveforms and conclusion to Segment 1. So that the inductor current ripple can be expressed as follows:

$$\frac{\mathrm{d}i_{\mathrm{Lo}}}{\mathrm{d}t} = \frac{V_{\mathrm{in}}}{L_1} + \frac{V_{\mathrm{in}}-V_{\mathrm{Co}}}{L_2} + \frac{V_{\mathrm{in}}}{L_3} + \frac{V_{\mathrm{in}}}{L_4} \tag{14}$$

$$\Delta i_{\mathrm{Lo}} = \frac{V_{\mathrm{Co}}}{Lf}(3-4d)(d-\frac{1}{2}) \tag{15}$$

Segment 4 [Figure 4(d)]: $3\mathrm{T}/4 < d\mathrm{T} \le \mathrm{T}$. This segment also has similar current waveforms and conclusion to Segment 1. With the increase of duty cycle, the current increase time becomes longer from Segment 1 to Segment 4. Therefore, the expression of inductor current ripple is as follows:

$$\frac{\mathrm{d}i_{\mathrm{Lo}}}{\mathrm{d}t} = \frac{V_{\mathrm{in}}}{L_1} + \frac{V_{\mathrm{in}}}{L_2} + \frac{V_{\mathrm{in}}}{L_3} + \frac{V_{\mathrm{in}}}{L_4} \tag{16}$$

$$\Delta i_{\mathrm{Lo}} = \frac{V_{\mathrm{Co}}}{Lf}(4-4d)(d-\frac{3}{4}) \tag{17}$$

Combining equation (2), (3), (11), (13), (15), and (17), the mathematical relationship between the Δi_{Lo} and the duty cycle d of the CLC-FIBC are obtained. The relational expression is:

$$\Delta i_{\mathrm{Lo}} = \begin{cases} \dfrac{V_{\mathrm{Co}}}{Lf}(1-4d), 0 < d\mathrm{T} \le \dfrac{1}{4}\mathrm{T} \\ \dfrac{V_{\mathrm{Co}}}{Lf}\dfrac{(2-4d)}{d}\left(d-\dfrac{1}{4}\right), \dfrac{1}{4}\mathrm{T} < d\mathrm{T} \le \dfrac{1}{2}\mathrm{T} \\ \dfrac{V_{\mathrm{Co}}}{Lf}\dfrac{(3-4d)}{d}\left(d-\dfrac{1}{2}\right), \dfrac{1}{2}\mathrm{T} < d\mathrm{T} \le \dfrac{3}{4}\mathrm{T} \\ \dfrac{V_{\mathrm{Co}}}{Lf}\dfrac{(4-4d)}{d}\left(d-\dfrac{3}{4}\right), \dfrac{3}{4}\mathrm{T} < d\mathrm{T} \le \mathrm{T} \end{cases} \tag{18}$$

where L is the inductance of each phase inductor, f is the switching frequency of the power transistors, and V_{o} is the voltage at the output load. Comparing the output inductor current ripple of the CLC-FIBC and the CLC-SBC with the duty cycle function, we can see that under the same switching frequency condition, the maximum current ripple of CLC-FIBC is only a quarter of the CLC-SBCs. In addition, the current ripple of zero ripple current point will be zero.

The function of the capacitor in the CLC-FIBC can be regarded as a buffer unit for energy storage and release. Generally, the value of the capacitor is large, and is approximately equivalent to a constant voltage source. According to the relationship between the charge amount ΔQ and the capacitance C_o in one switching period, the output capacitor voltage ripple ΔV_{Co} can be expressed as the equation (20). Combined with equation (18), the high side voltage ripple of

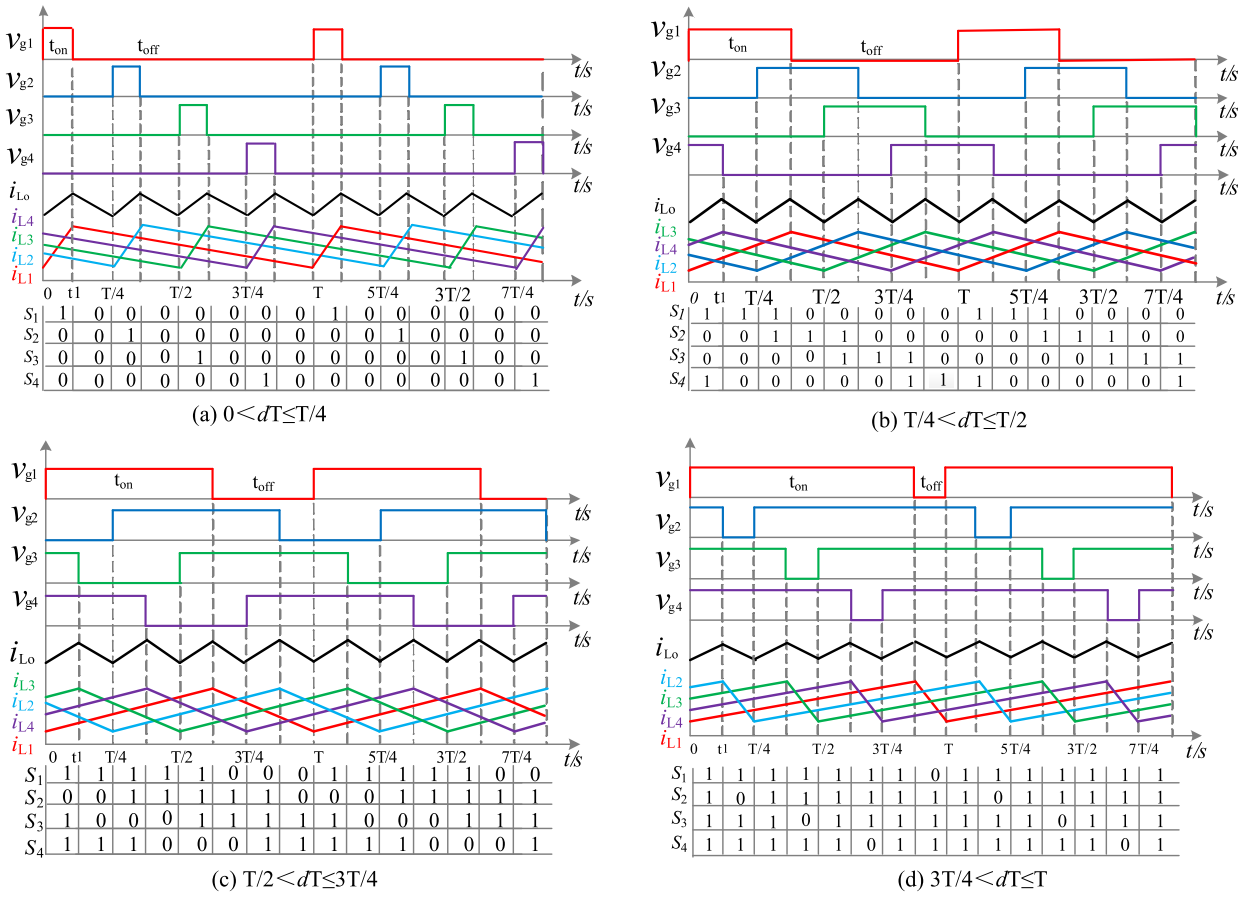

FIGURE 4. Schematic diagram of transistors (IGBT) gate drive signal and each phase inductance current ripple of the CLC-FIBC.

the proposed CLC-FIBC under different duty cycles can be calculated as

$$\Delta Q = \frac{1}{2}\frac{\Delta i_{\mathrm{Lo}}}{2}\frac{\mathrm{T}}{2} = \frac{\Delta i_{\mathrm{Lo}}}{8fC} \tag{19}$$

$$\Delta V_{\mathrm{Co}} = \frac{\Delta Q}{C} = \frac{\Delta i_{\mathrm{Lo}}}{8f} \tag{20}$$

where: C is the capacitance of C_o.

III. FEATURES AND DESIGN CONSIDERATIONS

A. SUPERIORITY AND COMPARISON

The proposed CLC-FIBC obtains features such as wide input current, high-power, and reduced current ripple by changing the load connection and adopting multiphase interleaved technology. Comparing to other non-isolated DC-DC converters as single phase boost converter (SBC), four-phase interleaved boost converter (FIBC), and four-phase interleaved two-switch buck-boost converter (FITBC). Although the SBC has a very simple structure (adopt fewest devices), the input power, the voltage ratio, and current ripples cannot satisfy the demand of FC power conditioner. The FIBC solved the problems of the input power and the current ripple, and the FITBC solve the problems of voltage ratio by introducing

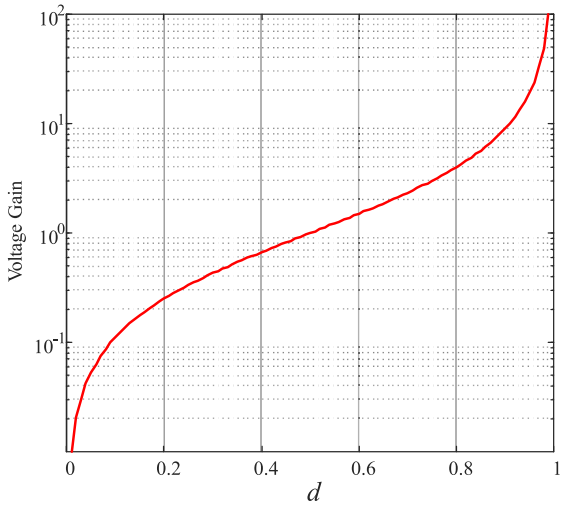

FIGURE 5. The voltage gain versus the duty cycle.

more semiconductor devices. The CLC-FIBC has simple structure (has same semiconductor devices to FIBC), both step up/down voltage conversion characteristics, and reduced current ripples. The voltage gain versus the duty cycle of the CLC-FIBC is shown in Figure 5.

TABLE 1. Comparisons to other converters.

Items	[20]	[29]	[16]	CLC-FIBC
Max. Power	0.3kW	0.5 kW	1 kW	**Up to 40 kW**
Peak Efficiency	96%	-	>94%	>93%
Voltage Conversion	Step-up	Step-up	Step-up	**Step-up/ down**
Voltage Ratio	$\frac{M}{1-d}$	$\frac{1}{1-d}$	$\frac{1}{1-d}$	$\boldsymbol{\frac{d}{1-d}}$
Current Ripples	-	$\leq\Delta i/3$	$\leq\Delta i/2$	$\boldsymbol{\leq\Delta i/4}$
Voltage Stress	Refer to [20]	$\frac{V_{in}}{1-d}$	$\frac{V_{in}}{1-d}$	$\frac{V_{in}}{1-d}$
Current Stress	Refer to [20]	$\frac{d^2V_{in}}{(1-d)^2\cdot R}$	$\frac{d^2V_{in}}{(1-d)^2\cdot R}$	$\frac{d^2V_{in}}{(1-d)^2\cdot R}$
Switching Frequency	200 kHz	5 kHz	100 kHz	9 kHz

Table 1 gives some comparisons between the proposed CLC-FIBC and interleaved DC-DC converters in other papers as [16], [20], [29]. The voltage and current tress of [20] has a complex expression, and therefore is not listed in Table 1. The voltage and current tress of [20] is larger than the CLC-FIBC. The superiority of the CLC-FIBC is marked in bold. The CLC-FIBC has the maximum output power of 40 kW, which is at the product level, and was used by many companies. Meanwhile this CLC-FIBC has a low current ripple, both step-up/step-down functions, and the peak efficiency of 93%. These parameters all satisfy the demand of FC activation. Although this CLC-FIBC has a floating load, it does not affect its using in the FC activation. Because the fuel cell activation more concern about input characteristics and the floating load is usually a resistor. The floating output voltage and resistive load will have a weak influence on the input current.

B. LOSS AND EFFICIENCY ANALYSIS

The loss of the CLC-FIBC can be divided into 3 sections as: switching losses, inductor losses, and conductive losses. The switching loss can be calculated by:

$$P_s = f(P_{on} + P_{off}) \tag{21}$$

The CLC-FIBC adopts four IGBT s (FF300R12KT4) as switching devices. According to the loss parameters from the data sheet the total switching loss will be 324 Watts.

The conductive loss mainly occurs in semiconductor devices. For maximum current state (300 A), this loss will be 525 Watts @ the forward voltage of 1.75V. The conductive loss on wires (includes inductors, assuming the total conductive resistance is only 0.01 Ω) will be 900 Watts.

The inductor loss is also a major loss source, which cannot be precise estimated. In summary, due to hardware constraints, the theoretical efficiency of the proposed CLC-FIBC will be not very high. The efficiency can be optimized through the soft-switching technology and using low loss devices.

C. DESIGN CONSIDERATIONS

The design of the CLC-FIBC has three steps: selection of semiconductor devices, the design of inductors and capacitors, and the modulation of the four-phase PWM drive signal for power transistors. Based on input and output voltage/current range, transistors and diodes can be selected using stress equations (7), (8), and (9). For the FC power conditioner, IGBT modules are a commonly used choice. The value of inductors and capacitors determines current ripples and voltage ripples respectively. They can be designed using (18) and (20) based on actual ripple requirements. Besides, the magnetic core of inductors also needs to be design appropriately. Finally the digital signal controller can be used to generate the four-phase PWM signal.

IV. EXPERIMENTAL RESULTS AND DISCUSS

A. CONTROL STRATEGY

Since the proposed CLC-FIBC is used for the FC power conditioner with the high-power and wide input current demand, a suitable control strategy is important to obtain both the wide current input range and the fast load transient response when the load varies. The proposed CLC-FIBC has a floating load, and therefore we control this converter as a boost converter. Four IGBTs in the proposed CLC-FIBC has the common ground, and then the drive power supply design can be simplified. The control strategy includes two sections: the input current controller, and the multiphase interleaved modulation strategy. The multiphase interleaved modulation strategy adopts the phase shift control strategy, and the phase shift between two adjacent driving signals is 90°. The input current controller measures and samples the input voltage and current signals through the Hall current sensor and the voltage collector. Then measured voltage and current values of the CLC-FIBC are fed back to the microcontroller unit (MCU) by analog to digital conversion (ADC) module. Finally measured voltage and current values, the given voltage value (I_{ref}) are used to calculate the duty cycle by a current regulator with voltage limit. Besides, the CAN bus is used to communicate with the human-computer interaction (HCI). Simultaneously, the protection circuit will also have corresponding actions according to the collected amount of feedback. The control schematic of the proposed converter is shown in Figure 6.

The control system as shown in Figure 6 adopts a single input current control loop with the voltage limit to control the value of the input current. First the current error is calculated by using the reference current (I_{ref}) and the actual input current (I_{in}). Then according to the current error, the control duty cycle (d) can be calculated using a current regulator with considerations of the limitations of input and output voltages. Finally four PWM signals are generated to drive the converter by modulating the duty cycle. In order to obtain current balancing, we choose one phase as the master control phase, and

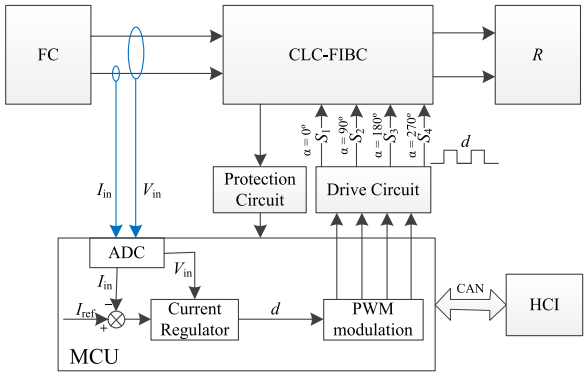

FIGURE 6. System control strategy schematic.

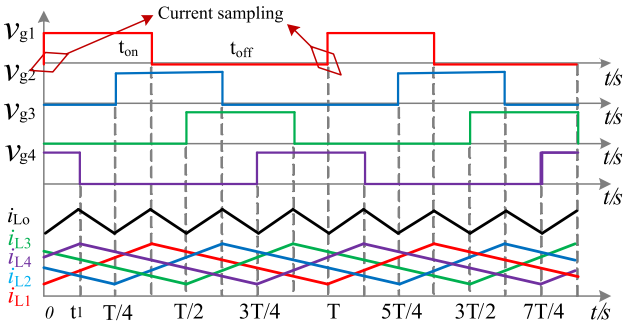

FIGURE 7. Current sampling points.

the other three phases as the slave control phases. The master control phase has the phase-shift of 0°, the slave control phases respectively has the phase-shift of 90°, 180° and 270°. Besides, we try our best to ensure that the parameters of each phase are the same to obtain a good current sharing ability. The input current is sampled as shown in Figure 7. We use the turn-on point of the main phase transistor as the current sampling point.

B. SIMULATION

In order to evaluate the operational characteristics and feasibility of the proposed CLC-FIBC, a simulation prototype has been implemented by MATLAB/Simulink software. The CLC-FIBC parameters can be summarized as shown in Table 2. The switching frequency is set as 9 kHz. The applied 4-phase inductor has the same specifications, and the single inductance is 100 μH. Besides, the input filter capacitor C_1 has a capacity of 400 μF. Meanwhile, the output filter capacitor C_o has a capacity of 20 μF.

Figure 8 shows simulation results of four-phase current waveforms, total input current waveforms, voltage and current transient response. The load resistance is 0.1 Ω, the input voltage is 70V, and the output voltage is 10V. Figure 8(a) shows that the current ripples of the total input current is reduced by using four-phase interleaved control. Figure 8(b) presents waveforms of the input current, the high side voltage, and the output voltage when the input current steps up to 200 A from 100 A, and steps down to 100 A from 200 A. the transient response of. The two transient processes

TABLE 2. Converter system specifications.

Items	Value
Input voltage V_{in}	0-700 VDC
Input current i_{in}	0-300 A
Inductance of each phase	100 μH
Input filter capacitor C_1	400 μF
Output filter capacitor C_o	20 μF
Switching frequency f	9kHz

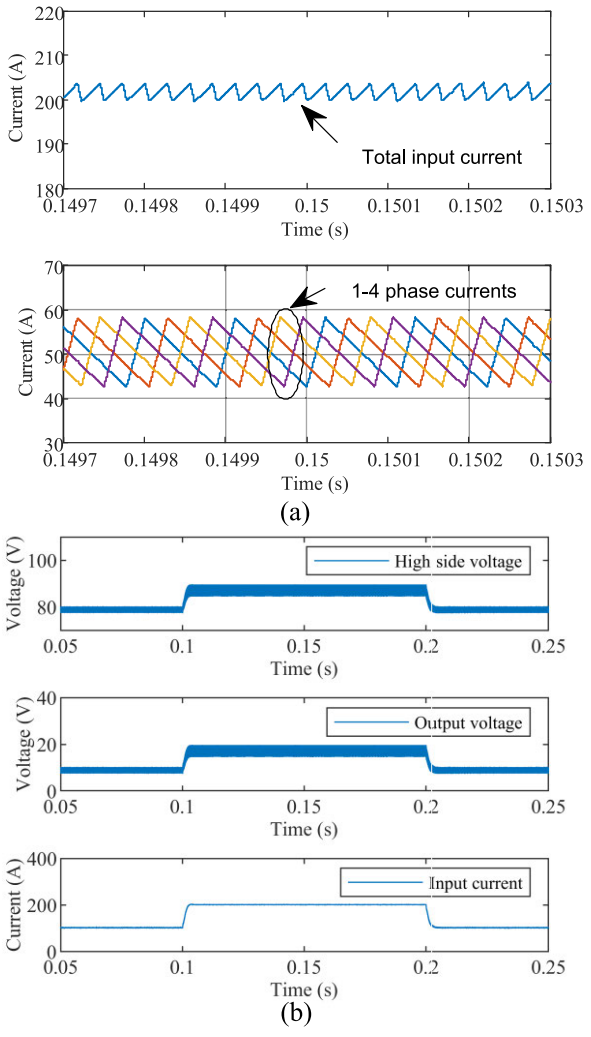

FIGURE 8. Simulation results. (a) CLC-FIBC 1-4 phase inductor current and total input current waveform. (b) Voltage and current transient response.

bots are completed quickly within 5 ms with a small overshoot. The proposed CLC-FIBC has a good transient response characteristic.

C. EXPERIMENTAL RESULTS

In this section, an experimental prototype has been implemented. The input voltage range of this prototype is 0-700 VDC and the input current range is 0-300 A. Four power transistors S_1, S_2, S_3 and S_4 are all IGBTs of Infineon

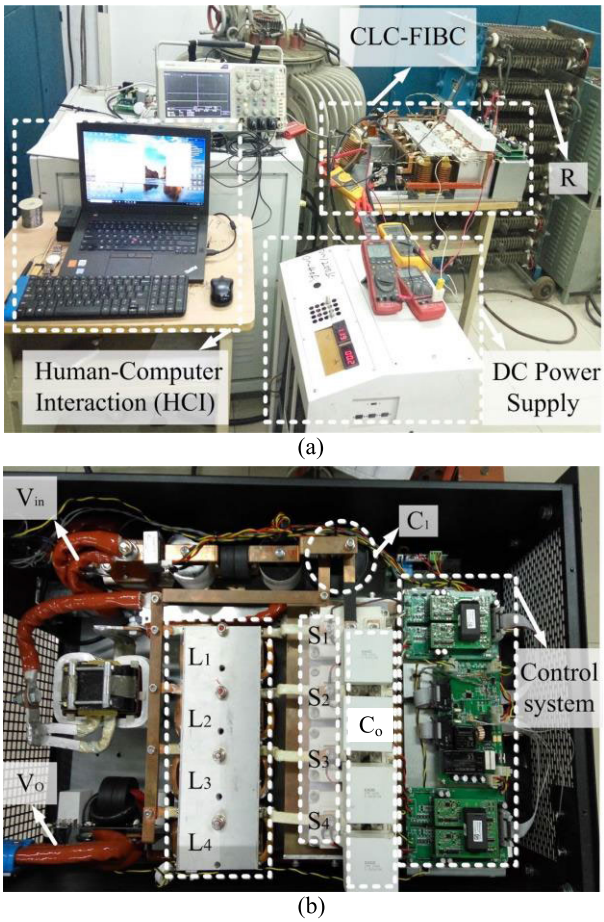

FIGURE 9. FC activation detection test system. (a) Test platform system. (b) CLC-FIBC internal structure distribution.

FF300R12KT4. The other CLC-FIBC parameters can be shown in Table 2.

Figure 9(a) is the FC power conditioner test platform based on laboratory conditions, which is composed of three parts. The front stage is a high-power DC power supply that can output voltage 0-700VDC and output current 0-300A. This DC power supply is used to simulate a wide input range of the FC. The intermediate stage is the CLC-FIBC for achieving power conversion function. And the latter stage is a high-power resistive load. Figure 9(b) is the internal structure distribution of the proposed CLC-FIBC.

D. EXPERIMENTAL RESULT AND ANALYSIS

The important experimental result measured on the experimental platform is shown in Figure 10 and Figure 11. In Figure 10(b), the input voltage is 70V, and the output voltage is 10V. In Figure 10(b) the input voltage is 23V, and the output voltage is 10V. Figure 10(a) shows the driving signal waveform of the four-channel IGBT of the CLC-FIBC. The phase difference between the adjacent two-phase driving signals is 90°, and the driving signal voltage amplitude is 15V. In Figure 10(b), when the proposed CLC-FIBC has a voltage of 80V across C_o, it shows that the proposed CLC-FIBC

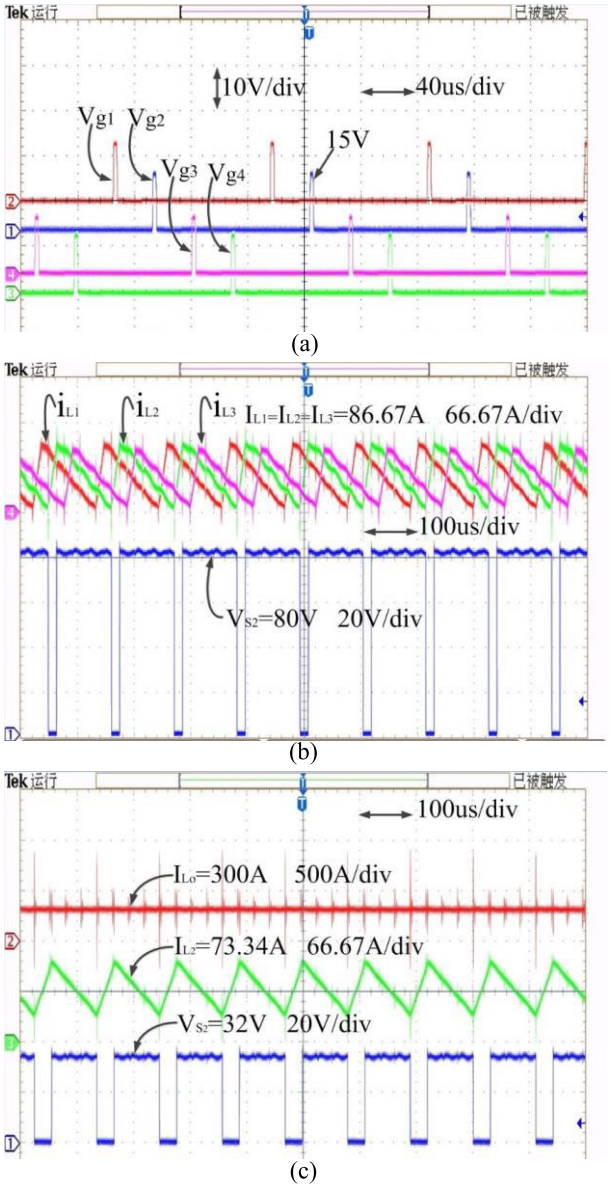

FIGURE 10. Experimental results. (a) IGBTs gate drive signal. (b) CLC-FIBC 1-3 phase inductor current and second phase power transistor voltage waveform. (c) Inductor current and IGBT voltage waveform of the proposed converter.

can achieve a good current sharing of the inductor current of each phase. And the total inductor input current i_{Lo} is approach 175A, while the current ripple is about 6%. The total output power is about 1.5 kW. The voltage stress of IGBTs is 80V. The waveform of Figure 10(c) is measured under the condition of the voltage 32V across C_o, the average current of each phase inductor is 73.34A, and the upper waveform is the total input current waveform of the 4-phase inductor obtained by interleaved control of the CLC-FIBC. The total power is about 2 kW. The voltage stress of IGBTs is 32V. It can be seen that the output current ripple has been greatly reduced. The middle and lower waveforms are the second phase inductor current waveform and the second

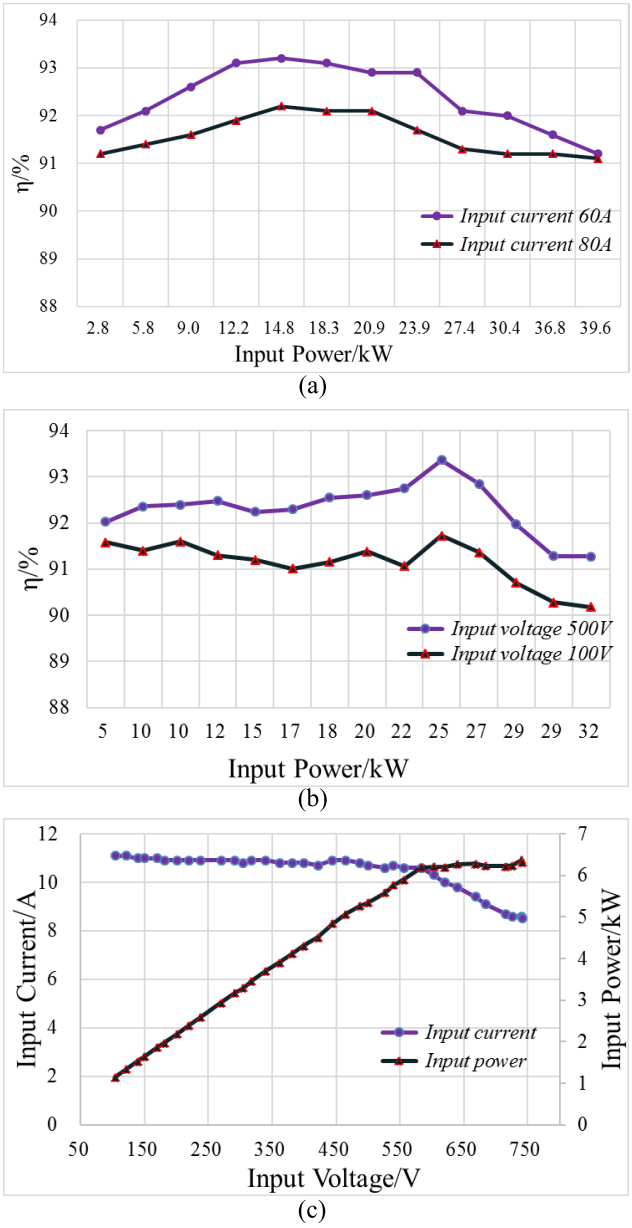

FIGURE 11. Result analysis. (a) Constant input current changes input voltage. (b) Constant input voltage changes input current. (c) Constant input power control.

phase IGBT voltage waveform. The inductor components are accompanied by significant energy storage and release process in each switching period, which is consistent with the theoretical analysis results in Section II.

In addition, in order to verify that the proposed CLC-FIBC that fits the wide input current range requirement of the FC, the efficiency of the CLC-FIBC was tested. The test is performed under the condition that the constant input current but the input voltage changes, the constant input voltage but the input current changes, and the constant input power, the efficiency curves are shown in Figure 11(a) and (b).

Figure 11(a) and (b) record the experimental data of the system under constant voltage and current control, respectively. The proposed CLC-FIBC and control strategy can get the maximum conversion efficiency, up to 93%. Figure 11(c) shows the data curve measured at an input power of 6 kW, which is achieved by first adjusting the input voltage with a constant input current. When the set power is reached, the input current decreases, but the input voltage increases. It is easy to see that when the input voltage rises to approximately 600 VDC, the converter is switched from constant current control to constant power operation. Through the experimental analysis results, the CLC-FIBC can adapt to the power supply with the wide input current range and the working efficiency has more than 90%. At the same time, under the condition of interleaved driving control, the CLC-FIBC can obtain the current sharing control of each phase, and has a small output current ripple. The maximum current ripple of the CLC-FIBC is not more than 6.2%.

V. CONCLUSION

This paper proposed, analyzed and designed a CLC-FIBC with characteristics of wide input current range, low inductor current ripple and high output efficiency in continuous current mode. Mathematical models, operating principle analysis, On the basis of this structure, features and design considerations are also presented. A fast-precision digital current controller is adopted to be the controller of the proposed CLC-FIBC. Finally the simulation model and experimental prototype are built to verify above-mentioned analysis.

Simulation and experimental results show: The CLC-FIBC prototype has the same voltage gain as the buck-boost converter and the characteristics with wide input current range. The maximum input current ripple the proposed CLC-FIBC does not exceed 6.2%. When the proposed CLC-FIBC adopts constant current, constant voltage and constant power control, the system efficiency can reach more than 90%, the highest working efficiency can go up to 93%, and the proposed topology has desirable conversion efficiency.

REFERENCES

[1] D. Gao, Z. Jin, J. Liu, and M. Ouyang, "An interleaved step-up/step-down converter for fuel cell vehicle applications," *Int. J. Hydrogen Energy*, vol. 41, no. 47, pp. 22422–22432, Dec. 2016.

[2] L. Sun, G. Wu, Y. Xue, J. Shen, D. Li, and K. Y. Lee, "Coordinated control strategies for fuel cell power plant in a microgrid," *IEEE Trans. Energy Convers.*, vol. 33, no. 1, pp. 1–9, Mar. 2018.

[3] J. Chen and Q. Song, "A decentralized energy management strategy for a fuel cell/supercapacitor-based auxiliary power unit of a more electric aircraft," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5736–5747, Jul. 2019.

[4] A. Misra, "Energy storage for electrified aircraft: The need for better batteries, fuel cells, and supercapacitors," *IEEE Electrific. Mag.*, vol. 6, no. 3, pp. 54–61, Sep. 2018.

[5] L. Palma, M. H. Todorovic, and P. N. Enjeti, "Analysis of common-mode voltage in utility-interactive fuel cell power conditioners," *IEEE Trans. Ind. Electron.*, vol. 56, no. 1, pp. 20–27, Jan. 2009.

[6] D. Mzoughi, H. Allagui, and A. Mami, "Study of a boost converter for PEM fuel cell," in *Proc. 10th Int. Multi-Conf. Syst., Signals Devices (SSD)*, Hammamet, Tunisia, Mar. 2013, pp. 1–5.

[7] J. E. Valdez-Resendiz, V. M. Sanchez, J. C. Rosas-Caro, J. C. Mayo-Maldonado, J. M. Sierra, and R. Barbosa, "Continuous input-current buck-boost DC-DC converter for PEM fuel cell applications," *Int. J. Hydrogen Energy*, vol. 42, no. 51, pp. 30389–30399, Dec. 2017.

[8] E. Schaltz, P. O. Rasmussen, and A. Khaligh, "Non-inverting buck-boost converter for fuel cell applications," in *Proc. 34th Annu. Conf. IEEE Ind. Electron.*, Orlando, FL, USA, Nov. 2008, pp. 855–860.

[9] V. F. Pires, A. Cordeiro, D. Foito, and J. F. Silva, "High step-up DC–DC converter for fuel cell vehicles based on merged quadratic boost–Ćuk," *IEEE Trans. Veh. Technol.*, vol. 68, no. 8, pp. 7521–7530, Aug. 2019.

[10] K.-C. Tseng, J.-T. Lin, and C.-C. Huang, "High step-up converter with three-winding coupled inductor for fuel cell energy source applications," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 574–581, Feb. 2015.

[11] Y. Zheng, B. Brown, W. Xie, S. Li, and K. Smedley, "High step-up DC–DC converter with zero voltage switching and low input current ripple," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9418–9431, Sep. 2020.

[12] H. Pourfarzad, M. Saremi, and T. Jalilzadeh, "An extended high-voltage-gain DC–DC converter with reduced voltage stress on switches/diodes," *Electr. Eng.*, vol. 102, no. 4, pp. 2435–2452, Jun. 2020.

[13] T. Jalilzadeh, N. Rostami, E. Babaei, and M. Maalandish, "Non-isolated topology for high step-up DC-DC converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, early access, Jun. 20, 2018, doi: 10.1109/JESTPE.2018.2849096.

[14] D. Liang and H.-B. Shin, "Coupled inductor design method for 2-phase interleaved boost converters," *J. Power Electron.*, vol. 19, no. 2, pp. 344–352, Mar. 2019.

[15] W. Gu and I. Batarseh, "Interleaved synchronous buck regulator with hysteretic voltage control," in *Proc. PESC*, 2001, pp. 1512–1516.

[16] S. Somkun, C. Sirisamphanwong, and S. Sukchai, "A DSP-based interleaved boost DC–DC converter for fuel cell applications," *Int. J. Hydrogen Energy*, vol. 40, no. 19, pp. 6391–6404, May 2015.

[17] P. Mungporn, P. Thounthong, B. Yodwong, C. Ekkaravarodome, A. Bilsalam, S. Pierfederici, D. Guilbert, B. Nahid-Mobarakeh, N. Bizon, Z. Shah, S. Khomfoi, P. Kumam, and P. Burikham, "Modeling and control of multiphase interleaved fuel-cell boost converter based on Hamiltonian control theory for transportation applications," *IEEE Trans. Transport. Electrific.*, vol. 6, no. 2, pp. 519–529, Jun. 2020.

[18] Y. Huangfu, S. Zhuo, F. Chen, S. Pang, D. Zhao, and F. Gao, "Robust voltage control of floating interleaved boost converter for fuel cell systems," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 665–674, Jan./Feb. 2018.

[19] V. Samavatian and A. Radan, "A high efficiency input/output magnetically coupled interleaved buck–boost converter with low internal oscillation for fuel-cell applications: CCM steady-state analysis," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5560–5568, Sep. 2015.

[20] H. Xiao, T. Xu, L. Xiang, Z. Zhang, S. Xie, and D. Liu, "A variable phase-shift control scheme for extended-duty-ratio boost converter with automatic current sharing in high step-up high current application," *IEEE Trans. Ind. Electron.*, vol. 68, no. 8, pp. 6794–6805, Aug. 2021.

[21] L.-W. Zhou, Y.-Z. Zhou, Q.-M. Luo, and B.-X. Zhu, "Interleaved high step-up DC/DC converter," *Electr. Mach. Control*, vol. 18, no. 12, pp. 10–16, Dec. 2014.

[22] Z. Lu, L. Zheng, Z. Ma, J. Liu, and Y. Qin, "Interleaved high gain boost converter with switched capacitor network," *Trans. China Electrotech. Soc.*, vol. 27, no. 11, pp. 153–159, Nov. 2012.

[23] G. A. L. Henn, R. N. A. L. Silva, P. P. Praça, L. H. S. C. Barreto, and D. S. Oliveira, "Interleaved-Boost converter with high voltage gain," *IEEE Trans. Power Electron.*, vol. 25, no. 11, pp. 2573–2761, Nov. 2010.

[24] L. Zhang, D. Xu, G. Shen, M. Chen, A. Ioinovici, and X. Wu, "A high step-up DC to DC converter under alternating phase shift control for fuel cell power system," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1694–1703, Mar. 2015.

[25] H. Moradisizkoohi, N. Elsayad, and O. A. Mohammed, "An integrated interleaved ultrahigh step-up DC–DC converter using dual cross-coupled inductors with built-in input current balancing for electric vehicles," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 644–657, Mar. 2020.

[26] M. Kazimierczuk, *Pulse-Width Modulated DC-DC Power Converters*. Hoboken, NJ, USA: Wiley, 2016, pp. 180–181.

[27] S. Zhang, R. Lu, and J. Sun, "Buck-boost equalizer for super-capacitor modules," in *Proc. IEEE Vehicle Power Propuls. Conf.*, Lille, France, Sep. 2010, pp. 1–5.

[28] Y. Babazadeh, E. Babaei, and M. Sabahi, "A new non-isolated buck-boost converter with high voltage gain and positive output voltage for renewable energy applications," in *Proc. 10th Int. Power Electron., Drive Syst. Technol. Conf. (PEDSTC)*, Shiraz, Iran, Feb. 2019, pp. 201–206.

[29] N. Benyahia, H. Denoun, A. Badji, M. Zaouia, T. Rekioua, N. Benamrouche, and D. Rekioua, "MPPT controller for an interleaved boost DC–DC converter used in fuel cell electric vehicles," *Int. J. Hydrogen Energy*, vol. 39, no. 27, pp. 15196–15205, 2014.

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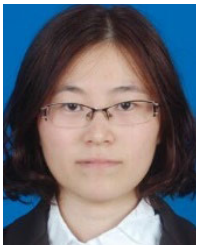

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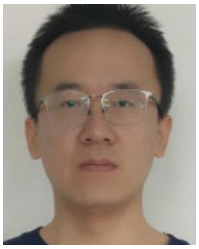

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