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340-GHz Heterogeneously-Integrated THz Imager With 4°-Beamwidth 16 × 16 IPD Antenna Array for Lensless Terahertz Imaging Applications

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ABSTRACT A low-cost and planar heterogeneously-integrated 340-GHz THz imager is proposed for lensless THz imaging applications. The proposed THz imager is composed of a 16 × 16 antenna array realized in an integrated-passive-device (IPD) technology, an IPD-to-CMOS THz interconnect, and a power detector implemented in a 0.18-μm CMOS technology. The 16 × 16 IPD antenna array can provide simulated antenna gain of 23.9 dBi, antenna directivity of 30 dB, and half-power beamwidth (HPBW) of 5.6° at 340 GHz. The proposed THz interconnect utilizes a transmission line coupling technique to provide low-loss and broadband signal transition from a CMOS chip to an IPD one while occupying a small chip area. The simulated insertion loss of the THz interconnect is only 1.8 dB at 340 GHz while providing 3-dB bandwidth from 230 to 446 GHz. The power detector exploits the transistor's inherent even-order nonlinearity to rectify the input signal for power detection. The power detector can give simulated voltage responsivity R_V and noise equivalent power (NEP) of 190.2 kV/W and 1.9 nW/Hz$^{0.5}$ at 340 GHz, respectively, as the chopping frequency f_{mod} is 1 kHz. A nonlinear curve fit technique is proposed to tackle the undesired fluctuation of the measured output voltage due to a standing-wave effect. Experimental results show that the proposed heterogeneously-integrated THz imager can provide measured effective R_V and NEP of 0.967 MV/W and 0.18 nW/Hz$^{0.5}$ at 328 GHz, respectively, as f_{mod} is 1 kHz. The measured antenna directivity and HPBW can be 30 dB and 4° at 340 GHz, respectively. Such a THz imager with advantages of high antenna directivity and narrow HPBW can be employed to realize a simple, low-cost, and lensless THz imaging system. To the best of the authors' knowledge, the proposed THz imager integrates the highest number of antennas and exhibits the highest antenna directivity and the narrowest HPBW at THz frequencies reported thus far.

INDEX TERMS Antenna array, CMOS, heterogeneous integration, lensless THz imaging system, integrated-passive-device, IPD, interconnect, terahertz, THz.

I. INTRODUCTION

THz science and technology have attracted great attention in recent years since they can be used for many useful applications, including the next sixth-generation (6G) wireless communications, non-invasive biomedical and medical imaging, stand-off detection of concealed weapons and explosives, pharmaceutical, and semiconductor packaging inspection [1]–[6]. Moreover, THz wave is nonionizing, very safe as compared to the X-ray.

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Utilizing CMOS technologies to realize THz electronic systems for the aforementioned applications is appealing because it can deliver a low-cost, compact, high-integration, and mass-producible solution. Many electronic THz imaging systems have been reported using silicon technologies [7]–[17]. Of the building blocks of these THz imaging systems, an antenna plays a critical role since it directly determines the equivalent isotropically radiated power a transmitter can provide and how much power a THz imager can collect. Unfortunately, CMOS on-chip antennas exhibit extremely low antenna directivity and antenna gain due to lossy silicon substrates and unfavorable back end of

lines (BEOL), drastically impacting the imaging system performance [5], [18]. Many techniques have been reported to improve on-chip antenna performance, such as antennas with bulky and nonplanar silicon lens [19], [20], superstrates [21], [22], dielectric resonator antennas [12], [23], substrate thinning [19], [24], artificial magnetic conductors [25], [26], and micromachined antennas [27]. However, these techniques either need complicated fabrication process or provide limited gain improvement. A heterogeneous integration approach is a good alternative to deal with the low-gain issue of on-chip antennas [18]. However, the realization of the antenna array in [18] requires an in-house fabrication process, which is merely not accessible to the interested researchers, but the reliability and manufacturing yield are also low.

Due to the aforementioned issues of low-directivity and low-gain on-chip antennas, most of the reported THz imaging systems rely on optical lenses and mirrors to focus the transmitted beam on a device under test (DUT) first and then focus the output beam emitted from the DUT on a THz imager later. These optical components not only increase the cost and system complexity, but they also increase the system size which is limited by the focal length of the optical lenses. Moreover, focal-plane THz imaging requires precise alignment and beam focus which might be more difficult as compared to its counterpart using a visible light [28]. THz detector arrays were proposed to remove the optical lenses and mirrors for realizing lensless THz imaging systems [8], [9], [29]. However, THz detector arrays have limited image resolution due to a small number of pixels. Moreover, the signal power emitting out from the DUT is also diverged to hit on all the pixels, which decreases the power received by each pixel and hence degrades the dynamic range of the THz imaging systems. Three-dimensional (3D) printed micromachining horn antennas with high antenna directivity and antenna gain were presented to carry out a lensless THz imaging system [30]. Nevertheless, the fabrication steps are complicated. Furthermore, good alignment is hard to be achieved since the Epotek H54 epoxy material and a vacuum probe with an additional glass substrate are used to glue a horn antenna onto a CMOS chip [31]. Any mis-alignment reduces the signal coupling strength, dramatically increasing the insertion loss. Therefore, a THz imager with high- directivity, high-gain, and narrow half-power beamwidth (HPBW) antennas and reliable assembly is extremely desired in order to remove the optical components for realizing a simple, low-cost, compact, and lensless THz imaging system.

In this paper, a low-cost and planar 340-GHz heterogeneously-integrated THz imager which can solve the aforementioned issues is proposed for lensless THz imaging applications. The proposed THz imager adopts a heterogeneous integration approach to integrate a power detector in a 0.18-μm CMOS technology with a 4°-HPBW 16 × 16 antenna array implemented in a commercially-available integrated-passive-device (IPD) technology through a proposed low-loss and broadband THz interconnect. A gold-gold thermo-compressive flip-chip packaging technique is employed to conduct the THz imager assembly, which is much reliable as compared to that using glues and vacuum probes in [30]. Such a heterogeneously-integrated THz imager with sharp detection angles is very suitable to realize a simple, low-cost, compact, and lensless THz imaging system without any optical lenses and mirrors required. This paper is organized as follows. Section II explains the design of the proposed heterogeneously-integrated THz imager. A characterization method for measuring the proposed THz imager is described in Section III. Section IV illustrates the experimental results. Finally, Section V concludes this work.

II. HETEROGENEOUSLY-INTEGRATED THZ IMAGER DESIGN

Fig. 1 shows the proposed lensless THz imaging system. A THz signal generated by a commercial signal source module is radiated out by a horn antenna. This signal then penetrates through a DUT and then received by a THz imager with sharp detection angles. The output voltage of the THz imager is proportional to the input received power. Step motors are used to move the DUT within an interested imaging area. By recording the output voltage of the THz imager, the image of the DUT can be constructed. Since the horn antenna and the proposed THz imager have narrow HPBW with sharp detection angles, the conventional optical lenses and mirrors for beam focus can be removed [30]. Therefore, a simple, low-cost, compact, and lensless THz imaging system can be established for THz imaging applications. Note that this work only realizes the THz imager of the proposed THz imaging system. However, the same heterogeneous integration approach can also be employed to implement the THz signal source and other THz transmitters in the future designs. For example, with the proposed heterogeneous integration approach, the equivalent isotropically radiated power (EIRP) defined as $P_{TX} \times G_{ant,TX}$ of a THz transmitter can be dramatically enhanced, which can improve the dynamic range of THz radar and imaging systems, where P_{TX} and $G_{ant,TX}$ are the transmitter output power and the transmitter antenna gain, respectively.

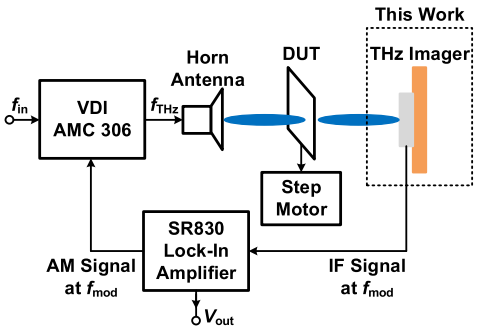

FIGURE 1. Lensless THz imaging system.

Fig. 2(a) illustrates the system architecture of the proposed 340-GHz heterogeneously-integrated THz imager for

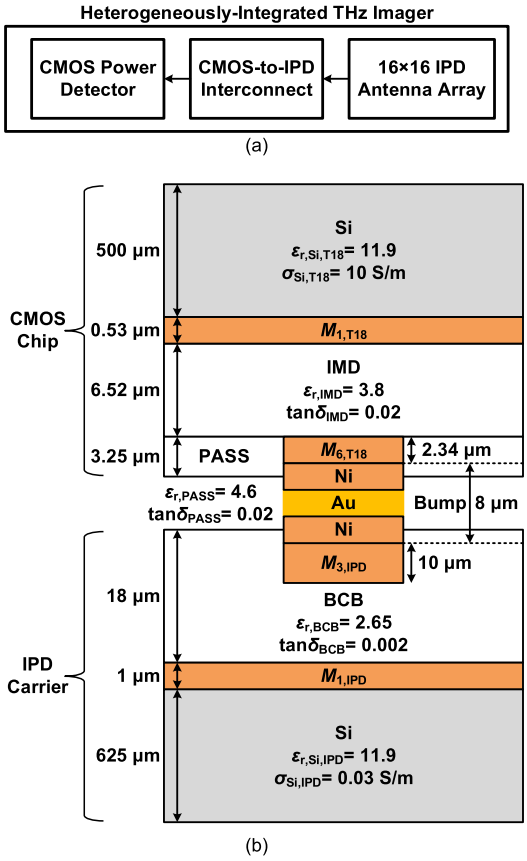

FIGURE 2. (a) System architecture of the proposed heterogeneously-integrated THz imager. (b) Cross-sectional view of the adopted 0.18-μm CMOS and IPD technologies.

lensless THz imaging applications. The proposed THz imager is composed of a CMOS power detector realized in a 0.18-μm CMOS technology, a 16 × 16 antenna array implemented in a commercially-available IPD technology, and a CMOS-to-IPD THz interconnect. The cross-sectional views of the adopted CMOS and IPD technologies are shown in Fig. 2(b). Nickel-gold (Ni-Au) bumps with thickness of 8 μm are used to bond the CMOS chip to the IPD antenna array using an Au-Au thermo-compressive flip-chip bonding technique [32]. The incoming signal can be captured by the antenna array and is then transferred to the input of the CMOS power detector through the THz interconnect. By recording the detector's output voltage, the THz image of a DUT can be obtained. The following sub-sections explain the design detail of each sub-block of the proposed heterogeneously-integrated THz imager.

A. 16 × 16 THZ IPD ANTENNA ARRAY DESIGN

The proposed 16 × 16 THz IPD antenna array at 340 GHz is shown in Fig. 3. It consists of a 1-to-16 corporate-feed network and 16 1 × 16 series-fed antenna arrays with a patch antenna being the element. The 1-to-16 corporate-feed network is employed to equally distribute the input power to 16 output ports. These 16 output signals subsequently excite

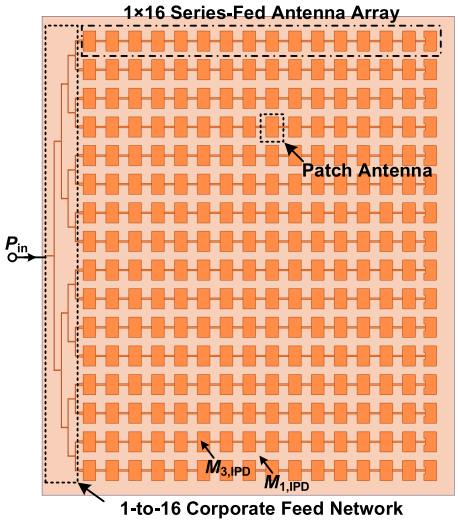

FIGURE 3. Proposed 16 × 16 IPD antenna array.

the 16 1 × 16 series-fed antenna arrays. By designing the input signal of each antenna to be in phase, these 256 antenna elements can all radiate along the broadside direction, resulting in a high-gain, high-directivity, and narrow-HPBW antenna array. The array gain of the 16 × 16 THz IPD antenna array can be estimated by

$$G_{16\times16\ \text{Array}} = G_{1\times16\ \text{Series Array}} - IL_{\text{FN1}} + 10\text{Log}N_1, \quad (1)$$

where $G_{1\times16\ \text{Series Array}}$, IL_{FN1}, and N_1 are the antenna gain of the 1 × 16 series-fed antenna array, the insertion loss of the 1-to-16 corporate-feed network, and the total numbers of the 1 × 16 series-fed antenna arrays, i.e., 16 in this work, respectively. Hence, the array gain can be enhanced by reducing the insertion loss of the feeding network and increasing the antenna numbers. Since the minimum line width of $M_{3,\text{IPD}}$ allowed by the design-rule-check (DRC) rules of the IPD technology is 10 μm, the maximum achievable characteristic impedance Z_0 of a microstrip line is 43.1 Ω. Therefore, the input impedances of the 16 × 16 antenna array, 1 × 16 antenna array, and 1-to-16 corporate feed network are all designed as 43.1 Ω. The following paragraphs explain the design detail of each sub-block of the proposed 16 × 16 THz IPD antenna array.

The proposed 1-to-16 corporate-feed network is used to equally distribute the input power to 16 output ports at 340 GHz. Its operation principle can be explained by the inset showing a 1-to-2 power dividing network in Fig. 4(a). The output ports P_2 and P_3 are terminated with 43.1-Ω loads. The line width $W_{\text{FD},1}$ of the transmission line $TL_{\text{FD},1}$ and $TL_{\text{FD},2}$ is designed as 10 μm to have Z_0 of 43.1 Ω. These two transmission lines with Z_0 of 43.1 Ω are shunt at the junction to present an input impedance of 21.6 Ω. Thereafter, a quarter-wave transmission line $TL_{\text{FD},3}$ with the line width $W_{\text{FD},2}$, length, and Z_0 of 20.4 μm, 147 μm, and 30.5 Ω, respectively, is employed to transform the input impedance from 21.6 to the desired 43.1 Ω at the input port

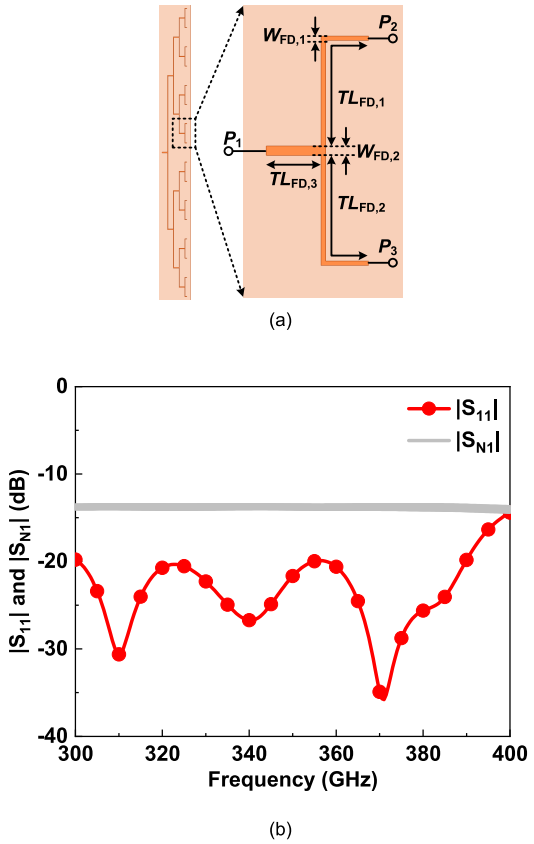

FIGURE 4. (a) Proposed 1-to-16 corporate-feed network. (b) Simulated S-parameters of the proposed 1-to-16 corporate-feed network where *N* is an integer ranging from 2 to 17.

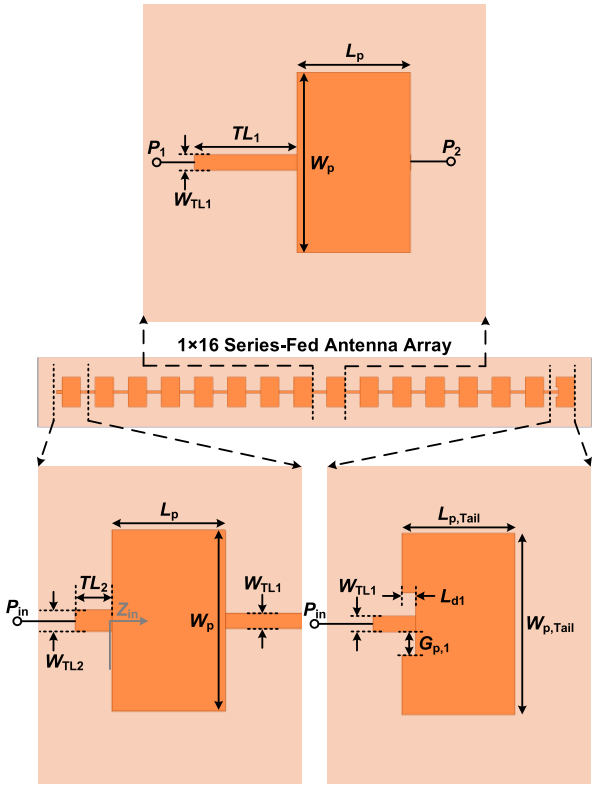

FIGURE 5. Proposed 1 × 16 series-fed antenna array.

of P_1 at 340 GHz. The same 1-to-2 power dividing networks are then cascaded to form the proposed 1-to-16 corporate-feed network. As shown in Fig. 4(b), the proposed 1-to-16 corporate-feed network can give simulated $|S_{11}|$ and $|S_{N1}|$ of −26.7 and 13.5∼13.9 dB at 340 GHz, respectively, while keeping $|S_{11}|$ lower than −14.4 dB and $|S_{N1}|$ better than −14.3 dB from 300 to 400 GHz, where N is an integer ranging from 2 to 17. The power dividing ratio of an ideally lossless 1-to-16 corporate-feed network shall be −12 dB. Hence, the insertion loss of the proposed 1-to-16 corporate-feed network, that is, IL_{FN1} in (1), varies from 1.5 to 1.9 dB at 340 GHz among the 16 output ports.

Fig. 5 illustrates the proposed 1 × 16 series-fed antenna array which comprises of a 1-to-16 series-feed network and 16 patch antennas being the antenna elements. The array gain of the 1 × 16 series-fed antenna array can be estimated by

$$G_{1\times16\ \text{Series Array}} = G_{\text{Patch}} - IL_{\text{FN2}} + 10\text{Log}N_2, \quad (2)$$

where G_{Patch}, IL_{FN2}, and N_2 are the antenna gain of the single patch antenna, the insertion loss of the 1-to-16 series-feed network, and the total antenna numbers in the 1 × 16 series-fed antenna array, i.e., 16 in this work, respectively. Hence, the array gain can be enhanced by increasing the antenna numbers and reducing the insertion loss of the feeding network. The operation principle of the proposed 1 × 16 series-fed antenna array can be understood by explaining the design of the patch on the tail first as shown in the bottom-right inset in Fig. 5. Since the patch length and width are much larger than the thickness of the dielectric layer beneath the patch, the dominant mode of the patch antenna is the transverse magnetic mode of TM_{010} whose resonant frequency is given by

$$f_{\text{R},010} = \frac{c}{2L\sqrt{\varepsilon_r}}, \quad (3)$$

where c, ε_r, and L are the speed of the light in the free space, the effective dielectric constant of the dielectric material, and the patch length, respectively [33]. According to (3), the patch length shall be designed around half wavelength at the frequency of interest. Subsequently, ANSYS HFSS, a commercial three-dimensional electromagnetic simulator, is employed to optimize the patch antenna. Therefore, the patch length $L_{\text{p,Tail}}$ is selected as 264 μm, around half wavelength at 340 GHz. The width $W_{\text{p,Tail}}$ and the insertion distance L_{d1} are designed as 420 and 47 μm, respectively, to match the input impedance of the patch to 25.1 Ω at 340 GHz. The simulated input return loss, antenna gain G_{ant}, and the 3D radiation pattern of the patch antenna are depicted in Fig. 6. The proposed patch antenna can provide simulated $|S_{11}|$, antenna gain G_{ant}, i.e., G_{Patch} in (2), antenna directivity D_{ant}, and radiation efficiency of −33.2 dB, 5.5 dBi, 8.1 dB, and 55% at 340 GHz, respectively, while maintaining $|S_{11}|$ lower than −10 dB from 337.5 to 342 GHz. The 3-dB antenna

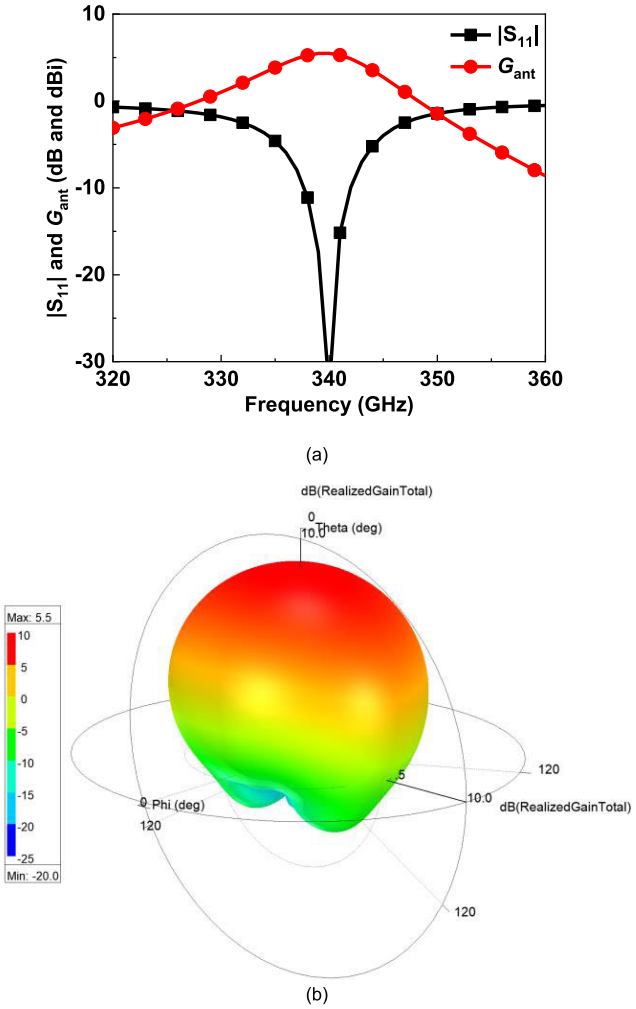

FIGURE 6. (a) Simulated input return loss and antenna gain, and (b) radiation pattern of the patch antenna on the tail.

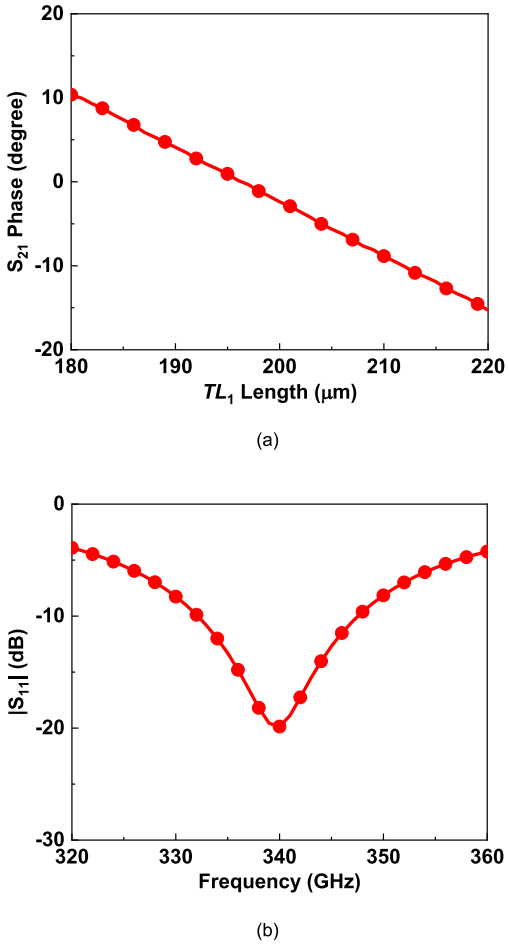

FIGURE 7. (a) Simulated S_{21} phase of the antenna unit cell versus the length of the interconnecting transmission line TL_1. (b) Simulated input return loss of the antenna unit cell.

gain bandwidth is from 332 to 345 GHz. For the design of other patch antennas in the 1 × 16 series-fed antenna array as shown in the top inset in Fig. 5, designated as an antenna unit cell, they have an input port P_1 and an output port P_2. The line width W_{TL1} of an interconnecting transmission line TL_1 is designed as 36.2 μm to have Z_0 of 25.1 Ω at 340 GHz. The patch length L_p and width W_p are designed as 264 and 420 μm, respectively, to match the input impedance of the antenna unit cell to 25.1 Ω at 340 GHz. The phase difference between the ports P_1 and P_2, i.e., $\angle S_{21}$, must be 0° in order to have all the antennas radiate along the broadside direction. Fig. 7(a) illustrates the simulated $\angle S_{21}$ versus the TL_1 length as P_2 is terminated with a 25.1-Ω load. The length of TL_1 is designed as 196 μm to have $\angle S_{21}$ around 0°. The simulated input return loss of the antenna unit cell is shown in Fig. 7(b). The simulated $|S_{11}|$ is −19.9 dB at 340 GHz and lower than −10 dB from 332 to 348 GHz. The patch antenna on the tail and the antenna unit cells are then integrated together to form the proposed 1 × 16 series-fed antenna. Fig. 8(a) illustrates the simulated input return loss and antenna gain of the 1 × 16 series-fed antenna array without any design tuning. The simulated $|S_{11}|$ and antenna gain are only −9.5 dB and 11 dBi at 340 GHz, respectively, due to the undesired coupling between antenna elements. Appropriate design tuning is required to improve the performance of the antenna array. As shown in the bottom-left inset in Fig. 5, an additional transmission line TL_2 is added to improve the input impedance matching. The line width of TL_2 is designed as 50 μm to have Z_0 of 19 Ω. As the TL_2 length is selected as 85 μm, TL_2 can transform the input impedance to the desired value of 43.1 Ω at 340 GHz. Moreover, the length of the interconnecting transmission line TL_1 is adjusted from 196 to 211 μm to ensure that all the 16 patch antennas radiate in phase along the broadside direction. Fig. 8(a) shows the simulated input return loss and antenna gain of the 1 × 16 series-fed antenna array after design tuning. The simulated $|S_{11}|$ and G_{ant} can be improved from −9.5 to −23.8 dB and 11 to 14.9 dBi, respectively. The simulated radiation pattern is illustrated in Fig. 8(b). Clearly, the main beam of the 1 × 16 series-fed antenna array is along the desired broadside direction. Moreover, the insertion loss IL_{FN2} of the 1-to-16 series-feed network can be found to be

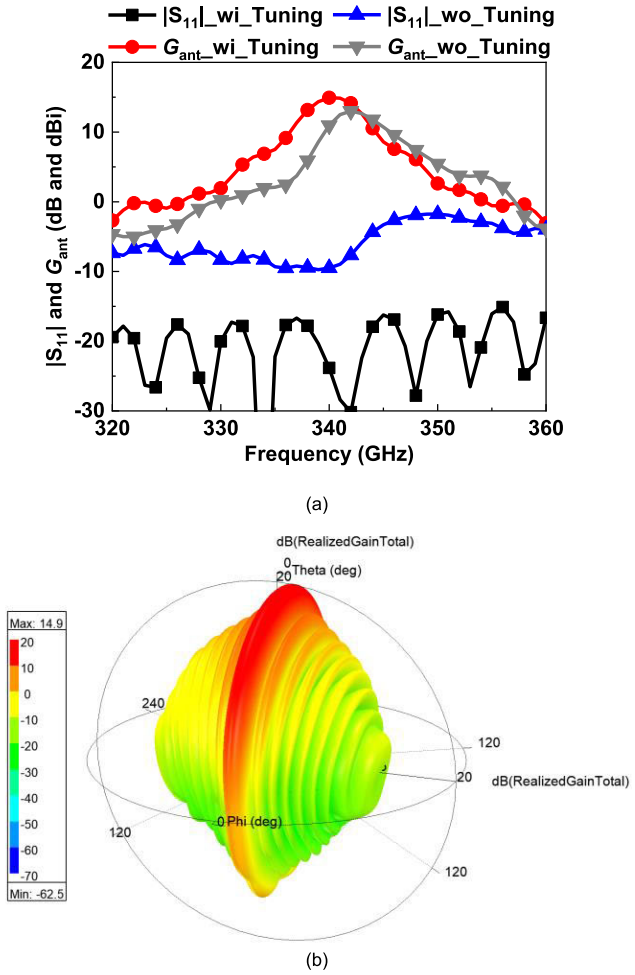

FIGURE 8. (a) Simulated input return loss and antenna gain, and (b) radiation pattern of the 1 × 16 series-fed IPD antenna array.

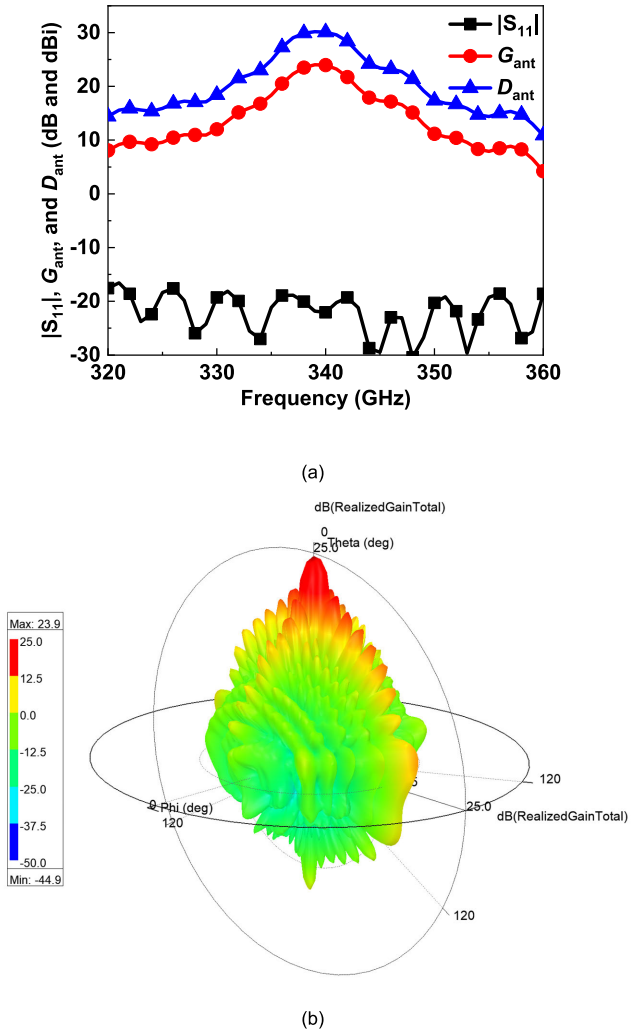

FIGURE 9. (a) Simulated input return loss and antenna gain, and (b) radiation pattern of the 16 × 16 THz IPD antenna array.

2.6 dB at 340 GHz, estimated by (2) as $G_{1\times16\ \text{Series Array}}$, G_{Patch}, and N_2 of 14.9 dBi, 5.5 dBi, and 16, respectively, are given.

Once the designs of the 1-to-16 corporate-feed network and the 1 × 16 series-fed antenna array are completed, they are integrated together to form the proposed 16 × 16 THz IPD antenna array. The array gain of the 16 × 16 THz IPD antenna array can be estimated to be 25 dBi by (1) as $G_{1\times16\ \text{Series Array}}$, IL_{FN1}, and N_1 of 14.9 dBi, 1.9 dB, and 16, respectively, are given. As shown in Fig. 9(a), the proposed 16 × 16 antenna array can give simulated $|S_{11}|$ of −22.1 dB, antenna gain G_{ant} of 23.9 dBi, and antenna directivity D_{ant} of 30 dB at 340 GHz while having $|S_{11}|$ lower than −16.6 dB from 320 to 360 GHz. The simulated array gain is close to the estimated one of 25 dBi using (1), which verifies the proposed design procedure for the antenna array design. The 3-dB gain bandwidth is from 336.5 to 342.5 GHz. The 3D radiation pattern is depicted in Fig. 9(b). The proposed antenna array can give simulated HPBW of 5.6° at 340 GHz. Given the HPBW, the antenna directivity of the proposed antenna array can also be estimated to be 30.1 dB by 32400/HPBW^2 [34], which is close to the simulated one of 30 dB. Such an antenna array with high directivity and narrow HPBW is very suitable for lensless THz imaging applications.

B. THZ INTERCONNECT DESIGN

A THz interconnect is used to smoothly trasfer a signal from a CMOS chip to an IPD one. It shall provide good input return loss and low insertion loss at the frequency of interest. Fig. 10(a) shows the proposed 340-GHz THz interconnect with the source impedance Z_{Chip} and load impedance Z_{IPD} of 43.1 Ω, respectively. Two transmission lines TL_3 and TL_4 are deployed on a CMOS chip and an IPD chip, respectively. As Ni-Au micro-bumps with thickness of 8 μm are used to bond the CMOS chip to the IPD chip using an Au-Au thermo-compressive flip-chip packaging technique, the vertical distance between TL_3 and TL_4 becomes close. TL_3 can electromagnetically couple to TL_4 to form a broadside coupled-line structure. The Ni-Au bumps are also utilized to connect the chip ground to the IPD ground, which can reduce the power loss occurred in the signal return path.

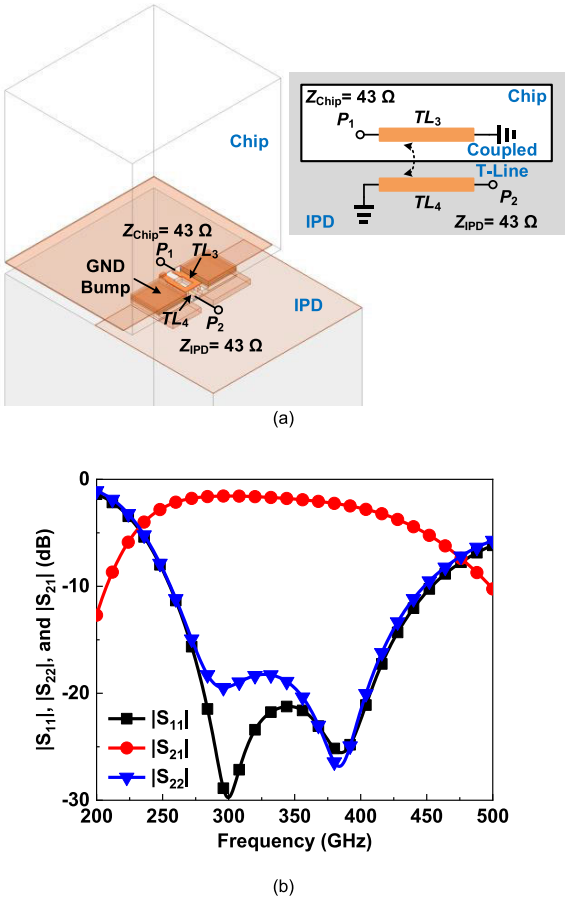

FIGURE 10. (a) Proposed CMOS-to-IPD THz interconnect and its physical structure. (b) Simulated S-parameters of the proposed THz interconnect.

In addition, TL_3 and TL_4 are routed as coils to reduce the interconnect size. By properly designing the lengh and width of TL_3 and TL_4 to control the operaton band and coupling strength and in-band gain ripple, respectively, the proposed THz interconnect can carry a signal at the input port P_1 on the CMOS chip to the output port P_2 on the IPD chip with low-loss and broadband characterisics. Fig. 10(b) exhibits the simulated S-parameters of the proposed THz interconnect as the lengh and width of TL_3 and TL_4 are designed as 179 and 14 μm and 191 and 10 μm, respectively. The proposed THz interconnect can give simulated $|S_{11}|$, $|S_{22}|$, and $|S_{21}|$ of -21.3, -18.6, and -1.8 dB at 340 GHz, respectivley, while keeping $|S_{11}|$ and $|S_{22}|$ lower than -10 dB from 256 to 448 GHz. The 3-dB bandwidth of $|S_{21}|$ is from 230 to 446 GHz. Such a low-loss and broadband THz interconnect is very suitable to heterogeneously integrate different chip modules realized in different technologies onto a common IPD carrier for realizing high-performance and high-integration THz systems.

C. CMOS POWER DETECTOR DESIGN

As shown in Fig. 2(a), a CMOW power detector plays one of the critical roles of the proposed heterogeneously-integrated THz imager for lensless THz imaging applications. The 16 × 16 THz IPD antenna array receives a signal from a DUT and outputs the received signal to the CMOS power detector. The power detector can detect the power level P_{in} of the input signal and then produces an output voltage V_{out} proportional to P_{in}. As illustrated in Fig. 1(a), step motors are used to move the DUT within an interested imaging area. By recording the output voltage of the CMOS power detector, the THz image of the DUT can be constructed.

For the design considerations of the CMOS power detector, it shall provide high voltage responsivity R_V defined as V_{out}/P_{in} and low noise equivalent power (NEP) at the frequency of interest. Fig. 11 shows the proposed THz power detector implemented in a 0.18-μm CMOS technology. It utilizes the transistor's even-order nonlinearity to detect the input power level. The transistor's I/V equation can be written as a power series expansion

$$i_D = I_{D0} + \sum_{n=1}^{\infty} \frac{f^{(n)}(V_{GS})}{n!} v_{gs}^n, \tag{4}$$

where I_{D0}, V_{GS}, and v_{gs} are the dc bias current of the transistor, the gate bias voltage of the transistor, and the small-signal gate-to-source voltage, respectively. For small signal detection, i_D can be approximately as

$$i_D \cong I_{D0} + f^{(1)}(V_{GS}) v_{gs} + \frac{f^{(2)}(V_{GS})}{2} v_{gs}^2. \tag{5}$$

Assume the signal to be detected can be writing as $A\cos(2\pi f_{THz} t)$ where A and f_{THz} are the voltage amplitude and the frequency of the input signal, respectively. After substituting v_{gs} of $A\cos(2\pi f_{THz} t)$ into (5), the differential output voltage $v_{D,diff}$ at the drains of M_1 and M_2 can be derived

$$\begin{aligned} v_{D,diff} &= (i_{D1} - i_{D2}) R_D = (i_{D1} - I_{D0}) R_D \\ &= f^{(1)}(V_{GS}) \cos(2\pi f_{THz} t) A R_D \\ &\quad + \frac{f^{(2)}(V_{GS})}{2} \left[\frac{1 + \cos(4\pi f_{THz} t)}{2} \right] A^2 R_D, \end{aligned} \tag{6}$$

where $R_{D1} = R_{D2} = R_D$ is the load resistor. Note that a replica circuit composed of C_{B2}, R_{B2}, M_2, and R_{D2} is grounded at its input to provide a voltage reference for the differential IF amplifier. The high frequency terms at f_{THz} and $2f_{THz}$, respectively, in (6) are filtered out by the low-pass filters formed by the load resistor R_D and the parasitic capacitances existed at the drains of M_1 and M_2. Hence, only the dc term in (6) remains at the drains of M_1 and M_2, that is,

$$v_{D,diff} \approx \frac{f^{(2)}(V_{GS})}{4} A^2 R_D. \tag{7}$$

Equation (7) indicates that the output differential voltage is proportional to the input power. Therefore, the power detection function can be achieved. To maximize the detector's voltage responsivity R_V, the second-order nonlinear term $f^{(2)}(V_{GS})$ must be maximized by appropriately selecting the gate bias V_{GS} of the transistors. The transistor M_1 with the minimum transistor size of 1.5 μm is selected to reduce the transistor's parasitic effect. The gate bias V_{GS} applied

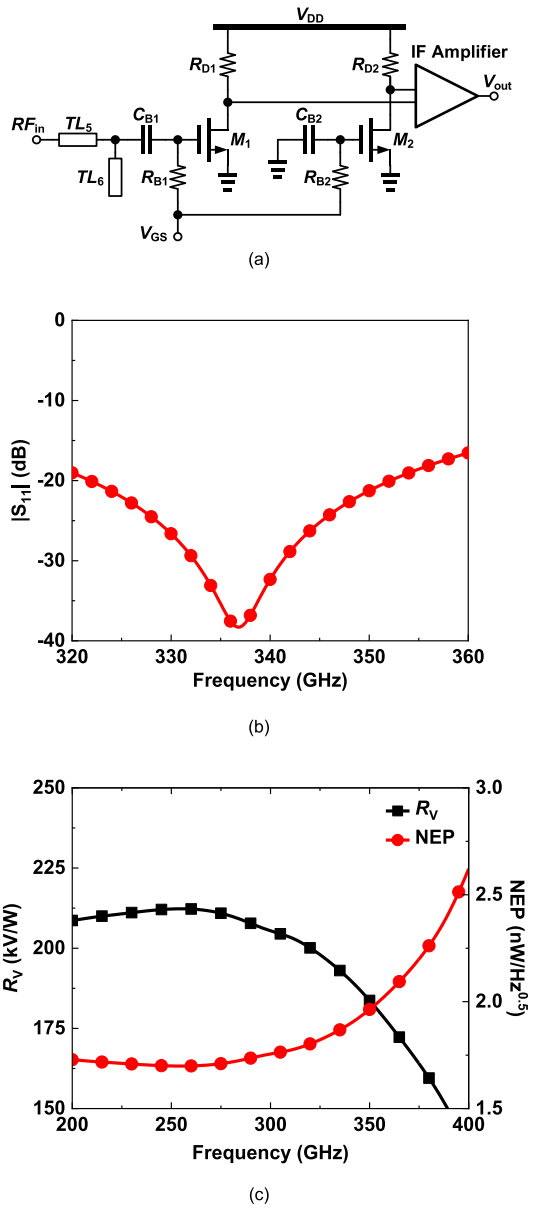

FIGURE 11. (a) Proposed THz CMOS power detector circuit. (b) Simulated input return loss. (c) Simulated R_V and NEP.

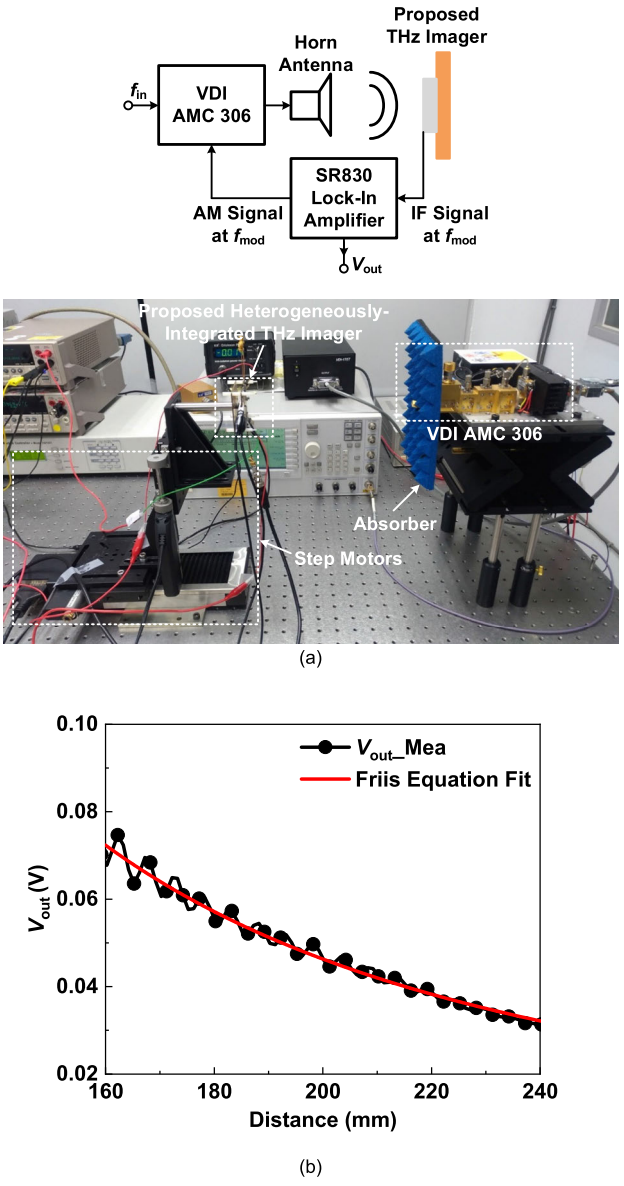

FIGURE 12. (a) Experimental setup for measuring R_V and NEP. (b) Measured output voltage versus the distance between the signal source and the THz imager and the fitting of the Friis transmission equation.

through an 8-kΩ resistor R_{B1} is designed at 0.48 V to give the maximal second-order nonlinear term $f^{(2)}(V_{GS})$, leading to the maximal second-order nonlinear output current. Finally, the load resistor R_{D1} converts the output current to the desired output voltage. An input matching network formed by the transmission lines of TL_5 and TL_6 is exploited to match the input impedance to 43.1 Ω. As will be explained later in Section III, a locking-amplifier technique is used to catch the desired signal while rejecting undesired noise at the detector output. The IF bandwidth at the drain of M_1 shall be wider than the chopping frequency f_{mod} of the locking-amplifier. To maximize R_V, the value of the load resistor R_{D1} shall be as high as possible. However, higher R_{D1} exhibits narrower IF bandwidth. To make good tradeoff between R_V and IF bandwidth, R_{D1} is designed as 200 kΩ to have R_V of 11.5 kV/W while ensuring the IF bandwidth wider than 1.1 MHz to satisfy the lock-in amplifier requirement. R_V is further increased by a differential IF amplifier with phase margin of 88°, voltage gain of 24.4 dB, and input referred noise of 7.7 μV/Hz$^{0.5}$ at 1 kHz.

Fig. 11 shows the simulated input return loss, R_V, and NEP of the proposed CMOS power detector as the chopping frequency f_{mod} is 1 kHz. The simulated $|S_{11}|$ is −30.5 dB at 340 GHz and lower than −10 dB from 288 to 390 GHz. R_V and NEP at 1-kHz f_{mod} can be 190.2 kV/W and 1.9 nW/Hz$^{0.5}$ at 340 GHz, respectively. Note that the highest f_{mod} is only 1 kHz due to the available lock-in amplifier in the measurement. If a lock-in amplifier with a higher f_{mod} can be acquired, for example, a 1-MHz f_{mod}, the NEP of the proposed THz power detector can be

TABLE 1. Performance Summary and Comparison with Prior Works.

Reference	JSSC'13 [8]	TTST'16 [9]	TTST'18 [12]	TTST'17[(g)] [35]	TTST'19[(d)] [30]	JIMTW'20 [29]	SJ'20 [17]	**This Work**
Support Lensless THz Imaging Systems?	Yes	Yes	No	No	Yes	Yes	No	**Yes**
f_o (GHz)	282	823	320	860	402	303	200	**328**
R_V (kV/W)	5.1	2.6	3.8	3.3	39[(e)]	3.6	19	**967[(a)]**
NEP (pW/Hz$^{0.5}$)	33	42	16.9	106	45[(f)]	12.46	535	**180[(b)]**
Chopping Frequency (kHz)	1000	1000	78.125	0.117	--	500	NA	**1**
Antenna Directivity (dB)	6.7[(c)]	7[(c)]	NA	5.36[(c)]	NA	7.27	NA	**30**
Antenna Gain (dBi)	1.3[(c)]	5.8[(c)]	NA	3.41[(c)]	18.7	NA	NA	**23.9[(c)]**
HPBW (degree)	83.2[(h)]	80.4[(h)]	NA	97.1[(h)]	20.9[(h)(i)]	77.9[(h)]	NA[(h)]	**4**
Technology	130-nm CMOS	130-nm CMOS	130-nm SiGe	180-nm CMOS	28-nm CMOS + 3D Printed + Micromachining	65-nm CMOS	350-nm CMOS	**180-nm CMOS + IPD**

(a) Effective voltage responsivity as defined in (5). (b) NEP of 16.6 pW/Hz$^{0.5}$ can be obtained if the chopping frequency can be increased to 1 MHz. (c) Simulated result. (d) Heterodyne receiver, instead of a power detector. (e) Conversion gain in dB. (f) Noise figure in dB. (g) Integrate an ADC. (h) HPBW is estimated by $(32400/D_{ant})^{0.5}$ where D_{ant} represents the antenna directivity [34]. (i) Estimated by using the antenna gain of 18.7 dB.

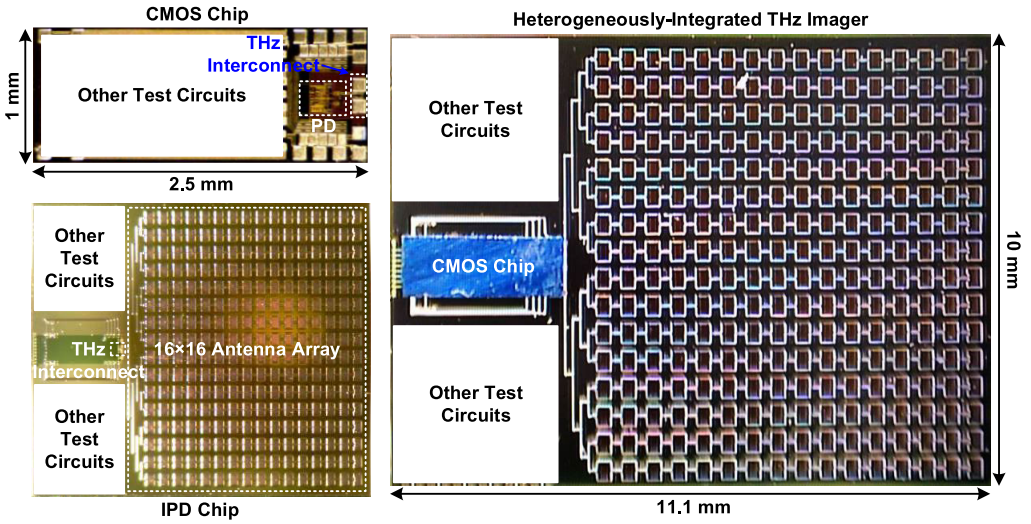

FIGURE 13. Photo of the proposed heterogeneously-integrated THz imager. PD represents the CMOS power detector.

reduced dramatically from 1.9 nW/Hz$^{0.5}$ to 24 pW/Hz$^{0.5}$ at 340 GHz.

III. CHARACTERIZATION METHOD

To characterize the proposed heterogeneously-integrated THz imager, a far-field measurement setup as shown in Fig. 12(a) is established. A locking-amplifier technique is employed to measure a weak desired signal from a noisy environment. A commercial signal source module with a model number of AMC 306 from the Virginia Diodes Inc. (VDI) is used to generate a THz signal from 315 to 350 GHz with the output power of 8 dBm. Absorbers are attached around the THz signal source to reduce reflections for minimizing a standing-wave effect. The THz signal which is amplitude modulated (AM) by a chopping signal with a frequency of f_{mod} from a lock-in amplifier is radiated out by a WR2.2 horn antenna, propagates in the air, and is then received by the proposed THz imager. Finally, the THz imager's IF output is sent back to the lock-in amplifier to generate the desired output volage V_{out}.

The THz imager is attached on three step motors from Newport with minimum incremental motion better than 0.3 μm to control its motion along the x, y, and z directions. The alignment between the signal source and the THz imager is achieved by moving the THz imager to a position where the measured V_{out} is maximal as it is scanned along an x-y plane. The received power by the THz imager can be estimated by the Friis transmission equation

$$P_R = G_T G_R (\frac{\lambda}{4\pi R})^2 P_T, \tag{8}$$

where P_R, P_T, G_T, G_R, R, and λ are the received power, the output power of the signal source, the antenna gain of the horn antenna, the antenna gain of the THz imager, the distance between the signal source and the THz imager, and the wavelength, respectively. The output voltage V_{out} of the THz

imager can be found as

$$\begin{aligned} V_{\text{out}} &= R_{\text{V}} P_{\text{R}} \\ &= R_{\text{V}} G_{\text{T}} G_{\text{R}} (\frac{\lambda}{4\pi R})^2 P_{\text{T}}. \\ &= (\frac{\lambda}{4\pi R})^2 G_{\text{T}} P_{\text{T}} R_{\text{V,eff}}. \end{aligned} \tag{9}$$

where R_{V} is the voltage responsivity of the CMOS power detector and $R_{\text{V,eff}}$ is defined as $R_{\text{V}} \times G_{\text{R}}$. Since P_{T}, G_{T}, R, and λ are known, $R_{\text{V,eff}}$ can be acquired by measuring V_{out}. Note that prior works reported the measured R_{V} instead of $R_{\text{V,eff}}$ [8], [9]. However, they use simulated antenna directivity to estimate R_{V}, which is not only inaccurate, but it also did not take the receiver antenna performance into consideration. $R_{\text{V,eff}}$ defined in this work is more meaningful since it considers the characteristics of the receiver antenna and the power detector simultaneously. Moreover, $R_{\text{V,eff}}$ is completed determined by the experimental results without using any simulated parameters. The proposed concept of $R_{\text{V,eff}}$ for the THz imager characterization is similar to the equivalent isotropically radiated power defined as $G_{\text{T}} \times P_{\text{T}}$ which is used to represent the performance of a transmitter.

As (9) is used to find $R_{\text{V,eff}}$, the exact distance R between the signal source and the THz imager cannot be accurately measured by a ruler. The equation (9) can be modified as

$$V_{out} = \frac{C}{(R_m + \Delta R)^2}, \tag{10}$$

where C, R_{m}, and ΔR are a constant equal to $R_{\text{V,eff}} G_{\text{T}} P_{\text{T}} \lambda^2 / (16\pi^2)$, the distance measured by a ruler, and a constant used to calibrate the distance R_{m}, respectively. In addition, as shown in Fig. 12(b), the measured output voltage fluctuates as the distance between the signal source and the THz imager is varied due to an unavoidable standing-wave effect, even though the absorbers have been deployed around the measurement environment. This standing-wave effect makes it ambiguous to determine the measured V_{out} for $R_{\text{V,eff}}$ calculation. If higher or lower V_{out} is taken at a specific distance, it will result in overestimation or underestimation of $R_{\text{V,eff}}$, respectively. To solve the issue, a nonlinear curve fit technique provided by the Origin tool is exploited to fit the measured output voltages at different distances to the Friis transmission equation in (10). Fig. 12(b) shows the result of the nonlinear curve fit as the fitting values of C and ΔR are 1.85×10^3 V-mm^2 and 5.2 mm, respectively. Clearly, the fitting curve follows the measured V_{out} very well. Once C is acquired from the measured results, $R_{\text{V,eff}}$ can be obtained by $16\pi^2 C / (R_{\text{V,eff}} G_{\text{T}} P_{\text{T}} \lambda^2)$ accordingly.

IV. EXPERIMENTAL RESULTS

Fig. 13 shows the photos of a 0.18-μm CMOS chip, an IPD chip, and a heterogeneously-integrated THz imager. The CMOS and IPD chips with sizes of 1 mm × 1.5 mm and 10 mm × 11.1 mm, including other test circuits, are fabricated by Taiwan Semiconductor Manufacturing Company and Advanced Furnace Systems Corp., respectively. The Ni/Au bumps for the THz packaging are fabricated using a mask-less metallization process by TAIWAN UYEMURA [36]. The CMOS chip is then bonded to the IPD one by a flip-chip bonding machine to form the proposed heterogeneously-integrated THz imager using an Au-Au thermo-compressive packaging technique conducted in Taiwan Semiconductor Research Institute. The proposed characterization method explained in Section III is employed to characterize the THz imager.

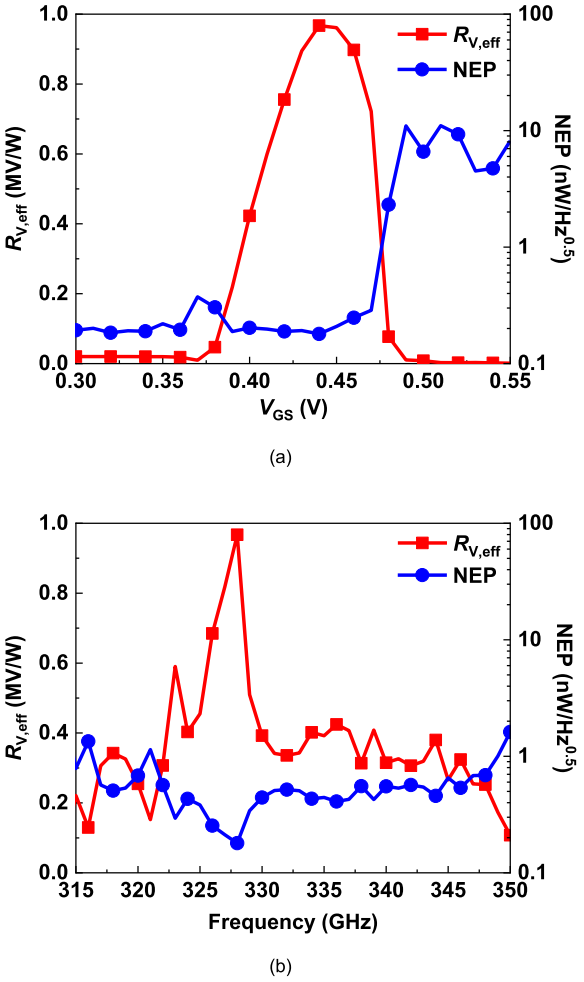

FIGURE 14. (a) Measured $R_{\text{V,eff}}$ and NEP versus the transistor gate bias. (b) Measured $R_{\text{V,eff}}$ and NEP versus the operation frequency.

The voltage responsivity and noise equivalent power of the proposed THz imager are measured using the experimental setup shown in Fig. 12(a). The chopping frequency f_{mod} is 1 kHz. Fig. 14(a) shows the measured $R_{\text{V,eff}}$ and NEP versus the transistor's gate bias V_{GS} as the input frequency is 328 GHz. The optimal gate bias of 0.44 V is obtained to provide peak $R_{\text{V,eff}}$ and minimum NEP of 0.967 MV/W and 0.18 nW/Hz$^{0.5}$ at 340 GHz, respectively. The measured frequency response of $R_{\text{V,eff}}$ and NEP is illustrated in Fig. 14(b) as the THz imager is biased at the optimal V_{GS} of 0.44 V. The proposed THz imager can give maximal $R_{\text{V,eff}}$ of 0.967 MV/W and minimum NEP of 0.18 nW/Hz$^{0.5}$

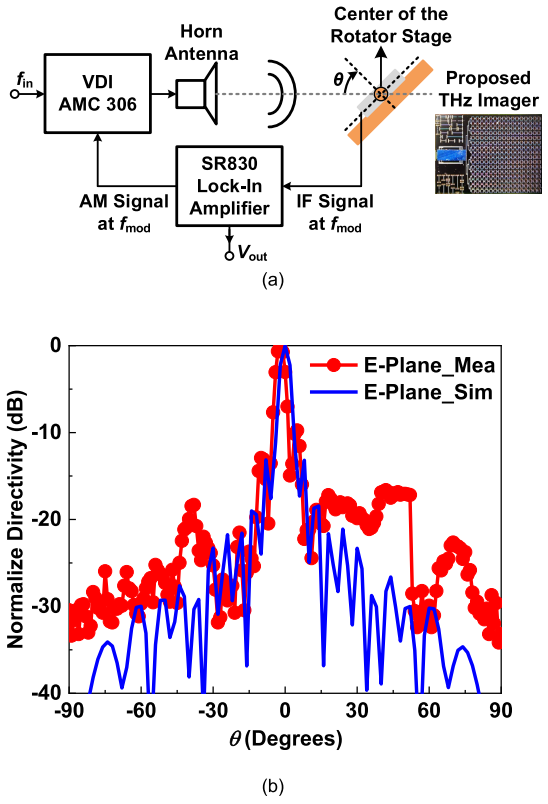

FIGURE 15. (a) Experimental setup for measuring the radiation pattern. (b) Measured radiation pattern.

at 328 GHz. Note that if a lock-in amplifier with higher f_{mod} is available, for instance, 1-MHz f_{mod}, the NEP can be reduced dramatically from 0.18 nW/Hz$^{0.5}$ to 16.6 pW/Hz$^{0.5}$ at 328 GHz.

The radiation pattern of the proposed THz imager is characterized by an experimental setup shown in Fig. 15(a) using the same characterization method explained in Section III. The THz imager is attached and aligned to the center of a rotator stage, which ensures the distance between the signal source and the THz imager is fixed as the rotator stage rotates. Therefore, the output voltage at different reception angle of θ can be measured, i.e., the radiation pattern of the THz imager can be acquired. Fig. 15(b) shows the measured radiation pattern of the THz imager at 328 GHz. The measured result tracks the simulated one very well. The measured HPBW is 4°, close to the simulated value of 5.6°, that is, the measured directivity of the proposed THz imager is roughly equal to the simulated one, i.e., 30 dB at 328 GHz. Note that as compared to the prior work in [30] which realizes a 3D printed micromachining horn antenna with simulated antenna gain of 18.7 dB at 440 GHz, the proposed THz imager with the 16 × 16 IPD antenna array has higher measured antenna directivity of 30 dB. This implies that the proposed THz imager not only can be employed to implement a lensless THz imaging system, but it can also provide better image resolution as compared to that in [30]. Table 1 shows the performance summary of the proposed heterogeneously-integrated THz imager and its comparison with prior works. Clearly, the proposed heterogeneously-integrated THz imager exhibits higher voltage responsivity, lower NEP, low complexity, higher directivity, and narrower HPBW as compared with prior works. Such a THz imager with advantages of high directivity and narrow HPBW is very suitable for lensless THz imaging applications. Moreover, to the best of the authors' knowledge, the proposed THz imager integrates the highest number of antennas and provides the highest antenna directivity and the narrowest HPBW at THz frequencies reported thus far.

V. CONCLUSION

A low-cost and planar 328-GHz heterogeneously-integrated THz imager is proposed and verified by experimentla results. An Au-Au thermo-compressive packaging technique using the proposed low-loss and broadband THz interconnect is employed to heterogueneously package a CMOS THz power detector in a 0.18-μm CMOS tehcnoogoy with a 16 × 16 THz antenna array in an IPD technology. The proposed THz imager can give the measured effective voltage responsivity of 0.967 MV/W and minimum NEP of 0.18 nW/Hz$^{0.5}$ at 328 GHz as the chopping frequency is 1 kHz. The measured antenna directivity and HPBW can be 30 dB and 4° at 328 GHz, respectively. Such a THz imager with high-directivity and narrow-HPBW advantages is very suitable for lensless THz imaging applications.

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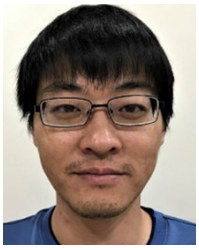

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