IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received June 22, 2021, accepted July 8, 2021, date of publication July 15, 2021, date of current version July 26, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3097371

Switched-Capacitor-Inductor Active-Switched Boost Inverters With High Boost Ability

ANH-TUAN HUYNH[1], ANH-VU HO[2], AND TAE-WON CHUN[1], (Member, IEEE)
[1]Department of Electrical Engineering, University of Ulsan, Ulsan 44610, South Korea
[2]School of Engineering, Eastern International University, Binh Duong 75115, Vietnam

Corresponding author: Tae-Won Chun (twchun@mail.ulsan.ac.kr)

This work was supported in part by the Korea Institute of Energy Technology Evaluation and Planning (KETEP), and in part by the Ministry of Trade, Industry and Energy (MOTIE) of the Republic of Korea under Grant 20194030202310.

ABSTRACT This paper proposes a novel topology, named the switched-capacitor-inductor active-switched boost inverter (SCL-ASBI), based on a switched boost inverter (SBI). The proposed SCL-ASBI allows a high voltage gain with fewer components used in the impedance network. It can be extended to an *n*-cell by adding one inductor, one diode, and two capacitors for further improving the boost capability. A comparative analysis between the proposed SCL-ASBI topology and four different topologies based on the SBI is presented. The closed-loop output voltage control scheme of the SCL-ASBI is suggested to linearly control the ac output voltage in a wide range. The extended-boost SCL-ASBI (EB/SCL-ASBI) topology, implemented by adding one cell to the SCL-ASBI, is introduced to achieve a higher voltage gain. Both the simulation studies and the experimental results obtained from a prototype built in the laboratory are carried out to verify the theoretical analysis and performance of the proposed topologies.

INDEX TERMS Boost capability, high voltage gain, impedance network, multicell topology, switched-capacitor-inductor.

I. INTRODUCTION

The quasi-Z-source inverter (qZSI) is an attractive choice in renewable energy generation applications due to its boost capability in a single power conversion stage and the continuous dc input current [1]. It can raise the dc-link voltage with a shoot-through state implemented by conducting both the upper and lower switches at the same phase leg of the inverter. Because dead-time is not needed, the reliability can be enhanced and the distortion of the ac output voltage due to the dead-time can be reduced. The qZSI has been applied to photovoltaic (PV) power generation systems and electric vehicles due to its advantages [2]–[6]. In spite of the above-mentioned merits of the classic qZSI, its practical boost ability is not enough for industrial applications requiring a high voltage gain.

To achieve higher voltage gain, several topologies have been implemented by inserting additional inductors, capacitors, and diodes into the impedance network based on the (quasi-) Z-source inverter, as introduced in [7]–[14]. These are referred to as switched-inductor (SL) qZSI/ZSI [7], [8], diode-assisted or capacitor-assisted extended boost continuous qZSI [9], generalized multicell switched-inductor and switched-capacitor ZSIs [10], ripple input current SL-qZSI (rSL-qZSI) and continuous current SL-qZSI (cSL-qZSI) [11], enhanced-boost ZSI with switched Z-impedance [12], enhanced-boost qZSI with two switched impedance networks (EB-qZSI) [13], and qZSI with two quasi-Z-source networks [14]. These topologies require many passive components, which leads to an increase in the volume and cost of the power circuit.

The switched boost inverter (SBI) topology was introduced in [15], [16]. The SBI can reduce the number of passive components in the impedance network by adding one more switching device. However, it has a lower boost factor compared with classic ZSI/qZSI, and its source current is discontinuous. To solve the drawbacks of the basic SBI, the embedded-type quasi-switched boost inverter (qSBI) was proposed in [17]. Its boost factor builds up to the same value as that of the classic qZSI while keeping the same number of components as those of the basic SBI. In addition, the embedded-type qSBI has a continuous dc source current. The comparative analysis between a single-phase embedded-type qSBI and a single-phase qZSI is presented

The associate editor coordinating the review of this manuscript and approving it for publication was Chi-Seng Lam.

in [18]. The pulse width modulation (PWM) strategies for a single-phase qSBI proposed by [19] and [20] can reduce the voltage stress across the capacitors and switches and obtain a lower high-frequency inductor current and capacitor voltage ripples with higher efficiency, compared with the conventional PWM method.

A half-bridge switched boost inverter (HBSBI) topology combining two basic SBIs and a single-phase half-bridge inverter is presented in [21]. The HBSBI topology has a higher boost factor compared to the classic ZSI. However, its dc source current is discontinuous. To achieve a continuous dc source current while retaining the benefits of the HBSBI, the topology implemented by replacing the SBI of the HBSBI topology with the qSBI [17] is proposed by [22].

Several topologies to further enhance the voltage gain by adding inductors, capacitors, and diodes to the basic SBI structure are introduced [23]–[29]. A topology for ZSI based on a switched impedance network is proposed in [23]. In [24], two types of high voltage gain quasi-switched boost inverter (HG-qSBI) and the PWM technique are presented to achieve a high voltage gain with low input current ripple. By applying the concept of the SL technique to the SBI topology, a class of SL boost inverters (SLBIs) in [25] and the continuous active SL boost quasi-ZSI (cASLB-qZSI) in [26] provide a higher boost ability. The enhanced-boost quasi-ZSI with an active switched Z-network (EB/ASN-qZSI) proposed in [27] has the same boost factor as the EB-qZSI [13] but reduces the number of LC pairs. The capacitor-assisted switched capacitor extended boost ZSI (CSC-EB-ZSI) proposed in [28] is implemented by adding one switch and one diode to the capacitor-assisted extended boost qZSI (CEB-qZSI) [9] to increase the voltage conversion ratio. Another possible solution to further increase the voltage gain is to apply the multicell scheme, which can be implemented by connecting n number of cells in a cascade, to the topologies based on the active switched boost inverters such as: the active-switched-capacitor/switched-inductor qZSI (ASC/SL qZSI) [29], continuous input current qZSI (CC-qZSI) [30], and active-switched-capacitor qZSI (ASC-qZSI) [31].

In this paper, a novel topology, named a switched-capacitor-inductor active-switched boost inverter (SCL-ASBI) based on the SBI structure, is proposed. The proposed SCL-ASBI offers a higher boost ability with a smaller number of components in the impedance network in comparison with the different SBI-based topologies. The operation analysis and the impedance parameter design of the proposed SCL-ASBI topology are presented. A comparison between the proposed SCL-ASBI and four other SBI-based topologies is performed. The closed-loop output voltage control scheme is suggested to linearly control the ac output voltage of the proposed SCL-ASBI topology over a wide range. It can be extended to achieve a higher voltage gain by cascading n-cells, where one cell consists of one inductor, one diode, and two capacitors. By adding one cell to the SCL-ASBI, the extended-boost SCL-ASBI (EB/SCL-ASBI) topology is introduced. The proposed topologies and voltage control scheme can be applied to provide the desired voltage to the critical or local load under islanding mode of a microgrid connecting the low-voltage renewable energy sources like a PV array or fuel-cell (FC) stack, and to drive the traction motor of small-sized FC vehicles. The performances of the two proposed topologies and the output voltage control scheme are validated by both simulations and the experimental results obtained from the prototype built in the laboratory.

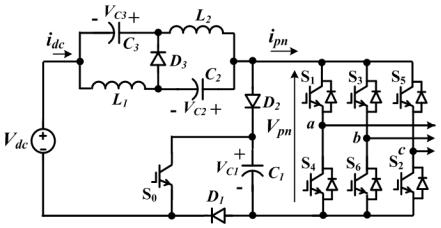


FIGURE 1. Structure of the proposed SCL-ASBI topology.

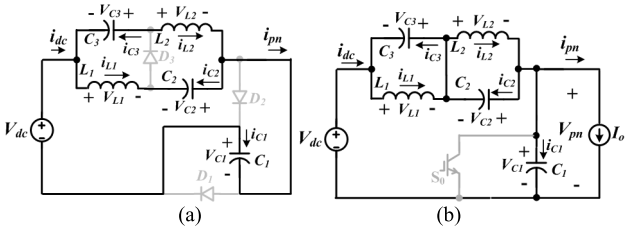


FIGURE 2. Equivalent circuits for the SCL-ASBI: (a) ST state, (b) NST state.

II. OPERATION ANALYSIS OF PROPOSED SCL-ASBI TOPOLOGY

The operation principle of the proposed SCL-ASBI topology will be described.

A. OPERATING PRINCIPLES OF SCL-ASBI

Fig. 1 shows the structure of the proposed SCL-ASBI topology in which an impedance network, composed of one switch (S_0), two inductors (L_1, L_2), three capacitors (C_1, C_2, C_3), and three diodes (D_1, D_2, D_3), is connected to the three-phase inverter bridge. The proposed SCL-ASBI has two operating states like a non-shoot-through (NST) state and shoot-through (ST) state. The equivalent circuits of the SCL-ASBI topology in the ST and NST states are shown in Figs. 2(a) and 2(b), respectively.

In the ST state shown in Fig. 2(a), the inverter side is shorted by both upper and lower switches on any phase leg, and the switching device S_0 is switched on during this state. The three diodes D_1, D_2, and D_3 are off in the ST state. The two inductors L_1 and L_2 store energy from the dc input source and the three capacitors C_1, C_2, and C_3 through the inverter bridge and switch S_0. The three capacitors are then discharged. From Fig. 2(a), the inductor voltages, capacitor currents, and dc-link voltage are written by

$$V_{L1} = V_{dc} + V_{C2} + V_{C1}, \quad V_{L2} = V_{dc} + V_{C3} + V_{C1} \quad (1)$$

$$i_{C2} = -i_{L1} = -i_{L2} - i_{C1}, \quad i_{C3} = -i_{L2} = -i_{L1} - i_{C1} \quad (2)$$

$$V_{pn} = 0. \tag{3}$$

In the NST state shown in Fig. 2(b), the proposed inverter operates as a conventional voltage source inverter. During this state, the switch S_0 is switched off, whereas the three diodes D_1, D_2, and D_3 are on. The three capacitors are charged, and the two inductors supply energy to the inverter. The peak dc-link voltage across the inverter bridge $\hat{V}_{pn}$ is equal to the capacitor voltage V_{C1}. From Fig. 2(b), the inductor voltages, capacitor currents, and dc-link voltage are written by

$$V_{L1} = -V_{C3} = V_{dc} + V_{C2} - V_{C1}, \quad V_{L2} = -V_{C2} \tag{4}$$
$$i_{C2} = i_{L2} - i_{C1} - I_0, \quad i_{C3} = i_{L1} - i_{C1} - I_o \tag{5}$$
$$V_{pn} = \hat{V}_{pn} = V_{C1}. \tag{6}$$

It can be assumed that $V_{L1} = V_{L2}$, $V_{C2} = V_{C3}$, $i_{L1} = i_{L2}$, $i_{C2} = i_{C3}$ due to the symmetrical structure of the impedance network. Utilizing the voltage-second balance principle to the inductor L_1 or L_2 from (1) and (4) over one switching period T_s, the three capacitor voltages can be expressed as a function of the shoot-through duty ratio D, which is defined as a ratio of the shoot-through time T_{sh} to one switching period T_s, as follows:

$$V_{C1} = \frac{1}{1-4D} V_{dc}, \quad V_{C2} = V_{C3} = \frac{2D}{1-4D} V_{dc} \tag{7}$$

Utilizing the ampere-second balance principle to the capacitors C_1 and C_2 from (2) and (5) over one switching period T_s, the average of the two inductor currents can be derived as

$$\bar{i}_{L1} = \bar{i}_{L2} = \frac{1-D}{1-4D} I_o. \tag{8}$$

Because the peak dc-link voltage across the inverter bridge $\hat{V}_{pn}$ is identical with the capacitor voltage V_{C1} from (6), the boost factor of the proposed SCL-ASBI can be derived as

$$B = \frac{\hat{V}_{pn}}{V_{dc}} = \frac{V_{C1}}{V_{dc}} = \frac{1}{1-4D}. \tag{9}$$

B. IMPEDANCE PARAMETER DESIGN OF SCL-ASBI

The inductors and capacitors in the impedance network of the proposed SCL-ASBI topology are designed to limit the switching frequency current and voltage ripples within the desired values. The equivalent series resistances (ESRs) of the capacitors influence the capacitor voltage ripple at the transition between the NST and ST states. In this paper, the capacitors are designed neglecting the effects of the ESRs of the capacitors. Using the concept for a simplified equivalent dc load R_I, the load current I_o can be expressed as [24]

$$I_o = \frac{\hat{V}_{pn}}{R_I}. \tag{10}$$

The operating frequency of the capacitor and the inductor is twice the switching frequency. In the ST state, the inductor current increases linearly while charging energy from the capacitors and dc voltage source. From (1), the peak-to-peak current ripple of the inductors L_1 and L_2 during the ST state of the proposed SCL-ASBI is expressed as

$$\Delta i_{L1,2} = \frac{V_{dc} + V_{C2} + V_{C1}}{L_{1,2}} \frac{DT_s}{2}. \tag{11}$$

From (7), (8), (9), (10), and (11), the inductances of L_1 and L_2 can be designed as

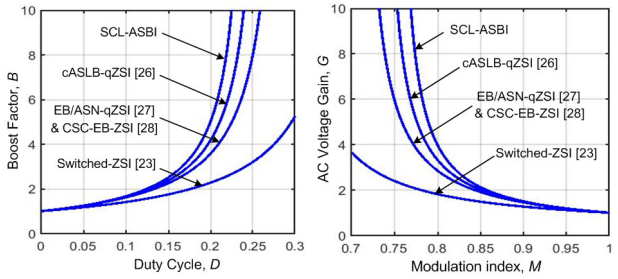
$$L_{1,2} = \frac{D(1-4D)R_I}{r_{L1,2}\% \cdot f_s} \tag{12}$$

where $r_{L1,2}\%$ is defined as a ratio of the peak-to-peak inductor current ripple to the average current of inductors L_1 and L_2 as $\Delta i_{L1,2}/\bar{i}_{L1,2}$, and f_s is the switching frequency.

Similarly, from (2), (7), (8), (9), and (10), the capacitances can be designed as

$$C_1 = \frac{D(1-D)}{(1-4D)R_I \cdot r_{C1}\% \cdot f_s} \tag{13}$$
$$C_2 = C_3 = \frac{(1-D)}{4(1-4D)R_I \cdot r_{C2,3}\% \cdot f_s} \tag{14}$$

where $r_{C1}\% = \Delta V_{C1}/V_{C1}$ and $r_{C2,3}\% = \Delta V_{C2,3}/V_{C2,3}$.



(a) (b)

FIGURE 3. A comparison of the boost factor and ac voltage gain: (a) boost factor versus a duty ratio, (b) ac voltage gain versus the modulation index.

III. COMPARATIVE ANALYSIS WITH THE SAME TYPE OF TOPOLOGIES

The comparative analysis is performed in terms of the number of components, boost factor, voltage and current stresses of the proposed SCL-ASBI topology with the four other SBI-based topologies such as the Switched-ZSI [23], cASLB-qZSI [26], EB/ASN-qZSI [27], and CSC-EB-ZSI [28].

A. COMPARISON OF THE BOOST FACTOR AND AC VOLTAGE GAIN

The boost factor is an important item to evaluate the performance of the topology. Fig. 3(a) shows plots of the boost factors with the variation of the shoot-through duty ratio for the proposed SCL-ASBI and four different topologies. The proposed SCL-ASBI has the highest boost factor over the overall range of the shoot-through duty ratio, compared with four different topologies.

The ac voltage gain G is defined as

$$G = \frac{\hat{v}_o}{V_{dc}} = M \cdot B \tag{15}$$

TABLE 1. Number of components used in the impedance networks.

Components	cASLB-qZSI	Switched-ZSI	EB/ASN-qZSI	CSC-EB-ZSI	SLC-ASBI
Inductors	3	2	2	3	2
Capacitors	3	2	2	4	3
Diodes	6	4	4	3	3
Switches	1	1	1	1	1

where M and $\hat{v}_o$ are the modulation index and the peak output phase voltage, respectively. The relationship between M and B is dependent on the modulation techniques. The simple boost PWM control method [20] is applied to the proposed topology. In the simple boost PWM control method, the shoot-through duty ratio D is lower than $(1 - M)$. Using the relationship of $D = 1 - M$, the ac voltage gain G can be expressed as a function of M. Fig. 3(b) shows plots of the ac voltage gains G versus the modulation index M for the analyzed topologies. The proposed topology has the highest ac voltage gain, which results in a high-quality output voltage waveform with a low total harmonic distortion (THD).

B. COMPARISON OF THE NUMBER OF COMPONENTS

Table 1 displays a comparison of the number of passive and active components used in the impedance network of the five topologies. From this table, the proposed SCL-ASBI requires one more capacitor and one less diode than the switched-ZSI and EB/ASN-qZSI topologies. Compared with the CSC-EB-ZSI and cASLB-qZSI topologies, the proposed SCL-ASBI approach saves one inductor and one capacitor (or three diodes).

C. COMPARISON OF VOLTAGE AND CURRENT STRESSES

The voltage stresses across the capacitors, diodes, and switch in the impedance network change with the boost factor and dc input voltage. The inductor current stress varies with the boost factor and load current. To achieve a fair comparison of the voltage stresses for five topologies, the ratio of voltage stress to the root mean square (RMS) value of ac output voltage is compared. The inductor current stress is expressed as the boost factor and shoot-through duty ratio. The ratios of the voltage stresses across capacitors, diodes, and switch to the RMS value of the ac output voltage, the inductor current stresses, and the diode and capacitor current stresses for the five topologies are summarized in Table 2.

Figs. 4(a) and 4(b) compare the total voltage stress ratios of the capacitors and diodes, respectively, between the proposed SCL-ABSI topology and four different topologies. The total capacitor voltage stress ratio of the proposed SCL-ABSI is lower than that of the EB/ASN-qZSI when the duty ratio D is less than 0.17, and it is lower than cASLB-qZSI when the duty ratio D is less than 0.2. The total diode voltage stress ratio of the proposed SCL-ASBI is slightly higher than that of the EB/ASN-qZSI. The proposed SCL-ASBI topology provides the total capacitor and diode voltage stress ratios in the comparatively intermediate range. Fig. 4(c) depicts the

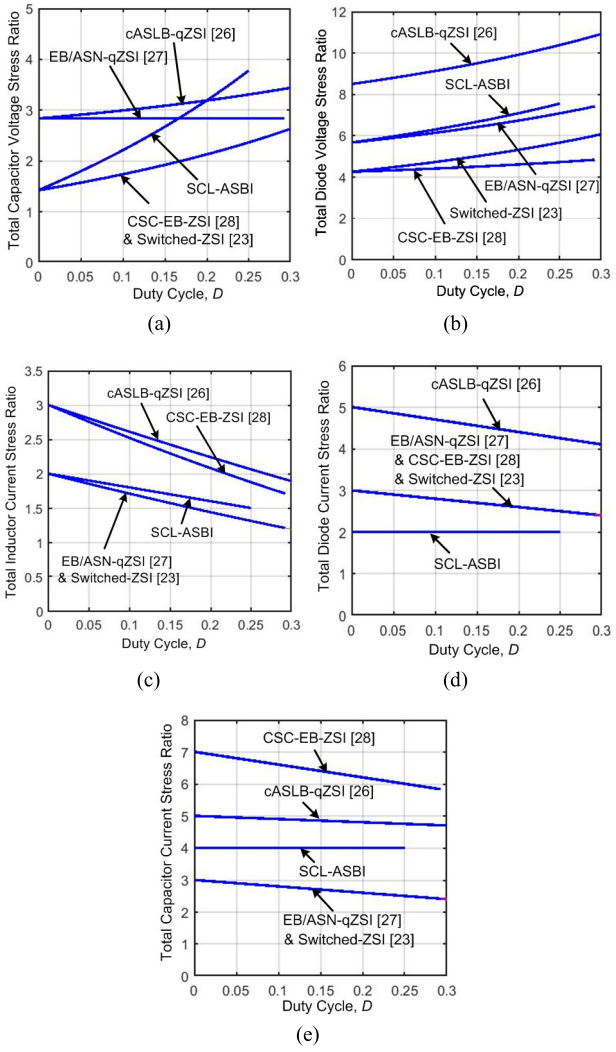


FIGURE 4. Voltage and current stresses comparison: (a) capacitor voltage stress comparison, (b) diode voltage stress comparison, (c) inductor current stress comparison, (d) diode current stress comparison, (e) capacitor current stress comparison.

ratio of the total inductor current stress to $(B \cdot I_o)$ for the five topologies. The EB/ASN-qZSI topology has the lowest total inductor current stress ratio, followed by the proposed SCL-ASBI topology. The proposed SCL-ASBI topology provides the total inductor current stress ratio in a relatively low range. Figs. 4(d) and 4(e) depict the ratio of the total diode and capacitor current stresses to $(B \cdot I_o)$ for the five topologies, respectively. The proposed SCL-ASBI topology provides the lowest total diode current stress ratio. Both the EB/ASN-qZSI and switched-ZSI topologies have the lowest total capacitor current stress ratio, followed by the proposed SCL-ASBI topology.

D. COMPARISON SUMMARY

Compared with the four other SBI-based topologies, the proposed SCL-ASBI topology has the highest ac voltage gain, which is an important item to evaluate the performance of the topology. The highest ac voltage gain results in a high output voltage with a low THD.

TABLE 2. Comparison of voltage stresses across capacitors, diodes and switch, and current stresses of inductors, diodes, and capacitors.

	cASLB-qZSI [26]		Switched-ZSI [23]		EB/ASN-qZSI [27]		CSC-EB-ZSI [28]		SCL-ASBI	
Capacitor Voltage Stress Ratio	C_1, C_2	$\sqrt{2}$	C_1	$\frac{\sqrt{2}}{1-D}$	C_1	$\frac{\sqrt{2}}{1-D}$	C_1, C_3 C_4	$\frac{\sqrt{2}D}{1-D}$	C_1	$\frac{\sqrt{2}}{1-D}$
	C_3,	$\frac{\sqrt{2}D}{1-D}$	C_2	$\frac{\sqrt{2}D}{1-D}$	C_2	$\frac{\sqrt{2}(1-2D)}{1-D}$	C_2	$\frac{\sqrt{2}(1-2D)}{1-D}$	C_2, C_3	$\frac{2\sqrt{2}D}{1-D}$
	$\sum_{i=1} V_{Ci}$	$\frac{\sqrt{2}(2-D)}{1-D}$	$\frac{\sqrt{2}(1+D)}{1-D}$		$2\sqrt{2}$		$\frac{\sqrt{2}(1+D)}{1-D}$		$\frac{\sqrt{2}(1+4D)}{1-D}$	
Diode Voltage Stress Ratio	D_1, D_4	$\sqrt{2}$	D_1, D_2	$\frac{\sqrt{2}}{1-D}$	D_1, D_2	$\frac{\sqrt{2}}{1-D}$	D_1, D_3	$\frac{\sqrt{2}}{1-D}$	D_1,D_2	$\frac{\sqrt{2}}{1-D}$
	D_2, D_3 D_5, D_6	$\frac{\sqrt{2}}{1-D}$	D_3	$\sqrt{2}$	D_3	$2\sqrt{2}$	D_2	$\frac{\sqrt{2}(1-2D)}{1-D}$	D_3	$\frac{2\sqrt{2}}{1-D}$
			D_4	$\frac{\sqrt{2}D}{1-D}$	D_4	$\frac{\sqrt{2}D}{1-D}$				
	$\sum_{i=1} V_{Di}$	$\frac{2\sqrt{2}(3-D)}{1-D}$	$\frac{3\sqrt{2}}{1-D}$		$\frac{\sqrt{2}(4-D)}{1-D}$		$\frac{\sqrt{2}(3-2D)}{1-D}$		$\frac{4\sqrt{2}}{1-D}$	
Switch Voltage Stress Ratio	S	$\sqrt{2}$	S_0	$\frac{\sqrt{2}}{1-D}$	S	$\frac{\sqrt{2}}{1-D}$	S_0	$\frac{\sqrt{2}(1-2D)}{1-D}$	S_0	$\frac{\sqrt{2}}{1-D}$
Inductor Current Stress	L_1, L_2	$(1-D)BI_o$	L_1	$(1-D)BI_o$	L_1	$(1-D)BI_o$	L_1	$(1-D)BI_o$	L_1, L_2	$(1-D)BI_o$
	L_3	$(1-D)^2 BI_o$	L_2	$(1-D)^2 BI_o$	L_2	$(1-D)^2 BI_o$	L_2, L_3	$(1-D)^2 BI_o$		
	$\sum_{i=1} I_{Li}$	$(D^2-4D+3)BI_o$	$(D^2-3D+2)BI_o$		$(D^2-3D+2)BI_o$		$(2D^2-5D+3)BI_o$		$2(1-D)BI_o$	
Diode Current Stress	D_1, D_2, D_3 D_4, D_6	$(1-D)BI_o$	D_1, D_3 D_4	$(1-D)BI_o$	D_1	$(1-D)^2 BI_o$	D_1	BI_o	D_1	$(1-2D)BI_o$
					D_2	$D(2-D)BI_o$			D_2	$2DBI_o$
	D_5	$2DBI_o$	D_2	DBI_o	D_3, D_4	$(1-D)BI_o$	D_2, D_3	$(1-D)BI_o$	D_3	BI_o
	$\sum_{i=1} I_{Di}$	$(5-3D)BI_o$	$(3-2D)BI_o$		$(3-2D)BI_o$		$(3-2D)BI_o$		$2BI_o$	
Capacitor Current Stress	C_1, C_3	$2BI_o$	C_1	$(2-D)BI_o$	C_1	$(2-D)BI_o$	C_1	BI_o	C_1	$2BI_o$
							C_2	$(3-2D)BI_o$		
	C_2	$(1-D)BI_o$	C_2	$(1-D)BI_o$	C_2	$(1-D)BI_o$	C_3	$(2-D)BI_o$	C_2, C_3	BI_o
							C_4	$(1-D)BI_o$		
	$\sum_{i=1} I_{Ci}$	$(5-D)BI_o$	$(3-2D)BI_o$		$(3-2D)BI_o$		$(7-4D)BI_o$		$4BI_o$	

The proposed SCL-ASBI topology with the two inductors exhibits the total inductor current stress ratio in a relatively low range. It provides the lowest total diode current stress ratio. The total capacitor voltage and current stress ratios, and the total diode voltage stress ratio of the proposed topology are in the comparatively intermediate range. The number of components used in the impedance network of the proposed SCL-ASBI is the same as that of the switched-ZSI and EB/ASN-qZSI topologies, and less than that of the CSC-EB-ZSI and cASLB-qZSI topologies.

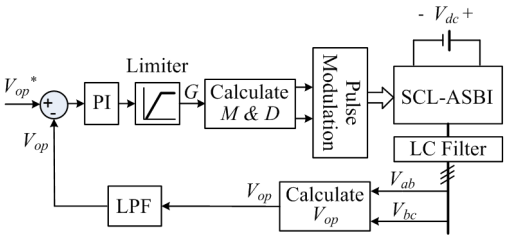


FIGURE 5. AC output voltage control loop of the SCL-ASBI topology.

IV. AC OUTPUT VOLTAGE CONTROL SCHEME

Fig. 5 shows the ac output voltage control loop of the proposed SCL-ASBI topology to offer a desired voltage to the ac load or microgrid. Substituting (9) into (15) and using the relationship of ($D = 1 - M$) under the simple boost PWM control method, the peak ac output voltage can be expressed as the modulation index as follows:

$$\hat{v}_o = \frac{M}{4M-3} V_{dc} = G \cdot V_{dc} \tag{16}$$

The ac output voltage can be adjusted by regulating the modulation index M. The plot of the ac voltage gain G versus M of the proposed SCL-ASBI topology is shown

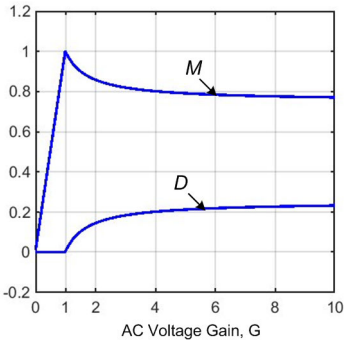


FIGURE 6. Variations of *M* and *D* versus *G*.

in Fig. 3(b). From Fig. 3(b), the ac voltage gain (or output voltage) decreases nonlinearly as M increases. This nonlinearity between the output voltage and M may deteriorate the performance of the transient response of the ac output voltage control. The ac voltage gain G is adopted at the ac output voltage control loop to improve the transient response of the ac output voltage control. Because the ac voltage gain G is proportional to the ac output voltage from (16), it can linearly control the output voltage.

The peak output voltage V_{op} is estimated from the two measured line-to-line voltages V_{ab} and V_{bc}. The ac voltage gain G is assigned as the output of the peak output voltage PI (Proportional-Integral) controller. There are two voltage control modes according to the range of G, the boost control mode at $G \geq 1$ and the buck mode at $0 \leq G < 1$. The M and D values are determined in the range of G as follows:

$$M = \frac{3G}{4G-1}, \quad D = 1 - M \text{ at } G > 1 \tag{17}$$

$$M = G, \quad D = 0 \text{ at } 0 \leq G < 1 \tag{18}$$

Fig. 6 shows the variations of M and D in the range from 0 to 10 of G. When the proposed SCL-ASBI operates in the buck mode in the range $0 \leq G < 1$, the modulation index M is proportional to the ac voltage gain G under $D = 0$. Therefore, the ac output control is only controlled by the modulation index M without the shoot-through state. When the proposed SCL-ASBI operates in the boost mode where $G \geq 1$, the modulation index M decreases and the shoot-through duty ratio D increases as the ac voltage gain G increases. The PWM signals of the seven switches are generated by the values of both M and D calculated from (17) and (18).

V. OPERATION ANALYSIS OF MULTICELL SCL-ASBI TOPOLOGY

The extended-boost SCL-ASBI (EB/SCL-ASBI) topology is implemented by adding one cell to the SCL-ASBI topology. To further enhance the boost ability, n member cells are added in the impedance network of the proposed SCL-ASBI structure to form the multi-cell SCL-ASBI (Mc/SCL-ASBI) topology. The structures and operation principles for both the EB/SCL-ASBI and Mc/SCL-ASBI topologies will be described, respectively.

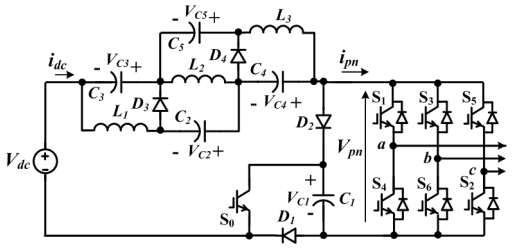


FIGURE 7. Structure of the proposed EB/SCL-ASBI topology.

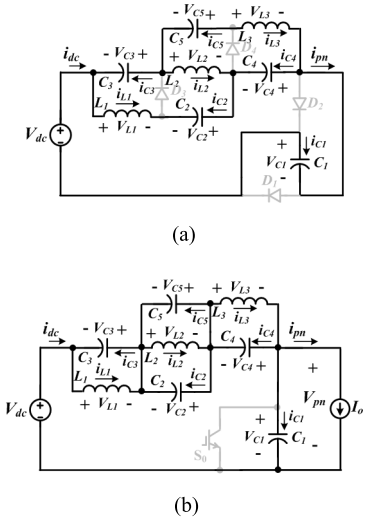


FIGURE 8. Equivalent circuits for the EB/SCL-ASBI: (a) ST state, (b) NST state.

A. OPERATING PRINCIPLES OF EB/SCL-ASBI

One cell consisting of two capacitors, one inductor, and one diode is connected to the SCL-ASBI in cascade, as shown in Fig. 7. This topology is named the extended-boost SCL-ASBI (EB/SCL-ASBI). Fig. 8 shows the equivalent circuits of the EB/SCL-ASBI in the ST and NST states, respectively.

In the ST state shown in Fig. 8(a), the inverter side is shorted by both upper and lower switches of any phase leg, and the switching device S_0 is switched on. All four diodes are off during this state. Three inductors L_1, L_2, and L_3 store energy from the dc input source, along with the five capacitors C_1, C_2, C_3, C_4, and C_5. All five capacitors are discharged. From Fig. 8(a), the inductor voltages and capacitor currents are written by

$$V_{L1} = V_{dc} + V_{C2} + V_{C4} + V_{C1} \tag{19}$$

$$i_{C1} = i_{C3} - i_{L1}, \quad i_{C2} = -i_{L1}, \quad i_{C3} = i_{C5} - i_{L2}. \tag{20}$$

In the NST state shown in Fig. 8(b), the inverter provides voltage to the load side. During this state, the switching device S_0 is switched off, whereas all four diodes are on. The dc input voltage and three inductors transfer energy to both the inverter and the capacitors. Thus, all five capacitors are charged. From Fig. 8(b), the inductor voltages, capacitor currents, and dc-link voltage are written by

$$V_{L1} = -V_{C3}, \quad V_{L1} + V_{L2} + V_{L3} = V_{dc} - V_{C1} \tag{21}$$

$$i_{C1} + i_{C3} = -I_o + i_{L1} \tag{22}$$
$$V_{pn} = V_{C1}. \tag{23}$$

It can be assumed that $V_{L1} = V_{L2} = V_{L3}$, $V_{C2} = V_{C3} = V_{C4} = V_{C5}$, $i_{L1} = i_{L2} = i_{L3}$, $i_{C2} = i_{C5}$, $i_{C3} = i_{C4}$ due to the symmetrical structure of the impedance network. Utilizing the voltage-second balance principle to the inductor L_1 from (19) and (21) over one switching period T_s, the five capacitor voltages can be derived as

$$V_{C1} = \frac{1}{1-6D} V_{dc} \tag{24}$$
$$V_{C2} = V_{C3} = V_{C4} = V_{C5} = \frac{2D}{1-6D} V_{dc}. \tag{25}$$

Utilizing the ampere-second balance principle to the capacitors C_1 and C_3 from (20) and (22) over one switching period T_s, the average of the three inductor currents can be derived as

$$\bar{i}_{L1} = \bar{i}_{L2} = \bar{i}_{L3} = \frac{1-D}{1-6D} I_o. \tag{26}$$

Because the peak dc-link voltage across the inverter bridge $\hat{V}_{pn}$ is identical with the capacitor voltage V_{C1} from (23), the boost factor of the proposed EB/SCL-ASBI topology can be derived as

$$B = \frac{\hat{V}_{pn}}{V_{dc}} = \frac{V_{C1}}{V_{dc}} = \frac{1}{1-6D} \tag{27}$$

where the duty ratio is limited to 1/6. Fig. 9 shows the boost factor and ac voltage gain versus the duty ratio D of the two proposed topologies. The boost factor and ac voltage gain of the EB/SCL-ASBI are considerably higher than those of SCL-ASBI.

B. IMPEDANCE PARAMETER DESIGN OF EB/SCL-ASBI

The inductors and capacitances of the proposed EB/SCL-ASBI topology are design with the same method as the SCL-ASBI topology. From (19), the peak-to-peak current ripple of the three inductors during ST state of the proposed EB/SCL-ASBI are written by

$$\Delta i_{L1,2,3} = \frac{V_{dc} + V_{C1} + V_{C2} + V_{C4}}{L_{1,2,3}} \frac{DT_s}{2}. \tag{28}$$

From (10), (24), (25), (26) and (27), the inductances of L_1, L_2, and L_3 can be designed as

$$L_{1,2,3} = \frac{D(1-6D)R_I}{r_{L1,2,3}\% \cdot f_s} \tag{29}$$

where $r_{L1,2,3}\%$ is defined as a ratio of the peak-to-peak inductor current ripple to the average current of the three inductors as $\Delta i_{L1,2,3}/\bar{i}_{L1,2,3}$.

Similarly, from (10), (20), (24), (25), (26), and (27), the capacitances can be designed as

$$C_1 = \frac{3D(1-D)}{2(1-6D)R_I \cdot r_{C1}\% \cdot f_s} \tag{30}$$
$$C_2 = C_5 = \frac{(1-D)}{4(1-6D)R_I \cdot r_{C2,5}\% \cdot f_s} \tag{31}$$

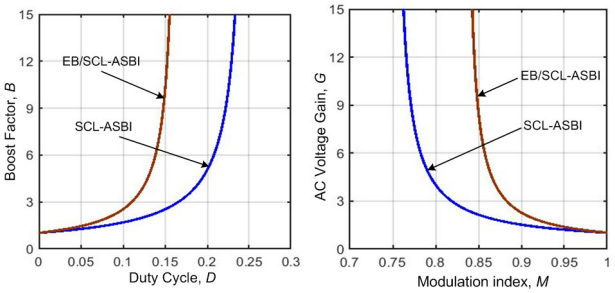


FIGURE 9. A comparison of the two proposed topologies: (a) boost factor versus duty ratio, (b) ac voltage gain versus modulation index.

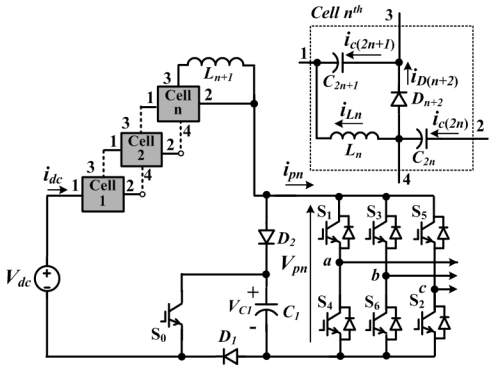


FIGURE 10. Structure of the Mc/SCL-ASBI topology.

$$C_3 = C_4 = \frac{(1-D)}{2(1-6D)R_I \cdot r_{C3,4}\% \cdot f_s} \tag{32}$$

where $r_{C1}\% = \Delta V_{C1}/V_{C1}$, $r_{C2,5}\% = \Delta V_{C2,5}/V_{C2,5}$, and $r_{C3,4}\% = \Delta V_{C3,4}/V_{C3,4}$.

C. OPERATING PRINCIPLES OF MC/SCL-ASBI

The structure of a multi-cell SCL-ASBI (Mc/SCL-ASBI) topology is shown in Fig. 10. It can be extended by adding more cells to the impedance network in order to achieve higher boost capability. The n^{th} cell is organized using one inductor L_n, one diode D_{n+2}, and two capacitors C_{2n} and C_{2n+1}. The operations in the ST and NST states of the Mc/SCL-ASBI are nearly the same as those of the EB/SCL-ASBI. By applying a similar method to the Mc/SCL-ASBI, the capacitor voltages, the average of the inductor currents, and boost factor can be expressed as

$$V_{C1} = \frac{1}{1-2(n+1)D} V_{dc} \tag{33}$$
$$V_{C2} = \cdots = V_{C(2n+1)} = \frac{2D}{1-2(n+1)D} V_{dc} \tag{34}$$
$$I_{L1} = \cdots = I_{Ln} = I_{L(n+1)} = \frac{1-D}{1-2(n+1)D} I_o \tag{35}$$
$$B = \frac{\hat{V}_{pn}}{V_{dc}} = \frac{V_{C1}}{V_{dc}} = \frac{1}{1-2(n+1)D} \tag{36}$$

where the range of D is between 0 and $1/2(n+1)$.

D. IMPEDANCE PRAMETER DESIGN OF MC/SCL-ASBI

The inductors and capacitances of the proposed Mc/SCL-ASBI topology are design with the same method as the SCL-ASBI and EB/SCL-ASBI topologies.

The inductances of $L_1 \cdots$, and L_n can be designed as

$$L_{1\cdots n} = \frac{D(1-(2n+1)D)R_I}{r_{L1\cdots n}\% \cdot f_s} \tag{37}$$

where $r_{L1\cdots n}\%$ is defined as a ratio of the peak-to-peak inductor current ripple to the average current of the n number of inductors as $\Delta i_{L1\cdots n}/\bar{i}_{L1\cdots n}$.

Similarly, the capacitances can be designed as

$$\begin{aligned} C_1 &= \frac{(n+1)D(1-D)}{2[1-2(n+1)D]R_I \cdot r_{C1}\% \cdot f_s} \\ C_2 = C_{2n+1} &= \frac{(1-D)}{4[1-2(n+1)D]R_I \cdot r_{C2}\% \cdot f_s} \\ C_3 = C_{2n} &= \frac{2(1-D)}{4[1-2(n+1)D]R_I \cdot r_{C3}\% \cdot f_s} \end{aligned} \tag{38}$$

$$C_4 = C_{2n-1} = \frac{3(1-D)}{4[1-2(n+1)D]R_I \cdot r_{C4}\% \cdot f_s} \tag{39}$$

$$\bullet \quad \bullet$$

where $r_{C1}\% = \Delta V_{C1}/V_{C1}$, $r_{C2}\% = \Delta V_{C2}/V_{C2}$, $r_{C3}\% = \Delta V_{C3}/V_{C3}$, and $r_{C4}\% = \Delta V_{C4}/V_{C4}$.

E. COMPARATIVE ANALYSIS OF MC/SCL-ASBI

Figs. 11(a), 11(b), 11(c), and 11(d) compare the boost factors, the total voltage stress ratios of the capacitors and diodes, and the ratio of the total inductor current stress to $(B \cdot I_o)$ for SCL-ASBI, EB/SCL-ASBI, Mc/SCL-ASBI with three cells, and Mc/SCL-ASBI with four cells, respectively. The range of D is from 0 to $1/2(n+1)$. The Mc/SCL-ASBI with one cell becomes equivalent to the SCL-ASBI, and the Mc/SCL-ASBI with two cells becomes equivalent to the EB/SCL-ASBI. The boost factor is considerably increased by adding more cells. The total capacitor voltage stress ratio increases almost linearly with respect to D, and its slope is shaper as the number of cells increases. Both the total diode voltage stress and total inductor current stress increase in almost proportion to the increase in the number of cells.

The power loss of n^{th} cell shown in Fig. 10 is calculated for analyzing the efficiency variations to the increase in the number of cells. The power loss of n^{th} cell consists of capacitor loss, inductor loss, and diode loss.

The power loss of the two capacitors C_{2n} and C_{2n+1} is calculated as

$$P_{c(n)} = r_{c(2n)} \cdot I^2_{c(2n)\_rms} + r_{c(2n+1)} \cdot I^2_{c(2n+1)\_rms} \tag{40}$$

where $r_{c(2n)}$ and $r_{c(2n+1)}$ represent the ESRs of C_{2n} and C_{2n+1}, respectively, and $I_{c(2n)\_rms}$ and $I_{c(2n+1)\_rms}$ are the RMS values of two capacitor currents, respectively, and derived as

$$I_{c(2n)\_rms} = \frac{2\sqrt{D(1-D)}}{1-2(n+1)D} I_o \tag{41}$$

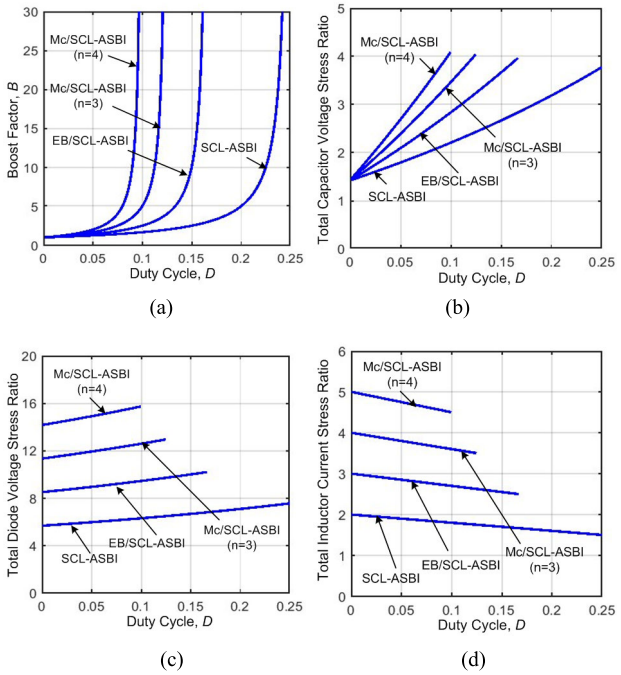


FIGURE 11. A comparison of the boost factor, voltage and current stresses of Mc/SCL-ASBI: (a) boost factor comparison, (b) capacitor voltage stress comparison, (c) diode voltage stress comparison, (d) inductor current stress comparison.

$$I_{c(2n+1)\_rms} = \frac{\sqrt{D(1-D)}}{1-2(n+1)D} I_o. \tag{42}$$

The power loss of inductor L_n is calculated as

$$P_{Ln} = r_{Ln} \cdot I^2_{Ln\_rms} \tag{43}$$

where r_{Ln} represents the ESR of L_n, and I_{Ln_rms} is the RMS value of inductor current and derived as [32]

$$I_{Ln\_rms} = \sqrt{I^2_{Ln} + \Delta I^2_{Ln}/12} \tag{44}$$

where ΔI_{Ln} is the peak-to-peak current ripple of L_n.

The conduction loss of diode D_{n+2} associated with the forward voltage drop $(V_{F(n+2)})$ and series resistance $(R_{D(n+2)})$ is calculated as

$$P_{D(n+2)} = V_{F(n+2)} \cdot I_{Ln} + R_{D(n+2)} I^2_{D(n+2)\_rms} \tag{45}$$

where $I_{D(n+2)\_rms}$ is the RMS value of diode current and calculated as

$$I_{D(n+2)\_rms} = \frac{\sqrt{1-D}}{1-2(n+1)D} I_o. \tag{46}$$

From (41), (42), (44), and (46), the two capacitor currents, inductor current, and diode current of the n^{th} cell increase as the number of cells n increases. Assuming the parameters relative to the cell power loss calculation constant, the power loss of each cell depends on the output power and the number of cell stage. Thus, the power loss of higher stage cell is further increased.

Fig 12 compares the efficiencies of the proposed topologies with increase in the number of cells. The PLECS software

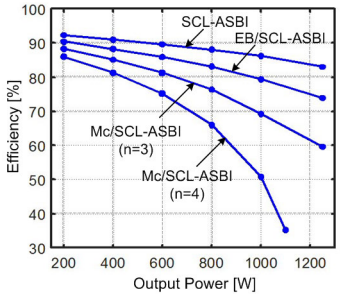


FIGURE 12. A comparison of the efficiency of Mc/SCL-ASBI.

TABLE 3. System parameters.

Parameter		Value
DC input voltage, V_{dc}		40 V
Fundamental frequency, f		60 Hz
Switching frequency, f_s		5 kHz
Output filter inductor, L_f		0.6 mH
Output filter capacitor, C_f		100 μF
SCL-ASBI	Capacitor, C_1	200 μF
	Capacitors, $C_2 = C_3$	260 μF
	Inductor, $L_1 = L_2$	3 mH
	Resistive load	50 Ω
EB/SCL-ASBI	Capacitor, C_1	100 μF
	Capacitor, $C_2 = C_5$	200 μF
	Capacitor, $C_3 = C_4$	400 μF
	Inductor, $L_1 = L_2 = L_3$	2 mH
	Resistive load	100 Ω

is employed to calculate the efficiency. The efficiency of the proposed topologies decreases by adding more cells. When the output power increases, the efficiency of the Mc/SCL-ASBI with four cells is rapidly lowered due to the increase in the power loss of high stage cell.

The appropriate number of cells of the Mc/SCL-ASBI topology is chosen by considering the overall efficiency, capacitor and diode voltage stresses, and inductor current stress as well as the boost capability.

VI. SIMULATION AND EXPERIMENTAL RESULTS

For the validation of the effectiveness of the two proposed topologies, simulations and experimental results are carried out. The system parameters adopted at the simulation and experiment are depicted in Table 3. The capacitances of the proposed SCL-ASBI from Table 3 are selected so that their capacitor voltage ripple ratio is within the range between 1 % and 1.5 % by using (13) and (14). The inductances are determined so that their peak-to-peak inductor current ripple ratio is within 20 - 25 % by using (12). The capacitances and inductances of the EB/SCL-ASBI topology are designed by using similar methods applied to the SCL-ASBI.

A. SIMULATION RESULTS

The simulations are performed by using the PSIM program. Fig. 13 shows the simulation results of the proposed

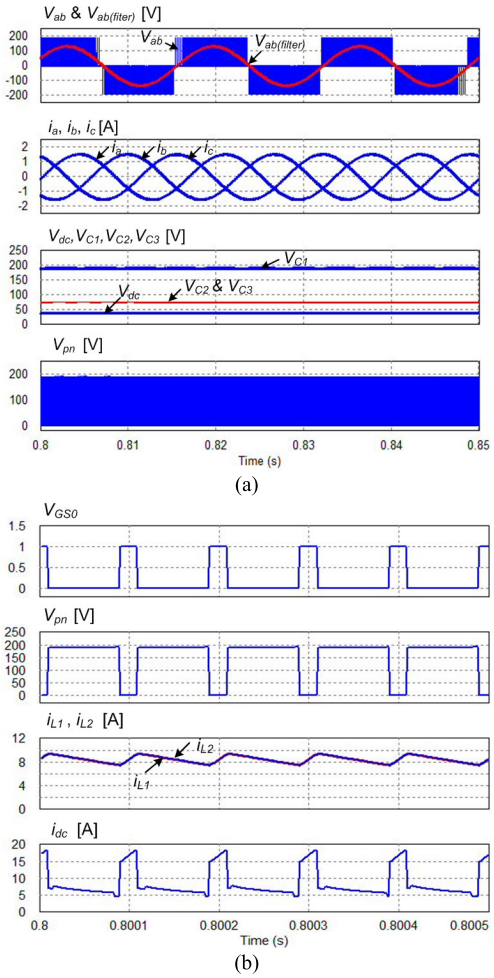


FIGURE 13. Simulation results for the SCL-ASBI when $D = 0.2$, $M = 0.8$, and $V_{dc} = 40$ V.

SCL-ASBI topology when $D = 0.2$, $M = 0.8$, and $V_{dc} = 40$ V. From 13(a), the ac output voltage filtered by the LC filter of 94 Vrms is provided. The average voltage of C_2 and C_3 is 76 V, and peak dc-link voltage is boosted to 191 V from a dc input voltage of 40 V. Fig. 13(b) shows waveforms of the gating signal of switch S_0, dc-link voltage, two inductor currents, and dc input current during four switching cycles. The gating signal of switch S_o is applied and the dc-link voltage is zero during the shoot-through period. The two inductor currents have almost identical waveforms. Their average current is 8.5 A, and the peak-to-peak inductor current ripple ratio is about 23 %. The dc input current has a ripple, because the dc input current is (i_{L1} - i_{c1}) in the NST state and $2i_L$ in the ST state.

Fig. 14 shows the simulation results of the proposed EB/SCL-ASBI topology when $D = 0.15$, $M = 0.85$, and $V_{dc} = 40$ V. The three-phase output voltages after filtering are balanced and boosted to 190 Vrms from a dc input voltage of 40 V. The voltages across the four capacitors C_2, C_3, C_4, and C_5 are the same 110 V value. The dc-link voltage, which is equal to the capacitor voltage V_{C1}, is boosted to 366 V.

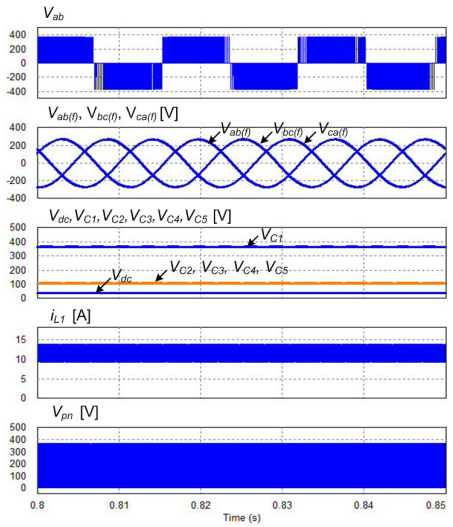


FIGURE 14. Simulation results for the EB/SCL-ASBI when $D = 0.15$, $M = 0.85$, and $V_{dc} = 40$ V.

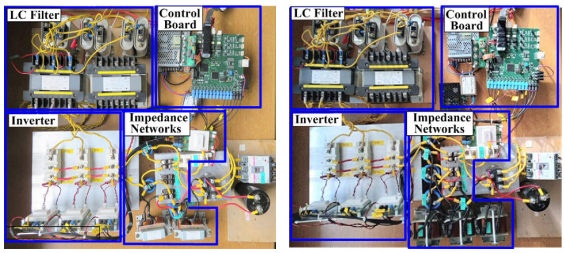


FIGURE 15. Photographs of the experimental prototypes: (a) SCL-ASBI, (b) EB/SCL-ASBI.

B. EXPERIMENTAL RESULTS

The experimental prototypes built in the laboratory for the two proposed topologies are shown in Fig. 15. Each prototype consists of the control board, impedance network, three-phase inverter, and three-phase output LC filter. The three-phase resistive load is connected to the three-phase output LC filter. The ac output voltage control system with PWM signals generation is implemented by 32-bit DSP and a Cyclone-III FPGA. A four-channel 12-bit Digital/Analog (D/A) converter is connected to the DSP in order to investigate the waveforms of the important variables of the ac output voltage control loop shown in Fig. 5 through an oscilloscope.

Fig. 16 shows the experimental results of the proposed SCL-ASBI topology when $D = 0.2$ and $M = 0.8$, which are the same operating conditions as the simulation results shown in Fig. 13. The dc-link voltage, which is equal to the capacitor voltage V_{C1}, is boosted to 187 V from a dc input voltage of 40 V. The capacitor voltage V_{C2} ($=V_{C3}$) is 74 V, and the ac output voltage is boosted to 91 Vrms, which is 2.3 times the dc input voltage of 40 V. From Fig. 16(c), the average and peak-to-peak ripple currents of the inductor are 7.3 A and 1.8 A, respectively. Fig. 16(d) shows the harmonic analysis of the ac output voltage filtered by an LC filter. The THD of the filtered ac output voltage calculated from the harmonic analysis is 0.7%, which is a low value. Fig. 16(e) shows the

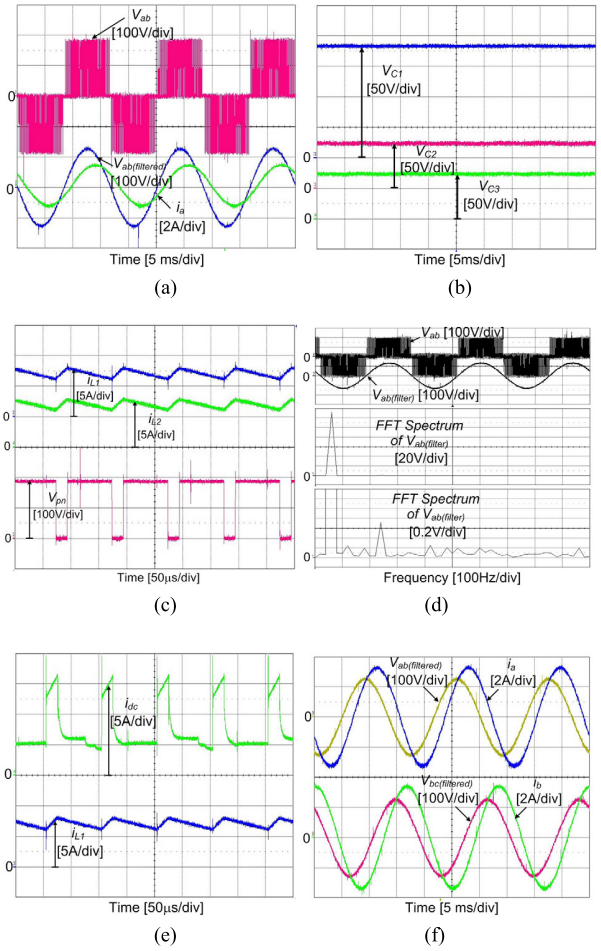


FIGURE 16. Experimental results for the SCL-ASBI when $M = 0.8$, $D = 0.2$, and $V_{dc} = 40$ V: (a) ac output voltage and current, (b) three capacitor voltages, (c) two inductor currents and dc-link voltage, (d) FFT analysis of V_{ab} after filtering, (e) dc input and inductor currents, (f) ac output voltages and currents at $R_L = 20\ \Omega$, $L_L = 8$ mH.

dc input current and inductor current. The dc input current is (i_{L1} - i_{c1}) during the NST state, and it jumps to twice inductor current during the ST state. Fig. 16(f) shows the two-phase line-to-line voltages and two- phase output currents, when the load resistance decreases from 50 Ω to 20 Ω and the inductive load with 8 mH is appended for achieving a resistive-inductive load with low impedance. The magnitude of the output currents increases and the output currents lag more to the output voltage.

Fig. 17 shows the experimental results of the proposed EB/SCL-ASBI topology when $D = 0.15$, $M = 0.85$, and $V_{dc} = 40$ V. The dc-link voltage, which is equal to the capacitor voltage V_{C1}, the capacitor voltage V_{C2} ($=V_{C3} = V_{C4} = V_{C5}$), and the ac output voltage are boosted to 330 V, 100 V, and 175 Vrms, which is 4.38 times the dc input voltage, respectively. The gate-source voltage of switch S_o is applied during the shoot-through state, and the average of the two inductor currents is 20.4 A.

The capacitor, dc-link, ac output voltages of the experimental results of the proposed SCL-ASBI are slightly lower than those of the simulation results under the same operating

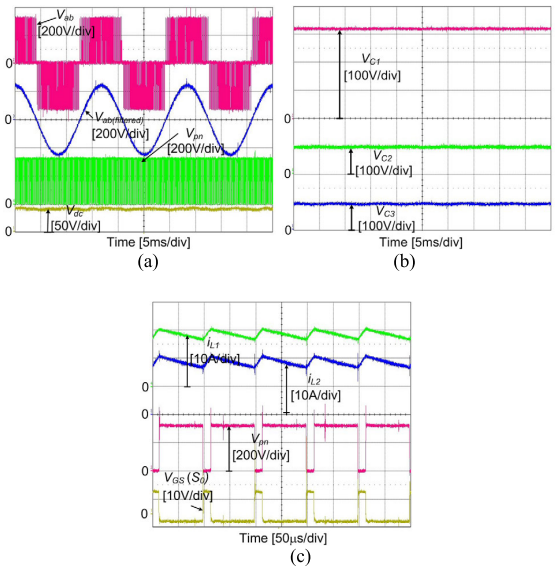


FIGURE 17. Experimental results for the EB/SCL-ASBI when $D = 0.15$, $M = 0.85$, and $V_{dc} = 40$ V: (a) ac output voltage, dc-link and dc input voltages, (b) three capacitor voltages, (c) two inductor currents, dc-link voltage, gating signal of S_0.

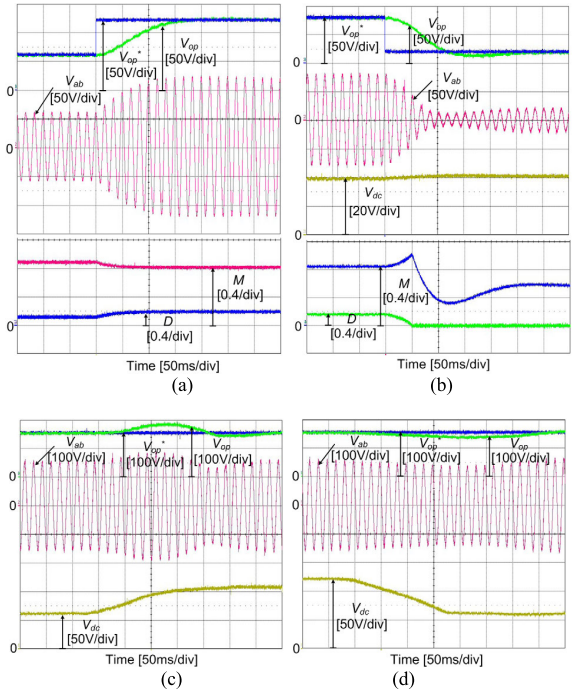


FIGURE 18. Experimental results for closed-loop control of output voltage of the SCL-ASBI: (a) when V_{op}^* increases from 60 V to 120 V, (b) when V_{op}^* decreases from 80 V to 20 V, (c) when V_{dc} changes from 60 V to105 V, (d) when V_{dc} changes from 120 V to 60 V.

conditions due to the ESRs of the inductors and capacitors as well as the voltage drops of diodes and switching devices. The proposed EB/SCL-ASBI is more affected by parasitic effects, because it has one more cell, compared with the SCL-ASBI topology. Therefore, the ac output voltage differences between the simulation results and experimental results of the EB/SCL-ASBI are greater than those of the SCL-ASBI.

Fig. 18 shows the experimental results for the closed-loop control of the ac output voltage of the proposed SCL-ASBI. Figs. 18(a) and 18(b) show the transient responses of the output voltage when the reference peak output voltage V_{op}^* increases from 60 V to 120 V and decreases from 80 V to 20 V, respectively, at $V_{dc} = 40$ V. As shown in Fig. 18(a), the duty ratio increases from 0.1 to 0.19 while the modulation index decreases from 0.9 to 0.81, as the peak output voltage V_{op} increases from 60 V to 120 V. From Fig. 18(b), the voltage control mode of the inverter changes from boost mode to buck mode. The inverter operates in buck mode, when the peak output voltage V_{op} approaches 20 V. In buck mode operation, the modulation index M controls the output voltage without the shoot-through state ($D = 0$). It can be noted that the peak output voltage V_{op} tracks its reference voltage V_{op}^* well, and the output voltage is smoothly controlled at the transition from boost mode to buck mode. Figs. 18(c) and 18(d) show the transient responses of the ac output voltage when the dc input voltage is varied. The peak output voltage is well regulated to its reference voltage $110\sqrt{2}\,V$ for keeping the output voltage to 110 Vrms, when the dc input voltage increases from 60 V to 105 V and decreases from 120 V to 60 V. The waveforms of V_{op}^*, V_{op}, M, and D shown in Fig. 18 can be investigated with an oscilloscope by using a four-channel 12-bit D/A converter connected to the DSP.

VII. CONCLUSION

In this paper, the switched-capacitor-inductor active-switched boost inverter (SCL-ASBI) topology based on the SBI structure is proposed. In comparison to the four different state-of-the-art topologies of Switched-ZSI, cASLB-qZSI, EB/ASN-qZSI, and CSC-EB-ZSI, the proposed SCL-ASBI topology provides a higher boost factor and ac voltage gain. Additionally, the proposed topology can easily extend to n- cell for further increasing the boost capability. The appropriate number of cells n is chosen by considering the overall efficiency, capacitor and diode voltage stresses, and inductor current stress as well as the boost capability. As demonstrated by the experimental results, the dc-link voltage is boosted to 187 V, and the inverter produces a line-to-line output voltage of 91 Vrms under a 40 V dc input voltage when $D = 0.2$ and $M = 0.8$. The output voltage after filtering has a low THD of 0.7 %. By cascading one more cell to the SCL-ASBI topology, the dc-link and the ac output voltages can be boosted to 330 V and 175 Vrms from a dc input voltage of 40 V, respectively, when the duty cycle D decreases to 0.15. The closed-loop output voltage control scheme is suggested to linearly control the ac output voltage over a wide range. The peak output voltage is well regulated to its reference voltage when the reference peak output voltage or the dc input voltage changes. The proposed topologies and voltage control scheme can be applied to provide the desired voltage to the critical or local load in islanding mode of a microgrid connecting low-voltage renewable energy sources, like PV array or FC stack, and to drive the traction motor of the FC vehicles.

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ANH-TUAN HUYNH received the B.S. degree in electrical and electronics engineering from Eastern International University, Binh Duong, Vietnam, in 2017, and the M.S. degree in electrical and electronics engineering from the University of Ulsan, Ulsan, South Korea, in 2020, where he is currently pursuing the Ph.D. degree with the Power Electronics Laboratory.

His research interests include power converters, power inverters, and motor controllers.

ANH-VU HO received the B.S. and M.S. degrees in electrical engineering from the HCMC University of Technology and Education, Vietnam, in 2005 and 2009, respectively, and the Ph.D. degree in electrical engineering from the University of Ulsan, South Korea, in 2015.

Since 2015, he has been as a Lecturer with Eastern International University, Vietnam. He is currently working as a Postdoctoral Research Fellow with the Energy Research Institute, Nanyang Technological University (NTU), Singapore. His current research interests include power converters/inverters, microgrids, and renewable energy applications.

TAE-WON CHUN (Member, IEEE) received the B.S. degree in electrical engineering from Pusan National University, in 1981, and the M.S. and Ph.D. degrees in electrical engineering from Seoul National University, in 1983 and 1987, respectively.

Since 1986, he has been a member of the faculty of the Department of Electrical Engineering, Ulsan University, where he is currently a Full Professor. From 2005 to 2006, he served as a Visiting Scholar with the Department of Electrical and Computer Engineering, Virginia Polytechnic Institute and State University, USA. His current research interests include the design of multilevel converter topology, the control of grid-connected inverter systems, and ac motor control.