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A Simulation Study on the Effects of Interface Charges and Geometry on Vertical GAA GaN Nanowire MOSFET for Low-Power Application

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ABSTRACT The effects of interface charges on the performances of gate-all-around (GAA) GaN vertical nanowire MOSFETs with different geometries have been studied. Geometrical effect on the gate current of vertical GAA GaN nanowire MOSFET has also been analysed for the first time. In the ideal condition, the circular geometry nanowire (CGN) MOSFET exhibits the best performance with subthreshold swing (SS) of 62 mV/dec, drain-induced barrier lowering (DIBL) of 14 mV/V, and ON/OFF current ratio (I_{ON}/I_{OFF}) of $\sim 10^8$. The triangular or hexagonal geometry nanowire (TGN or HGN) MOSFET suffer from large gate leakage current due to the field enhancement at sidewall corners. It is also known that interface traps at the sidewall surface of vertical nanowires deteriorate the overall device performance. The HGN MOSFET with m-plane sidewall demonstrates the best performance with SS of 69 mV/dec and DIBL of 13 mV/V, while the TGN MOSFET with a-plane sidewall exhibits the worst performance with SS of 112 mV/dec and DIBL of 101 mV/V.

INDEX TERMS Field enhancement, GAA, Gallium Nitride, geometry, interface trap, vertical nanowire.

I. INTRODUCTION

The continuous scaling of transistor demands the evolution of devices in terms of material and device structure. As the scaling of Fin Field-Effect-Transistor (FinFET) has already reached the limit [1]–[3], a transition to gate-all-around (GAA) structures have been proposed to further enhance the electrostatic controllability of the gate and to effectively suppress the short channel effects (SCEs) [4]–[6]. Gallium Nitride (GaN), being one of the most promising candidate to replace silicon, is also known for their superior material properties, such as wide bandgap energy, large saturation velocity, and relatively smaller permittivity [7]–[9]. GaN-based devices are well-known for their remarkable performance in RF and power due to such prominent properties [10]–[12]. Many research works have also demonstrated that the GaN-based nanowire devices, along with their material advantages, can show strong immunity to SCEs [13], [14]. Vertical nanowire architectures are also reported to show excellent performances due to its structural advantages [15]–[17]. Recently, we have reported a successful fabrication of the GAA GaN vertical nanowire MOSFET for a possible logic application with top-down approach and already analysed the performances in details [18]–[20]. Studies on nanowire channels with different geometry, based on basic material parameters of GaN, have shown that MOSFET with triangular-shaped nanowire channel exhibits better performances [21], [22]. However, nanowire MOSFET geometries like triangular and hexagonal usually suffer from large gate leakage current (I_G) due to high gate electric field at the sharp corners [23]–[25].

This work analyze the GAA GaN vertical nanowire MOSFET by considering the geometrical effect of the nanowire channel as well as the interface trap effects at corresponding sidewall planes of the nanowire channel for the first time. The effect of field enhancement in a nanowire of certain geometries such as triangular and hexagonal has never been studied. The novelty of this work lies in the study of the field

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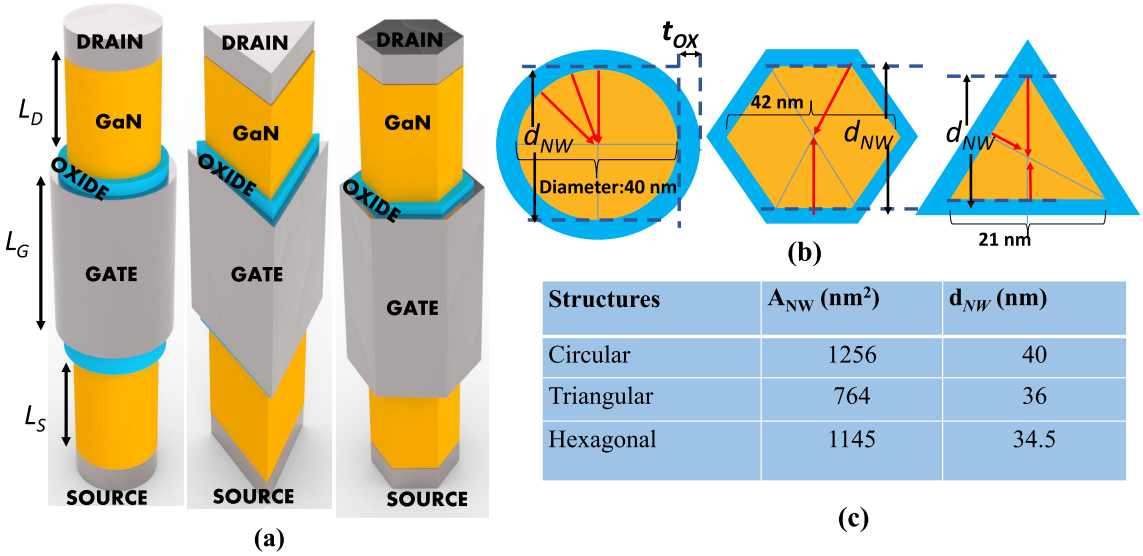

Structures	A_{NW} (nm^2)	d_{NW} (nm)
Circular	1256	40
Triangular	764	36
Hexagonal	1145	34.5

(c)

FIGURE 1. (a) Schematic diagram (b) Horizontal cross-section and (c) Geometrical parameters, of the three different nanowire structures investigated in this work.

enhancement effect based on the geometry of a nanowire, which plays an important role in gate leakage current. The interface trap effect based on the non-polar sidewall planes of nanowires of different geometry is also analysed in depth.

II. STRUCTURE AND SIMULATION MODEL

The structures investigated in this work were developed in DEVEDIT3D and the device simulations were performed in SILVACO ATLAS. Fig. 1(a) and (b) show the structures of nanowires with different geometries considered in this work and their horizontal cross-section, respectively. Hexagonal nanowire pillar has six m-plane sidewalls. Circular nanowire pillar does not have a specific crystal plane, but a mixed sidewall of various crystal planes. Sidewalls of the triangular nanowire pillar can either be a-plane or m-plane depending on the orientation of the triangular-shaped mask pattern for dry etching.

For the simulation, the perimeters of the nanowire channels were fixed at 126 nm, but their areas and cross-sectional widths (d_{NW}) and area (A_{NW}) were different as shown in Fig. 1(c). In order to suppress SCEs, the channel length (L_G) of 100 nm and the oxide thickness (t_{OX}) of 5 nm were chosen to satisfy $L_G \geq 2 \times d_{NW}$. The channel and the source/drain access regions were doped with $5 \times 10^{17}\ cm^{-3}$ and $2 \times 10^{18}\ cm^{-3}$, respectively. The dimensions of the MOSFETs considered in this work are based on the experimentally obtained devices [19] already fitted to simulation in [18], scaled down considering experimentally obtainable dimensions based on the present technology for GaN material.

A self-consistent Fowler-Nordheim (FN) tunnelling model is included to calculate the I_G in which the tunnelling current is directly included in current-continuity equation. A low field mobility model developed by Albrecht using Monte Carlo simulation and a high field mobility model

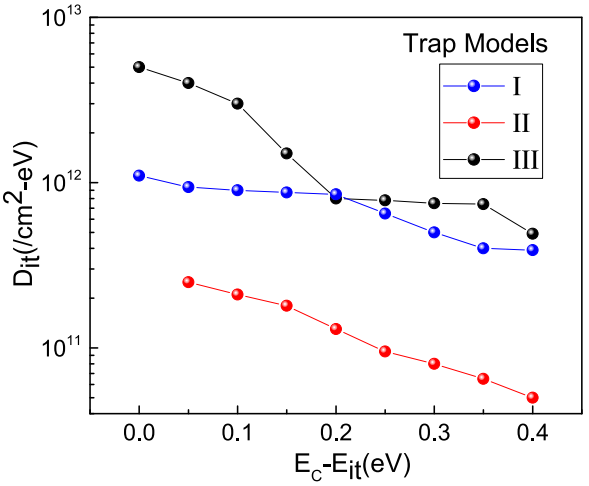

FIGURE 2. Trap densities, D_{IT} vs trap energy level, E_{IT} for different models used in this work.

for GaN material are used [26], [27]. The models consider the field-dependent electron mobility based on the doping concentration and temperature (room temperature is assumed in this work).

As shown in Fig. 2, three trap Models I, II, and III are considered in this work. The trap models are based on the trap information for the Al_2O_3/GaN interface with a distributed trap density (D_{IT}) and trap energy (E_{IT}) from 0.0 - 0.5 eV, given in [28], [29]. Non-polar sidewall of a Wurtzite GaN-based nanowire can be an m-plane or a-plane or a mixture of both. An m-plane surface is reported to be smoother and have less interface trapped charges due to less surface density of atomic bonds than the a-plane surface [30]. The fixed charge was assumed to attain a reasonable and preferrable threshold voltage for logic application. Hexagonal geometry nanowire (HGN) is assumed to have m-plane sidewall surfaces, which has the trap distribution in Model II,

the lowest total trap density of $1 \times 10^{12}\ cm^{-2}$. Triangular geometry nanowire (TGN) is assumed to have either m-plane, or a-plane side wall surface. The a-plane TGN (a-TGN) MOSFET has the trap distribution as described in Model III and has a total trap density of $1.1 \times 10^{13}\ cm^{-2}$. The sidewall surface of the circular geometry nanowire (CGN) should have a modified distribution as described in Model I having a total trap density of $6.6 \times 10^{12}\ cm^{-2}$, a value between that of a-plane and m-plane. An equal fixed positive interface charge of $1 \times 10^{12}\ cm^{-2}$ is also assumed regardless of the nanowire geometries. As shown in Fig. 2, Model II has relatively lower deep trap as well as shallow trap density than Model I and III. Model III, which is designed as the trap density for an a-plane sidewall, has the highest deep-trap density.

III. RESULTS AND DISCUSSIONS

Fig. 3(a) and (b) show the linear and logarithmic transfer characteristics for the ideal GAA GaN vertical nanowire MOSFETs without interface charges and their corresponding I_G. The current levels and the transconductances were normalized with perimeter of the nanowire channel. The threshold voltages (V_{TH}), estimated at drain current of 1 μA/μm, are 0.79 V, 0.86 V, and 0.89 V for the CGN, HGN, and TGN MOSFET, respectively. The CGN MOSFET has the lowest V_{TH} because the channel is less deeply depleted at equilibrium, owing to its larger cross-sectional area A_{NW}, as shown in conduction band diagrams in Fig. 4. The cutline for the band diagram is taken along the line AB as shown in the figures. It should be noted that all of the three nanowire channels are deeply depleted. The CGN MOSFET with lower V_{TH} also exhibits the highest current drivability and transconductance because the CGN structure has better electrostatic control due to uniform gate electric field distribution. However, the TGN MOSFET shows the lowest current drivability due to the deeply depleted channel at equilibrium because of the smaller cross-sectional area, which results in the highest V_{TH}.

On the contrary, as observed in Fig. 3(b), all MOSFETs show similar subthreshold characteristics such as excellent subthreshold swing (SS) of 61 - 62 mV/dec, a low drain-induced barrier lowering (DIBL) of 6.6 - 14 mV/V and low off-state leakage current (I_{OFF}) of 10^{-6} μA/μm to yield high I_{ON}/I_{OFF} ratio of $\sim 10^8$. It is also noticed that I_{OFF} for the MOSFET is closely related to the I_G. To obtain low I_{OFF}, it is required to reduce I_G, which is strongly dependent on the channel geometry. The TGN MOSFET exhibits considerably higher I_{OFF} as well as I_G at off-state, compared to the other two MOSFETs, even though it has the same channel perimeter. This is believed to be due to the strong field enhancement in the sharp corners of the TGN channel. HGN MOSFET has less sharp corners and the CGN MOSFET has a smooth perimeter, which leads to lower I_G. The effect of field enhancement due to sharp corner is more prominent at positive V_G.

Fig. 5 shows the simulation profiles of electric field, the electron concentration, and the electron mobility in the

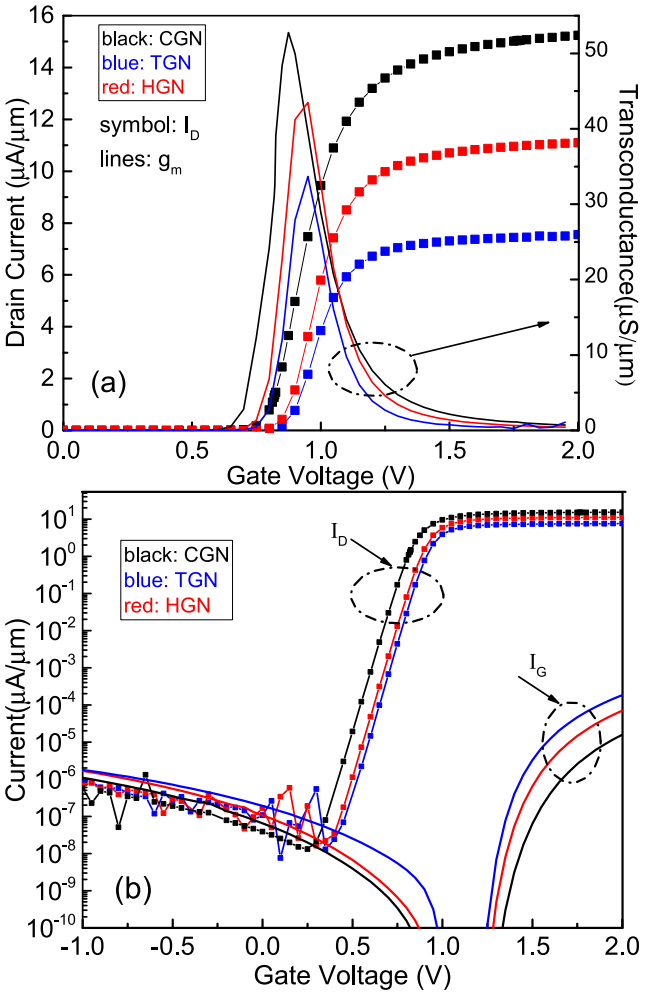

FIGURE 3. Device simulation with interface charges at $V_D = 0.1$ V showing (a) transfer curve in linear scale (b) overlay of I_D - V_G and I_G - V_G curves in log scale.

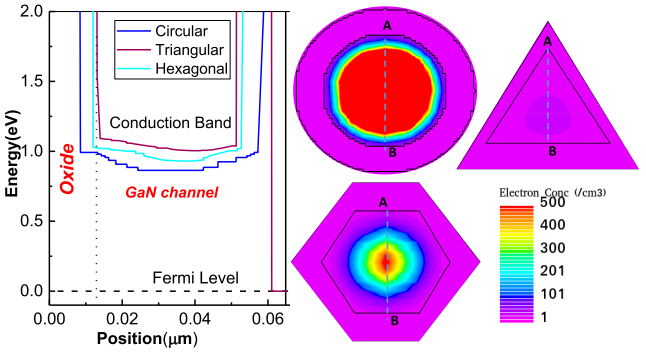

FIGURE 4. Band diagram and electron concentration profile at equilibrium. It is noticed that the electron concentration in the conduction band of the nanowire channel is nearly zero at equilibrium.

nanowire channels under strong accumulation (at $V_G = 2$ V). CGN MOSFET has uniform electric field strength at the surface which also induces uniform electron concentration distribution at surface, as shown in Fig. 5(a) and (b). On the other hand, TGN and HGN have non-uniform electric field strength at surface with higher electric field at the corner giving a higher electron concentration at the corners. CGN

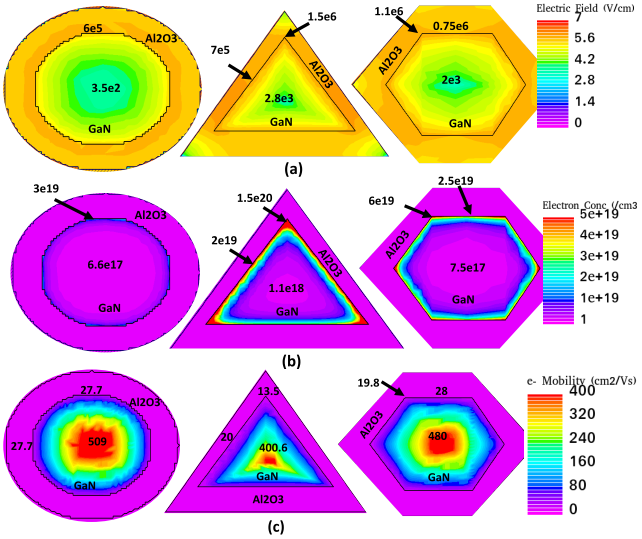

FIGURE 5. Simulation profiles of the horizontal cross-section in ideal condition at $V_G = 2$ V showing (a) electron mobility (b) electron concentration and (c) electric field in the nanowire channel for different geometry.

has the highest electron mobility distribution that varies from 509 at the center to 27.7 cm^{-2}/V-s at surface while TGN and HGN MOSFETs has the corresponding distribution from 400 to 20 cm^{-2}/V-s and from 480 to 28 cm^{-2}/V-s. Considering all MOSFETs have the same surface perimeter, the CGN MOSFET has the highest ($\boldsymbol{\mu.n.A_{NW}}$) product, where $\boldsymbol{\mu}$ and **n** are the average electron mobility and the average electron concentration in the nanowire channel, respectively. This is the reason for the highest ON-current in CGN MOSFET as shown in Fig. 3. On the other hand, TGN exhibits the lowest value of the product, which leads to the lowest ON-current. As mentioned above, the TGN MOSFET and the HGN MOSFET have higher electric field and electron concentration at the corners due to the field enhancement at the sharp corners. The TGN MOSFET has the highest electric field strength of 1.5 MV/cm and electron concentration of 1.5×10^{20} $/cm^3$ at the corners giving the highest I_G in TGN MOSFET.

Fig. 6(a) shows the linear transfer characteristics at $V_D = 0.1$ V with interface charges. Compared to the ideal case, the performance of the MOSFETs were significantly degraded due to the existence of traps and the fixed charges at interface. The fixed positive charge of 1×10^{12} cm^{-2} lowers the V_{TH} while the electrons captured in deep interface traps increase V_{TH}. Therefore, the threshold voltage shift ($\Delta\ V_{TH}$) is determined by the amount of the net effective charge density at the interface. The HGN MOSFET with m-plane sidewall surface (m-HGN) has the lowest deep trap density giving the highest net positive effective charge density, which yields the largest $\Delta\ V_{TH}$ of 0.34 V, (V_{TH} shifts from 0.86 to 0.52 V). The TGN MOSFET with m-plane sidewall surface (m-TGN MOSFET) also has the same net positive effective charge density, but shows less $\Delta\ V_{TH}$ of 0.25 V (V_{TH} shift from 0.89 to 0.64 V) due to more depleted nanowire channel. The CGN MOSFET has less net effective charge density, which leads to even lesser

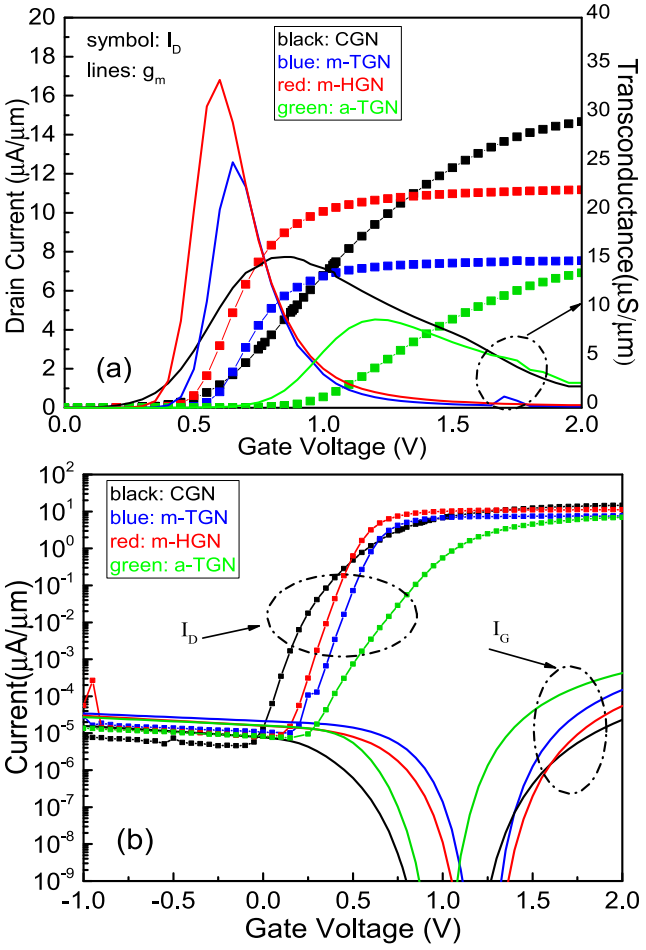

FIGURE 6. Device simulation with trap at $V_D = 0.1$V showing (a) linear I_D - V_G and g_m - V_G curves (b) overlay of I_D - V_G and I_G - V_G curves in log scale.

$\Delta\ V_{TH}$ of 0.24 V (V_{TH} shift from 0.79 V to 0.55 V). On the other hand, the TGN MOSFET with a-plane sidewall surface (a-TGN MOSFET) shows an increased V_{TH} of 1.04 V from 0.89 V, because the net effective charge is negative due to higher deep interface trap density.

The existence of the shallow interface traps also affect the device performances. As shown in Fig. 6(a), all MOSFETs exhibit degraded transconductance and SS. Nevertheless, both HGN and the m-TGN MOSFETs exhibit relatively better transconductance and SS due to relatively low shallow interface trap density at Al_2O_3/m-plane GaN interface. The CGN MOSFET, which has higher shallow trap density, shows poor transconductance and larger SS. The a-TGN MOSFET with highest trap density demonstrates even worse performance with transconductance of less than 10 μS/μm and SS of 112 mV/dec.

Fig. 6(b) shows the logarithmic transfer curve along with I_G curve. Due to interface trap charges, all MOSFETs show larger SS and DIBL than the ideal MOSFETs without interface trap charges and exhibit 1-2 orders larger I_{OFF}. The m-HGN and m-TGN MOSFETs show SS of 69 and 70 mV/dec, increased from the value of 61 mV/dec in the ideal MOSFETs. They also show increased DIBL of 20 and

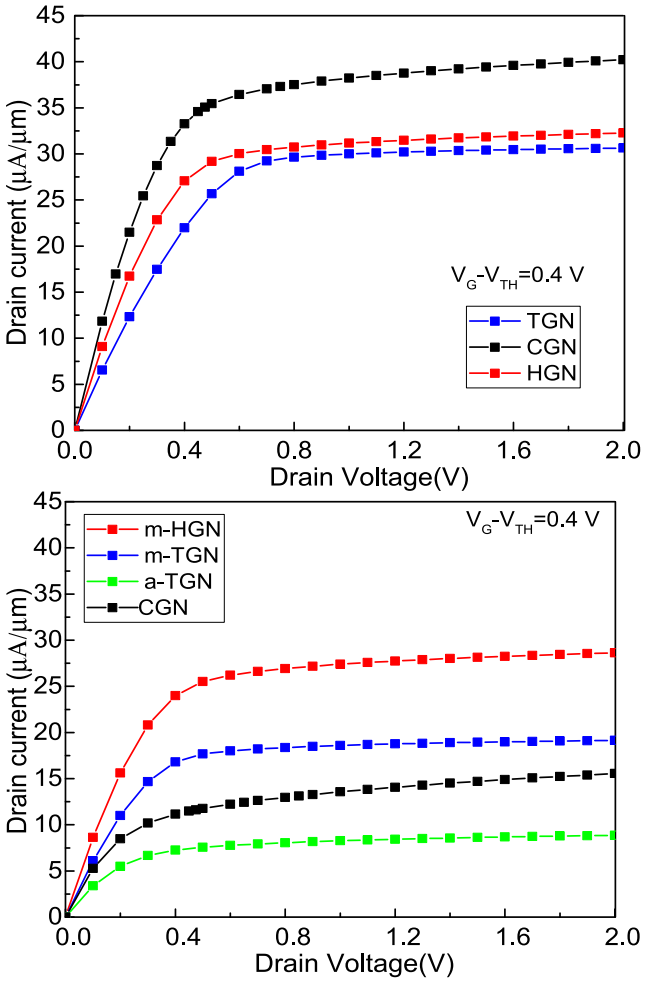

FIGURE 7. Output curve of the devices at a fixed overdrive voltage, $V_G - V_{TH} = 0.4$ V (a) in ideal condition (b) with interface charge.

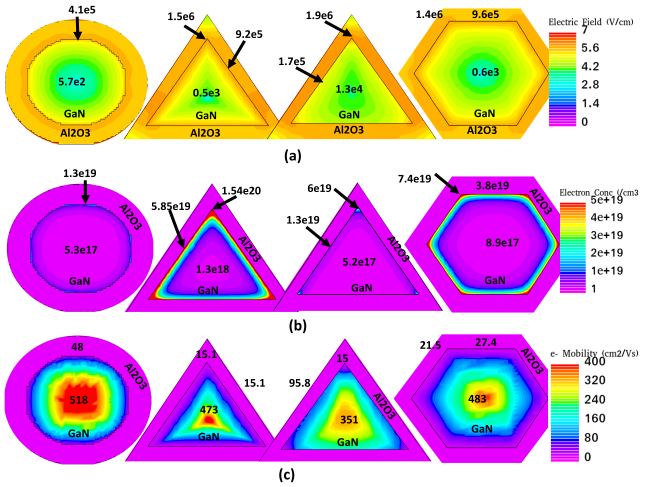

FIGURE 8. Simulation profiles of the horizontal cross-section with interface charges at $V_G = 2$ V showing (a) electric field (b) electron concentration and (c) electron mobility in the nanowire channel for different geometry.

13 mV/V from the value of 8.89 and 6.6 mV/V in the ideal MOSFETs, respectively. The CGN MOSFET exhibits degraded SS of 75.5 mV/dec and DIBL of 97.8 mV/V and the a-TGN MOSFET exhibits worst SS of 112 mV/dec and DIBL of 101 mV/V.

Fig. 7 shows the output characteristics of the investigated nanowire MOSFETs at fixed gate overdrive voltage of ($V_G - V_{TH}$) of 0.4 V. In the ideal case, as shown in Fig. 7(a), the CGN MOSFET exhibits a relatively higher I_{ON} with the low knee voltage of ∼0.5 V for the current saturation, which demonstrates that the MOSFET can be used for low voltage application. The HGN and TGN MOSFETs show similar performances except that they have relatively low I_{ON}. As shown in Fig. 7(b), the m-HGN MOSFET with relatively low interface trapped charges exhibits slightly lower I_{ON} and higher on-resistance (R_{ON}), compared to the ideal HGN MOSFET, while both the CGN and the a-TGN MOSFETs exhibit significantly degraded I_{ON} with higher R_{ON} due to the presence of relatively higher interface trapped charges. It is noted that CGN MOSFET shows slightly non- saturated I_D both in ideal device and device with traps. The reason may be due to larger diameter in CGN MOSFET. A comparatively larger diameter has slightly less gate controllability, which results in a weak channel pinch-off for the CGN MOSFET. However, the knee voltages for all nanowire MOSFETs remain low and almost unchanged from their ideal values regardless of the interface trapped charge. The arguments discussed above indicate that the interface trapped charges, mostly in the deeper traps, compensate the positive fixed interface charges and act as the effective fixed charge to raise or lower the V_{TH} for the MOSFET according to the net amount of interface charges, while the interface charges in shallow traps tend to increase R_{ON} and lower I_{ON}.

Fig. 8 shows simulation profiles of electric field, electron concentration, and electron mobility in the nanowire channels which has positive fixed and trapped charges at the interface (at $V_G = 2$ V). The point electric field, electron concentration, and electron mobility at the side, corner, and centre are summarized in Table 1. As shown in Fig. 8(a) and Table 1, the electric field strength for CGN, m-HGN, and m-TGN is slightly increased at the surface of the sidewall and the corner while decreased in the centre from the ideal case. This is because the density of the negatively charged trap is slightly lower than the positive fixed charge density at interface and hence the net effective charge at the surface is positive. This net positive charges increase the electric field strength at the surface, but in turn decrease the electric field strength at the center of the nanowire channel. On the contrary, the electric field strength for a-TGN is decreased from 0.7 to 0.17 MV/cm at the surface of the sidewall. This is because much higher negatively charged trap density at the surface of a-plane sidewall screens the gate electric field to lower the electric field strength in the surface. The decreased in electric field in the surface increases the electric field at the center of a-TGN at the given V_G.

As shown in Fig. 8(b), electron concentration at surface of the nanowire channel is proportional to the electric field strength at the surface, however, the concentration near the

TABLE 1. Table comparing the values of point electric field, electron concentration, and electron mobility in the nanowires.

		Electric Field (V/cm)			Electron Concentration ($/cm^3$)			Electron Mobility (cm^2/Vs)		
		Corner	Sides	Center	Corner	Sides	Center	Corner	Sides	Center
Circular	Ideal	-	6×10^5	3.5×10^2	-	3×10^{19}	6.6×10^{19}	-	22.7	509
	With traps	-	4.1×10^5	5.7×10^2	-	1.3×10^{19}	5.3×10^{17}	-	48	513
Triangular	Ideal	1.5×10^6	7×10^5	2.8×10^3	1.5×10^{20}	2×10^{19}	1.1×10^{18}	13.5	20	400
	With traps (m-plane)	1.54×10^6	9.2×10^5	0.5×10^3	1.5×10^{20}	2×10^{19}	1.1×10^{18}	12.8	15.1	473
	With traps (a-plane)	1.7×10^6	1.7×10^5	1.3×10^4	6.0×10^{19}	1.3×10^{19}	5.2×10^{17}	15	95.8	351
Hexagonal	Ideal	1.1×10^6	7.5×10^5	2×10^3	6×10^{19}	2.5×10^{19}	7.5×10^{17}	19.8	28	480
	With traps (m-plane)	1.4×10^6	9.6×10^5	0.6×10^3	7.4×10^{19}	3.8×10^{19}	8.9×10^{17}	21.5	27.4	483

TABLE 2. Performance Metrics of the analysed MOSFET devices.

Performance Metrics	Circular		Triangular			Hexagonal	
	w/o traps	with traps	w/o traps	with traps a-plane	with traps m-plane	w/o traps	with traps
$V_{TH}(V)$	0.79	0.551	0.893	1.04	0.64	0.86	0.515
SS (mV/dec)	62.1	75.5	61	112	70	61	69.5
DIBL (mV/V)	14.4	97.7	6.6	101	13.3	8.9	20
I_{ON}/I_{OFF} ($\times 10^7$)	10	0.14	7	0.07	0.07	10	0.1

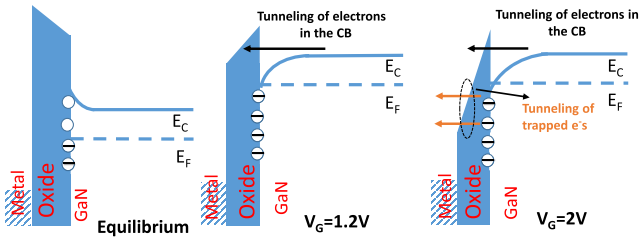

FIGURE 9. Illustration of band bending and tunneling of traps.

center of nanowire is related not only to the electric field, but also the distance between the conduction band and the fermi energy ($E_C - E_F$). The electron mobilities at the surface and near the center, shown in Fig. 8(c), are inversely proportional to the electric field strength at each region. Compared to the ideal TGN MOSFET, for example, the electron mobility for the m-TGN MOSFET is decreased from 20 to 15.1 cm^2/V-s at side surface, but increases from 400 to 473 cm^2/V-s at the center, in an opposite way to the electric field. On the contrary, the electron mobility for a-TGN MOSFET is increased to 95.8 cm^2/V-s at surface, but decreases to 351 cm^2/V-s at the center, because the electric field decreases at the surface and increases at the center.

In addition, the interface traps tend to increase I_G, which also raise I_{OFF}. Regardless of geometry, as shown in Fig. 6(b), the MOSFETs show increased I_G as well as I_{OFF} at negative V_G, one order higher compared to the currents in ideal MOSFETs. At low positive V_G ($0 < V_G < \sim 1$ V), I_G of the CGN MOSFET is lower than that of the m-HGN or m-TGN MOSFET due to the geometrical effect as discussed above. I_G of the a-TGN MOSFET is lower than that of m-TGN and m-HGN, even though the a-plane surface has higher interface trap density. This is due to the captured electrons in the interface traps which screens the gate electric field. However, at $V_G > \sim 1$ V, a-TGN MOSFET shows highest I_G and it increases rapidly due to the higher FNT probability as well as possible re-emission of the trapped electrons, as illustrated in Fig. 9. Similarly, the CGN MOSFET exhibits larger I_G than HGN or m-TGN MOSFET, because the surface of CGN has higher trap density than m-plane surfaces. It is, however, important to note that there are crossovers of I_G between the CGN MOSFET and m-TGN MOSFET (at $V_G = \sim 1.3$ V), and the CGN MOSFET and HGN MOSFET (at $V_G = \sim 1.6$ V). These crossovers is due to the strong field enhancement at the corners of the TGN and HGN structures. The summary of the performance metrics of the analysed devices are given in Table 2.

IV. CONCLUSION

The effects of interface charges on the performance of the GAA GaN vertical nanowire MOSFETs with different geometries have been investigated. It was proved that I_G is strongly dependent on the gate geometry for the first time, especially at large V_G where the gate electric field is higher. The TGN MOSFET suffers from large I_G, which in turn affects I_{OFF}. The shallow interface traps affects the MOSFET performance parameters such as SS, R_{ON}, and I_{ON} while deeper trapped charges act as fixed charge and shifts threshold voltages. Interface charges, along with the geometrical effect degrades the overall device performances. The CGN MOSFET exhibits the best performance in the ideal condition. Considering the interface charges, the HGN MOSFET, however exhibits the best performance, such as lowest SS of 69 mV/dec, DIBL of 13 mV/V, and I_{ON}/I_{OFF} ratio of $\sim 10^6$ while the a-TGN MOSFET shows the worst subthreshold and the on-state performances.

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