IEEE Access
Multidisciplinary : Rapid Review : Open Access Journal

Received July 1, 2021, accepted July 8, 2021, date of publication July 13, 2021, date of current version July 21, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3096988

Introspection Into Reliability Aspects in AlGaN/GaN HEMTs With Gate Geometry Modification

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ABSTRACT Reliability enhancement of AlGaN / GaN HEMT is a significant thrust area due to rapidly improving material and processing technology. In this paper, a detailed analysis of gate–shaped AlGaN / GaN HEMT with field plate is presented. Although AlGaN / GaN HEMT with field–plate is well known, its blending with gate–shaping leading to a more robust and reliable behaviour is described in this paper. It is observed that the threshold voltage and transconductance invariably remain constant for various combinations of gate–shaped and field plate placements. The threshold voltage for all the devices are found to be – 5.8 V. The peak transconductance for the devices without field plate and with field plate is $\sim$ 0.16 S/mm and $\sim$ 0.15 S/mm, respectively. Apart from leakage current, the electric field also gets mitigated for both gate–shaped and field–plated devices by $\sim$ 45% and $\sim$ 68%, respectively. The moderation in electric field further assists in the reduction of electron temperature for gate–shaped and field–plated structures by $\sim$ 12% and $\sim$ 85%, respectively. Additionally, breakdown voltage increases for the gate–shaped devices to 133 V as compared to 120 V of conventional devices without field plate. Significant reduction in leakage current, electric field, and electron temperature is accompanied by a minor increment in capacitance for the field–plated structure, hence, the proposed structure is expected to enhance reliability of the device. Thus, it is anticipated that the proposed devices with enhanced reliability would be a step ahead of conventional devices and would find major applications in high power domain.

INDEX TERMS Capacitance voltage (CV), electron temperature, GaN HEMT, gate shape, leakage current.

I. INTRODUCTION

AlGaN/GaN High Electron Mobility Transistors (HEMT) are best known for their superiority in operating at elevated voltage and temperature along with outstanding integrity in handling high-frequency signals [1]–[3]. GaN being an important member of III–V semiconductor group finds its application in optoelectronic, high-power and high frequency device technologies [4]–[6]. Such an ability of AlGaN/GaN HEMT is primarily due to the large bandgap, high critical electric field and high carrier saturation velocity of the materials involved [7], [8]. The AlGaN/GaN HEMTs are normally-ON devices as a 2DEG (2 Dimensional Electron Gas) naturally forms at the AlGaN/GaN interface due to polarization [9]. However, a normally-OFF operation is achieved by gate recess [10], fluorine implantation [11], and inclusion of additional layer like InGaN, SiN_x [12], [13] etc. The performance of these devices are affected by the leakage current [14], which lowers the device breakdown voltage and can lead to its early breakdown [15]. This issue can be addressed by using a thicker buffer layer, which is doped either with Iron (Fe) or Carbon (C) [16]–[18].

The potential of AlGaN/GaN HEMT technology cannot be realized until the reliability aspect is probed and enhanced. As the majority of degradation phenomenon originates in the gate edge of these devices, modifications in the conventional gate geometry can be one of the alternatives to address this issue [19]–[22]. We postulate that mitigation of electric

The associate editor coordinating the review of this manuscript and approving it for publication was Giambattista Gruosso.

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field at the gate edge can suppress degradation mechanisms. In this paper, a detailed analysis for gate–shaped AlGaN/GaN HEMT with and without field plate is presented. The reliability aspects are studied by evaluating the electric field profile, leakage current, electron temperature (eTemperature), and capacitance–voltage characteristics (CV). Pei *et al.* [23] emphasized that reduction in peak electric field and parasitic capacitance can lead to increased reliability of sub-μm AlGaN/GaN HEMTs. The proposed research work emphasizes the impact of above mentioned factors on the device reliability by varying gate geometry along with simultaneous introduction of field–plates in the device structure. Field plate is usually implemented to scale down electric field in the drain access region. Several configuration are reported in the literature such as, gate field plate [24]–[28], source-connected field plate [29]–[31], and drain-connected field plate [32]–[35]. Although field plate design exhibit high breakdown voltage due to electric field modulation at the gate, however a negative aspect of lateral/gate connected field plate design is that it increases Miller capacitance. Moreover, lateral scaling is limited in gate connected field configuration [25], [36], [37] as it hinders the ON–state performance of a device [28], [38]. It is worth mentioning that the RF performance of the device degrades with scaling down as Miller capacitance dominates in the devices having field plate. Although CV characteristics of GaN-based Metal Oxide Semiconductor (MOS) HEMT (normally-OFF HEMTs) is presented in literature [39]–[47], it is also imperative to understand CV characteristics of a normally-ON HEMT for reliability perspectives.

In this paper, we primarily discuss key degradation mechanism in a device and introspect into the following approaches to increase the reliability of AlGaN/GaN HEMT devices.

- We propose alteration in gate geometry of HEMT (so called gate–shaped device). To examine the benefits of such an approach in device performance, the device characteristics namely current-voltage (I–V) characteristics (transfer characteristics and output characteristics), leakage current, electric field profile along the channel, eTemperature profile, breakdown voltage, capacitance–voltage characteristics for the gate-shaped devices is observed.
- Field plate technology is widely implemented, and various configurations of field plates are reported in the literature. The proposed work focuses on examining the effect of field plates in gate-shaped devices and its impact on the device reliability by studying their electrical characteristics.

Our major contribution in this work is implementation of gate–shape device, and a well planned investigative study of the device structure to understand the reliability and performance aspect. Although, gate shape engineering (slant gate) is well known for enhancement of device performance, this work explores a particular gate-shape (rounded gate edge), which is unique. It is essential to investigate rounded gate edge for the device reliability on the context of gate–shape engineering, and an attempt is made in this work to carry out an investigative study. With this study, reliability and performance aspect of rounded gate shape geometry by analyzing the electric field profile, eTemperature profile, current–voltage characteristics, breakdown voltage, and capacitance–voltage is presented.

The rest of paper is organized as follows. Section II describes physical model considered for the numerical analysis. Section III is dedicated to results and discussion consisting of six sub-sections namely, Current–Voltage Characteristics, Leakage Current, Electron Temperature Profile, Electric Field Profile, Breakdown Voltage and Capacitance – Voltage Characteristics. Finally, a conclusion is presented in section IV.

II. NUMERICAL SIMULATION/PHYSICAL MODEL

In the proposed work, device structures are examined with variations in the gate geometry (gate–shaped) for distinct value of 'dr', and field plate represented by 'L_{FP}'. An $Al_{0.25}GaN_{0.75}$/GaN HEMT is chosen for the proposed work wherein the thickness of AlGaN and GaN layer is kept at 25 nm and 3 μm, respectively. For passivation, $Si_3 N_4$ is employed in both the access regions. The schematic of device structures are shown in Fig. 1. It is stated in [48] that for a heterostructure containing AlGaN barrier, whose thickness is in the range of 20–40 nm is expected to be fully strained for $0 \leq x \leq 0.38$, partially relaxed for $0.38 \leq x \leq 0.67$, and fully relaxed for $0.67 \leq x \leq 1$. Further it is reported in [49], AlGaN layer with mole-fraction, $x > 0.4$ and $x < 0.15$ are not applicable for high quality HFETs. It is described in [49], for $x > 0.4$, the high lattice and thermal mismatch between GaN buffer and AlGaN barrier layer causes high density of structural defects in AlGaN, while rough interfaces limits 2DEG mobility. Further, for $x < 0.15$, the conduction band offset becomes small ($\Delta E_C < 0.28$ eV), resulting in the poor confinement of the polarization induced sheet carrier concentration. However, with an increase in the mole-fraction, strain along $c - axis$ increases, which boosts in-plane stress significantly deteriorating device reliability [50]. Therefore, it is preferred to have mole-fraction, x in the range of 0.15 – 0.38. The RG HEMT is numerically analyzed by varying x from 0.15 to 0.38. The extracted 2DEG and strain is shown in Fig. 2. It is evident that rise in x increases 2DEG and strain. For instance, strain changes by 9.26% and 16.36% as x is varied from 0.20 to 0.25 and, 0.25 to 0.30, respectively. It is to mention that 2DEG varies by 28.2% and 21.3% for above mentioned variations in x. As we know, the surge in strain affects reliability of the device. The rise in strain is quite significant when x changes from 0.25 to 0.30, which is not recommended considering device reliability. It is to be noted that at $x = 0.20$ and $x = 0.25$, strain values are very close, but 2DEG concentration at $x = 0.25$ is 28.2% more as compared to 2DEG concentration at $x = 0.20$. Therefore, it is preferred to have mole-fraction of Al as 0.25 or 25%, which not only helps in

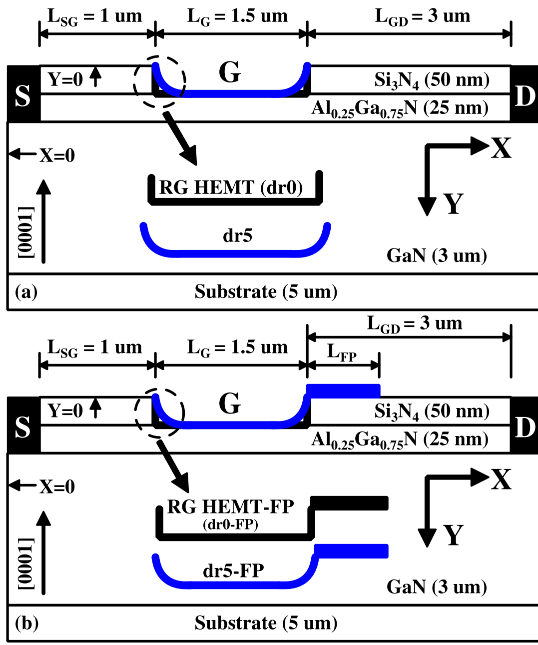

FIGURE 1. Schematics of the structure: (a) Gate–shaped without Field plate, and (b) Gate–shaped with Field plate considered for this work. Here, 'dr5' is gate shape parameter for gate–shaped structure, and 'L_{FP}' is the length of field plate for Field-plated structures.

the formation of 2DEG but also keeps device reliability high. Study of various device structures having mole-fraction of Al as 0.25 can be found in [51]–[53] justifying the same. The device is designed and is numerical analyzed using Sentaurus TCAD [54]. In a hetero-structured device, the interface is of prime significance and energy exchange happens between the interface. In order to model such phenomenon hydrodynamic carrier transport model is implemented [54]. A 2DEG at AlGaN/GaN interface is formed by activating the polarization model. Shockley-Read-Hall (SRH) model is utilized to describe Generation–recombination in the device. Since, GaN and AlGaN are thermodynamically stable wurtzite hexagonal close-packed crystal structure [55], as AlGaN (having smaller lattice constant compared to GaN) layer is grown on top of GaN, a tensile strain develops in the AlGaN layer, which gets uniformly distributed in the basal plane of the AlGaN/GaN to match the lattice constant of GaN [56]. At the AlGaN/GaN interface, the polarization sheet charge density, σ is defined by

$$\sigma = \sigma_{GaN} - \sigma_{AlGaN} = \{P^{sp}_{GaN} + P^{pz}_{GaN}\} - \{P^{sp}_{AlGaN} + P^{pz}_{AlGaN}\} \quad (1)$$

where, P^{sp} and P^{pz} denotes the spontaneous and piezoelectric polarization, respectively.

The spontaneous polarization of $Al_xGa_{1-x}N$ in terms of mole fraction, x is expressed as [57], [58]

$$P^{sp}_{Al_xGa_{1-x}N} = -0.09x - 0.034(1-x) + 0.0191x(1-x) \quad (2)$$

The piezoelectric polarization arises due to lattice match between the layers that results into mechanical perturbation

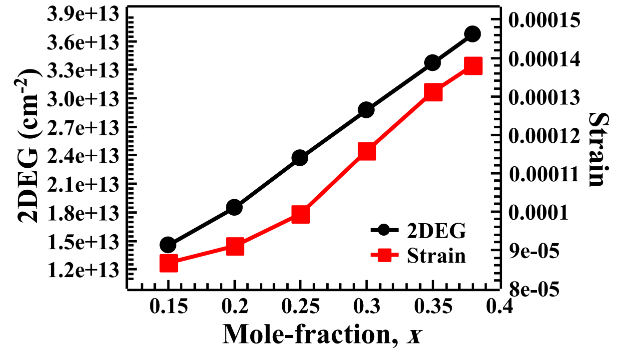

FIGURE 2. 2DEG and strain in the RG HEMT with respect to mole-fraction variation.

(strain), which is evaluated by Vegard's interpolation formula [57], [58]

$$\begin{aligned} P^{pz}_{AlN} &= -1.808\eta_1 + 5.624\eta_1^2 \quad \text{for } \eta_1 < 0 \\ P^{pz}_{AlN} &= -1.808\eta_1 - 7.888\eta_1^2 \quad \text{for } \eta_1 > 0 \\ P^{pz}_{GaN} &= -0.918\eta_1 - 9.541\eta_1^2 \end{aligned} \quad (3)$$

where, η_1 represents the basal strain in the AlN or GaN (binary compound). Similarly, the piezoelectric strain of $Al_xGa_{1-x}N$ using Vegard's interpolation formula can be expressed as [57], [58]

$$P^{pz}_{Al_xGa_{1-x}N} = xP^{pz}_{AlN}(\eta_1) + x(1-x)P^{pz}_{GaN}(\eta_1) \quad (4)$$

further details can be referred from [57]–[59].

GaN crystal being anisotropic along c-axis ([0001]), to model this Anisotropic model is activated. Bias dependent converse piezoelectric phenomena is modelled through gate-dependent polarization model. The model incorporated in the numerical analysis framework for the piezoelectric strain is as follow.

$$\begin{bmatrix} P_x \\ P_y \\ P_z \end{bmatrix} = \begin{bmatrix} P^{sp}_x \\ P^{sp}_y \\ P^{sp}_z + P_{strain} \end{bmatrix} \quad (5)$$

where, $P^{sp}_{x/y/z}$ stands for the spontaneous polarization vector (C/cm^2) in x, y, and z-axis respectively. P_{strain} stands for piezoelectric strain which is expressed as

$$P_{strain} = 2d_{31} \cdot strain \cdot \left(c_{11} + c_{12} - 2c_{13}^2/c_{33}\right) \quad (6)$$

where, d_{31} stands for piezoelectric coefficient (cm/V), and c_{ij} are the stiffness constant (Pa). The *strain* can be further simplified as

$$strain = (1-r) \cdot (a_0 - a)/a \quad (7)$$

where, a_0, a stands for strained and unstrained lattice constant (A°), and r is a relaxation parameter. On inclusion of the above model, piezoelectric charge, q_{PE} is computed as

$$q_{PE} = -C_{act}\nabla P \quad (8)$$

TABLE 1. Parameters of polarization model used in TCAD simulation.

Symbols	Units	GaN	AlN
P_z^{sp}	C/cm^2	- 2.9 $\times 10^{-6}$	- 8.1 $\times 10^{-6}$
e_{31}	C/cm^2	- 3.5 $\times 10^{-5}$	- 5.0 $\times 10^{-5}$
e_{33}	C/cm^2	1.27 $\times 10^{-4}$	1.79 $\times 10^{-4}$
c_{13}	GPa	106	108
c_{33}	GPa	398	373
a_0	A°	3.189	3.189
a	A°	3.189	3.112
relax	–	0.1	0.1

TABLE 2. Physical parameters used in TCAD simulation.

S. No.	Parameter	Description	Dimension
1	L_G	Gate Length	1.5 μm
2	L_{SG}	Source to Gate Spacing	1 μm
3	L_{GD}	Gate to Drain Spacing	3.0 μm
4	L_{FP}	Field Plate Length	$0.5 - 1.5$ μm
5	dr	Gate shape parameter	$0.0 - 0.07$ μm
6	$t_{Si_3N_4}$	Thickness of Si_3N_4 layer	50 nm
7	t_{AlGaN}	Thickness of AlGaN layer	25 nm
8	t_{GaN}	Thickness of GaN layer	3.0 μm
9	t_{SUB}	Thickness of Substrate layer	5.0 μm

where, C_{act} is a calibration parameter used to adjust the piezoelectric charge. The piezoelectric charge, q_{PE} adds up to the Poisson equation. The modified Poisson equation is

$$\nabla\epsilon \cdot \nabla\phi = -q\,(p - n + N_D - N_A + q_{PE}) \tag{9}$$

where, ϕ is the potential and q is the charge of an electron. p and n are the hole and electron density, respectively. N_D, N_A, q_{PE} are the ionized donor concentration, ionized acceptor concentration, and piezoelectric charge, respectively. From the above equation, we can infer that the potential at any point is evaluated by solving the Poisson's partial differential equation considering the charges: p, n, N_D, N_A, and q_{PE}. Hence, the evaluated potential includes the entire charge (mobile and immobile) in the device. The model parameters for polarization models are referred from [60], and are listed in Table 1.

The Schottky gate contact, which corresponds to Nickel has a work-function, ϕ_m of 5.2 eV and, the work function for AlGaN (ϕ_s) is 4.3 eV. Hence, the work function difference is $\phi_{ms} = \phi_m - \phi_s = 0.9$ eV. Surface donor trap in AlGaN is set to 2×10^{13} cm^{-2} and the GaN bulk layer is C–doped having the concentration of 1×10^{16} cm^{-3}. The models employed for the numerical analysis are referenced from [61]. The physical parameters and dimensions are stated in Table 2 for the completeness.

For the numerical analysis, the gate–shape parameter 'dr' and field–plate length parameter 'L_{FP}' in the device structure are varied from 0 – 0.07 μm (0.0, 0.02 μm, 0.05 μm, 0.07 μm), and 0.5 – 1.5 μm (0.5 μm, 1.0 μm, 1.5 μm), respectively. The proposed gate–shape parameter 'dr' represents rounding radius of gate. The device structure with 'dr' = 0.0 is termed as RG HEMT, and remaining structures with 'dr' = 0.02, 0.05, 0.07 are nominated as dr2, dr5 and dr7, respectively. As there will be a series of combinations for 'dr' and 'L_{FP}', results for dr7 is stated in this paper for sake of brevity. This is due to the fact that trend of change in results for gate–shaped devices tends to stabilize as 'dr' approaches 0.07 μm. Therefore dr7 is considered for the comparison with the field–plated devices. However, in some case results for dr2 and dr5 are stated to showcase the variations in the parameters of gate–shaped devices without field plate as compared to the gate–shaped devices with field plate.

In numerical simulation, meshing plays a crucial role especially around the corner at the interface. And it is essential to extracted the results at a distance greater than 3 A° [62]. The results stated for the Y-cut section (along the channel) is obtained at 20 A° below the SiN/AlGaN interface [at Y = 52 nm] and results for X-cut section is taken at the right edge of the gate contact (in the drain access region).

In this work, we have proposed a new gate shape for which only numerical analysis is performed. This work aims at portraying the change in device's electrical and reliability behaviour with respect to the variation in the gate shape. However, with current advancements in fabrication technology, realization of un/non-conventional gate shapes is possible [23], [63], [64]. For instance, Dannecker and Baringhaus [64] demonstrated 2 μm deep trenches in GaN with a width of 4 μm or less, etched with SF_6 based dry etching process. Followed by a wet etching post-treatment employing tetramethylammonium hydroxide (TMAH) and potassium hydroxide (KOH), a smooth and vertical side-wall as well as rounded corners at the trench bottom is obtained. Chen [65] proposed the idea of modulating the light intensity on the photoresist to create a gray scale mask with a sloped profile in it. The mask then transfer the slope profile to realize a sloped field plate structure. These processes can be tuned accordingly to realize the proposed devices. It is expected that research community may explore this aspect given the benefit of these proposed devices.

III. RESULTS AND DISCUSSION

In this section results are presented in five sub–sections; Current–Voltage characteristics, Leakage current, eTemperature profile, Electric Field profile, and Capacitance–Voltage characteristics. In the subsequent sub–sections, four sets of result(s) for the devices are depicted. First set (SET 1) of the results corresponds to the change in gate–shape parameter of the device (without field plate), and the devices in this group are RG HEMT followed by dr2, dr5 and dr7. The second set (SET 2) of results corresponds to device structure with field plate ('L_{FP}' = 0.5 μm) incorporated on the same sequence of devices as in SET 1. Third set (SET 3) highlights the results obtained for the change in 'L_{FP}' (= 0, 0.5 μm, 1.0 μm and 1.5 μm) in RG HEMT. For fourth set (SET 4), dr7 is chosen as the candidate and the field plate length is varied in the range 'L_{FP}' (= 0, 0.5 μm, 1.0 μm and 1.5 μm). The rationale behind the selection of aforementioned four sets is to exhibit the change in electrical property of the device whenever either the gate–shape parameter, 'dr' or field length plate parameter, 'L_{FP}' varies. In the subsequent section, it is found that the change in electrical property stabilizes for gate–shaped devices as gate–shape parameter 'dr' approaches 0.07 μm, therefore, it is desirable to draw the comparison

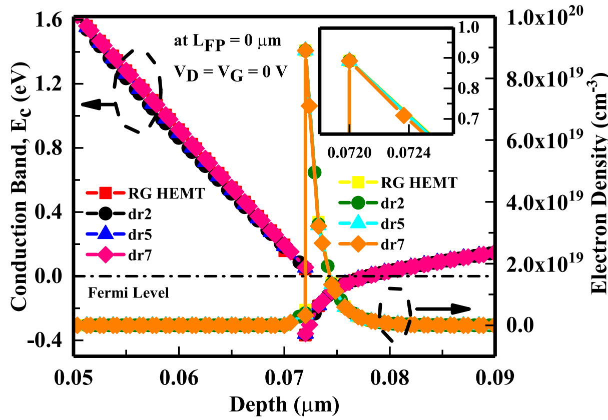

FIGURE 3. Conduction band and electron density profile at the AlGaN/GaN heterostructure for gate-shaped devices (without field plate) at gate voltage = drain voltage = 0 V.

with gate–shaped devices with the extreme design parameters i.e., RG HEMT, and dr7 with/without field plate. The requisite interpretation for the observations is stated in the subsequent subsections. For brevity, results for other possible combinations of gate–shape parameter, 'dr' and field length plate, 'L_{FP}' are not presented unless it is essential to corroborate the facts.

For preliminary investigation of the proposed gate–shaped devices, we have extracted the conduction band profile and electron density profile of the devices at equilibrium condition (gate voltage = drain voltage = 0V) as shown in Fig. 3. It is evident that 2DEG is originates at the proposed gate–shaped device. The sheet carrier concentration, n_{sheet} at the hetero-interface assuming no doping in the AlGaN layer is expressed as:

$$n_{\text{sheet}} = \frac{\sigma(x)}{e} - \left(\frac{\epsilon_0 \epsilon(x)}{d_{\text{AlGaN}}\, e^2}\right)[e\phi_B(x) + E_F(x) - \Delta E_C(x)] \tag{10}$$

where, $\sigma(x)$ is mole fraction dependent polarization sheet charge density, thickness of the $Al_xGa_{1-x}N$ barrier denoted by d_{AlGaN}, $e\phi_b$ is the Schottky barrier of the gate contact, E_F is the Fermi level w.r.t the GaN conduction band edge energy, and ΔE_C is the conduction band offset at the AlGaN/GaN interface, related information can be found in [49], [66], [67]. From Eq. 10, it is apparent that n_{sheet} depends on the polarization sheet charge density, σ, and conduction band offset ΔE_C. The electron density of the devices is found to be 8.90×10^{19} cm^{-3}($\approx 2.36 \times 10^{12}$ cm^{-2}). The conduction band offset of the proposed devices is observed to be 0.37 eV. The polarization sheet charge density varies with mole fraction of the binary compound (refer Eq. 1,2, & 4), therefore, for the proposed gate–shaped devices, $\sigma(x)$ does not vary. Similarly, as the thickness of the layers in the proposed gate–shaped devices is same, ΔE_C remains constant. Hence, the observed electron density at the interface is same for all the devices, RG HEMT, dr2, dr5, and dr7, which means gate–shape does not modulate 2DEG in the proposed devices.

A. CURRENT–VOLTAGE CHARACTERISTICS

In this subsection, two fundamental aspects of a device namely Transfer Characteristics (I_D vs V_{GS}) & Transconductance (g_m), and Output Characteristics (I_D vs V_{DS}) are discussed.

1) TRANSFER CHARACTERISTICS & TRANSCONDUCTANCE

Transconductance, g_m is a key parameter from a circuit designer's perspective. As we know, the transconductance has its roots in the devices' electrical characteristics, which ultimately depends on the quality of device design. Transconductance, g_m, can be expressed as [68]

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \left(\frac{\Delta n}{\Delta V_{GS}}\right) qv + \left(\frac{\Delta v}{\Delta V_{GS}}\right) nq \tag{11}$$

where Δn represents change in carrier concentration; q is the charge of an electron; Δv represents change in carrier velocity, ΔV_{GS} denotes change in gate to source voltage, and ΔI_D is the change in drain current. The change in Δn is notable in the gate region for the change in V_{GS}. The swift enhancement of carrier concentration as V_{GS} is changed from – 10 V to 2 V, and the rise in electron velocity ascertains the contribution of first term of equation (11) to g_m. This is because of the drop in Δv due to rapid decrease in the electron velocity as V_{GS} moves toward the positive domain [68], and reduces the impact of second terms of equation (11) on g_m. Hence, g_m gradual increase and then decreases as gate voltage is varied from – 10 V to 2 V.

The transconductance and transfer characteristics I_D vs V_{GS} for the devices under observation are shown in Fig. 4. As it can be seen from the Fig. 4 (a,b,c,d), there is no variation in the transconductance when 'dr' and 'L_{FP}' are varied. The peak transconductance observed for the devices without field plate and with field plate is $\sim$ 0.16 S/mm and $\sim$ 0.15 S/mm, respectively. The slight reduction in transfer characteristics (current level & transconductance) for the devices with field plate is attributed to decrease electron density with introduction of field plate [69].

The threshold voltage for the devices (with and without field plate) extracted from the transfer characteristics curves (I_D vs V_{GS}) is found to be – 5.8 V. The numerical analysis is performed with gate voltage sweep from – 10 V to 2 V. The threshold voltage for the AlGaN/GaN HEMT (V_{T_HEMT}) can be expressed as [70]

$$V_{T_HEMT} = \phi_b + \frac{Q_{p1}}{C_{\text{AlGaN}}} \tag{12}$$

where Q_{p1} stands for the polarization charge at AlGaN/GaN interface; ϕ_b is the Gate-Metal/AlGaN interface barrier height, and C_{AlGaN} is the capacitance of AlGaN barrier layer. For the device structures, which are considered in this paper, as shape of the gate varies, the [Gate-Metal/AlGaN] contact interface remains consistent i.e. the barrier height is constant for all the structures. Also, the interface of AlGaN/GaN does not shift in any of the structures and it is observed that Q_{p1} is constant and C_{AlGaN} varies slightly. This indicates that the

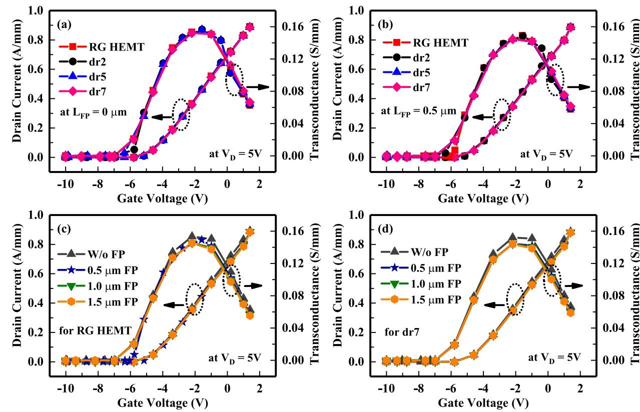

FIGURE 4. Comparison of Transfer characteristics (I_D vs V_{GS}) and Transconductance (g_m) for AlGaN/GaN HEMT devices with drain voltage = 5 V: (a) with variation in gate shape parameter 'dr', (b) with a constant field plate length 'L_{FP}'= 0.5 μm and variation in gate shape parameter 'dr', (c) Field plate length variation 'L_{FP}' for RG HEMT (dr = 0), and (d) Field plate length variation 'L_{FP}' for dr7.

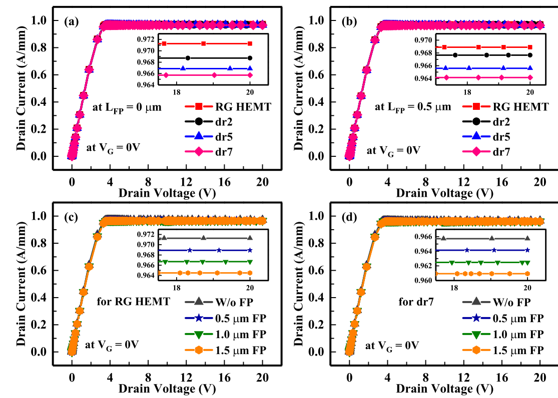

FIGURE 5. Output characteristics for AlGaN/GaN HEMT with gate voltage = 0 V: (a) variation in drain current for change in gate shape parameter 'dr' (b) drain current for gate–shaped device with a constant field plate length 'L_{FP}'= 0.5 μm, (c) Field plate length variation 'L_{FP}' for RG HEMT (dr = 0), and (d) Field plate length variation 'L_{FP}' for dr7.

threshold voltage for the devices does not vary much and the marginal fluctuation in it is reported due to the incremental variations in the capacitance. In succession, we can surmise that the threshold voltage for the device structures with or without field plate barely varies and the peak transconductance observed is $\sim$ 0.16 S/mm and $\sim$ 0.15 S/mm for the devices without field plate and with field plate, respectively.

2) OUTPUT CHARACTERISTICS

Output characteristics of the device is essential to understand the performance of a device, basically the current handling capacity. Heterostructure devices, especially III-N devices, are expected to have higher current due to the formation of 2DEG at the AlGaN/GaN interface which facilitates better electron confinement and lesser electron scattering. In contrary to Si based devices (where the maximum current is in order of mA), maximum current in the AlGaN/GaN HEMT is higher by an order of 10^3. The $I_D - V_{DS}$ characteristics for the devices RG HEMT, dr2, dr5, and dr7 are shown in Fig. 5 with the variation in field plate length 'L_{FP}'. It is observed that drain current, I_D, decreases as gate–shape parameter for the devices changes (RG HEMT, dr2, dr5 and dr7). This is attributed to the decrease in electron density in the channel region for the devices. The drain electric field interacts with 2DEG through the gate contact. For gate–shaped devices, as the magnitude of the vertical electric field is reduced (refer Section III-D for detail), the total strain inclusive of the converse piezoelectric effect is low. As a consequence, the total piezoelectric polarization reduces for gate–shaped devices. This leads to the reduced drain current for gate–shaped devices as reported in [61]. Similar observations are noted in HEMTs with field plate where electric field further reduces due to the introduction of the field plate (refer Section III-D for detail). It can be deduced from Fig. 5 (a,b,c,d) that the drain current of field–plated device is less as compared to the drain current of the device without field plate. Therefore, drain current subsides marginally when gate geometry is modified or/and field plate is introduced.

B. LEAKAGE CURRENT

In this subsection, issues related with leakage current (I_G vs V_{DS}) of the gate–shaped devices with/without field plate are discussed. Leakage current, I_G shows a diminishing trend as gate–shape parameter 'dr' varies. Two orders of magnitude reduction in I_G is observed when gate–shape parameter changes (SET 1), as shown in the Fig. 6 (a). With the introduction of field plate (SET 2), I_G decreases by a factor of 10^2 as depicted in Fig. 6 (b). Similar behaviour is observed for RG HEMT and dr7 devices with different field plate length, 'L_{FP}', wherein I_G scales down by a factor of 10^3, as shown in Fig. 6 (c) and (d).

The reduction of leakage current is due to the decrease in space charge density in AlGaN layer (refer Table 3). With the introduction of field plate or/and change in gate–shape parameter of the device, the depletion width extends below the gate region as well as into AlGaN layer. Since the mobile carriers (2DEG) are of the order of 10^{19} cm^{-3}, which is higher than immobile carriers having the order 10^{16} cm^{-3}, contribution of mobile carrier is significant to the overall space charge. It can also be inferred using Fig. 7 (a,b,c,d), which describes space charge profile of the devices with and without field plate with varying gate–shape parameter. The extension of depletion region into AlGaN layer leads to mobile carrier concentration reduction that results in scaling down of space charge and leakage current. The order of magnitude change in leakage current for device(s) with field plate is higher than the device(s) without field plate. A similar phenomenon is depicted in Saito *et al.* [71].

The significant reduction in I_G translates to higher I_{ON}/I_{OFF} ratio. Gate leakage is one of the dominant phenomenon triggering the breakdown of devices, reduction in I_G increases breakdown voltage of the device [32], [72]. Therefore, considerable drop in leakage current of gate–shaped

TABLE 3. Integrated Space Charge (SC) value in AlGaN layer value for different device structure (as gate shape parameter 'dr' and field plate length 'L_{FP}' vary).

SET	Device Geometry	SC ($10^3\ \mu m^{-1}$)
1	RG HEMT	- 7.16
	dr2	- 6.85
	dr5	- 6.72
	dr7	- 6.61
2	RG HEMT, $L_{FP} = 0.5\mu m$	- 6.38
	dr2, $L_{FP} = 0.5\mu m$	- 6.24
	dr5, $L_{FP} = 0.5\mu m$	- 6.13
	dr7, $L_{FP} = 0.5\mu m$	- 6.05
3	RG HEMT	- 7.16
	RG HEMT, $L_{FP} = 0.5\mu m$	- 6.38
	RG HEMT, $L_{FP} = 1.0\mu m$	- 6.21
	RG HEMT, $L_{FP} = 1.5\mu m$	- 6.04
4	dr7	- 6.61
	dr7, $L_{FP} = 0.5\mu m$	- 6.05
	dr7, $L_{FP} = 1.0\mu m$	- 5.93
	dr7, $L_{FP} = 1.5\mu m$	- 5.85

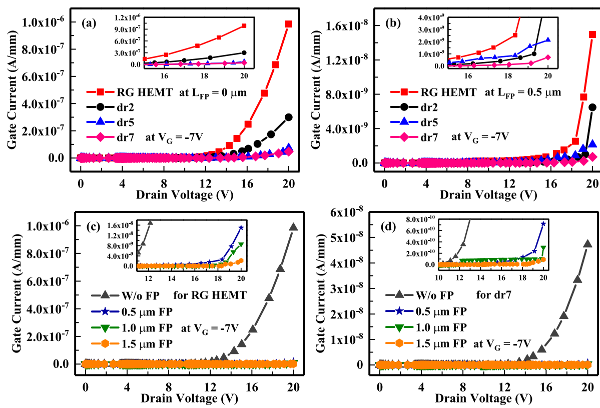

FIGURE 6. Leakage current for AlGaN/GaN HEMT with gate voltage = − 7 V: (a) with different gate shape parameter 'dr', (b) with fixed field plate length 'L_{FP}'= 0.5 μm and change in gate shape parameter 'dr', (c) for RG HEMT as 'L_{FP}' vary, and (d) for devices with same gate shape parameter of dr7 and variation in field plate length 'L_{FP}'.

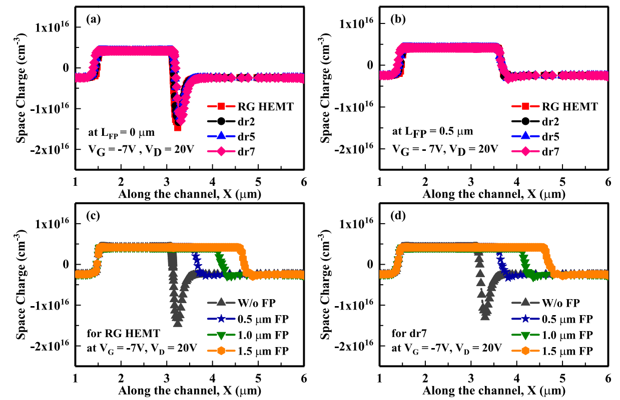

FIGURE 7. Space Charge profile for AlGaN/GaN HEMT (at gate voltage = −7 V and drain voltage = 20 V): (a) gate–shaped devices, (b) with field plate length 'L_{FP}'= 0.5 μm and as gate shape parameter 'dr' vary, (c) for RG HEMT as 'L_{FP}' vary, and (d) change in field plate length 'L_{FP}' for device with gate shape parameter as dr7.

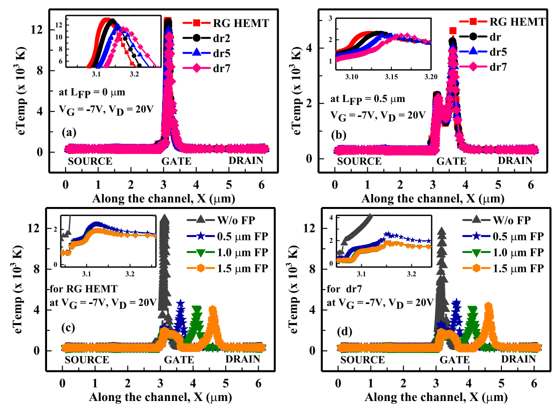

FIGURE 8. eTemperature profile along the channel (Y–Cut) for AlGaN/GaN HEMT (at gate voltage = − 7 V and drain voltage = 20 V): (a) with different gate shape parameter 'dr', (b) with field plate length 'L_{FP}'= 0.5 μm as gate shape parameter 'dr' vary, (c) for RG HEMT as 'L_{FP}' vary, and (d) for device with gate shape parameter as dr7, and variation in 'L_{FP}'.

devices with and without field plate restrains device degradation and increases its breakdown voltage.

C. ELECTRON TEMPERATURE PROFILE

In general, drift-diffusion model fails to consider the velocity overshoot and usually overestimates the impact ionization rate. In order to model the aforementioned observation, hydrodynamic model is implemented where driving force is the carrier energy. Since AlGaN/GaN HEMTs are uni-polar devices, the hole concentration is negligible as compared to electron concentration. Therefore, holes have minimum influence on the device characteristics [73]. Thus, the electron carrier temperature in hydrodynamic model needs to be analyzed. It is to be mentioned that the electron temperature (e-Temp) profile is essential to study device degradation as it has been reported in [74] that the high energy electrons are responsible for electrochemical degradation of AlGaN layer. The e-Temp profile of the devices with variation in gate–shape parameter, 'dr' and field plate length, 'L_{FP}' is depicted in Fig. 8. It is observed that as gate–shape parameter 'dr' varies, the peak electron temperature at the gate edge decreases as shown in Fig. 8 (a)). This can be attributed to the diffused electric field due to 'dr' variations. Similarly, for the device structure with field plate, the electron temperature decreases at the gate edge and a second peak appears at the end of field plate extension. Although the second peak appears for the field plate devices, the magnitude of the peak electron temperature at the gate edge is significantly less as exhibited in Fig. 8 (b,c,d). The change in peak e-Temp at the gate edge toward drain side of the gate–shaped device is ∼ 12% and is ∼ 85% for the field–plated device in both the cases of RG HEMT and dr7 as depicted in Table 4.

The affect of gate–shaped devices on eTemp profile can be observed in Fig. 9. There is a substantial decrease in cross-section area of the region with higher electron temperature. The decrease in quantity of electron with higher electron temperature may contribute for the observed reduction in gate leakage current. Similarly, the decrease in cross-sectional area of higher electron temperature can be correlated with the reduce electric field at the gate edge of the gate–shaped devices.

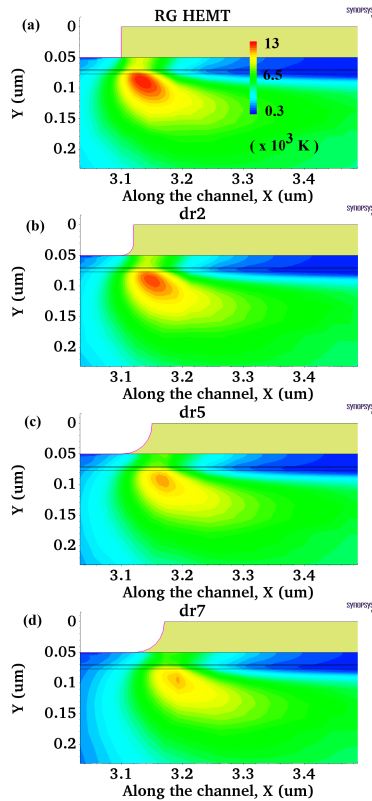

FIGURE 9. Illustration of eTemperature profile for gate–shaped devices (without field plate, at gate voltage = – 7 V and drain voltage = 20 V) extracted from the numerical analysis for: (a) RG HEMT, (b) dr2, (c) dr5, and (d) dr7.

For a device operating in ON state, an additional rise in temperature leads to hot electron induced device degradation, which plays a pivotal role in determining device reliability [75], [76]. A significant change in hot electron temperature in the vicinity of gate edge, which then migrates towards the drain access region, trigger generation of traps [77], defects by piezoelectric stress [78], or dislocations [79]. This can affect the device stability and may initiate device breakdown [80]. Also, due to high electric field at the gate edge (refer Section III-D), a hot spot is formed and the peak temperature of around 6000K [68] to 7000K [81] is reported in the literature. Hence, decrease in the hot electron temperature at the gate edge of the gate–shaped devices with/without field plate helps in reduction of degradation activities.

D. ELECTRIC FIELD PROFILE

Vertical electric field along the channel is a crucial internal parameter influencing the device reliability. This field controls physical properties of the device such as, built-in strain, converse piezoelectric-electric strain, and critical voltage [82]. It is well established that one of the breakdown mechanisms originates from gate edge toward drain-side due to the presence of high electric field under normal operation [83]. This electric field initiates avalanche breakdown and thermally-assisted tunnelling in the device [84]. For an AlGaN/GaN HEMT, it is a well-known fact that the electric

TABLE 4. Observed peak electron temperature (e-Temp) value for different device structure at gate edge toward drain side (as gate shape parameter 'dr' and field plate length 'L_{FP}' vary), and change (in %) from the maximum e-Temp value.

Device Geometry	Peak e-Temp (10^3 K)	% Change
RG HEMT	12.89	–
dr2	12.75	↓ 1.09
dr5	11.92	↓ 7.53
dr7	11.37	↓ 11.79
RG HEMT	12.89	–
RG HEMT, $L_{FP} = 0.5\mu$m	2.34	↓ 81.85
RG HEMT, $L_{FP} = 1.0\mu$m	2.01	↓ 84.41
RG HEMT, $L_{FP} = 1.5\mu$m	1.91	↓ 85.18
dr7	11.37	↓ 11.79
dr7, $L_{FP} = 0.5\mu$m	2.32	↓ 82.00
dr7, $L_{FP} = 1.0\mu$m	1.87	↓ 85.49
dr7, $L_{FP} = 1.5\mu$m	1.82	↓ 85.88

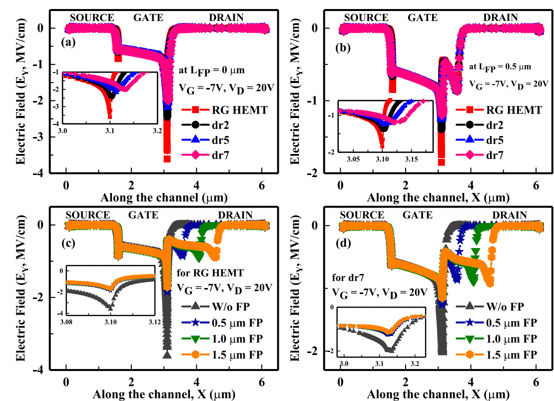

FIGURE 10. Electric Field profile along the channel (Y–Cut) for AlGaN/GaN HEMT at gate voltage = – 7 V and drain voltage = 20 V: (a) with different gate shape parameter 'dr', (b) with field plate length 'L_{FP}'= 0.5 μm as gate shape parameter 'dr' vary, (c) for RG HEMT as 'L_{FP}' vary, and (d) for gate–shape device dr7 with variation in 'L_{FP}'.

field is higher in magnitude at the gate edge in the drain access region. The peak vertical electric field reported in literature is around – 7 MV/cm [81]. This high electrical field can lead to localized Schottky-barrier breakdown at a small drain voltage [24]. Therefore, it becomes imperative to engineer electric field in the vicinity of the gate for the improvement in device performance.

From Fig. 10 (a), it can be observed that the peak electric field at the gate edge toward the drain side for RG HEMT is approximately – 3.61 MV/cm. The magnitude of peak electric field gradually decreases as gate–shape parameter 'dr' varies; – 2.45 MV/cm for dr2, – 2.18 MV/cm for dr5, – 1.99 MV/cm for dr7. This is due to the reduced electric field at the corner of gate edge, which subsides electric field crowding at the gate edge. The proposed gate structure helps not only in reducing electric field significantly but also enhancing device reliability as stated in [61].

Similar behaviour is observed for the field plate structure(s). Its detailed information is enlisted in Table 5 and is shown in Fig. 10 (b,c,d). Introduction of the field plate brings up electric field with $n + 1$ peaks, where n is the number of field plate [85]. In the proposed research work, we have taken $n = 1$. As shown in Fig. 10 (b,c,d), the second peak helps in reducing maximum electric field at the gate edge as the

TABLE 5. Extracted peak vertical component of electric field, E_Y [at the right gate edge] for the devices with different gate shape parameter 'dr' (RG HEMT, dr2, dr5, and dr7) and field plate length 'L_{FP}', and change (in %) from the maximum E_Y value.

Field Plate	Device Geometry	Peak E_Y (MV/cm)	% Change
$L_{FP} = 0$	RG HEMT	- 3.61	–
	dr2	- 2.45	↓ 32.13
	dr5	- 2.18	↓ 39.61
	dr7	- 1.99	↓ 44.88
$L_{FP} = 0.5\ \mu m$	RG HEMT	- 1.85	↓ 48.75
	dr2	- 1.39	↓ 58.72
	dr5	- 1.25	↓ 65.37
	dr7	- 1.19	↓ 67.03
$L_{FP} = 1.0\ \mu m$	RG HEMT	- 1.72	↓ 52.35
	dr2	- 1.26	↓ 65.09
	dr5	- 1.18	↓ 67.31
	dr7	- 1.15	↓ 68.14
$L_{FP} = 1.5\ \mu m$	RG HEMT	- 1.70	↓ 52.90
	dr2	- 1.20	↓ 66.75
	dr5	- 1.16	↓ 67.86
	dr7	- 1.14	↓ 68.42

field is spread out over a region. By spreading the electric field between the large gate-drain spacing, the breakdown voltage is enhanced up to the limit of channel-substrate junction breakdown, which is quite high due to shallow doping of the substrate [85]. However, for longer field plate, 'L_{FP}' breakdown voltage of the device becomes less. As it is evident from Fig. 10 (b,c,d) that with the increase in 'L_{FP}', the second electric field peak moves closer to the drain terminal and its interaction with drain terminal results in isolation breakdown [29].

A detailed comparison of electric field reduction at gate edge of the proposed gate structure with existing literature is enlisted in Table 6. As electric field at the gate edge of a device is primarily responsible for triggering the degradation mechanisms, the minimized electric field for the proposed gate–shaped devices with/without field plate further restrict effects of converse piezoelectric-electric strain, electron temperature, and critical voltage etc. And it is expected that reliability of these devices is enhanced.

E. BREAKDOWN VOLTAGE

The breakdown voltage of a device limits its high voltage operation. Leakage current is one of the key factors, which affects the device reliability [89]. In the previous section (refer III-B), we have discussed the reduction in leakage current for the proposed devices. So, suppressing leakage current with suitable technological approach such as, the proposed devices presented in this work increases the breakdown voltage for a given gate-to-drain spacing. Furthermore, in certain cases, the drain current divides into source current and gate current. The gate current is basically due to the flow of electrons from the gate to the drain terminal as a result of the injection of an electron across the Schottky gate barrier. Since these effects are initiated by a high electric field at the gate edge of the device, the field plate helps in suppressing these effects and results in higher breakdown voltage [27], [90], [91].

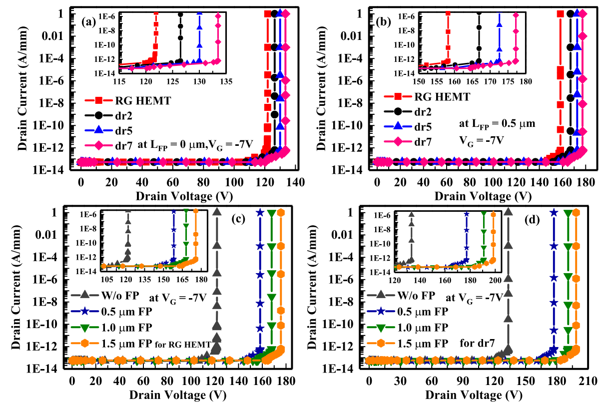

FIGURE 11. $I_D - V_D$ **characteristics for Breakdown Voltage: (a) with different gate shape parameter 'dr', (b) with field plate length 'L_{FP}'= 0.5 μm and as gate shape parameter 'dr' vary, (c) for RG HEMT as 'L_{FP}' vary, and (d) Field plate length variation 'L_{FP}' for dr7.**

The breakdown voltage for devices are extracted from $I_D - V_D$ characteristics at gate voltage = – 7 V (OFF–State) is shown in Fig. 11. As discussed in the preceding section, due to gate-shape parameter variation from RG HEMT to dr7, electric field at gate edge decreases and device breakdown voltage increases. Similarly, an introduction of field plate in the device structure increases breakdown voltage. The combined effect of gate-shape and field plate translates to breakdown voltage of 198 V for dr7 with $L_{FP} = 1.5\mu m$ as compared to the breakdown voltage of 120 V for RG HEMT without field plate. Table 7 may be referred for details.

F. CAPACITANCE–VOLTAGE CHARACTERISTICS

The dependency between gate capacitance C_g and gate voltage is studied by performing AC analysis with frequency of operation fixed at 1 MHz [92], source and drain terminals being grounded ($V_S = V_D = 0$ V), and gate voltage (V_G) being swept from – 10 V to 0 V. From Fig. 12, it is indicative that the CV characteristics changes around the same gate voltage, which reaffirm the feature that threshold voltage for the devices (combination of gate–shape and field plate) is uniform. The magnitude of capacitance C_g dropping almost to 0 fF below V_G = – 7 V suggest that the channel is depleted of electron density or so called typical phenomenon of 2DEG population [93]. Since the threshold voltage of the devices is – 5.8 V, it can also be inferred that below V_G = – 7 V the devices are turned OFF. Similarly, when V_G surges toward 0 V, electron starts filling up the channel and due to this C_g increases. It can be observed that depletion of channel (below V_G = – 7 V), and accumulation of channel (as $V_G >$ – 7 V and moves toward 0 V) are clearly exhibited by the proposed device. The slight shift in the CV characteristics for gate–shaped structure (Fig. 12 (a)) is consequence of slant nature of gate as 'dr' increases, which effectively boost the area under the gate electrode. The distinct vertical shift i.e., increase in capacitance C_g as field plate is incorporated (Fig. 12 (b,c,d)) to the device structure is consequence of increment to the area of the gate electrode. The inflation in

TABLE 6. Comparison of techniques employed for reduction in peak E-Field at the gate edge of the device.

S. No.	Reduction in peak E-Field (in %)	Technique employed
1	15%	Si_3N_4 region in the barrier [86]
2	29%	Slant Gate geometry [62]
3	42%	High-k passivation and gate-connected field plate [87]
4	48%	Incorporation of p-diamond back barriers and cap layers [88]
5	51%	Field plate [25]
6	45%	Proposed Gate-geometry modification without field plate
	68%	Proposed Gate-geometry modification with field plate

TABLE 7. Breakdown voltage, BV for the devices with different gate shape parameter 'dr' (RG HEMT, dr2, dr5, and dr7) for the scenario of without field plate and field plate length 'L_{FP}'= 1.5 μm.

Field Plate	Device Geometry	BV
$L_{FP} = 0$	RG HEMT	120 V
	dr2	126 V
	dr5	129 V
	dr7	133 V
L_{FP} = 1.5 μm	RG HEMT	175 V
	dr2	185 V
	dr5	190 V
	dr7	198 V

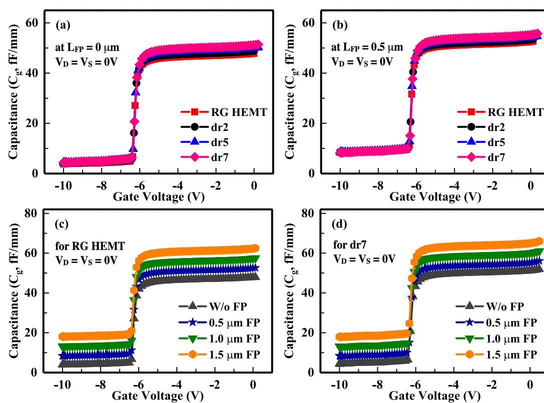

FIGURE 12. C_g **vs** V_G **profile for AlGaN/GaN HEMT (at source voltage = drain voltage = 0V, and frequency = 1 MHz): (a) with different gate shape parameter 'dr', (b) with field plate length 'L_{FP}'= 0.5 μm and as gate shape parameter 'dr' vary, (c) for RG HEMT as 'L_{FP}' vary, and (d) Field plate length variation 'L_{FP}'for dr7.**

capacitance for field plate structure is in agreement with [71]. Thus, gate capacitance increases slightly for the gate–shaped devices with and without field plate.

Similarly, as the gate voltage progress towards 0 V from the negative value, the C_{GD} suddenly jumps at a particular gate voltage as the depleted channel quickly replenishes. The peak in the jump is attributed to the device being in accumulation mode where the depletion region that exists due to polarization charge is non-existent at this point. As the gate voltage approaches 0 V, the depletion region due to polarization kicks in, and the 2DEG depletes, which causes a reduction in the C_{GD} (refer Figure 13 (a)). However, with the inclusion of field plate, the channel recovery occurs at a voltage lower than that in case of without field plate, consequently it is observed that the C_{GD} is higher as well as shoots up earlier for the devices with field plate (refer Figure 13 (b) & (c) & (d)).

Since AlGaN/GaN HEMT devices has wide application in high frequency domain, it is essential to assess the effect of

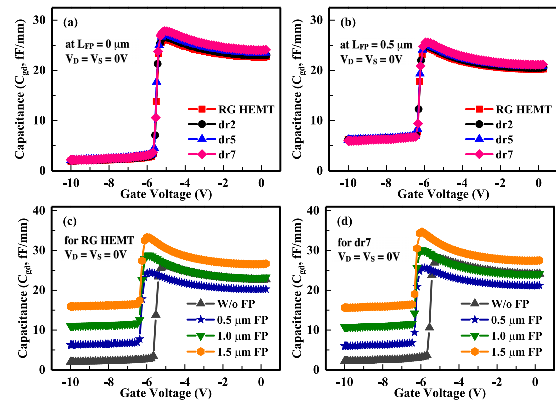

FIGURE 13. C_{gd} **vs** V_G **profile for AlGaN/GaN HEMT (at source voltage = drain voltage = 0V, and frequency = 1 MHz): (a) with different gate shape parameter 'dr', (b) with field plate length 'L_{FP}'= 0.5 μm and as gate shape parameter 'dr' vary, (c) for RG HEMT as 'L_{FP}' vary, and (d) Field plate length variation 'L_{FP}' for dr7.**

field plate on its frequency response. A comprehensive way to evaluate the frequency response is to estimate the change in unity current gain limit (f_m) when field plate is introduced in the device structures. This can be represented for the device structures under consideration as follows [25].

$$\frac{f_{mFP}}{f_m} = \frac{1}{\left[1 + C_{FP}/C_g\right]^2} = \left[1 + \frac{L_{FP}}{L}\right]^{-2} \tag{13}$$

where f_m (f_{mFP}) is unity current gain limit (unity current gain limit due to field plate); C_g is the gate capacitance; C_{FP} is the capacitance due to field plate. Since field plate is an extension of the gate, the capacitance due to field plate just add up to the gate capacitance [94]. Here, L is the length of channel. Thus, the field plate structure has a reduced unity current gain factor as compared to the structure without field plate and it further diminishes as 'L_{FP}' increases.

In this section, electrical characteristics of conventional gate structure and gate–shaped with/without field plate devices are presented. A concise representation of electrical characteristics of the devices is shown in Fig. 14. A comparison is drawn between the conventional gate structure i.e., RG HEMT and gate–shaped device structure dr7 with/without field plate. The electrical characteristics chosen for the comparison are Electric Field (at gate edge toward drain side), eTemperature (at gate edge toward drain side), Leakage current, and Capacitance (C_g). From Fig. 14, it is inferred that electric field, eTemperature (at gate edge toward drain side), and leakage current decreases in the gate–shaped devices as compared to RG HEMT. A similar behaviour is exhibited

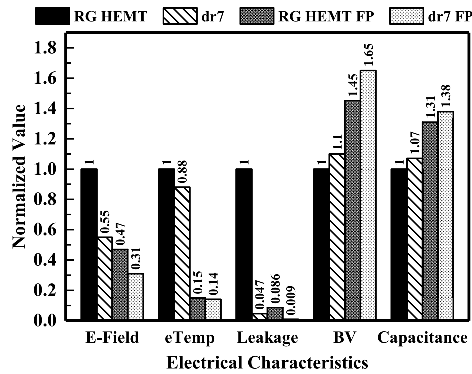

FIGURE 14. Representation of electrical characteristics (electric Field, electron temperature, leakage current, breakdown voltage, and capacitance C_g) for the gate–shaped devices with/without Field plate. A comparison is drawn between RG HEMT (the benchmark), dr7, RG HEMT with field plate (RG HEMT FP), and dr7 with field plate (dr7 FP). The devices considered here have a field plate length, $L_{FP} = 1.5$ μm.

when field plate is incorporated in these device structures. However, capacitance increases for the gate–shaped devices as compared to RG HEMT. An additional increment with the introduction of field plate to the gate–shaped devices is reported in the literature [71]. Also, on close inspection, it is quite evident that the gate–shaped device without a field plate showcases a better electrical characteristics as compared to RG HEMT barring capacitance. Although, the capacitance of the gate–shape devices increases, the magnitude/order of decrease in the electric field, eTemperature, and leakage current supersede the [nominal] increment in the capacitance. Therefore, gate–shaped device is expected to have enhanced reliability as compared to RG HEMT. It may be highlighted that the gate–shaped devices have almost the same threshold voltage and transconductance as RG HEMT, which further emphasizes the fact that the proposed device barely changes the operating point regardless of subdued degradation phenomena.

IV. CONCLUSION

In this paper, gate–shaped AlGaN/GaN HEMTs with and without field plate configuration are analyzed in detail to probe into their reliability aspect. In particular, it is observed that threshold voltage and transconductance have almost remained constant for the devices as gate shape is varied as well as when field plate is introduced to the device geometry. Leakage current reduces by an order of two, when device structure experiences change in the gate shape. It is to mention that incorporation of field plate in the devices leads to reduction by an order of three in the leakage current. It can be attributed to the drop in trapping phenomenon near the gate edge. The moderation of electric field at the gate edge toward the drain side of gate–shaped device by $\sim 45\%$ is due to diffusing effect that helps in easing electric field related degradation mechanism. Consequently, electron temperature is reduced at the gate edge by $\sim 12\%$. It is observed that devices with field plate facilitate the spread of electric field toward the drain side in the gate-drain access region minimizing electric field at the gate edge by $\sim 68\%$.

For field plate structure, capacitance increases slightly as it adds up to the existing capacitance. However, the increment in capacitance for field plate structure as compared to the structure without field plate is nominal. The decrease of device degradation assisting mechanisms such as, peak electric field and electron temperature at the gate edge as well as leakage current overpower the marginal increment in the capacitance(s) of gate–shaped devices with or without field plate. This helps in enhancing reliability of the proposed device structure. The breakdown voltage for gate–shaped device (dr7) is found to be 133 V which is more than 10% as compared to breakdown voltage of conventional HEMT (RG HEMT). Further, with incorporation of field plates to devices, the breakdown voltage increases by 64% for dr7 with field plate. The increase in breakdown voltage for the gate–shaped device thereby broaden its range of operations as a candidate for power electronics application. Among the candidates for gate–shaped devices, dr7 will be reliable as is inferred from the fact that degradation triggering factors such as, electric field and electron temperature at the gate contact is suppressed comparatively in larger magnitude as compared to conventional RG HEMT and other gate-shaped devices, which in turn assist to improve reliability aspect of the device. This makes the gate–shaped AlGaN/GaN HEMT with or without field plate as a suitable candidate for any high power application necessitating high reliability of the devices.

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