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A D-Band Power Amplifier in 65-nm CMOS by Adopting Simultaneous Output Power-and Gain-Matched G_{max}-Core

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ABSTRACT This paper proposes a simultaneous output power- and gain-matching technique in a sub-THz power amplifier (PA) design based on a maximum achievable gain (G_{max}) core. The optimum combination of three-passive-elements-based embedding networks for implementing the G_{max}-core is chosen considering the small- and large-signal performances at the same time. By adopting the proposed technique, the simultaneous output power- and gain-matching can be achieved, maximizing the small-signal power gain and large-signal output power simultaneously. A 150 GHz single-ended two-stage PA without power combining circuit is implemented in a 65-nm CMOS process based on the proposed technique. The amplifier achieves a peak power gain of 17.5 dB, peak power added efficiency (PAE) of 13.3 and 16.1 %, saturated output power (P_{sat}) of 10.3 and 9.4 dBm, and DC power consumption of 86.3 and 52.4 mW, respectively, under the bias voltage of 1.2 and 1 V, which corresponds to the highest PAE, gain per stage and P_{out} per single transistor among other reported CMOS D-band PAs.

INDEX TERMS Amplifier, power amplifier, CMOS, gain-boosting, maximum achievable gain (G_{max}), terahertz (THz), simultaneous conjugate matching, load-pull, 6G communication system.

I. INTRODUCTION

The technology for the implementation of terahertz (0.1∼1 THz) systems has been an active research area due to its various potential applications [1]–[13]. Among THz frequency ranges, the THz systems operating at the D-band frequency range (110-170 GHz) are developing rapidly for wireless applications such as radar, high-data-rate next generation (6G) communication system, and imaging [1]–[13].

The CMOS technologies have actively been utilized for implementing the THz systems among various available technologies due to their advantages of high-integration and low-cost. However, CMOS technology has clear disadvantages compared to the compound semiconductor process. For example, the intrinsic power gain and power capability of the transistor are relatively low at high operating frequencies due to the low maximum oscillation frequency (f_{max}) and break down voltage, respectively.

In terms of the transceiver link budget, the output power of the transmitter is an important performance metric considering high signal path loss and insufficient sensitivity of the receiver in sub-THz systems. The output power and efficiency of the transmitter are mainly dominated by the performance of power amplifiers (PAs).

Several previous researches have reported PAs in CMOS, SiGe, and compound semiconductor technologies operating at D-band frequency ranges [14]–[24]. Traditional ways to increase the output power are increasing the transistor size and power combining. In the case of increasing the transistor size, it can increase the output power, but generally it causes the degradation of f_{max} and power gain due to the additional parasitic components. Especially in extremely high frequency PA design, the dimension of the transistor can be highly limited due to the degradation in RF characteristics. Therefore, the reported output power of the single transistor is

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lower than 10 dBm [14]–[18], [20], [21], [25]. To achieve the required high output power, a power combining technique is generally adopted in a PA design, which, although, helps increase the output power but results in efficiency degradation due to the additional losses from power dividing and combining circuits. Moreover, to achieve the required amount of gain, a larger number of amplification stages are required, leading to higher power consumption and efficiency degradation.

Another problematic issue in the PA design is output matching. Similar to the distinct noise and gain input matching points in a low noise amplifier, there is also a discrepancy between the optimum power gain and the output power matching points in the PA design. Therefore, there is a trade-off between small- and large-signal matching points, inevitably causing degradation in both power gain and output power.

For resolving the problems mentioned earlier, this paper proposes the design technique of a simultaneous output power- and gain-matched maximum achievable gain (G_{max}) core for a high-gain, high-efficiency, and high-output-power PA design. The optimum combination of three-passive-elements-based embedding networks for implementing the G_{max}-core is chosen considering the small- and large-signal performances at the same time. By adopting the proposed design technique, the simultaneous output power- and gain-matching can be achieved, which maximizes not only small-signal power gain but also large-signal output power performances simultaneously. Although G_{max}-core with three-passive-components based amplifiers have been reported in [26]–[28], these works have only focused on small-signal performances for high-gain without considerations of large-signal performance. Therefore, the large-signal performances such as P_{sat} and OP_{1dB} are poor in [26]–[28]. Moreover, this paper introduces the step-by-step design procedure of the simultaneous output power- and gain-matched G_{max}-core as a design guideline.

The remainder of the paper is organized as follows. Section II explains the considerations for a high-gain, high-efficiency, and high-output-power PA design. Section III explains the limitations of a conventional PA output matching technique and deals with the proposed simultaneous output power- and gain-matched G_{max}-core. In Section IV, a detailed design procedure of power and driver amplification stages is presented. Section V presents the implementation of a two-stage 150 GHz PA as well as measurement results. Section VI concludes the paper.

II. CONSIDERATIONS FOR HIGH-GAIN, HIGH-EFFICIENCY, AND HIGH-OUTPUT-POWER PA DESIGN

A. CHOICE OF AMPLIFIER TOPOLOGY AND DEVICE SIZE

A common-source (CS) amplifier configuration is chosen for a 150 GHz PA design since a cascode structure has the uncertainty of the bulk effect, which increases the uncertainty of the whole design at operating frequencies over 100 GHz [14].

The device size in the design of the high-frequency PA should be carefully chosen. Although a larger device can provide higher output power, the power gain and f_{max} are decreased due to the larger parasitic components, which increases the power consumption and decreases the PAE. Therefore, considering the output power, power consumption, efficiency, and gain simultaneously, the total width is chosen around 38 um, which achieves a P_{sat} of around 10 dBm under the load and source pull matching conditions. There are various combinations for implementing the transistor with similar total width according to unit finger width and number of fingers (NOF). Fig. 1 shows the simulated f_{max} of five n-MOSFETs with a similar total width (around 38 um) and 60 nm gate length as a function of unit finger width and NOF at the bias conditions of $V_{GS} = V_{DS} = 1.2$ V and $I_{DS} \approx 48$ mA. As shown in Fig. 1, f_{max} increases as the unit finger width decreases to 800 nm, then it decreases at the unit finger width of 600 nm. In the given process, the minimum unit finger width provided by the foundry is limited to 600 nm. Therefore, there is an optimum point for achieving the highest f_{max} with the given total width. The n-MOSFET with a finger width = 800 nm and NOF = 48 is chosen as the output power amplification stage in this design. As a result of the next section, our PA design will use two stages. The transistor size for the input driver amplification stage is chosen to form a general 1:2 staging ratio having a total width of 19.2 um with a finger width = 800 nm and NOF = 24.

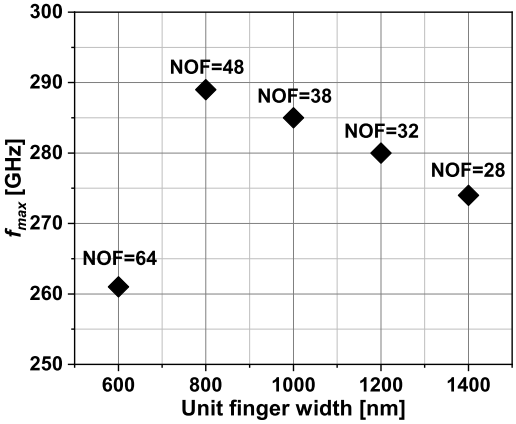


FIGURE 1. Simulated f_{max} of five n-MOSFETs with the similar total width (around 38 um) and 60 nm gate length as a function of unit finger width and number of fingers (NOF) at the bias conditions of $V_{GS} = V_{DS} = 1.2$ V and $I_{DS} \approx 48$ mA.

B. ADOPTION OF G_{max} FOR EFFICIENT SIGNAL AMPLIFICATION

There are various kinds of power gains adopted in mm-wave amplifier design; maximum available gain G_{ma}, maximum stable gain G_{ms}, unilateral gain U, and maximum achievable gain G_{max} [26]–[28]. G_{ma} and G_{ms} are intrinsic gains of the transistor. U is defined as G_{ma} of a transistor after it has been unilateralized using a linear, lossless, and reciprocal embedding network. Finally, G_{max} means the highest possible value

of G_{ma}, when the transistor meets the optimum conditions (see Section III. B) using a linear, lossless, and reciprocal embedding network [26], [28].

Fig. 2 shows the plots of $G_{ma} \sim G_{ms}$ and U in comparison with G_{max} versus frequency for an n-MOSFET having a channel length of 60 nm and an optimal layout with a total width of 38.4 um and 19.2 um, respectively. As shown in Fig. 2, at 150 GHz, G_{max} can provide a much higher gain than $G_{ma} \sim G_{ms}$ and U. The G_{max}, U and $G_{ma} \sim G_{ms}$ of the large (M_1) and small (M_2) transistors are 12.1, 12.8 dB and 6.6, 7.3 dB, and 4.2, 3.5 dB, respectively, at 150 GHz. The target power gain is set to 20 dB. In the given situation, the most effective way to decrease power consumption is to reduce the number of amplification stages. In the case of adopting U and $G_{ma} \sim G_{ms}$, three and five amplification stages are required to achieve the target power gain at least, respectively, considering the losses from passive components. However, by adopting the concept of G_{max}, only two amplification stages are enough to achieve the required amount of power gain while reducing DC power consumption and improving PAE. In addition, the optimized G_{max}-core is adopted in the driver stage for reducing the insertion loss of the interstage matching network, which will be explained in Section IV. B. Moreover, by adopting G_{max}, a large transistor size can be utilized since G_{max} concept can compensate for the large transistor's RF performance degradation. The f_{max} of M_1 and M_2 are simulated to be 289 and 312 GHz, respectively. For implementing G_{max} with a single transistor, a linear, lossless and reciprocal embedding network is adopted, which is generally implemented through transmission lines (TLs). For the ease of the design and reducing the design uncertainty, the transistor is biased in its diode-connected configuration [26]–[30]. Although separating each bias of gate and drain terminals could achieve higher G_{max} and efficiency, it would involve DC decoupling capacitors and more pads, which would lead to the design complexities and additional losses.

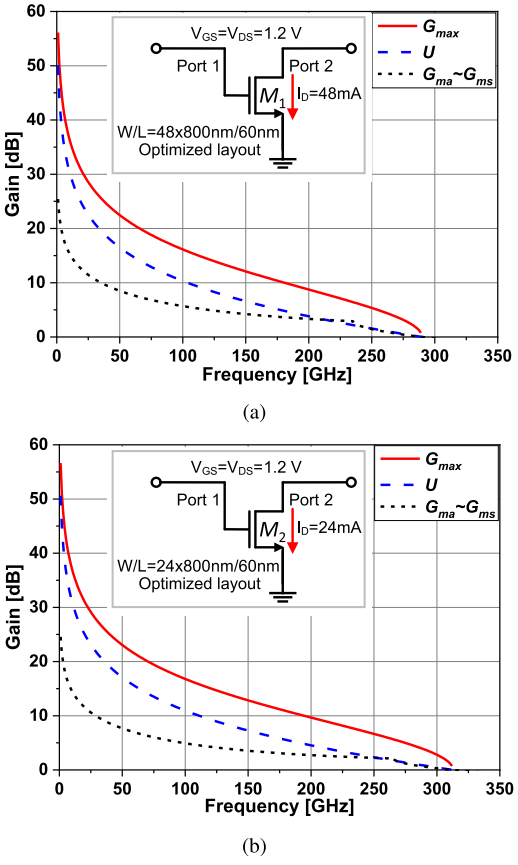


FIGURE 2. Plots of simulated $G_{ma} \sim G_{ms}$ and U in comparison with G_{max} versus frequency for an n-MOSFET having a channel length of 60 nm and an optimal layout with a total width of (a) 38.4 um with a finger width = 800 nm and NOF = 48 and (b) 19.2 um with a finger width = 800 nm and NOF = 24 in 65 nm CMOS.

III. PROPOSED SIMULTANEOUS OUTPUT POWER- AND GAIN-MATCHED G_{max}-CORE

A. LIMITATION OF CONVENTIONAL PA OUTPUT MATCHING TECHNIQUE

Fig. 3 shows the P_{IN} and P_{OUT} relationship of the amplifier under the conventional conjugate- and power-matching and proposed G_{max}-based simultaneous output power- and gain-matching. As shown in Fig. 3, there is a trade-off in the PA output matching design between the conventional power matching based saturated output power and conjugate matching based small-signal gain [31]. The conjugate matching can provide the higher small-signal gain but poor large-signal characteristics such as P_{sat} and OP_{1dB}. On the contrary, the power matching can provide the higher P_{sat} and OP_{1dB} but poor small-signal gain. Moreover, the important behavior in the power matching based PA output design is that the load is not conjugate matched to the output impedance of the last amplification stage, which causes some reflection at the output node of the last amplification stage, although it delivers a large amount of output power to the load [31].

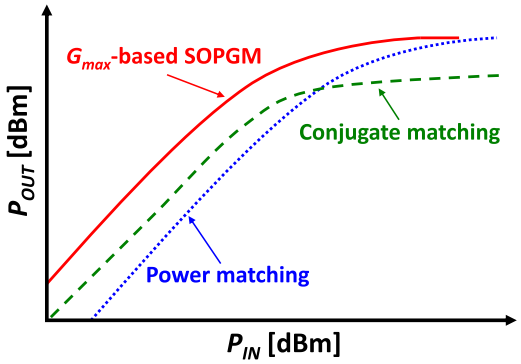


FIGURE 3. P_{IN} and P_{OUT} relationship of the amplifier under the conventional conjugate- and power-matching, and proposed G_{max}-based simultaneous output power- and gain-matching (SOPGM).

In the low frequency PA design, the optimum load impedance is often chosen based on output power consideration only since the transistor provides enough power

gain [32]. Such a design approach is not suitable at frequency ranges over 100 GHz due to the lack of the transistor's power gain. Therefore, the optimum load impedance of the high-frequency amplifier is generally chosen considering both small- and large-signal performance, which inevitably causes a degradation in both small- and large-signal performance. To resolve this problem, the G_{max}-based simultaneous output power- and gain-matching technique is proposed and will be explained in the following section.

B. PROPOSED G_{max} BASED SIMULTANEOUS OUTPUT POWER- AND GAIN-MATCHING TECHNIQUE

In Fig. 3, the advantages of the proposed G_{max} based simultaneous output power- and gain-matching technique are clearly illustrated. Firstly, the power gain is higher by adopting the G_{max} concept rather than U and $G_{ma} \sim G_{ms}$, which leads to the smaller number of amplification stages, as already explained in Section II. B. Secondly, the optimal performance in both small- and large-signal operations can be achieved at the same time.

Although a G_{max}-core can be implemented with a single transistor and a uniquely determined two-passive-element-based embedding network, a three-passive-element-based G_{max}-core is adopted to provide the additional degree of freedom in the design optimization [27]. Among the infinite combinations of the three-passive-element-based embedding networks for achieving G_{max}, the simultaneous output power- and gain-matching can be achieved by adopting the embedding network that shows the identical matching point between the small- and large-signals.

Fig. 4 shows the schematic of the three-passive-element-based G_{max}-core and its equivalent Y-parameter model. In Fig. 4, X_1, X_2, and X_3 represent the reactances of the three-passive-components Z_1, Z_2, and Z_3, respectively. Note that Z_3 is the dominant component in boosting gain and has the largest value [28]. Generally, the G_{max} based gain boosting can be achieved by utilizing the LC resonance concept. Therefore, with an increase in transistor size, the required values of shunt inductance (X_3) become small [29]. In Fig. 4, the overall equivalent Y-parameters (Y_{eq}) of the entire G_{max}-core consisting of Z_1, Z_2, Z_3, and transistor (M) are given by

$$Y_{11eq} = -\frac{(Y_{22M} + Y_{11Z2})Y_{12Z1}Y_{21Z1}}{(Y_{22Z1} + Y_{11M})(Y_{22M} + Y_{11Z2}) - (Y_{12M}Y_{21M})} + Y_{11Z1} + Y_{11Z3}, \quad (1)$$

$$Y_{12eq} = \frac{Y_{12Z1}Y_{12M}Y_{12Z2}}{(Y_{22Z1} + Y_{11M})(Y_{22M} + Y_{11Z2}) - (Y_{12M}Y_{21M})} + Y_{12Z3}, \quad (2)$$

$$Y_{21eq} = \frac{Y_{21M}Y_{21Z1}Y_{21Z2}}{(Y_{22Z1} + Y_{11M})(Y_{22M} + Y_{11Z2}) - (Y_{12M}Y_{21M})} + Y_{21Z3}, \quad (3)$$

and

$$Y_{22eq} = -\frac{(Y_{11Z1} + Y_{22M})Y_{12Z2}Y_{21Z2}}{(Y_{22Z1} + Y_{11M})(Y_{22M} + Y_{11Z2}) - (Y_{12M}Y_{21M})} + Y_{22Z2} + Y_{22Z3}. \quad (4)$$

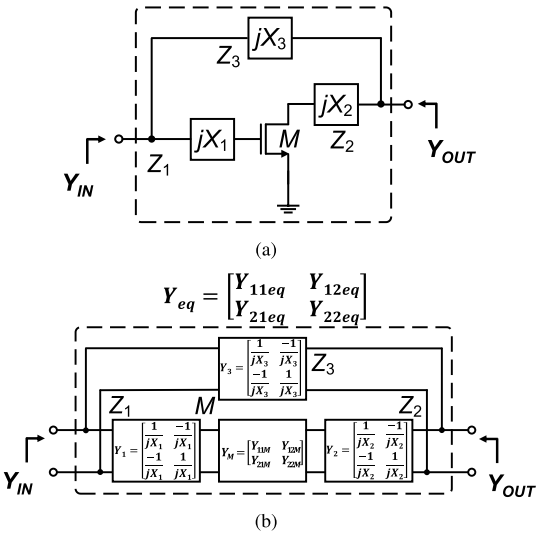


FIGURE 4. Schematic of the (a) three-passive-elements-based G_{max}-core and (b) its Y-parameter-based equivalent model.

In Fig. 4, Y_{IN} and Y_{OUT} represent the input and output admittances of the G_{max}-core, respectively, and can be derived by

$$Y_{IN} = Y_{11eq} - \frac{Y_{12eq}Y_{21eq}}{Y_{22eq} + Y_{LOAD}} \quad (5)$$

and

$$Y_{OUT} = Y_{22eq} - \frac{Y_{12eq}Y_{21eq}}{Y_{11eq} + Y_{SOURCE}}, \quad (6)$$

where Y_{LOAD} and Y_{SOURCE} represent the required admittance values at the input and output of the G_{max}-core for the simultaneous conjugate matching, respectively, and are given by

$$Y_{SOURCE} = Y_{IN}^{*} \quad (7)$$

and

$$Y_{LOAD} = Y_{OUT}^{*}. \quad (8)$$

By substituting (7) and (8) into (5) and (6), the conductances (g_{IN} and g_{OUT}) and susceptances (b_{IN} and b_{OUT}) of Y_{IN} and Y_{OUT} can be given by

$$g_{IN} = g_{11eq}\sqrt{1 - \frac{Re(Y_{21eq}Y_{12eq})}{g_{11eq}g_{22eq}} - \left[\frac{Im(Y_{21eq}Y_{12eq})}{2g_{11eq}g_{22eq}}\right]^2}, \quad (9)$$

$$b_{IN} = b_{11eq} - \frac{Im(Y_{21eq}Y_{12eq})}{2g_{22eq}}, \quad (10)$$

$$g_{OUT} = g_{22eq}\sqrt{1 - \frac{Re(Y_{21eq}Y_{12eq})}{g_{11eq}g_{22eq}} - \left[\frac{Im(Y_{21eq}Y_{12eq})}{2g_{11eq}g_{22eq}}\right]^2}, \quad (11)$$

and

$$b_{OUT} = b_{22eq} - \frac{Im(Y_{21eq}Y_{12eq})}{2g_{11eq}}, \quad (12)$$

respectively.

Assuming that the intrinsic Y-parameters of the transistor M are already known, the equation ($A = Y_{21eq}/Y_{12eq} = -G_{max}$, i.e., $\theta = phase(A) = \pi$ and $k = 1$, where A and k represents the transfer parameter ratio and Rollet's stability factor [27]) for achieving G_{max} can be readily solved to find the values of X_1, X_2, and X_3. As derived in (9)-(12), g_{IN}, g_{OUT}, b_{IN}, and b_{OUT} can be changed by varying the reactances (X_1, X_2, and X_3) of the embedding networks. By selecting the optimal embedding network combination, which shows the same matching points between the small-signal gain- and large-signal power-matching, the simultaneous output power- and gain-matched G_{max}-core can maximize the small-signal power gain and large-signal output power simultaneously.

Fig. 5 shows the proposed step-by-step design procedure for implementing the simultaneous output power and gain matched G_{max}-core at a given operating frequency. The outline of the design flow is shown as follows.

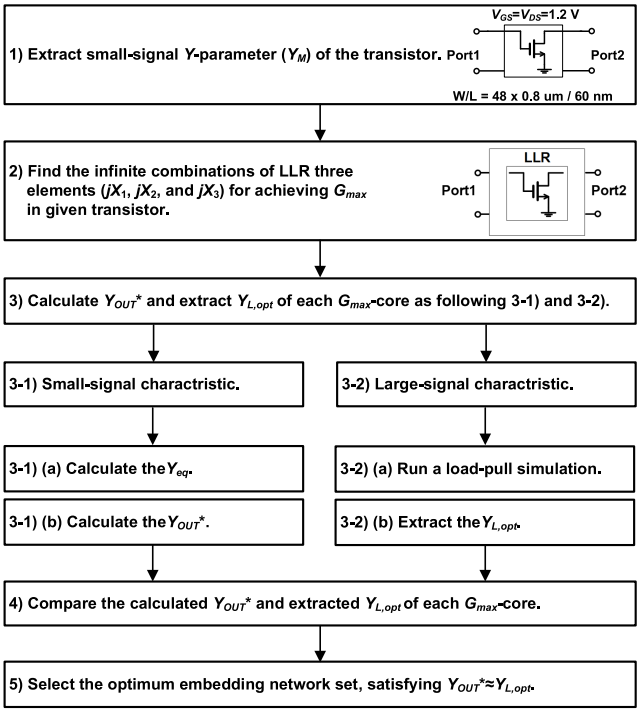


FIGURE 5. Proposed step-by-step design procedure for implementing the simultaneous output power and gain matched G_{max}-core at a given operating frequency.

1) Extract small-signal Y-parameter (Y_M) of a transistor with optimum size and dc bias, as shown in Fig. 2.
2) Find the infinite combinations of linear, lossless, and reciprocal (LLR) three elements (jX_1, jX_2, and jX_3) for achieving G_{max} condition, i.e., $Y_{eq,21}/Y_{eq,12} = -G_{max}$.
3) Calculate Y_{OUT}* and extract optimum load-pull matching point ($Y_{L,opt}$) as following 3-1) and 3-2).
   3-1) Small-signal characteristic.
      (a) Calculate the Y_{eq} based on (1)-(4).
      (b) Calculate the Y_{OUT}* based on (11) and (12).
   3-2) Large-signal characteristic.
      (a) Run a load-pull simulation.
      (b) Extract the $Y_{L,opt}$.
4) Compare the calculated Y_{OUT}* and extracted $Y_{L,opt}$ of each G_{max} core with various embedding networks.
5) Select the optimum set of embedding network, satisfying the simultaneous output power- and gain-matching (Y_{OUT}*≈$Y_{L,opt}$).

Detailed practical design procedure will be explained in the following sections.

IV. DESIGN OF POWER AND DRIVER AMPLIFICATION STAGES

A. POWER AMPLIFICATION STAGE DESIGN BASED ON SIMULTANEOUS OUTPUT POWER- AND GAIN-MATCHING TECHNIQUE

The transistor (M_1) explained in Fig. 2(a) is adopted for implementing the output G_{max}-core. The output G_{max}-core adopts the three-passive-elements-based embedding network as shown in Fig. 4. Fig. 6 shows the variation of X_3 and X_1 as a function of X_2 for achieving G_{max} at 150 GHz. Among infinite combinations of embedding networks, eight representative embedding networks are chosen to verify the proposed simultaneous output power- and gain-matching technique.

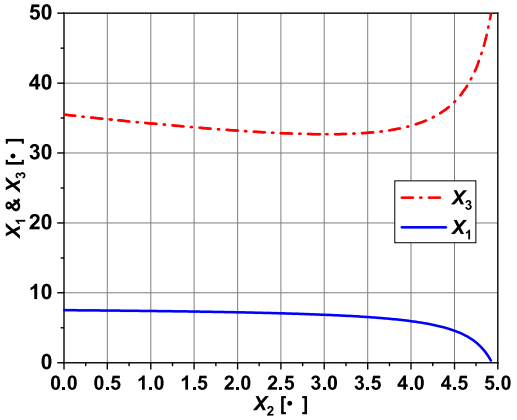


FIGURE 6. Variation of X_3 and X_1 as a function of X_2 in the output power amplification stage at 150 GHz.

Table 1 shows the eight representative embedding networks for achieving G_{max} and the required values of X_1, X_2, and X_3. The proposed simultaneous output power- and gain-matching technique can be verified by observing the output power of all eight representative embedding networks based G_{max}-cores under the simultaneous conjugate gain matching and load-pull based power matching conditions.

Fig. 7 shows the output power characteristics of each eight representative G_{max}-core under the simultaneous conjugate gain matching and load-pull based power matching conditions, respectively. The P_{sat} of the adopted transistor (M_1) at the output power amplification stage is simulated to be around 10.8 dBm. There are interesting properties worth noticing in Fig. 7 as follows.

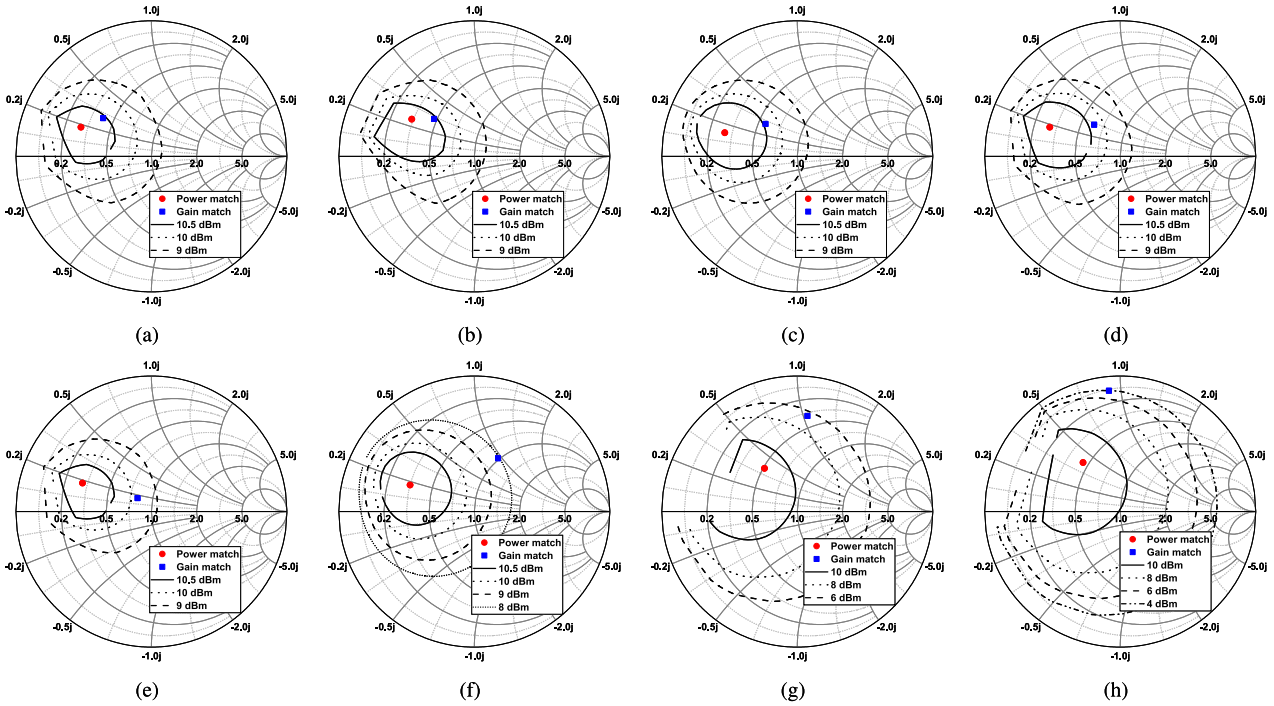


FIGURE 7. Output power characteristics of each eight representative G_{max}-core; (a) set 1, (b) set 2, (c) set 3, (d) set 4, (e) set 5, (f) set 6, (g) set 7, and (h) set 8 under the simultaneous conjugate matching and load-pull based power matching condition, respectively.

TABLE 1. Eight representative embedding networks for achieving G_{max} and the required reactance values of X_1, X_2 and X_3.

Set	X_1	X_2	X_3
Set 1	0 Ω	4.92 Ω	49.79 Ω
Set 2	1 Ω	4.88 Ω	47.35 Ω
Set 3	2 Ω	4.82 Ω	44.54 Ω
Set 4	3 Ω	4.74 Ω	41.84 Ω
Set 5	4 Ω	4.61 Ω	38.76 Ω
Set 6	5 Ω	4.38 Ω	36.06 Ω
Set 7	6 Ω	3.96 Ω	33.77 Ω
Set 8	7.5 Ω	0 Ω	35.48 Ω

1) As derived in (9)-(12), the small-signal conjugate gain matching points (blue square symbols) at the output node vary significantly with the varying combinations of the embedding networks.
2) The variation of the large-signal power matching points is relatively small among all eight sets as compared to the small-signal conjugate gain matching points.
3) In the case of set 2 (Fig. 7(b)), the small- and large-signal matching points are almost coincident. Under the simultaneous conjugate matching condition, it can achieve a P_{sat} of 10.5 dBm, which is quite close to the P_{sat} (10.8 dBm) of the transistor.
4) By adopting the proper embedding network, the simultaneous output power- and gain-matching condition can be achieved.
5) Moreover, the output return loss can be significantly improved by adopting the proper embedding network.

Fig. 8 shows the plot of the summarized P_{sat} and OP_{1dB} of each embedding network combination under the simultaneous input and output conjugate matched condition. As shown in Fig. 8, the set 2 based G_{max}-core shows the output power value of 10.5 dBm, and it is very close to the value of P_{sat} of the transistor; 10.8 dBm. However, in the worst case of set 8 that shows the most significant difference between the small- and large- signal matching points as shown in Fig. 7(h), the simulated output power under the simultaneous conju-

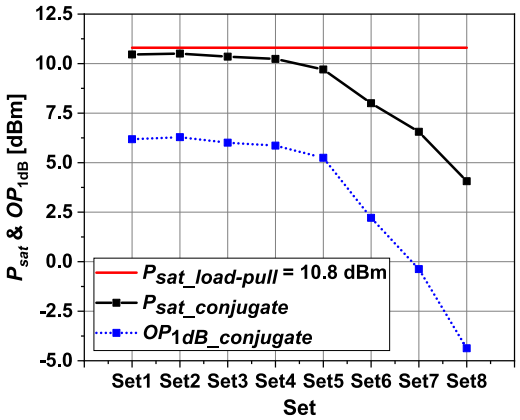


FIGURE 8. Plot of the summarized P_{sat} and OP_{1dB} at each embedding network combination under the simultaneous input and output conjugate matched condition.

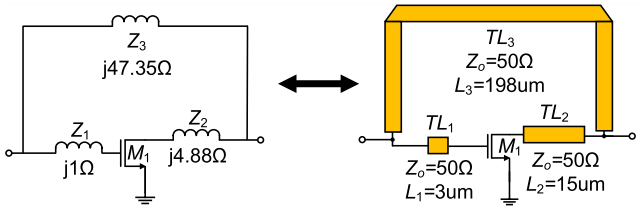
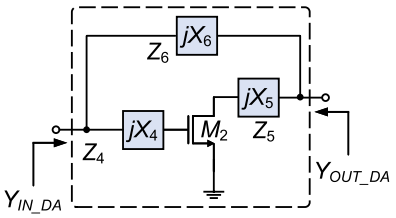
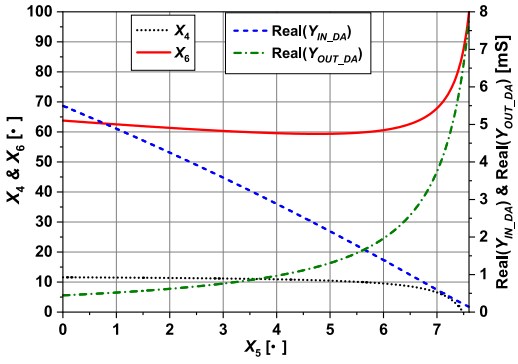


FIGURE 9. Design detail of the set 2 based G_{max}-core of the output stage.



(a)

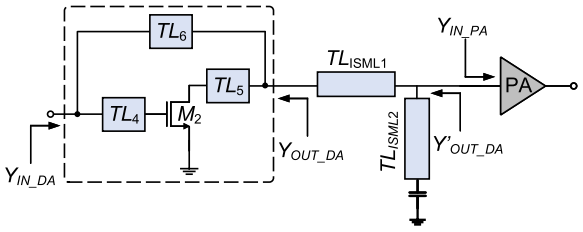


(b)

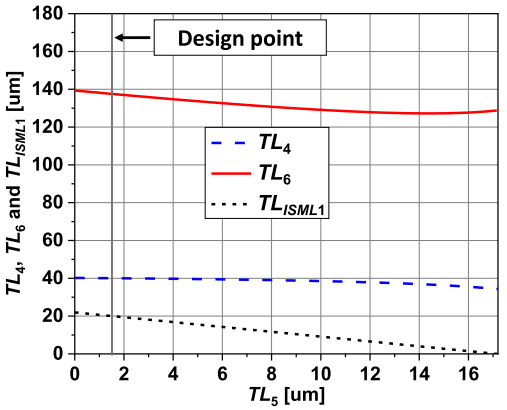
FIGURE 10. Design of the driver amplification stage G_{max}-core with the three-passive-elements. (a) Schematic of the G_{max}-core. (b) Variation of X_6, X_4, Real(Y_{IN_DA}), and Real(Y_{OUT_DA}) as a function of X_5 at 150 GHz.

gate matching is only 4 dBm which deviates far from the P_{sat} of 10.8 dBm that can be obtained at the load-pull matched condition. This means that adopting the optimum embedding network for the G_{max}-core not only boosts the small-signal power gain of the transistor to its maximum value but also maximizes the large-signal P_{sat}. Moreover, OP_{1dB} also shows a trend similar to P_{sat}. Set 2 shows the highest OP_{1dB} of 6.3 dBm, while set 8 shows the lowest OP_{1dB} of −4.5 dBm. As shown in Fig. 8, the difference between P_{sat} and OP_{1dB} increases as the small-signal gain matching point deviates from the load-pull matching point. Therefore, the linearity is also significantly improved at the simultaneous output power- and gain-matched condition. Considering both small- and large-signal characteristics for G_{max}-core design, the proposed simultaneous output power- and gain-matched G_{max}-core can achieve 6.5 dBm higher P_{sat} and 10.8 dBm higher OP_{1dB} compared to the worst-case (set 8), while achieving the same small-signal gain of G_{max}.

Fig. 9 shows the design detail of the set 2 based G_{max}-core of the output stage. To implement the G_{max}-core, the TLs are adopted for the physical implementation of the three-passive-element-based G_{max}-core with TL_1 (Z_o = 50 Ω, and L_1 = 3 um), TL_2 (Z_o = 50Ω, and L_2 = 15 um), and TL_3 (Z_o = 50 Ω, and L_3 = 198 um). At 150 GHz, the wavelength (λ) is equal to 1080 um. Note that, due to the losses from passive components, fine-tuning for gain and operating frequency optimization is required, which is achieved by varying the calculated lengths of each TL by less than 1 %.



(a)



(b)

FIGURE 11. Design of the G_{max}-core considering the interstage matching circuit. (a) Schematic and (b) variation of transmission line's length as a function of TL_5 at 150 GHz.

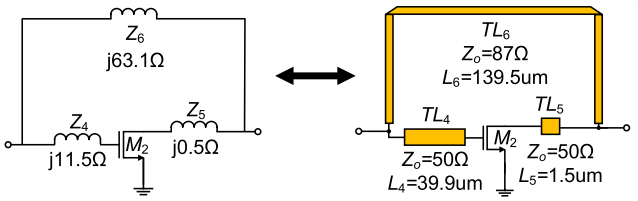


FIGURE 12. Design detail of the driver amplification stage G_{max}-core.

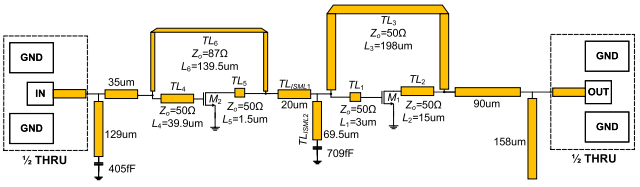


FIGURE 13. Schematic of the two-stage 150 GHz PA.

B. DRIVER AMPLIFICATION STAGE DESIGN

The transistor (M_2) mentioned in Fig. 2(b) is utilized in the driver amplification stage G_{max}-core. The G_{max}-core for the driver amplification stage also adopts the three-passive-elements-based embedding network similar to the PA stage.

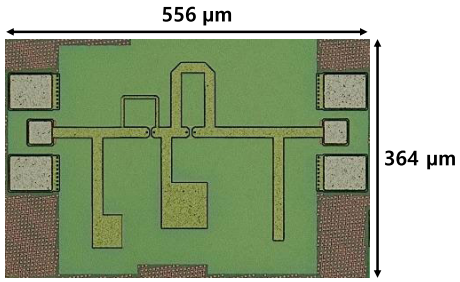


FIGURE 14. Chip micrograph of the two-stage 150 GHz PA.

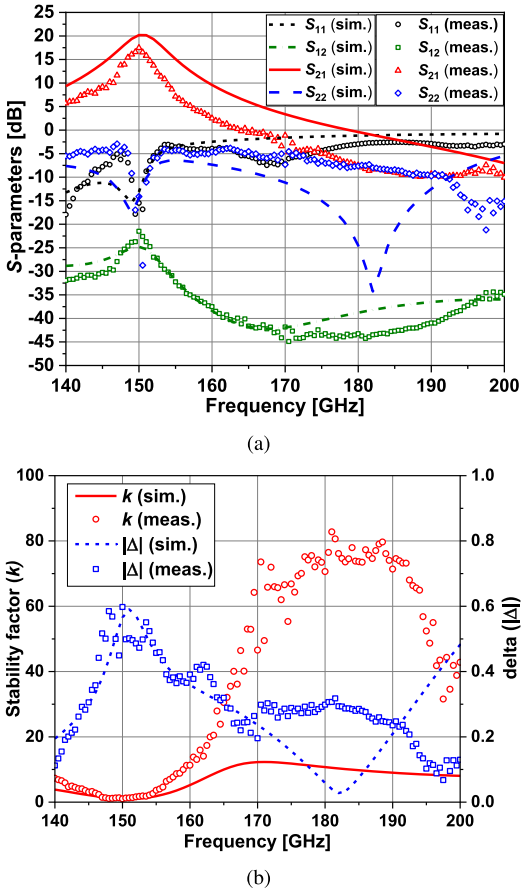


FIGURE 15. Measured (symbols) (a) *S*-parameters and (b) *k*-factor and $|\Delta|$ in comparison with simulations (solid and dotted lines).

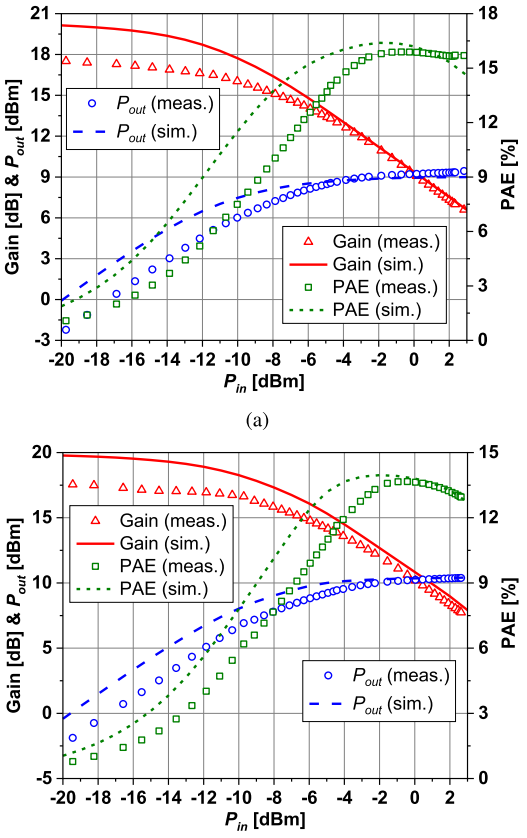


FIGURE 16. Measured (symbols) gain vs. P_{in}, P_{out} vs. P_{in}, and PAE vs. P_{in} at the V_{DD} = (a) 1 V and (b) 1.2 V, respectively, in comparison with the simulation results (solid and dotted lines) at the operating frequency of 150 GHz.

The design approach of the driver amplification stage G_{max}-core is to provide a high gain, as in the case of the output G_{max}-core, while being able to accommodate the inter-stage matching network with minimum loss to deliver enough power to the PA stage, similar to [27]. Fig. 10 shows the schematic of G_{max}-core with the three-passive-elements (X_4, X_5, and X_6) for achieving G_{max} at the driver amplification stage and the variation of X_6, X_4, Real(Y_{IN_DA}), and Real(Y_{OUT_DA}) as a function of X_5 at 150 GHz. In Fig. 10(a), Y_{IN_DA} and Y_{OUT_DA} represent the input and output admittances of the G_{max}-core at the driver amplification stage, respectively. It can be seen in Fig. 10(b) that, with variation in X_4, X_5, and X_6, Real(Y_{IN_DA}) and Real(Y_{OUT_DA}) change as derived in (9) and (11).

Fig. 11 shows the design of the G_{max}-core considering the interstage matching circuit. In Fig. 11(a), Y_{IN_PA} represents the input admittance of the power amplification stage G_{max}-core, which is obtained from Fig. 9. Compared to the interstage shunt matching line (TL_{ISML2}), the interstage series matching line (TL_{ISML1}) is the dominant component in the loss of the interstage matching circuit [15]. For the real part matching, Real(Y_{IN_PA}) and Real(Y'_{OUT_DA}) should be the same. Assuming that Z_4 and Z_5 are implemented in a 50 Ω and Z_6 is implemented in a 87 Ω *TL*s (λ = 1080 um at 150 GHz) for implementing the required embedding networks in Fig. 10(b). Fig. 11(b) shows the physical length of the *TL*s (TL_4, TL_5, and TL_6) to achieve G_{max} and required TL_{ISML1} for the real part matching at 150 GHz. The difference between Real(Y'_{OUT_DA}) and Real(Y_{IN_PA}) can be controlled as a function of TL_4, TL_5, TL_6, and TL_{ISML1}. This means that the interstage matching can be done with the smaller size TL_{ISML1} by adopting the optimally fixed TL_4, TL_5, and TL_6. Note that, even though the interstage matching for the real part between the driver and power amplification stages can be achieved without the interstage series matching

TABLE 2. Performance comparison of the state-of-the-art CMOS and sige amplifiers operating at 110∼190 GHz.

Ref.	Tech.	f_{max} (GHz)	f_o (GHz)	Topology	Power Combining	Gain (dB)	Gain/stage (dB)	P_{sat} (dBm)	P_{sat}/core* (dBm)	OP_{1dB} (dBm)	PAE† (%)	P_{DC} (mW)	3-dB Bandwidth (GHz)
This work	65 nm CMOS	289	150	Single-ended 2 CS	No Combining	17.5	8.8	10.4@1.2V 9.4@1V	10.4@1.2V 9.4@1V	5.3@1.2V 4@1V	13.3@1.2V 16.1@1V	86.3@1.2V 52.4@1V	5
[14]	40 nm CMOS	N/A	140	Differential 3 CS	2-way Combining	20.3	6.8	14.8	8.8	10.7	8.9	305	17
[15]***	65 nm CMOS	320	150	Single-ended 3 CS	No Combining	8.2***	2.7	6.3***	6.3	1.5	9.5	25.5	27
[16]	40 nm CMOS	N/A	133	Single-ended 6 CS	No Combining	16.8	2.8	8.6	8.6	6.8	7.4	89.1	13
[17]	65 nm CMOS	240	144	Differential 3 cascode	2-way Combining	20.6	6.87	5.7	-0.3	N/A	3.6	102	33
[18]	40 nm CMOS	N/A	120	Differential 3 CS	2-way Combining	16	5.3	14.6	8.6	9.3	9.4	N/A	38.5
[19]	130 nm SiGe	450	185	Single-ended 3 cascode	4-way Combining	25.9	8.6	18.1	12.1	8.5	3.5	1600	27
[20]	130 nm SiGe	280	173	Single-ended 3 CS	No Combining	18.5	6.2	0.9	0.9	N/A	N/A	42	8.2
[21]	130 nm SiGe	400	160	Differential 3 cascode	No Combining	32	10.7	10	7	8.5	N/A	N/A	< 6**
[22]	120 nm SiGe	330	124	Differential 3 cascode	No Combining	32	10.7	17.8	14.8	13.5	4.3	560	> 20
[23]***	130 nm SiGe	500	120	Differential 3 cascode	No Combining	26.7	8.9	16.5	13.5	N/A	12.8	380	28
[24]	90 nm SiGe	250	116	Single-ended 4 CS	8-way Combining	15	3.8	20.8	11.8	17	7.6	1520	12

* Differential structure is considered as 2 cores,
** Estimated from measurement graph,
*** Loss of RF pad and balun de-embedded,
† PAE= $100 \times (P_{out} - P_{in})/P_{DC}(\%)$.

line ($TL_{ISML1} = 0$ um) by adjusting the value of the embedding network as shown in Fig. 11(b), the adoption of TL_{ISML1}, 20 um as a minimum, not only makes the matching more efficient but also helps prevent the unwanted magnetic coupling between the adjacent G_{max}-cores in the driver and power amplification stages [27].

Fig. 12 shows the design detail of the driver amplification stage G_{max}-core. Similar to PA stage design, fine-tuning for gain and operating frequency optimization is required. The final design value of X_4, X_5 and X_6 are 11.5, 0.5 and 63.1 Ω, respectively, and its equivalent TL based implementation can be achieved by using TL_4 ($Z_o = 50\Omega$, and $L_4 = 39.9$ um), TL_5 ($Z_o = 50\Omega$, and $L_2 = 1.5$ um), and TL_6 ($Z_o = 87\Omega$, and $L_6 = 139.5$ um).

V. IMPLEMENTATION AND MEASUREMENT RESULTS OF PROPOSED PA

A. PA DESIGN ADOPTING PROPOSED TECHNIQUE

A two-stage 150 GHz PA is implemented in a 65 nm CMOS process to verify the feasibility of the proposed simultaneous output power- and gain-matching technique. Fig. 13 shows the schematic of the two-stage 150 GHz PA. All matching networks, including the input, output, and interstage, are designed using microstrip lines with Z_o of 50 Ω. The interstage matching is done by 20 um TL_{ISML1} in combination with the shunt stub (TL_{ISML2}). Even though each G_{max}-core in the PA and DA stages is designed to meet $k = 1$ and $\theta = 180°$ for achieving G_{max}, the losses from passive components increase the k-factor slightly higher than 1. After adding the interstage, input, output matching networks, the PA shows the unconditional stability ($k > 1$ and $|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1$) over the entire simulated frequency ranges (DC∼f_{max}). Moreover, the oscillation is not observed in the transient simulation.

Fig. 14 shows the chip micrograph of the two-stage 150 GHz PA. The PA occupies an area of 556 um × 364 um, including the pads. The supply voltage is provided at the input pad through the on-wafer probe.

B. MEASUREMENTS RESULTS

Fig. 15 shows the measured S-parameters, k-factor, and $|\Delta| = |S_{11}S_{22} - S_{12}S_{21}|$ in comparison with the simulation results. A G-band extension module (V05VNA2Series WR05) and an N5247A PNA-X are used in the S-parameter measurement. The PA shows a peak power gain of 17.5 dB at 150 GHz. The measured S_{11}, S_{12}, and S_{22} of the PA are −15.6 dB, −22.1 dB, and −14.3 dB at 150 GHz, respectively. As expected in the simulation result, a superior output return loss (S_{22}) is achieved due to the proposed simultaneous output power- and gain-matching technique. The PA shows the unconditional stability ($k > 1$ and $|\Delta| < 1$) over the entire measured frequency ranges. In Fig. 15(a), the measured S_{21} is lower than 1 (0 dB) above 165 GHz. Therefore, the proposed PA does not function as an amplifier at operating frequencies above 165 GHz. The discrepancies between the simulations and measurements can be attributed to the inaccuracies in models for the MOSFETs and passive elements as well as the substrate coupling, which is not easy to incorporate into the simulation at such high operating frequencies.

Fig. 16 shows the measured gain vs. P_{in}, P_{out} vs. P_{in}, and PAE vs. P_{in} at $V_{DD} = 1$ V and 1.2 V, respectively, in comparison with the simulation results at the operating frequency of 150 GHz. An Agilent E8247C PSG CW signal generator

along with an Agilent D-band source module is used as a signal source, and an Erickson PM5 power meter is used to measure the output power in the large-signal measurement. The PA achieves peak PAE of 13.3 and 16.1 %, saturated output power (P_{sat}) of 10.3 and 9.4 dBm, OP_{1dB} of 5.3 and 4 dBm, and DC power consumption of 86.3 and 52.4 mW, respectively, under the bias voltage of 1.2 and 1 V.

Table 2 shows the measured performance summary and its comparison with the state-of-the-art CMOS and SiGe amplifiers operating at 110∼190 GHz. The proposed PA achieves the highest PAE, gain per stage, and P_{out} per single transistor among other reported D-band CMOS PAs, while achieving P_{sat} over 10 dBm without power combining circuit. Moreover, the performance of the proposed amplifiers is comparable to that of the SiGe technology based amplifiers, which have a much higher f_{max} and supply voltage.

VI. CONCLUSION

This paper proposes a new design method of a G_{max}-based simultaneous output power and gain matching technique. By adopting the optimized three-passive-elements-based embedding network for achieving G_{max}, a simultaneous output power- and gain-matching, gain-boosting, and high-output-power can be achieved at the same time without power combining circuit. The step-by-step design procedure of the simultaneous output power- and gain-matched G_{max} is also introduced as a design guideline. To achieve the required amount of power gain with low power consumption, the G_{max} concept is adopted in driver and power amplification stages to reduce the number of amplification stages, and the G_{max}-core in the DA stage is optimized for reducing the insertion loss of the interstage matching network. To verify the proposed design technique, a 150 GHz two-stage single-ended common source PA is implemented in a 65 nm CMOS process. The measured results of the PA shows the highest PAE, gain per stage, and P_{out} per single transistor among other reported D-band CMOS PAs. Moreover, the performance of the proposed amplifiers is comparable to that of the SiGe technology based amplifiers, which have a much higher f_{max} and supply voltage. The proposed technique is advantageous for achieving higher PAE, gain per stage, and P_{out} in any CMOS, SiGe, and compound semiconductor technologies.

REFERENCES

[1] P. H. Siegel, "Terahertz technology," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 3, pp. 910–928, Mar. 2002.
[2] R. Al Hadi, H. Sherry, J. Grzyb, Y. Zhao, W. Forster, H. M. Keller, A. Cathelin, A. Kaiser, and U. R. Pfeiffer, "A 1 k-pixel video camera for 0.7–1.1 terahertz imaging applications in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2999–3012, Dec. 2012.
[3] S. Kim, K.-Y. Choi, D.-W. Park, J.-M. Kim, S.-K. Han, and S.-G. Lee, "0.5 and 1.5 THz monolithic imagers in a 65 nm CMOS adopting a VCO-based signal processing," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2017, pp. 149–152.
[4] M. C. Kemp, "Explosives detection by terahertz spectroscopy—A bridge too far?" *IEEE Trans. THz Sci. Technol.*, vol. 1, no. 1, pp. 282–292, Sep. 2011.
[5] K. B. Cooper, R. J. Dengler, N. Llombart, B. Thomas, G. Chattopadhyay, and P. H. Siegel, "THz imaging radar for standoff personnel screening," *IEEE Trans. THz Sci. Technol.*, vol. 1, no. 1, pp. 169–182, Jun. 2011.
[6] F. Friederich, W. von Spiegel, M. Bauer, F. Meng, M. D. Thomson, S. Boppel, A. Lisauskas, B. Hils, V. Krozer, A. Keil, T. Loffler, R. Henneberger, A. K. Huhn, G. Spickermann, P. H. Bolivar, and H. G. Roskos, "THz active imaging systems with real-time capabilities," in *THz and Security Applications*. Dordrecht, The Netherlands: Springer, 2014, pp. 153–187.
[7] K. Ajito and Y. Ueno, "THz chemical imaging for biological applications," *IEEE Trans. THz Sci. Technol.*, vol. 1, no. 1, pp. 293–300, Sep. 2011.
[8] K. Tanaka, H. Hirori, and M. Nagai, "THz nonlinear spectroscopy of solids," *IEEE Trans. THz Sci. Technol.*, vol. 1, no. 1, pp. 301–312, Sep. 2011.
[9] C. Kulesa, "Terahertz spectroscopy for astronomy: From comets to cosmology," *IEEE Trans. THz Sci. Technol.*, vol. 1, no. 1, pp. 232–240, Sep. 2011.
[10] Z. D. Taylor, R. S. Singh, D. B. Bennett, P. Tewari, C. P. Kealey, N. Bajwa, M. O. Culjat, A. Stojadinovic, H. Lee, J.-P. Hubschman, E. R. Brown, and W. S. Grundfest, "THz medical imaging: *In vivo* hydration sensing," *IEEE Trans. THz Sci. Technol.*, vol. 1, no. 1, pp. 201–219, Sep. 2011.
[11] N. Shimizu, T. Ikari, K. Kikuchi, K. Matsuyama, A. Wakatsuki, S. Kohjiro, and R. Fukasawa, "Remote gas sensing in full-scale fire with sub-terahertz waves," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2011, pp. 1–4.
[12] P. Nazari, S. Jafarlou, and P. Heydari, "A CMOS two-element 170-GHz fundamental-frequency transmitter with direct RF-8PSK modulation," *IEEE J. Solid-State Circuits*, vol. 55, no. 2, pp. 282–297, Feb. 2020.
[13] A. Visweswaran, K. Vaesen, S. Sinha, I. Ocket, M. Glassee, C. Desset, A. Bourdoux, and P. Wambacq, "A 145 GHz FMCW-radar transceiver in 28 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 168–170.
[14] D. Simic and P. Reynaert, "A 14.8 dBm 20.3 dB power amplifier for D-band applications in 40 nm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2018, pp. 232–235.
[15] M. Seo, B. Jagannathan, J. Pekarik, and M. J. W. Rodwell, "A 150 GHz amplifier with 8 dB gain and +6 dBm P_{sat} in digital 65 nm CMOS using dummy-prefilled microstrip lines," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3410–3421, Dec. 2009.
[16] K. Katayama, M. Motoyoshi, K. Takano, L. C. Yang, and M. Fujishima, "133 GHz CMOS power amplifier with 16 dB gain and +8 dBm saturated output power for multi-gigabit communication," in *Proc. Eur. Microw. Integr. Circuit Conf.*, 2013, pp. 69–72.
[17] Z. Xu, Q. J. Gu, and M.-C. F. Chang, "A three stage, fully differential 128–157 GHz CMOS amplifier with wide band matching," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 10, pp. 550–552, Oct. 2011.
[18] H. Son, T. Jang, S. Kim, K. Jung, J. Kim, and C. Park, "Pole-controlled wideband 120 GHz CMOS power amplifier for wireless chip-to-chip communication in 40-nm CMOS process," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 8, pp. 1351–1355, Aug. 2019.
[19] A. Ali, J. Yun, F. Giannini, H. J. Ng, D. Kissinger, and P. Colantonio, "168–195 GHz power amplifier with output power larger than 18 dBm in BiCMOS technology," *IEEE Access*, vol. 8, pp. 79299–79309, 2020.
[20] H. Khatibi, S. Khiyabani, and E. Afshari, "A 173 GHz amplifier with a 18.5 dB power gain in a 130 nm SiGe process: A systematic design of high-gain amplifiers above $f_{max}/2$," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 1, pp. 201–214, Jan. 2018.
[21] N. Sarmah, P. Chevalier, and U. R. Pfeiffer, "160-GHz power amplifier design in advanced SiGe HBT technologies with P_{sat} in excess of 10 dBm," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 2, pp. 939–947, Feb. 2013.
[22] R. B. Yishay and D. Elad, "A 14 dBm 110–130 GHz power amplifier and doubler chain in 90 nm SiGe BiCMOS technology," in *Proc. IEEE 16th Topical Meeting Silicon Monolithic Integr. Circuits RF Syst. (SiRF)*, Jan. 2016, pp. 391–394.
[23] M. Kucharski, J. Borngräber, D. Wang, D. Kissinger, and H. J. Ng, "A 109–137 GHz power amplifier in SiGe BiCMOS with 16.5 dBm output power and 12.8% PAE," in *Proc. 47th Eur. Microw. Conf. (EuMC)*, Oct. 2017, pp. 1021–1024.
[24] H.-C. Lin and G. M. Rebeiz, "A 112–134 GHz SiGe amplifier with peak output power of 120 mW," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2014, pp. 163–166.
[25] Y.-H. Hsiao, Z.-M. Tsai, H.-C. Liao, J.-C. Kao, and H. Wang, "Millimeter-wave CMOS power amplifiers with high output power and wideband performances," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4520–4533, Dec. 2013.
[26] H. Bameri and O. Momeni, "A high-gain mm-wave amplifier design: An analytical approach to power gain boosting," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 357–370, Feb. 2017.

[27] D. W. Park *et al.*, "A 280-/300-GHz three-stage amplifiers in 65-nm CMOS with 12-/9-dB gain and 1.6/1.4% PAE while dissipating 17.9 mW," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 1, pp. 79–81, Jan. 2018.
[28] D.-W. Park, D. R. Utomo, B. H. Lam, S.-G. Lee, and J.-P. Hong, "A 230–260-GHz wideband and high-gain amplifier in 65-nm CMOS based on dual-peak G_{max}-core," *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1613–1623, Jun. 2019.
[29] B. Yun, D.-W. Park, W.-J. Choi, H. U. Mahmood, and S.-G. Lee, "A 250-GHz 12.6-dB gain and 3.8-dBm P_{sat} power amplifier in 65-nm CMOS adopting dual-shunt elements based G_{max}-core," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 3, pp. 292–295, Mar. 2021.
[30] D.-W. Park, D. R. Utomo, J.-P. Hong, K. Vaesen, P. Wambacq, and S.-G. Lee, "A 247 and 272 GHz two-stage regenerative amplifiers in 65 nm CMOS with 18 and 15 dB gain based on double-G_{max} gain boosting technique," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2020, pp. 1–2.
[31] H. Wang and K. Sengupta, *RF and Mm-Wave Power Generation in Silicon*. New York, NY, USA: Academic, 2015.
[32] D. Chowdhury, P. Reynaert, and A. M. Niknejad, "Design considerations for 60 GHz transformer-coupled CMOS power amplifiers," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2733–2744, Oct. 2009.

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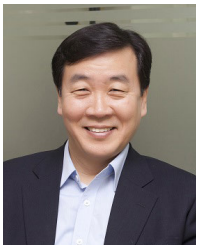

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