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A 24-Channel Neurostimulator IC With Channel-Specific Energy-Efficient Hybrid Preventive-Detective Dynamic-Precision Charge Balancing

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ABSTRACT This paper presents the design, development, and experimental characterization of a 24-channel programmable charge-balanced current-mode neurostimulator IC. Each channel is equipped with a quad-threshold voltage-based charge imbalance detection and a dedicated hybrid preventive-detective charge balancing circuit. The interplay of the preventive and detective control loops utilized for charge balancing has resulted in minimizing the power and timing overhead of the proposed strategy for maintaining a charge-neutral electrode-tissue interface, while avoiding the risk of unintended stimulation. The design offers dynamic programmability for the safe and unsafe charge imbalance thresholds, as well as for the balancing speed and precision. The IC is fabricated in a standard $0.18\mu m$ CMOS technology with an overall active area of $2.27mm^2$. Experimental characterization results of different circuit blocks are presented and discussed. Additionally, the IC's efficacy in conducting charge-balanced stimulation is experimentally validated under various scenarios and for the full range of stimulation current magnitude, showing the balancing accuracy, latency, and active time. Experiments are conducted both with a simplified electrical model of the interface impedance as well as *in vitro*. Compared to the state-of-the-art stimulators with a closed-loop charge balancer, the presented work offers the most energy-efficient charge balancing technique, the shortest required inter-pulse interval (i.e., neutralization time), and the highest balancing precision.

INDEX TERMS Charge balancing, neurostimulator, implantable IC, neural interface, energy-efficient design, closed-loop control, VNS, electrical current-mode stimulation.

I. INTRODUCTION

Over the past two decades, design and development of implantable neurostimulators of various modalities (voltage-, current-, or charge-mode) have been widely investigated [1]–[5]. Among them, current-mode stimulators have been utilized more than other schemes as they operate relatively independent of the electrode-tissue interface impedance variations, thus offer a precise control of charge transfer to the tissue. Such a control allows for maintaining the charge injection's spatial and temporal densities below unsafe levels, and also reduces the possibility of harmful charge accumulation at the electrode-tissue interface [6]–[8]. However, even a perfectly charge-balanced current-mode stimulation pulse (i.e., $Q_A = Q_C$ in Fig. 1(a)) does not guarantee balanced and reversible electrochemical processes at the interface. Therefore, residual charges will accumulate at the interface, allowing for oxidation/reduction to continue even after the stimulation is over, hence cause tissue damage in the long run [6], [7]. It is shown in [9] that a non-zero voltage remains at the electrode-tissue interface after a charge-balanced current-mode stimulation, mainly due to (i) interphasic charge leakage by the Faradaic resistor (defined in Fig. 1(b)), and (ii) irreversible over-potential

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chemical reactions during the stimulation [6]. Therefore, it is critical to continuously monitor the electrode potential and neutralize it during inter-pulse resting intervals (i.e., the time period between two biphasic stimulation pulses as defined in Fig. 1(a)) to avoid electrode/tissue damage and also to prevent from violating the charge injection rate during the anodic or cathodic phases.

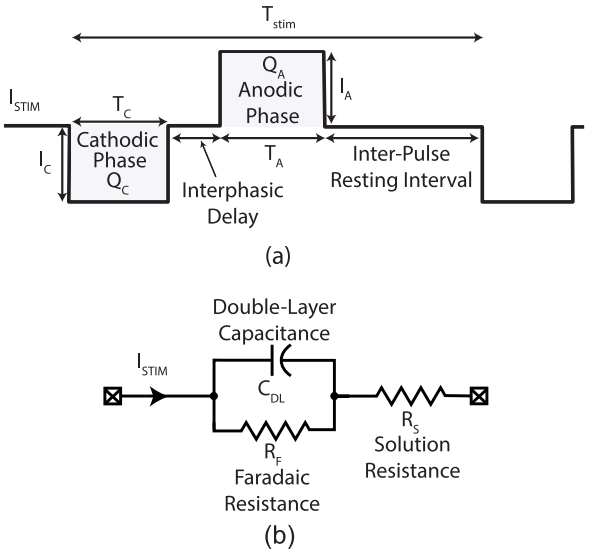

FIGURE 1. (a) A typical timing diagram of an interphasic-delayed cathodic-first biphasic constant-current stimulation pulse, with the definition of various timing parameters. (b) A simplified electrical model of the electrode-tissue interface.

Motivated by this, various passive and active charge balancing strategies have been investigated in the literature. The most conventional method uses an AC-coupling capacitor to block the unintended irreversible flow of charges to the interface [10], [11]. Despite the effectiveness of this method, it has been shown that to leave a sufficient voltage headroom for the stimulator's current driver, either the stimulation current has to be very small (e.g., a few μ As) or very-large off-chip capacitors (a few nF) should be used, which prevent from channel-count scaling [12], [13].

An on-chip alternative solution is to short circuit the electrode to a reference voltage during the inter-pulse resting interval to remove the residual charge accumulated on the electrode-tissue interface capacitance. A critical point in implementing the shorting technique is controlling/limiting the discharge rate. If not limited, the discharging current could stimulate the tissue unintentionally as it has been shown that even a few μ As could depolarize a cell membrane and evoke action potentials [14], [15]. On the other hand, maintaining a very slow (but safe) discharge rate translates into a longer required time for balancing, hence imposes timing/frequency limitation on stimulation [16]–[18]. To relax this speed-safety tradeoff, the shorting method is usually integrated with dynamic stimulation current matching to decrease the initial biphasic mismatch down to a few nanoamperes (nAs) [13], [16].

In recent years, several closed-loop charge balancing techniques have been reported, almost all of them being based on the idea of continuously monitoring the electrode voltage and responsively neutralizing the interface through the injection of anodic/cathodic micro-pulse trains [19]–[24]. The neutralization normally gets activated when the electrode voltage deviates from the reference voltage by a safety threshold value, typically defined a few times smaller than the water oxidation/reduction voltage window [6]. While a variety of implementations of this idea have been proposed, there are a few common major issues among them that have severely limited their performance.

The first problem is a safety-power tradeoff related to the detection of the safe/unsafe charge accumulation. An overly relaxed threshold increases the risk of tissue/electrode damage, while setting it too close to the reference makes the balancing circuit hypersensitive to any imbalance, hence, unnecessarily increasing the power consumption required for charge balancing. To set the threshold, first, the desired maximum DC current error (e.g. the widely-accepted 100nA European standard [16], [25], [26]) should be converted to a voltage error. As will be discussed in Section II.A., this conversion depends on the stimulation frequency and the double-layer capacitance (C_{DL}) value. Considering commonly used electrodes (C_{DL} <100nF) and a relatively-high stimulation frequency of 100Hz [20], [27], [28], the 100nA error translates into a few millivolts voltage error. This shows that (i) some of the threshold values used in the literature (20-100mV range [20], [21], [24], [29], [30]) might only work for low-frequency stimulation or small C_{DL} values; and (ii) the threshold value is dependent on both the application and the electrodes, so it must be programmable.

The second major issue is in handling persistent (e.g., systemic) imbalances. Because of their non-random nature, persistent errors must be removed after every single stimulation pulse. Failure to do so, not only promotes neural damaging reactions, but might also increase the mismatch in the subsequent stimulation pulses due to deviation of inter-pulse resting voltage from the reference level. On the other hand, activating the balancing circuit at every inter-pulse resting interval significantly increases power consumption. Additionally, since the balancer should inject sub-μA-pulses (to avoid unintended stimulation [15], [31], [32]), for a large persistent imbalance, the required inter-pulse resting interval could become considerably longer, thus, limiting the maximum stimulation frequency. It should also be noted that using these high-frequency balancing pulses after every stimulation pulse could cause major side effects on neural pathways which affect the long-term effectiveness of neural stimulation [33].

In this work, we present a 24-channel current-mode neurostimulator integrated circuit (IC) with a programmable quad-threshold charge imbalance detection, and a closed-loop hybrid preventive-detective charge balancing strategy. To overcome the first above-mentioned issue, each stimulation channel is equipped with a 4-level comparator circuit

(the four thresholds are individually programmable) that allows for breaking off the described safety-power tradeoff by defining a buffer zone between the *SAFE* and *UNSAFE* levels (i.e., introducing programmable hysteresis to the comparator). To fix the second mentioned issue, the IC conducts charge balancing with a hybrid preventive-detective strategy that employs (i) push/pull current pulse insertion upon detection of an unsafe imbalance (detective), and (ii) automatic adjustment of the subsequent stimulation pulses to remove/minimize persistent imbalances (preventive).

The combination of the hysteresis-based imbalance detection and the hybrid preventive-detective balancing strategy results in minimizing the required active time for charge balancing, hence, its required power consumption, without sacrificing balancing accuracy. We have tested the efficacy of the proposed method under challenging conditions by adding intentional mismatch to the stimulator. Our validation experiments cover various scenarios, all including the full range of stimulation current magnitudes both using an electrical model of the electrode-tissue interface and *in vitro*.

The rest of the paper is organized as follows. Section II describes the proposed algorithmic method used for detection and removal of charge imbalance and how it adapts to different stimulation frequencies and mismatch levels. This section also describes both system-level and circuit-level implementations of the presented 24-channel neurostimulator IC with a particular focus on the implementation of the proposed charge balancing strategy. Various design considerations related to balancing circuits, their speed, and accuracy adjustment are discussed. Section III presents various electrical characterization measurement results showing the efficacy of the presented system in several different scenarios and evaluating its precision limits. *In vitro* experimental setup and measurement results are also presented in this section. The section ends with a detailed comparison with the state of the art. Section IV discusses the experimental measurement results and design tradeoffs and compares the presented work with the state of the art. Section V concludes the paper.

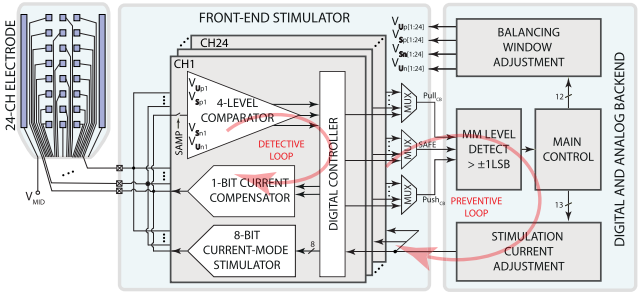

FIGURE 2. Top-level block diagram of the presented neurostimulator, employing the proposed hybrid preventive-detective charge balancing.

II. NEUTRALIZATION METHODOLOGY

Fig. 2 depicts the top-level block diagram of the presented neurostimulator microsystem and the employed hybrid charge balancing strategy. Each stimulation channel includes (i) an 8-bit current-mode digital-to-analog converter (IDAC) to generate biphasic current pulses, (ii) a 4-level comparator for continuous monitoring of the electrode voltage during the inter-pulse resting intervals, (iii) a digital controller to evaluate if the electrode voltage is safe or not, and to report persistent unsafe imbalances to the digital backend, and (iv) a push/pull current DAC for neutralizing the accumulated charge through pulse insertion (the detective loop).

All 24 channels are connected to a digital backend that (i) sets the stimulation magnitude, frequency, and pulse width, (ii) sets the safe and unsafe threshold voltages for each channel individually, and (iii) upon receiving a signal indicating a persistent error from any of the channels, calculates the necessary adjustment to the subsequent stimulation pulses for that channel to prevent the error from happening again (the preventive loop).

A. DETECTIVE AND PREVENTIVE LOOPS OPERATION PRINCIPLE

The detective control loop works based on (i) sampling the electrode voltage (V_E) during the inter-pulse resting interval, (ii) evaluating the level of accumulated charge, and (iii) triggering a responsive action if the charge imbalance is deemed unsafe. A safe/unsafe condition is typically defined based on an application-dependent maximum DC current error (I_{DC}) (e.g., 100nA) [25], [34], [35] and it is translated into a voltage level by

$$V_{unsafe-Threshold} = \frac{I_{DC} \times T_{stim}}{C_{DL}}, \tag{1}$$

where T_{stim} is the stimulation period (defined in Fig. 1(a)) and C_{DL} is the interface double-layer capacitance. According to (1), depending on the stimulation frequency and the electrode used (i.e., different C_{DL} values), the unsafe threshold could vary from a few millivolts to hundreds of millivolts (more details on the calculation of our safety thresholds in section III). Once V_E goes beyond the unsafe threshold, the charge balancer must bring it back to safety. However, if the balancer stops as soon as V_E becomes smaller than $V_{unsafe-threshold}$, a small residual charge in the next pulse could bring V_E back to the unsafe zone. Ideally, the loop should work until V_E is as close as possible to the reference (i.e., neutral) voltage. Therefore, as illustrated in Fig. 3(a), in addition to the negative and positive unsafe thresholds ($V_{\mathbf{U}n}$, $V_{\mathbf{U}p}$), we have defined safe threshold values ($V_{\mathbf{S}n}$, $V_{\mathbf{S}p}$), and designed the balancer so that it won't stop until $V_{\mathbf{S}n} < V_E < V_{\mathbf{S}p}$. As shown in Fig. 3(a), the four levels of comparison are defined to determine if V_E is in the safe range (i.e., $V_E \in [V_{\mathbf{S}n}, V_{\mathbf{S}p}]$ or inside $\Delta V_{\mathbf{S}}$), or the unsafe range (i.e., $V_E \notin [V_{\mathbf{U}n}, V_{\mathbf{U}p}]$, or outside $\Delta V_{\mathbf{U}}$), or neither (i.e., within $\Delta V_{\mathbf{U}}$ but outside $\Delta V_{\mathbf{S}}$). All threshold voltages ($V_{\mathbf{S}p}$, $V_{\mathbf{S}n}$, $V_{\mathbf{U}p}$, $V_{\mathbf{U}n}$) are individually programmable, which allows for adjusting the definition of safe and unsafe ranges as well as the hysteresis width (i.e., the yellow region in Fig. 3(a)). The threshold programmability is a critical

feature because electrode's capacitance could vary significantly depending on its size and material, hence, the same amount of accumulated charge could result in different voltages ($Q = C \times V$). The magnitude of the push/pull current source used for the detective loop's charge balancing ($I_{balance}$) is chosen based on the application, and also as a tradeoff between the latency and the accuracy of compensation. Increasing this current's magnitude allows for quick neutralization of the accumulated charges but comes at the cost of losing neutralization precision as well as risking an unintended stimulation of neurons [14], [15], [31]. As will be described in details (Section II.D), we have chosen the $I_{balance}$'s value to ensure safe and timely neutralization with sufficient accuracy demanded by the application.

The preventive control loop is designed to complement the detective loop to further minimize the time and power overhead of the neutralization process. Every time the detective loop performs charge balancing, a copy of the commands (i.e., *SAFE*, $Pull_{CB}$, and $Push_{CB}$ as shown in Fig. 2) is sent to a backend processing unit to store the error magnitude. If the charge error happens to be larger than $I_{LSB} \times T_A$ (or T_C), where T_A (or T_C) is the anodic (cathodic) phase duration and I_{LSB} is the smallest current that can be generated by the 8-bit stimulator DAC, then a red flag goes up. If the red flag stays up at two consecutive inter-pulse resting intervals, the preventive loop gets activated to adjust the amplitude of the next stimulation pulses to counter the large persistent error in a preventive manner.

Thanks to the stimulation pulse adjustments made by the preventive loop, the aforementioned accuracy-latency tradeoff in the detective loop is relaxed, as the detective loop only needs to get activated for minor non-persistent imbalances (e.g., due to unpredictable electrochemical reactions at the electrode-tissue interface). Therefore, a small push/pull charge injection by the detective loop is expected to bring V_E to the safe range within a very short period of time, yielding a low-power and timely neutralization that is unlikely to cause any unintended stimulation. Additionally, since the preventive loop works by just adding an offset to the stimulation parameters to account for the persistent error, it comes at almost zero additional energy cost and its added power consumption is limited to the few digital blocks used for detecting mismatch persistence.

B. BALANCING SYSTEM OPERATION SEQUENCE

Fig. 3(a) shows a conceptual operation sequence diagram of the presented charge balancing system. After each stimulation pulse and during the inter-pulse resting interval, the digital backend generates a pulse *CB* to initiate the charge balancing process with a programmable delay (controlled by the *CB* pulse-width). The delay is electrode-specific and is set according to the Faradaic discharge current. Once the *CB* goes back down to zero, the electrode voltage monitoring is initiated by activating the sampling signal (i.e., $SAMP = 1$), which is followed by subsequent compensation ($Pull_{CB}$ or $Push_{CB}$) if V_E is deemed unsafe. As shown, if the first sample

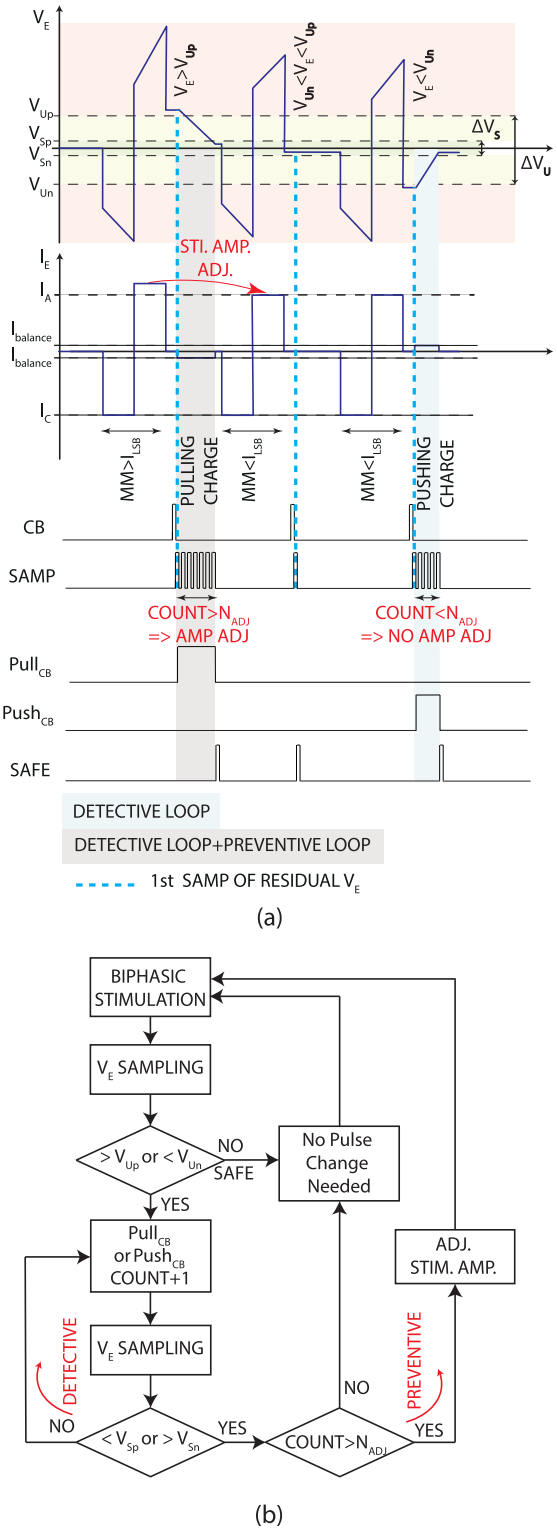

FIGURE 3. (a) Conceptual operation sequence of control signals during stimulation episodes that require balancing with one or both loops. (b) Simplified control flowchart of the proposed hybrid preventive-detective charge balancing technique.

falls in the unsafe zone (i.e., outside ΔV_U), the sampling and pulse insertion (i.e., the detective loop) continue until V_E is back in the safe range (i.e., within ΔV_S). ΔV_S is dynamically

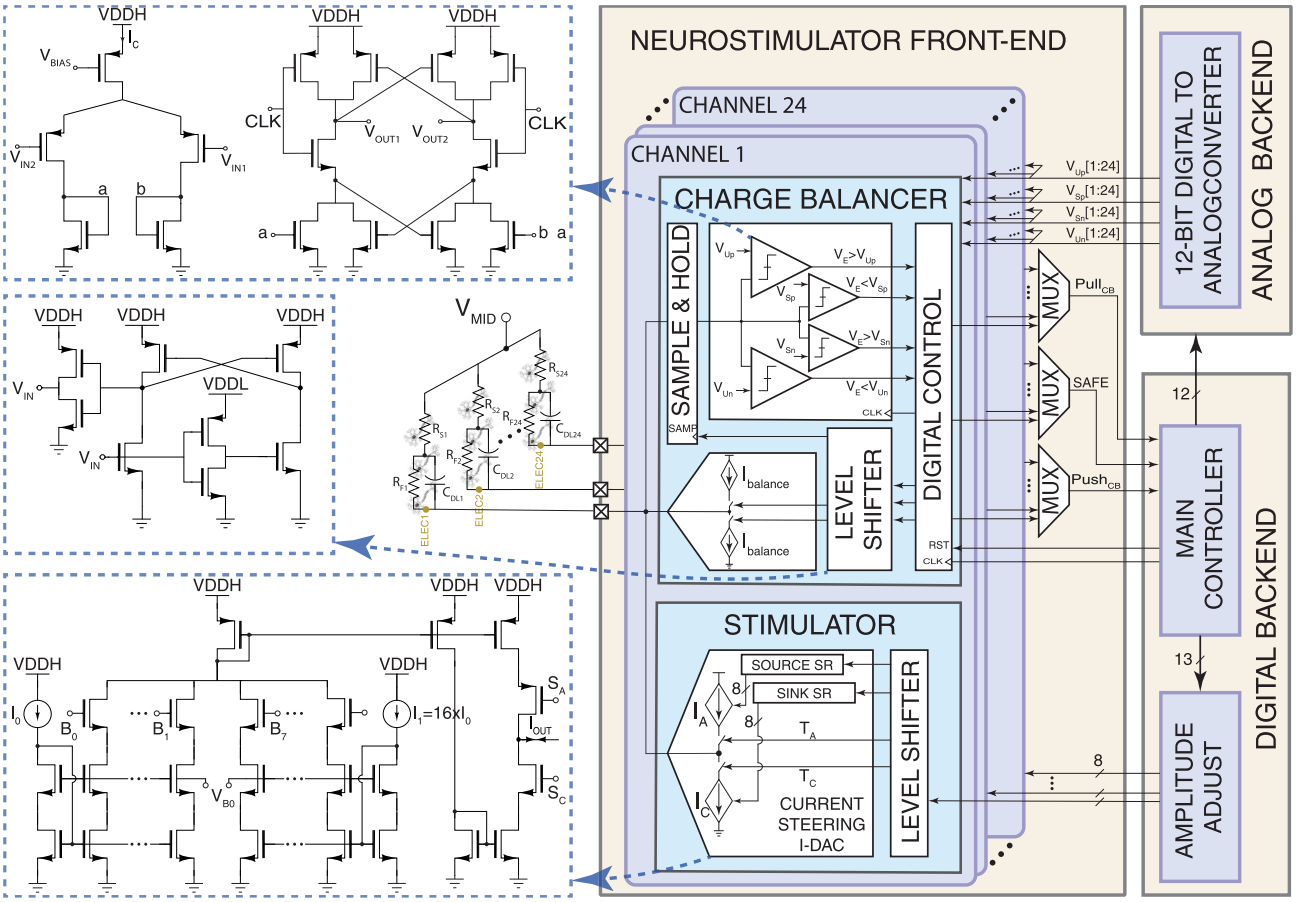

FIGURE 4. Detailed block diagram of the presented charge-balanced neurostimulator with simplified circuit schematics of the major blocks.

set based on the required accuracy for charge balancing when the neutralization process is accomplished. It is also shown in Fig. 3(a) that in the case that a large imbalance (i.e., mismatch (MM) $>$ I_{LSB}) is detected, the preventive loop gets activated to bring back the imbalance of the subsequent pulses to a range that can be safely and quickly handled by the detective loop. In case an unsafe condition for the first sample is not detected, no further sampling or balancing is performed until the next stimulation pulse. Fig. 3(b) shows the flowchart of the described charge balancing method, indicating the functions and conditions to activate the two loops.

C. SYSTEM- AND CIRCUIT-LEVEL IMPLEMENTATION

Fig. 4 depicts the detailed system-level implementation of the presented microsystem with simplified circuit schematics of its major blocks. Each of the 24 stimulating channels generates biphasic current pulses with a programmable (8 bits resolution) magnitude. The stimulator circuit is composed of two 4-bit binary-weighted segments, which are biased using two current sources different by a factor of 16 for a total resolution of 8 bits [36]. The stimulator has an output impedance of 160kΩ for the full range of working frequencies. Compared to the utilized electrode impedance (discussed in Section III.B), this is sufficiently large to warrant a constant stimulation current over the stimulator's voltage compliance. Four StrongArm latches with preamplifiers are used to quantize the sampled V_E during the inter-pulse resting interval and feed the results to the in-channel digital controller. The cascode transistors in the positive feedback latch along with the highly-matched diode-connected-load preamplifier isolate the regeneration nodes from input nodes to minimize the coupling of kickback noise to the electrode voltage. The in-channel controller decides whether a responsive balancing (i.e., detective loop) is required, and if it is, sends commands to the in-channel current DAC ($I_{balance}$) for detective control. Also, if it detects a persistent imbalance (i.e., the two consecutive red flags defined earlier), sends the imbalance magnitude (derived from pulse-width of $Pull_{CB}$ and $Push_{CB}$) to the backend controller to be used for preventive control. To maximize the stimulator voltage compliance, thick-oxide transistors are used for the 4-level comparator and both the stimulator's 8-bit IDAC and the balancing DAC. Therefore, logic level shifters are used to interface the low-voltage digital backend and the high-voltage mixed-signal front end.

D. ANALYTICAL TUNING OF CHARGE BALANCING LOOPS

To achieve charge neutralization in a single inter-pulse resting interval, the detective loop's $I_{balance}$ was set based

on (i) the maximum measured mismatch between stimulator IDAC's cathodic and anodic currents ($MM\%$), (ii) the application-specific minimum inter-pulse resting interval ($T_{rest,min}$), (iii) the size of C_{DL}, and (iv) the maximum amount of charge delivered during a single stimulation pulse phase (i.e., cathodic or anodic):

$$I_{balance} \geq \frac{MM\% \times T_{PW} \times I_{stim,max}}{T_{rest,min}}, \tag{2}$$

where, T_{PW} is the width of the cathodic/anodic phase and $I_{stim,max}$ is the maximum stimulation current magnitude. At the same time, the charge on C_{DL} must be fully compensated in one resting interval. C_{DL}'s value is determined through a calibration phase prior to stimulation onset, similar to the method described in [37]. To ensure a complete and timely discharge,

$$I_{balance} \geq \frac{(V_{Up} - V_{MID}) \times C_{DL}}{T_{rest,min}}, \tag{3}$$

where V_{Up} is the programmable positive unsafe threshold voltage defined previously, and V_{MID} is the reference voltage. $I_{balance}$ value must satisfy both (2) and (3). Moreover, to avoid an infinite series of positive and negative compensations when bringing the V_E back to the safe range, the electrode voltage sampling frequency ($1/T_{CLK}$) is set based on the size of the safe window (ΔV_S shown in Fig. 3(a)), such that the balancing voltage steps do not exceed ΔV_S,

$$T_{CLK} < \frac{\Delta V_S \times C_{DL}}{I_{balance}}. \tag{4}$$

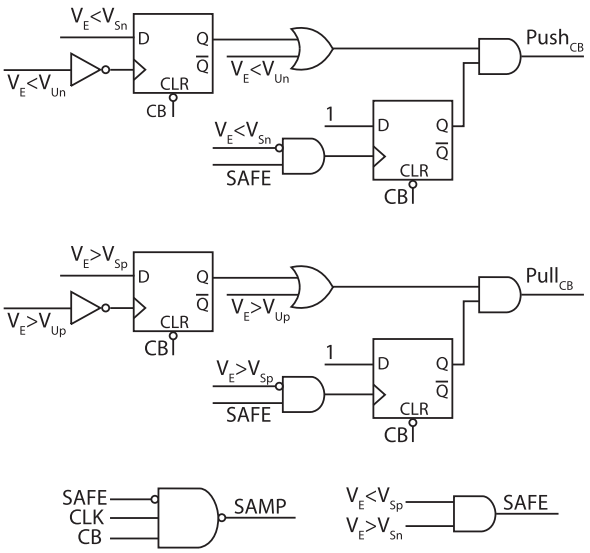

FIGURE 5. Simplified logic-level circuit schematic of the in-channel digital controller used for the detective loop.

Fig. 4 also shows that three signals from each channel (i.e., *SAFE*, $Push_{CB}$, and $Pull_{CB}$) are sent to the digital backend to communicate the existence of a persistent charge imbalance to the preventive controller. Fig. 5 shows how these signals are generated in the in-channel digital controller when *CB* is activated. If either $Push_{CB}$ or $Pull_{CB}$ turns on in two consecutive inter-pulse resting intervals, the digital processor starts to measure their pulse-width by counting the number of clock cycles that the $I_{balance}$ has been pulled/pushed (*COUNT*). Based on this, *N*, the number of required LSB adjustments in the neurostimulator's 8-bit IDAC is calculated as,

$$N = COUNT/N_{ADJ}, \tag{5}$$

where N_{ADJ} is defined as the number of T_{CLK} cycles that $I_{balance}$ should be injected to deliver the same amount of charge as stimulation IDAC's LSB during one phase (e.g., cathodic or anodic) of stimulation,

$$N_{ADJ} = \frac{I_{LSB}}{I_{balance}} \times \frac{T_{PW}}{T_{CLK}}. \tag{6}$$

The preventive charge balancing process is performed independently for each stimulation channel and continues until the error is reduced to within the $\pm I_{LSB}$ range, hence, relaxing the balancing requirement for the detective loop.

An FPGA (Intel Cyclone III, EP3C16) is used to program and control the stimulation and charge balancing on the fly. The magnitude, frequency, and pulse-width of the biphasic stimulation are set independently for each channel. These parameters are stored in on-chip data registers and can be updated on the fly. The parallel control interface is multiplexed among 24 channels to minimize the required I/O ports. The timing control of charge balancing, safe and unsafe thresholds, and the balancing current magnitude are also individually programmed for each channel and can be updated based on the application requirements.

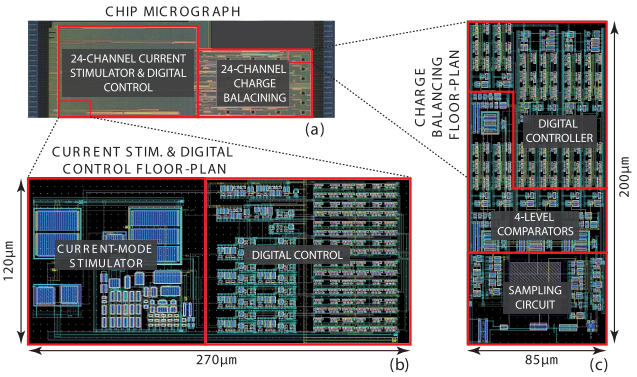

FIGURE 6. (a) Annotated chip micrograph with (b) layout floorplan of the stimulator and (c) charge balancing circuits.

Fig. 6(a)-(c) show the micrograph and layout floorplan of the stimulator and charge balancing circuits, respectively. The 24-channel neurostimulator is designed and fabricated in a standard 0.18μm CMOS technology with a total active area of 2.27mm^2. The chip works with two voltage supplies of 1.8V for digital controllers and 3.3V for the mixed-signal front end.

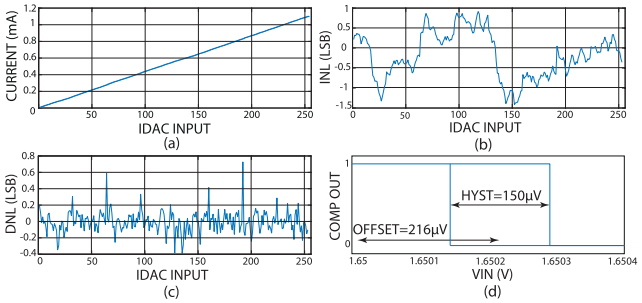

FIGURE 7. Measured (a) transfer function, (b) INL, and (c) DNL of the IDAC. (d) Post-layout simulated input-output characteristics of the comparator.

III. EXPERIMENTAL CHARACTERIZATION

A. CIRCUIT- AND SYSTEM-LEVEL MEASUREMENT RESULTS

Fig. 7(a)-(c) show the experimentally-measured transfer function, integral nonlinearity (INL), and differential nonlinearity (DNL) of the IDAC, respectively, all of them over the digital input range of 0 to 255 at a conversion rate of 100 Sa/sec. As shown, IDAC is capable of generating current magnitudes from 4μA to 1mA with an 8-bit resolution and has a maximum INL and DNL of -1.46LSB and 0.72LSB, respectively. The maximum mismatch (in all channels) between the anodic and cathodic currents of the presented 8-bit IDAC is measured to be $<2\%$. Fig. 7(d) shows the post-layout simulated input-output characteristics of the implemented comparator, showing offset and hysteresis voltages of 216μV and 150μV, respectively. The input dynamic range of the comparator covers from 0.8V to 2.4V.

For electrical characterization, after reviewing the literature and considering the most common range for interface capacitance values [38], we chose a large C_{DL} to create a challenging scenario (i.e., same accumulated charge results in smaller voltage, hence, more difficult to detect). This decision also ensures sufficient voltage headroom while delivering a wide range of charges to the interface (up to 500nC). According to (1) and considering the commonly-used maximum DC current error of 100nA (e.g., [16], [26]), the unsafe threshold voltages ($V_{\mathbf{U}p}$ and $V_{\mathbf{U}n}$) are programmed to $\pm$10mV (w.r.t. V_{MID}). To derive this unsafe range, we used the values of 100nF as the size of double-layer capacitance and 100Hz as the frequency of stimulation, which are considered the upper bound values [20], [27], [28], [39]. Using the electrodes with C_{DL} $<$100nF and stimulation frequency$<$100Hz will make the unsafe condition more relaxed (i.e., $\Delta V_{\mathbf{U}}$ $>$20mV). The 8-bit in-channel IDACs were programmed to generate the full current range (i.e., 4μA-1mA). T_{PW} and $T_{rest,min}$ were also programmed to be 500μs and 9ms, respectively, resulting in stimulation with 100Hz frequency and 10% maximum duty cycle. According to equations (2)-(6) and setting the safe range to $\pm$1mV, the balancing current $I_{balance}$, clock period (T_{CLK}) of sampling signal, and N_{ADJ} were calculated to be 1μA, 1μs, and 2000, respectively.

To make the charge balancing task more challenging, an additional 2% positive mismatch was intentionally added by setting the IDAC's anodic current 5LSB higher than its cathodic current in all measurements. Also, to have sufficient data to evaluate the balancing loops' performance, each test included 100 successive stimulation pulses.

Fig. 8 shows the measured electrode voltage waveforms with (black) and without (gray) charge neutralization. As shown, without charge balancing, a residual voltage higher than 700mV is accumulated on C_{DL} after 100 consecutive stimulation pulses. With charge balancing, we observed that both loops become active in the beginning because of the high mismatch between anodic and cathodic currents. As shown in the left inset, the initial interplay of the two loops results in some fluctuations in the inter-pulse resting voltage, which are damped quickly. Once the mismatch is reduced to less than $\pm I_{LSB}$, the preventive loop is automatically deactivated, leaving the detective loop as the only mechanism for neutralization, until another persistent mismatch reappears. As shown in the right inset, the detective loop runs on demand and only when needed (indicated by horizontal purple bars with the "*DETECTIVE*" label in the right inset).

Fig. 9 shows the average active time of the detective charge balancing loop over the full range of IDAC current magnitudes (averaged over 100 successive stimulation pulses for each IDAC input). As expected, the plot shows that the required time for balancing generally increases with the stimulation current magnitude. This is mainly because the absolute value of mismatch between the anodic and cathodic currents increases (despite the relative mismatch remaining the same) when the IDAC input increases. Therefore, for a fixed $I_{balance}$, it will take more time to remove the imbalance. The difference between the Pull and Push durations is due to the same polarity of both inherent and intentional mismatches. The figure also shows that the compensation time never exceeds 1.7ms, which is smaller than the available inter-pulse resting interval (9ms). This short balancing time for such a large mismatch (up to 4%) at maximum stimulation current magnitude confirms that a large portion of the mismatch is compensated by the preventive loop. To put this into perspective, without the preventive loop, the detective loop would have required 20ms to compensate for the same 4% mismatch (Q =20nC) with the same $I_{balance}$ = 1μA. Additionally, as mentioned previously, the charge balancing time is programmable and the 1.7ms could be decreased if needed (for high-frequency stimulation, at the cost of a higher power), or increased (for low-frequency stimulations, to save power).

Fig. 10 shows the measured average net compensation charge that is delivered to the interface by $I_{balance}$ versus the IDAC input (100 successive stimulation pulses for each digital input). It also shows the average energy consumption for charge balancing per biphasic stimulation pulse. As shown, a maximum charge of 1.2nC is delivered, which confirms that the preventive loop has successfully reduced the maximum 4% (i.e., 10$\times I_{LSB}$, 20nC) mismatch to under I_{LSB} (because $1.2nC/500\mu s = 2.4\mu A < I_{LSB}$). The figure also shows that a maximum energy of 8.8nJ is consumed to neutralize a single

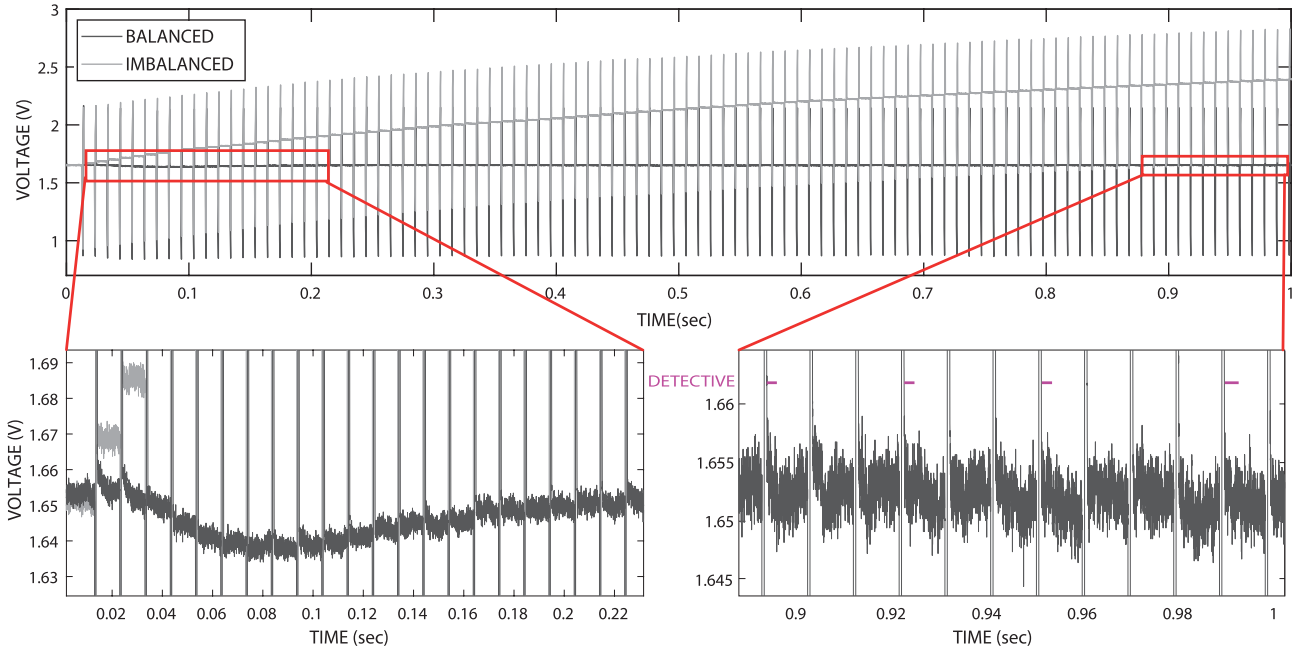

FIGURE 8. Measured V_E for 100 successive biphasic imbalanced and balanced current-mode stimulation pulses with amplitude of 105LSB and 100LSB for anodic and cathodic phases (to create an intentional mismatch), respectively.

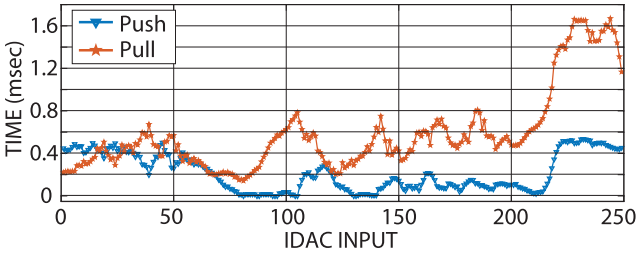

FIGURE 9. Experimentally measured active time of the detective charge balancing loop for a 100Hz (10% duty cycle) stimulation pulse, with a pulse magnitude of up to 1mA and up to 4% (inherent + intentional) mismatch, compensated with $I_{balance} = 1\mu$A. The active time is inversely proportional to the programmable $I_{balance}$.

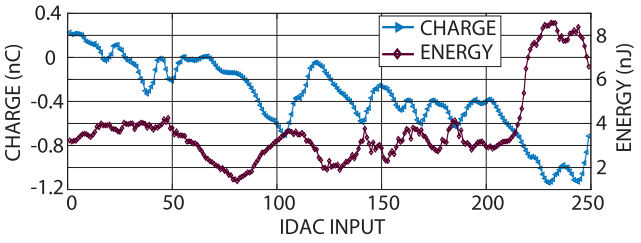

FIGURE 10. Measured delivered compensation charge by the detective loop, and the static energy consumption for active charge balancing per 1ms of biphasic stimulation, both over the full range of the stimulation IDAC.

stimulation pulse, which translates into a maximum power consumption of the charge balancing block for the described scenario (100Hz, 10% duty cycle) to be $8.8nJ \times 100Hz = 0.88\mu$W.

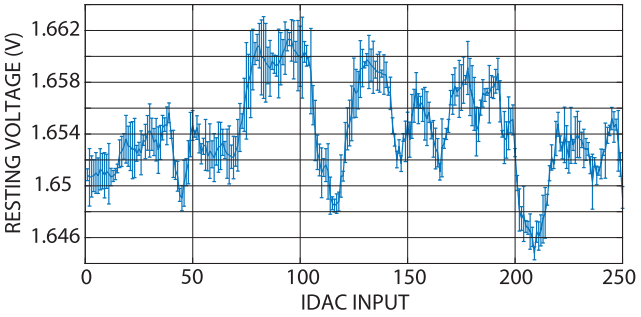

FIGURE 11. Measured resting voltage during the inter-pulse resting intervals showing the precision of the proposed hybrid charge balancing for the full range of digital inputs.

The balancing precision of the presented current-mode stimulator is obtained by measuring the residual voltage on the interface capacitor during the inter-pulse resting intervals, as shown in Fig. 11. The figure shows the mean values and error bars for residual voltages over the full range of IDAC current magnitudes (100 data points for each IDAC input). It confirms that the inter-pulse resting residual voltages for all IDAC inputs are within the predefined programmable unsafe window of $\pm$10mV.

B. IN VITRO MEASUREMENT RESULT

Fig. 12 shows the *in vitro* measurement setup for the presented charge balancer with the electrodes placed in phosphate-buffered saline solution (PBS). Custom-designed stainless steel-based surface electrodes were used for *in vitro* experiments. The impedance of each electrode with an active

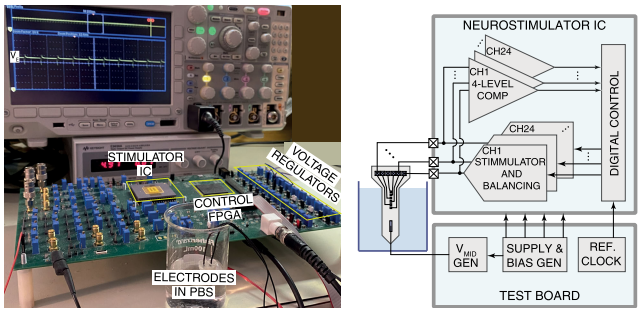

FIGURE 12. ***In vitro*** **measurement setup, showing the electrodes in PBS solution and the presented neurostimulator IC mounted on a testbench PCB.**

area of $2mm^2$ was extracted by applying the method introduced in [37]. The parameters are found to be approximately $R_S = 700\Omega$, $C_{DL} = 1.6\mu$F, and $R_F = 2\text{k}\Omega$ at our stimulation frequency (100Hz). To evaluate the functionality of the presented charge balancer, *in vitro* experiments were performed by applying cathodic-first biphasic stimulation pulses (full IDAC range of 0-255), and monitoring the charge balancing efficacy and precision. The stimulation pulses (100Hz and 10% biphasic duty cycle) were generated with an intentional 5LSB mismatch (similar to the electrical tests). The $I_{balance}$, T_{CLK} of the sampling signal, and N_{ADJ} were set to 1μA, 1μs, and 2000, respectively. Fig. 13(a) shows the measured electrode voltage for the IDAC's ten largest current magnitudes (246 to 255, 0.5ms for each magnitude), to evaluate the efficacy of the presented charge balancing method under the worst-case scenario. As shown in Fig. 13(a), the inter-pulse resting voltage is maintained steady for different stimulation currents despite applying intentional mismatch at the beginning of each 0.5ms interval. Fig. 13(b) shows the measured electrode voltage for the IDAC's digital input of 246 with and without charge balancing. As shown in Fig. 13(b), without charge balancing, a residual voltage of 169mV was accumulated on the electrode-solution interface after 50 consecutive stimulation pulses. Fig. 13(c) magnifies the measured electrode voltage during several consecutive pulses for the case that the balancing loops are active. In the beginning, both preventive and detective loops are engaged to compensate for the persistent mismatch. After reducing the persistent mismatch to less than $\pm I_{LSB}$, the preventive loop turns off automatically and the detective loop is the only mechanism responsible for on-demand charge balancing.

Fig. 14 shows the measured average active time of the detective loop's anodic and cathodic $I_{balance}$ over the full range of IDAC's current magnitudes (averaged over 100 successive stimulation pulses for each digital input). As shown, the compensation time never exceeds 1.2ms for each stimulation pulse, which is on average below the programmed allowed time of $N_{ADJ} \times T_{CLK} = 2$ms allocated for the detective charge balancing loop to compensate for each pulse. As mentioned previously, balancing could be accelerated by increasing the balancing current magnitude or decreasing the N_{ADJ} value.

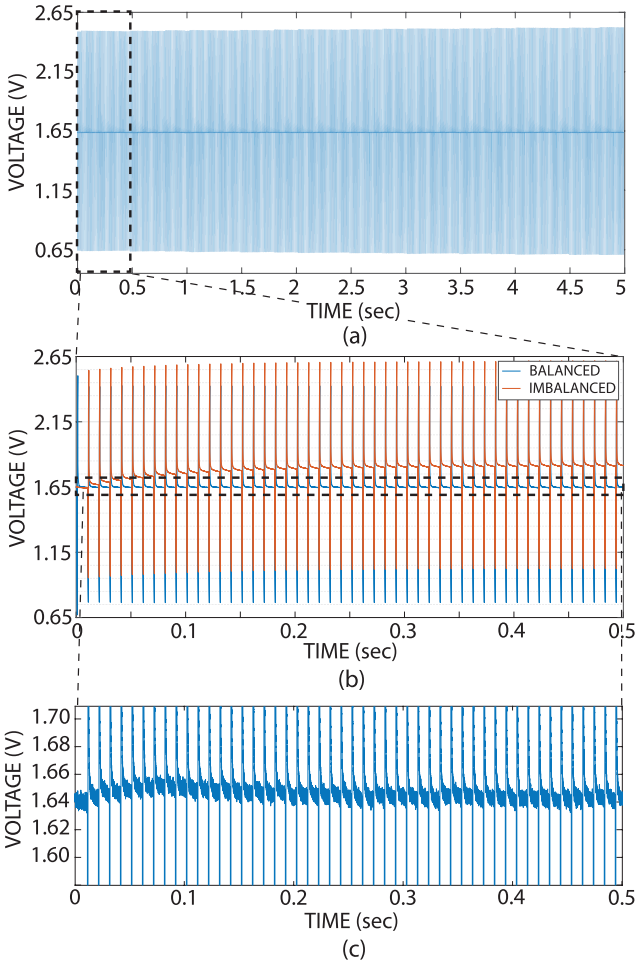

FIGURE 13. **Measured (*in vitro*) V_E (a) for stimulator IDAC's digital input range of 246-255 while the charge balancing is active, and (b) for the digital input 246, with and without charge balancing. (c) Magnified view of the measured V_E's inter-pulse resting interval's voltage while the charge balancing is active (digital input = 246).**

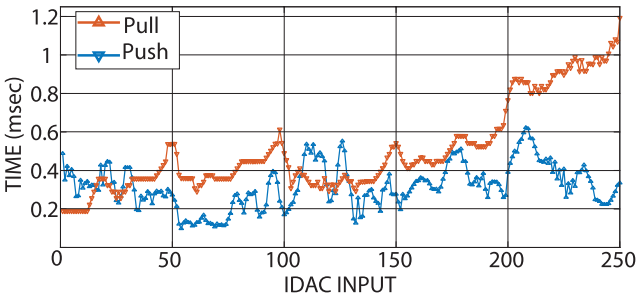

FIGURE 14. **Measured (*in vitro*) average active time of the detective charge balancing loop for a 100Hz (10% duty cycle) stimulation pulse, with a magnitude ranging from 4μA-1mA (i.e., 0-255), and up to 4% (inherent + intentional) mismatch, compensated with $I_{balance} = 1\mu$A. The active time is inversely proportional to the programmable $I_{balance}$.**

Fig. 15 shows the mean values and error bars of the measured electrode voltage during the inter-pulse resting intervals, displaying how much they deviate from the V_{MID} over the full range of IDAC's digital input (averaged over 100 stimulation for each current magnitude). As shown, the inter-pulse

TABLE 1. Performance comparison with the state-of-the-art charge-balanced neurostimulator.

Reference	TBioCAS'16 [40]	JSSC'18 [21]	BioCAS'18 [41]	IEECON'20 [42]	IEEE ACCESS'20 [31]	TBioCAS'17 [18]	This Work
Application	N/R	Blood Pressure Control	N/R	Epiretinal Implants	N/R	Neural Stimulation	Peripheral Neural Stimulation
Technology	0.18μm	0.35μm HV	0.35μm HV	0.35μm HV	0.18μm	0.18μm	0.18μm
Power Supply	12V	22V	49V	20V	12.8V	3.3V	3.3V
Number of Channels	1-Bipolar	N/R	6	4	1	8	24
Area/Ch	1.08mm^2	1.94mm^2	2.6mm^2	N/R	0.11mm^2	0.28mm^2	0.1mm^2
Current Range (Resolution)	Up to 3mA (15 bits)	1μA-5.12mA (9 bits)	2μA-10mA (9 bits)	4μA-1mA (5 bits)	Up to 1mA (5 bits)	Up to 0.25mA (8 bits)	4μA-1mA (8 bits)
Monitoring Method	Dual Loop Current Calibration	Voltage Monitoring	Voltage Monitoring	Voltage Monitoring	Voltage Monitoring	Error Current Sampling	Voltage Monitoring
Compensation Technique	Electrode Shorting	PI-Controlled Offset Compensation and Inter-Pulse Current Insertion	PI-Controlled Offset Compensation and Electrode Shorting	Offset Regulation	Anodic Pulse Modulation and Electrode Shorting	Biphasic Current Calibration and Electrode Shorting	Stimulation Pulse Adjustment and Inter-Pulse Current Insertion
Electrode Impedance Model	1kΩ + (100nF $\|$ 10kΩ)	1kΩ+(100nF$\|$ 500kΩ)	N/R	N/R	10kΩ + (100nF $\|$ 10MΩ)	N/R	1kΩ + 100nF
Experimental Validation	*In Vivo*	*In Vitro*	*In Vitro*	*In Vitro*	NO	*In Vitro &In Vivo*	*In Vitro*
Power Consumption (Charge Balancing Only)	<150μW	56μW	>41μW	N/R	N/R	N/R	<0.88μW/Ch
Charge Balancing Precision (Current Mismatch)	11.89mV (0.25%)	$\pm$20mV	$\pm$20mV	$\pm$50mV	N/R	N/R (0.3%)	$\pm$4mV (0.08%)

N/R: Not Reported
N/A: Not Applicable

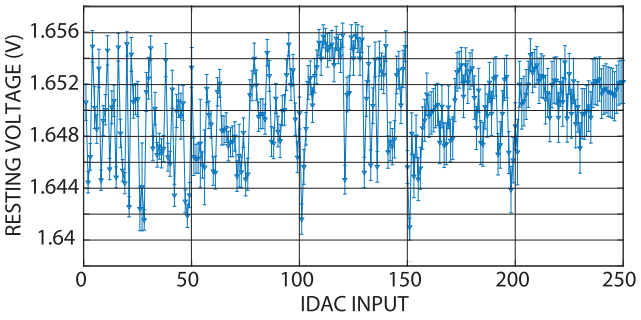

FIGURE 15. Measured (*in vitro*) resting voltage during the inter-pulse resting intervals, showing the precision of the proposed hybrid charge balancing for the full range of digital inputs.

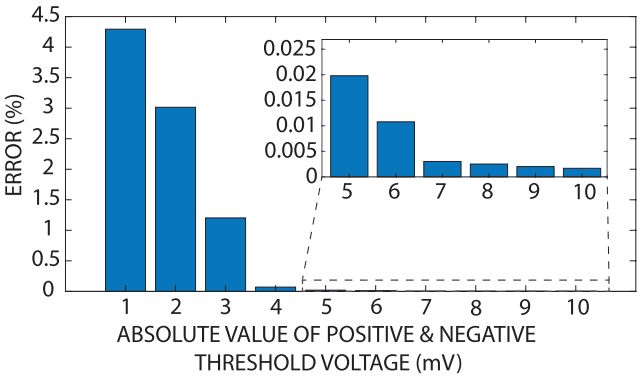

FIGURE 16. *In vitro* measured balancing error percentage versus the unsafe window range (the safe window is scaled proportionally), showing an error <1% for unsafe thresholds as small as $\pm$6mV.

resting voltages don't exceed the programmed unsafe window $[V_{Un}, V_{Up}]$ of $\pm$10mV for all current magnitudes.

We also investigated the efficacy of the presented charge balancing method when the unsafe window is narrowed down. Our expectation was that the offset and hysteresis of the detective loop's 4-level comparator will be the bottleneck in achieving higher neutralization precision. As such, we measured the error induced in the detective loop during the *in vitro* test as an indicator of inefficacy. The error is measured by calculating the average time when both push and pull balancing currents are switched on simultaneously or successively in the same inter-pulse resting interval (both being indicative of the comparator's malfunction). Fig. 16 shows the percentage of this error for the unsafe windows of $\pm$(1-10 mV). Each error bar is averaged over IDAC's digital input range of 0 to 255 with 100 stimulation pulses for each digital input (i.e., 25600 data points). The data in this figure shows an error of <0.5% when the thresholds for the unsafe zone are defined as $\pm$4mV or higher (i.e., $\pm$5mv, $\pm$6mV,..., $\pm$10mV), and a maximum error of 4.3% when choosing $\pm$1mV as the thresholds for the unsafe zone (and reducing the safe window to $\pm$0.5mV). Therefore, the presented device's balancing precision is evaluated to be $\pm$4mV, which leaves a residual charge of 400pC on an interface capacitance of 100nF. This translates into a residual charge mismatch of 0.08%, considering that 500nC is delivered per pulse.

IV. COMPARISON AND DISCUSSION

Table 1 compares the presented charge-balanced neurostimulator IC with the recently-published designs that employ various types of active charge balancing techniques. Thanks to the employed hybrid preventive-detective strategy, the presented work offers the highest energy efficiency compared to the state of the art. This is mainly because the required pulse insertion by the detective loop (hence, its active time) is minimized due to the removal of large persistent mismatches by the preventive loop. Minimizing the detective loop's active time also has the advantage of minimizing the timing constraints (i.e., minimum required inter-pulse resting interval or maximum frequency of stimulation) imposed by our method compared to the state of the art.

It should be noted that the charge balancing power consumption, precision, safety, and latency are interdependent and also are dependent on the charge imbalance severity. For our experiments, as described, we chose a stimulation frequency of 100Hz with 10% duty cycle (1ms ON, 9ms OFF) and up to 4% mismatch. Accordingly, for balancing, we chose $I_{balance} = 1\mu$A to simultaneously ensure (i) no unintended stimulation (safety), (ii) sub-μW power consumption, (iii) 4mV precision, and (iv) latency of less than 9ms (maximum of 1.7ms and 1.2ms measured in electrical and *in vitro* tests, respectively). Thanks to the programmability of the

safe/unsafe thresholds and the $I_{balance}$, the latency could be made even shorter (e.g., for stimulation frequency >100Hz) by slightly trading off the precision or power consumption. Similarly, for lower stimulation frequencies, lower power consumption could be achieved by trading off the speed.

V. CONCLUSION

A power- and time-efficient 24-channel charge-balanced current-mode neurostimulator IC was presented. Channel-specific charge balancing was performed with an in-channel-integrated quad-threshold interface charge imbalance detection circuit and a dedicated hybrid preventive-detective balancing strategy. Thanks to the dynamic programmability of unsafe and safe charge imbalance thresholds in each channel, the design is optimized to strike a tradeoff between required power consumption as well as the charge balancing latency and safety. Additionally, the interplay between the preventive (i.e., automatic stimulation pulse adjustments) and detective (i.e., closed-loop push/pull current pulse insertion) charge balancing loops resulted in minimizing the charge balancing power and timing overhead.

The IC was designed and fabricated in a standard 0.18μm CMOS technology with an active area of $2.27mm^2$. It was fully characterized and the circuit- and system-level measurement results were presented. The efficacy of the proposed charge balancing strategy was validated experimentally both using electrical model for the interface impedance and *in vitro* over the full range of stimulation current magnitude and various unsafe and safe windows. Compared to the state of the art, the presented work yields the lowest neutralization latency and power consumption while offering a programmable balancing precision, all thanks to the employed strategies for detection and correction/prevention of charge imbalance.

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