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A Cross Connected Asymmetrical Switched-Capacitor Multilevel Inverter

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ABSTRACT A Switched-Capacitor Multilevel Inverter (SCMLI) topology is proposed here, which can generate up to fifteen levels with one unit and can be extended further for getting higher levels. The proposed SCMLI has a lesser number of switching devices with respect to other recently proposed structures presented in this paper. It also has the capacitor self-balancing property. Power loss analysis has also been done using PLECS software. Maximum efficiency of 96.33 % has been achieved. A generalized comparative study has also been carried out with the newly presented topologies in different research articles considering several parameters. In order to validate the structure presented in this paper, simulation is done in Matlab®2018a, and the simulation results obtained are verified using an experimental prototype.

INDEX TERMS Level-shifted PWM, switched-capacitor MLI, total harmonic distortion, multilevel inverter, self- voltage balancing.

I. INTRODUCTION

Inverters play a very crucial role in various industrial applications. Enhanced power quality requirements in various industrial applications have led to the manifold increment in the research field of multilevel inverters, as conventional inverters have limitations in fulfilling these requirements. Multilevel inverters have superior output quality with respect to the conventional inverters, such as more sinusoidal-like output voltage, low total harmonic distortion (THD), low voltage and dv/dt stress, lesser power loss, minimized electromagnetic interference on output waveforms, the capability of handling higher power levels, etc. [1], [2]. MLIs have these qualities due to the fact that they have the potential to produce a staircase output waveform [3]. On the other hand, conventional MLIs require a higher component count to obtain more output levels, suffer from capacitor voltage balancing problems, and the absence of self-voltage boosting capability [4].

Different reduced device count MLIs have been presented in the literature [5]–[10] to remove the shortcoming of higher component requirements in conventional MLIs. However, these MLIs lack a boosting feature to get a desired output voltage level. To remove the problem of capacitor voltage unbalance in conventional MLIs, some complex control algorithms have been developed, or auxiliary circuits having multi-output boost converter have been added to the inverter structure [11]–[14]. These capacitor voltage balancing methods result in the increment of weight, complexity, and overall cost of the inverter. To mitigate the problems mentioned above in conventional MLIs and reduced device count MLIs, SCMLIs have come into the picture. Capacitors act as alternate DC voltage sources in SCMLIs. These MLIs utilize the charging and discharging of the capacitors in order to produce

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near the sinusoidal output. Additionally, SCMLIs do not have any complex control logic or auxiliary circuits for balancing the capacitor voltages.

Lately, a good number of novel SCMLIs have come into the picture. Papers presented in [15]–[17] have topologies with an H- bridge inverter at the end connected in series with the switched capacitors. Self-voltage balancing, voltage gain, and only one DC source are the merits of these topologies over the conventional MLIs. Nevertheless, these topologies have more capacitors and higher active switch count, which lead to large size, overall high cost, and increased complexity. An SCMLI structure has a cascaded connection of a boost converter, and a two-level inverter is proposed in [18]. The inverter is used to generate polarity, and the boost converter generates the multilevel step voltage. An SCMLI topology which is having an SC- frontend and backend as H-bridge, is presented in [19]. Higher output levels are produced using the SC-frontend. In [20], a nine-level inverter has been proposed having ten switches compared to the one proposed in [21] with twelve switches and the one in [22] with eleven switches for the same level. All three proposed topologies have the advantage of voltage gain and capacitor voltage balancing ability. A new SC-topology having cross-connected switches is proposed in [23]. The topology configuration is such that the leakage current is eliminated, but it uses a higher number of components for higher levels. A seven-level SCMLI with a gain of 1.5 and capacitor voltage balancing ability has been proposed in [24], which uses only one DC source. Shiva *et al.* [25] have proposed a nine-level single-source SCMLI structure with self-voltage balancing, boosting capability, and low switch stress. A novel asymmetrical SCMLI has been proposed in [26], where voltage gain of 2 is achieved, and comparative analysis show improvement in different components like the number of dc supply, voltage gain, etc. A new inverter having switched series-parallel asymmetric sources has been proposed in [27]. Power losses are reduced using a unique combination of the basic unit, and its comparison is also shown graphically. A new type of SCMLI with a quasi-resonant inductor which is connected in series with the capacitor charging loop to suppress the current spikes, has been proposed in [28]. An improvement on the previous structures by eliminating the bidirectional switches using an appropriate positioning of the DC supply is proposed in [29].

This paper proposes a new cross-connected asymmetrical SCMLI topology with a low voltage power switch for a single-phase system. This topology has the merit of a lesser component requirement. The proposed topology comprises two DC voltage sources, two diodes, one bidirectional switch, eight unidirectional switches, and two capacitors and can generate up to fifteen voltage levels per unit, which can also be extended to higher levels. The capacitor voltage balancing problem is not there as the charge balance is maintained over the full cycle. The performance of the proposed topology is verified by comparing DC supply count, number of switches, and switch stress with several other topologies.

II. THE PROPOSED 15 LEVEL INVERTER

This section discusses the structure of the proposed 15 level inverter, its working principle, and its extension for higher levels.

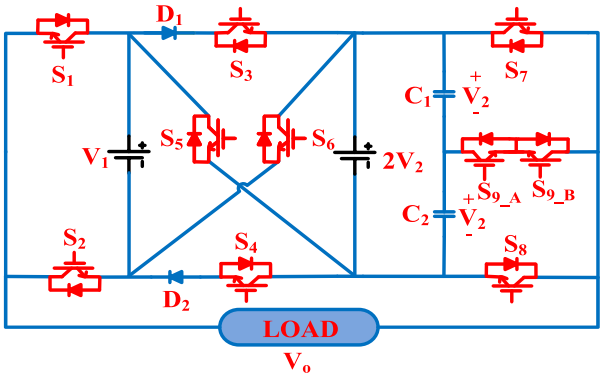


FIGURE 1. Proposed fifteen-level SCMLI topology.

A. CIRCUIT CONFIGURATION

The proposed structure has been shown in Fig. 1. It has two asymmetrical DC supplies (V_1 and $2V_2$), two diodes (D_1 and D_2), two capacitors (C_1 and C_2), one bidirectional (S_{9_A}, S_{9_B}), and eight unidirectional (S_1- S_8) switches. This structure is able to generate 15 levels at the output. The switch pairs (S_1, S_2), (S_3, S_5), (S_3, S_6), (S_4, S_5), (S_4, S_6), and (S_7, S_8) should not have simultaneous ON states so that short-circuiting of the DC voltage sources V_1 and $2V_2$ does not occur. The bidirectional switch is at the capacitor's midpoint, which clamps their voltage to V_2 and taps any of the capacitor voltage to the load.

B. DESCRIPTION AND WORKING OF THE PROPOSED SCMLI TOPOLOGY

All the 15 switching states of the inverter are shown in Fig. 2 and Table 1. The red-marked loops in the figure are the conductive paths. '0' and '1' denote that the corresponding switch is turned OFF and turned ON, respectively. Charged capacitors in the respective switching states are also given in the table. Here, the DC voltage sources are related to each other according to the following equation:

$$V_2 = \frac{1}{5} V_1 = V_{dc} \tag{1}$$

All the fifteen levels can be realized easily by looking at the switching table and its corresponding switching diagram. For instance, to generate the third level i: e $V_O = 3$V, switches S_2, S_3, and S_8 have to be turned ON simultaneously, as shown in Fig. 2. C_1 and C_2 are charged to V_{dc} through the DC voltage source '$2V_2$'. Capacitor voltage balancing in the basic unit can be understood by visualizing Fig. 3. Capacitors C_1 and C_2 should have equal voltages. It means that the energy released from the capacitor C_1 should be the same as that of the energy released from the capacitor C_2 in one complete cycle. Taking 3rd level as an example, the voltage waveforms at level $+3V_{dc}(\theta_2$ to $\theta_3)$ and $-3V_{dc}(\pi + \theta_2$ to $\pi + \theta_3)$ are the same,

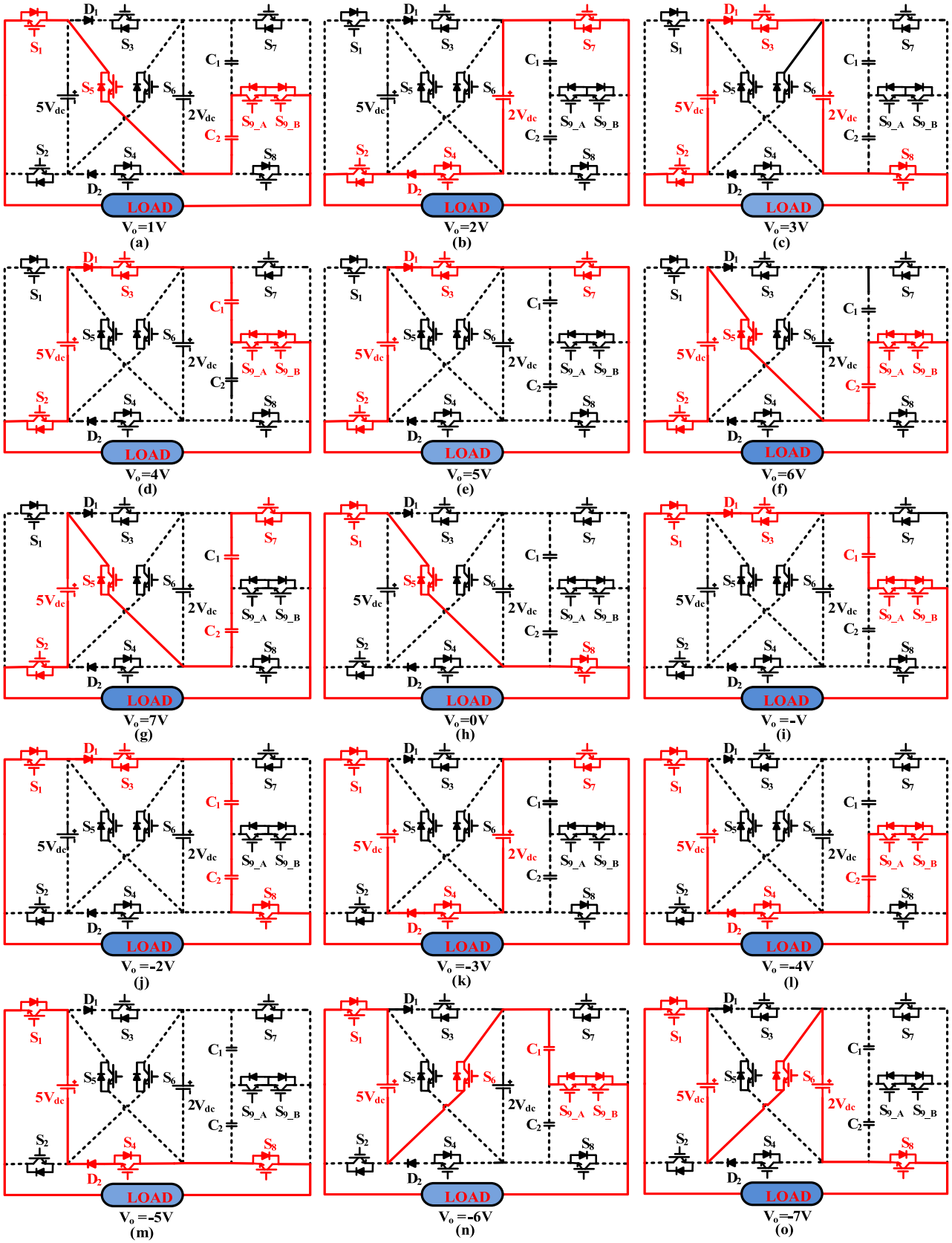


FIGURE 2. Switching states of the inverter.

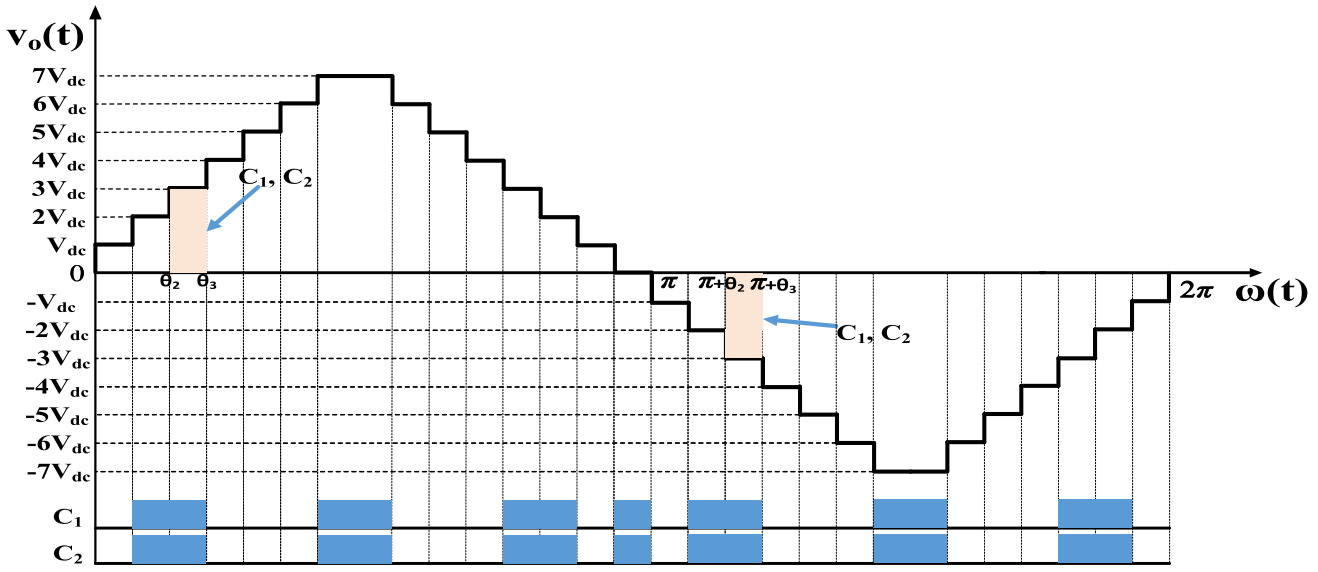


FIGURE 3. Typical 15 level output voltage showing capacitor voltage balance.

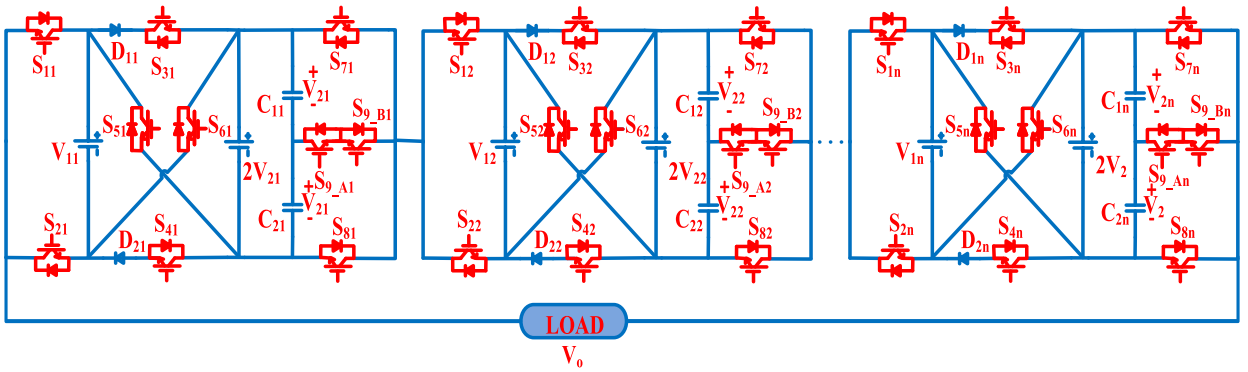


FIGURE 4. Extension of the proposed topology.

as shown in Fig. 3. Similarly, the current waveforms will also be equal. Hence energy stored in positive and corresponding negative levels is equal, and thus the capacitor voltage balance is maintained.

C. TOPOLOGY EXTENSION

Higher levels at the output can be achieved by connecting the basic unit in cascade form. Fig. 4 shows the extension of the presented structure. The output voltage of the overall system will be the sum of output voltages of the individual units i: e

$$V_o = V_1 + V_2 + \ldots + V_n \tag{2}$$

where V_1, V_2, V_n represents the output voltages of the first, second, and n^{th} unit, respectively. The required number of switches (N_{sw}), the number of levels (N_L), number of DC voltage sources (N_{dc}), number of capacitors (N_{cap}), number of drivers (N_{dr}) maximum output voltage ($V_{o,max}$) and total blocked voltage of all the switches (V_{TB}) can be expressed by

$$N_{sw} = 10n \tag{3}$$

$$N_L = 15n \tag{4}$$

TABLE 1. Different switching states of the proposed inverter.

Switches									Vo	Charging Capacitor
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9		
0	1	0	0	0	1	1	0	0	0	C_1, C_2
0	1	0	0	0	1	0	0	1	V_2	--
0	1	0	0	0	1	0	1	0	$2V_2$	C_1, C_2
1	0	0	1	0	0	1	0	0	$V_1 - 2V_2$	C_1, C_2
1	0	0	1	0	0	0	0	1	$V_1 - V_2$	--
1	0	0	1	0	0	0	1	0	V_1	--
1	0	0	0	0	1	0	0	1	$V_1 + V_2$	--
1	0	0	0	0	1	0	1	0	$V_1 + 2V_2$	C_1, C_2
1	0	0	0	1	0	0	1	0	0	C_1, C_2
1	0	0	0	1	0	0	0	1	$-V_2$	--
1	0	0	0	1	0	1	0	0	$-2V_2$	C_1, C_2
0	1	1	0	0	0	0	1	0	$-(V_1 - 2V_2)$	C_1, C_2
0	1	1	0	0	0	0	0	1	$-(V_1 - V_2)$	--
0	1	1	0	0	0	1	0	0	$-V_1$	--
0	1	0	0	1	0	0	0	1	$-(V_1 + V_2)$	--
0	1	0	0	1	0	1	0	0	$-(V_1 + 2V_2)$	C_1, C_2

$$N_{cap} = N_{dc} = 2n \tag{5}$$

$$N_{dr} = 8n \tag{6}$$

$$V_{o.max} = (15n - 1)/2 \tag{7}$$

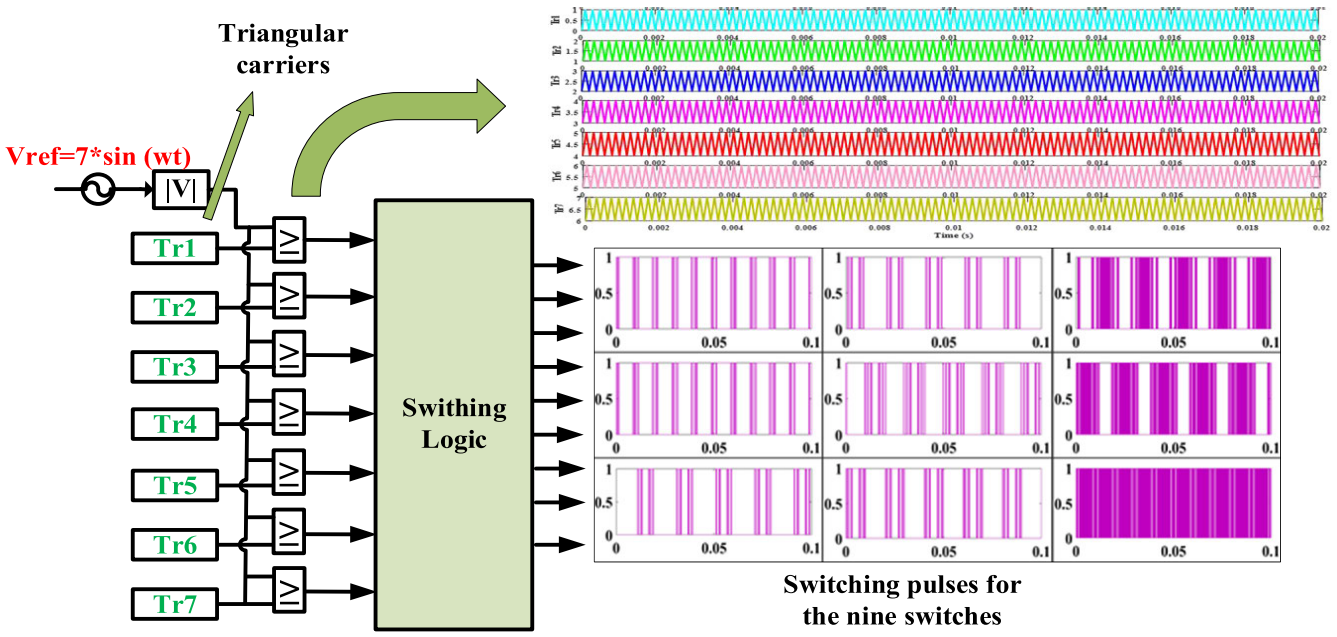


FIGURE 5. Level shifted PWM technique used for the proposed SCMLI.

$$V_{TB} = 44(15n - 1)/14 \tag{8}$$

where, n is the number of basic units.

III. MODULATION STRATEGY

Modulation techniques play an important role in multilevel inverters since they affect control dynamics, harmonics, switching loss, filter size, etc. Increased switching loss, high complexity, higher switching harmonics, and increased switching frequency exist in traditional modulation methods. The level-shifted PWM method has been used here to obtain the necessary gate pulses. A single sinusoidal reference waveform is compared with the seven carrier signals (Tr1 to Tr7), as shown in Fig. 5, to generate seven new signals, which are then modified according to the switching logic given in Table 1 to obtain the required gate pulses. The reference and carrier signals have the amplitude of 7 and 1, respectively. Here carrier frequency is taken to be 5 kHz.

IV. CALCULATION OF THE TOTAL BLOCKED VOLTAGE IN THE SWITCHES

The total blocked voltage (V_{TB}) of all the switches is an essential parameter in the design of inverter as it influences the overall price of the inverter. Its low value suggests a lower cost of the inverter. We can calculate it by using the following equation:

$$V_{TB} = V_{TB,u} + V_{TB,b} \tag{9}$$

where, $V_{TB,u}$ and $V_{TB,b}$ are the blocking voltages of the unidirectional and bidirectional switches, respectively. As there are eight unidirectional switches in each unit and the total unit count is 'n', $V_{TB,u}$ is written as:

$$\mathrm{V_{TB,u}} = \sum_{\mathrm{i=1}}^{\mathrm{n}} \sum_{\mathrm{j=1}}^{8} \mathrm{V_{Sji}} \tag{10}$$

where, $V_{S_{ji}}$ is the blocking voltage of the jth unidirectional switch for the ith unit. These blocked voltages can be calculated as follows:

$$V_{S_{1i}} = V_{S_{2i}} = V_{1i} = 5V_{2i} \tag{11}$$

$$V_{S_{3i}} = V_{S_{4i}} = V_{5i} = V_{6i} = V_{1i} + 2V_{2i} = 7V_{2i} \tag{12}$$

$$V_{7i} = V_{8i} = 2V_{2i} \tag{13}$$

$V_{S_{1i}}, V_{S_{2i}}, \ldots, V_{S_{8i}}$ are the blocked voltages of the unidirectional switches in the ith unit. So, the gross blocking voltage of the whole cascaded units will be the sum of all the individual units and can be written as:

$$V_{TB,u} = \sum_{i=1}^{n} 42V_{2i} \tag{14}$$

Since there is only one bidirectional switch i: e switch number 9,

$$V_{TB,b} = \sum_{i=1}^{n} V_{S_{9i}} = \sum_{i=1}^{n} 2V_{2i} \tag{15}$$

By substituting equations (14) and (15) in equation (9), the gross blocked voltage of all the switches will be:

$$V_{TB} = V_{TB,u} + V_{TB,b} = \sum_{i=1}^{n} 44V_{2i} \tag{16}$$

The maximum output voltage of the presented structure is given by:

$$V_{o,max} = \sum_{i=1}^{n} V_{1i} + \sum_{i=1}^{n} 2V_{2i} \tag{17}$$

Since, $V_{1i} = 5V_{2i}$, equation (17) can be written as:

$$V_{o,max} = \sum_{i=1}^{n} 7V_{2i} \tag{18}$$

Using equation (16) and (18), we have

$$V_{TB} = \frac{44}{7} V_{o,max} = 6.28V_{o,max} \tag{19}$$

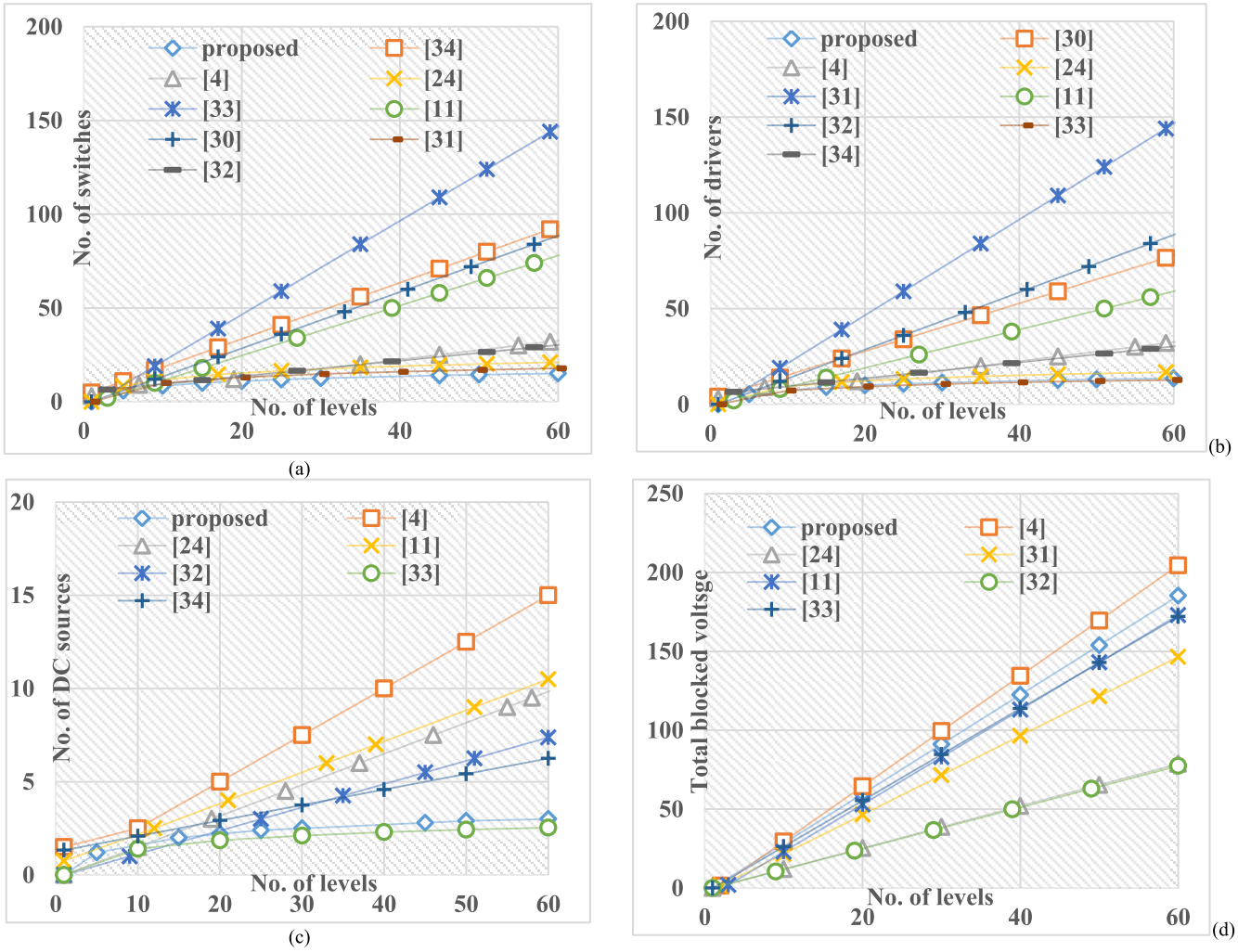


FIGURE 6. Comparison of presented structure with different structures in terms of (a) number of switches (N_{sw}) (b) number of drivers (N_{dr}) (c) number of DC sources (N_{dc}) (d) total blocked voltage (V_{TB}).

Relationship between $V_{o,max}$ and N_L(number of levels) can also be written as:

$$V_{o,max} = \frac{N_L - 1}{2} \tag{20}$$

By combining equations (19) and (20), the value of overall blocked voltage will be:

$$V_{TB} = \frac{44}{14}(N_L - 1) = 3.14(N_L - 1) \tag{21}$$

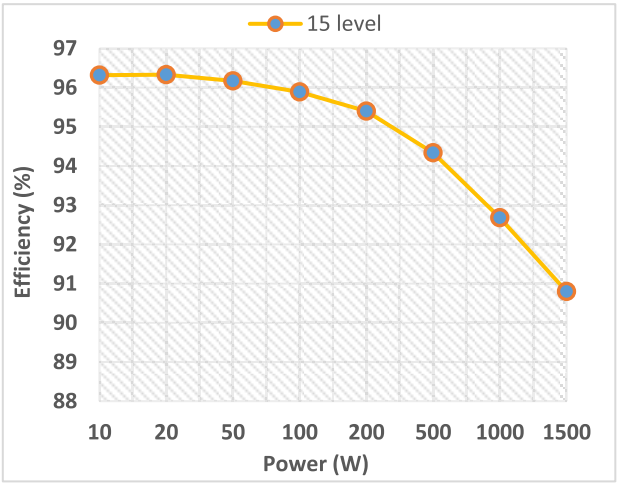
Table 2 gives the number of levels (N_L), number of units (n), number of DC voltage sources (N_{dc}), number of switches (N_{sw}), number of capacitors (N_{cap}), number of drivers (N_{dr}) maximum output voltage ($V_{o,max}$) and total blocked voltage of all the switches (V_{TB}) based on N_L and n.

TABLE 2. Different equations of the proposed MLI.

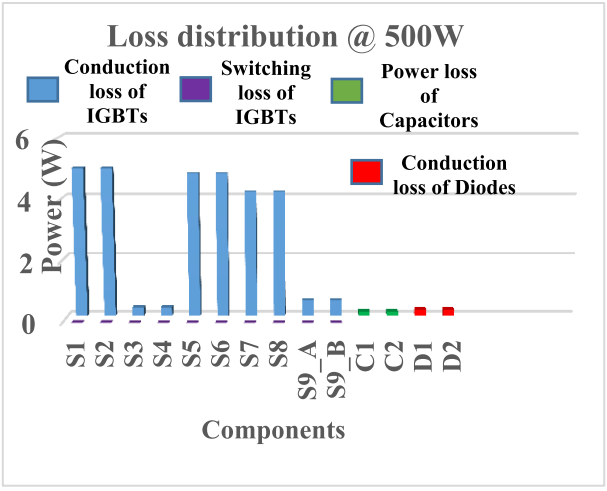
Parameters	In terms of number of levels (N_L)	In terms of number of units(n)
Units (n)	$log_{15}(N_L)$	n
Levels (N_L)	N_L	15n
D.C. voltage sources (N_{DC})	$2log_{15}(N_L)$	2n
Diodes (N_D)	$2log_{15}(N_L)$	2n
Switches (N_{SW})	$10log_{15}(N_L)$	10n
Drivers (N_{DR})	$9log_{15}(N_L)$	8n
Capacitors (N_C)	$2log_{15}(N_L)$	2n
Maximum output voltage ($V_{o,max}$)	$(N_L - 1)/2$	(15n-1)/2
Total blocked voltage (V_{TB})	$44(N_L - 1)/14$	44(15n-1)/14

V. COMPARISON OF THE PROPOSED MLI WITH OTHER STRUCTURES

In this section, the practicality of the presented MLI is validated by comparing the number of switches (N_{SW}), number of drivers (N_{DR}), number of DC sources (N_{DC}), number of capacitors (N_C), number of diodes (N_D) and total blocked voltage (V_{TB}) of all the switches with recently published topologies [4], [11], [24], [30]–[34]. Fig. 6(a) compares the number of switches, i: e, power IGBTs with respect to the number of levels for the presented topology and topologies given in [4], [11], [24], [30]–[34]. The figure clearly shows that the presented structure uses the least switch count among



(a)



(b)

FIGURE 7. (a) Inverter efficiency at different output power (b) Loss distribution of different components.

these topologies. The driver required is plotted against the number of levels in Fig. 6(b). The presented structure and the structures presented in [33] use the lowest number of drivers compared to these topologies. Fig. 6(c) shows the plot between the DC supply count and the number of levels. The topology presented in [33] has the least DC supply, and the proposed topology is very close to it in this respect. The proposed structure requires fewer DC sources than the structures presented in [4], [11], [24], [32], and [34]. Fig. 6(d) shows the plot of total blocked voltage and the number of levels. Structures presented in [11], [24], [31]–[33] have lower total block voltage values with respect to the proposed design. The proposed structure has a smaller gross blocked voltage than the one presented in [4]. Furthermore, a summary of recently published MLIs has been presented in Table 3.

VI. POWER LOSS ANALYSIS

Estimation of the losses of the proposed structure has been done using PLECS software. By using these losses, the efficiency of the suggested topology is calculated. The thermal

TABLE 3. Comparison with 15 level MLIs.

Topologies	N_{DC}	N_{SW}	N_{DR}	N_C	N_D	V_{TB}/N_L	η (%)
[3]	5	10	10	0	0	-	93.73
[20]	1	14	14	4	2	4.86	-
[32]	4	10	9	0	0	4.6	97.5
[33]	3	8	8	0	0	2	95.2
[34]	3	10	9	0	0	2.26	-
[35]	5	10	10	0	2	1.06	90
Proposed	2	10	8	2	2	3.6	96.3

modeling part of the software is used for the calculation of different losses in the switches, capacitors, and diodes. The switch used for this study is IGA30N60H3. Losses considered under this study include: conduction losses (P_C) of all the semiconductor devices, switching losses (P_S), and ESR losses (P_{ESR}) of the capacitors. Ripple loss is also there in capacitors, but here it is not included in the calculations. The calculations involved in this study are based on the fundamental switching frequency approach [15].

A. SWITCHING LOSS (P_S)

Switching losses occur at the point of turning ON or OFF of the switches. By considering the linear approximation of the switch voltage and current at the time of switching, the following relations for the kth switch can be written as:

Power loss during switching

$$\begin{aligned} \text{ON} = P_{S,on,k} &= f\int_0^{t_{on}} v(t)\, i(t)\, dt \\ &= f\int_0^{t_{on}} \left(\frac{V_{S,k}}{t_{on}}t\right)\left(-\frac{I_k}{t_{on}}(t-t_{on})\right) dt = \frac{1}{6} f V_{S,k} I_k \end{aligned} \tag{22}$$

Loss of power during switching

$$\begin{aligned} \text{OFF} = P_{S,off,k} &= f\int_0^{t_{off}} v(t)\, i(t)\, dt \\ &= f\int_0^{t_{off}} \left(\frac{V_{S,k}}{t_{off}}t\right)\left(-\frac{I_k{}'}{t_{off}}(t-t_{off})\right) dt = \frac{1}{6} f V_{S,k} I_k{}' t_{off} \end{aligned} \tag{23}$$

where I_k and $I_k{}'$ are the currents flowing through the kth switch at the time of switching ON, and before switching OFF respectively, f is the switching frequency and $V_{S,k}$ is the voltage of the switch in OFF-state. Switching loss of all the ten switches can be obtained by multiplying the ON (N_{on}) and the OFF number of switching states (N_{off}) in a cycle with (22) and (23) following (24):

$$P_S = \sum_{k=1}^{10} \left(\sum_{m=1}^{N_{on}} P_{S,on,km} + \sum_{m=1}^{N_{off}} P_{S,off,km} \right) \tag{24}$$

B. CONDUCTION LOSS (P_C)

The internal resistance of power switches and diodes is also considered for the calculation of losses in conduction mode for the steady-state condition. All capacitors are supposed to be equal. PLECS software is used for taking the results. The load is taken as resistive since resistive loading is considered

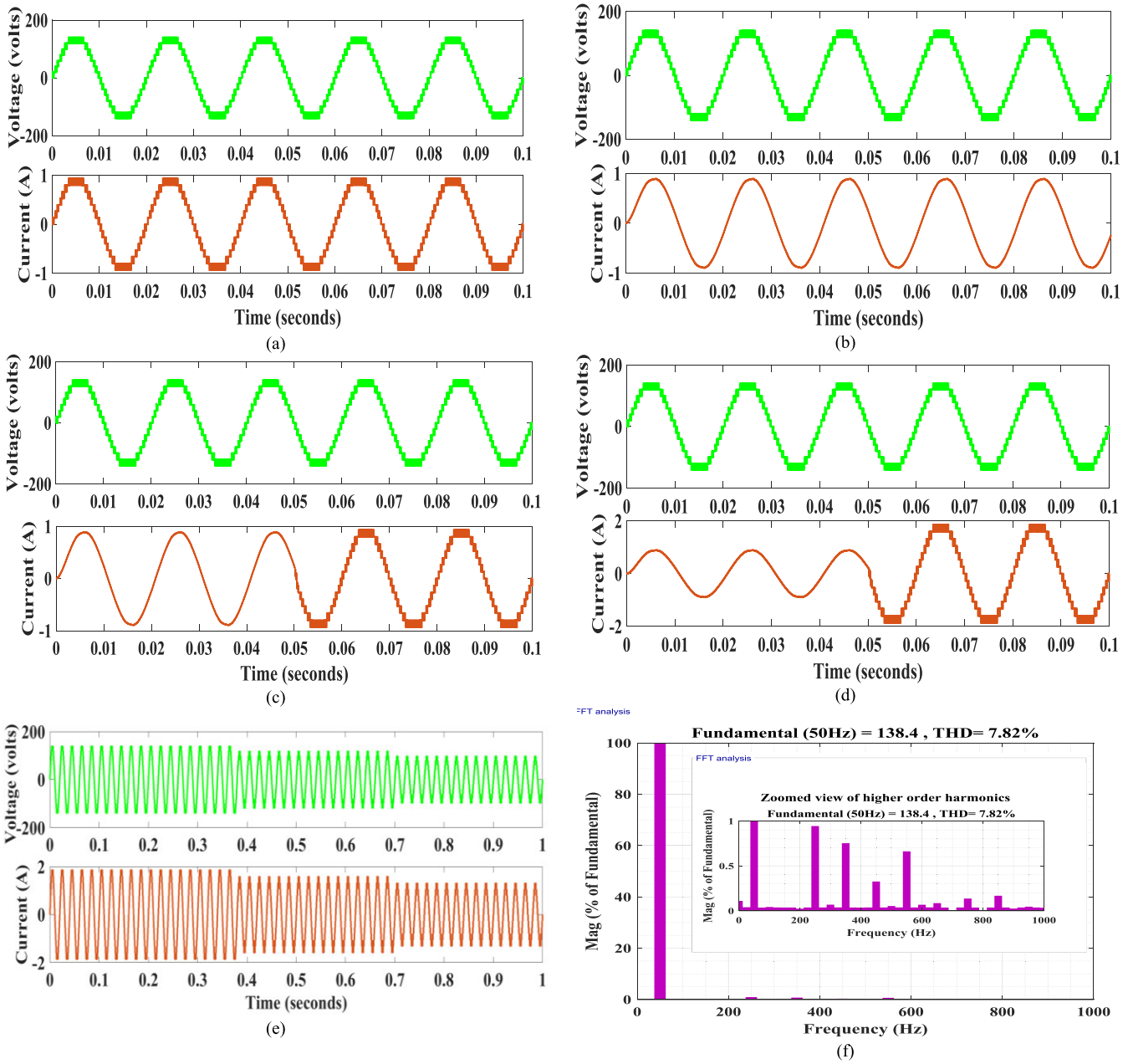


FIGURE 8. Simulation results (a) Output waveform for the resistive load of 150Ω (b) Output waveform of RL load of Z = 150Ω+120mH (c) Output waveform for dynamic change of load from Z = 150Ω+120mH to resistive load of 150 Ω (d) Output waveform for dynamic load change from Z = 150Ω+120mH to a resistive load of 75 Ω (e) Output voltage and current for dynamic alteration of MI (f) Harmonic profile of the output voltage at a load of 75 Ω.

the worst-case scenario in analyzing loss of power in SCMLIs [39], [40], [41].

C. CAPACITOR ESR LOSSES (P_{ESR})

The equivalent series resistance of the capacitors depends on the frequency of the current flowing through the capacitor [42]. It can be defined as the conduction loss caused by the internal resistance of the capacitor. Here 0.1 ohm is taken as the internal resistance of both the capacitors. These losses also affect the lifetime of capacitors due to thermal stress and heat dissipation caused. All these three losses are simulated in PLECS.

Therefore, the overall efficiency of the presented SCMLI is given by (25).

$$\eta = \frac{P_o}{P_o + P_S + P_C + P_{ESR}} \tag{25}$$

Fig. 7(a) shows the proposed topology's efficiency versus output power curve for a resistive load. The efficiency curve shows a peak value of about 96.33%, along with a 10 watts output power. The contribution of different components such

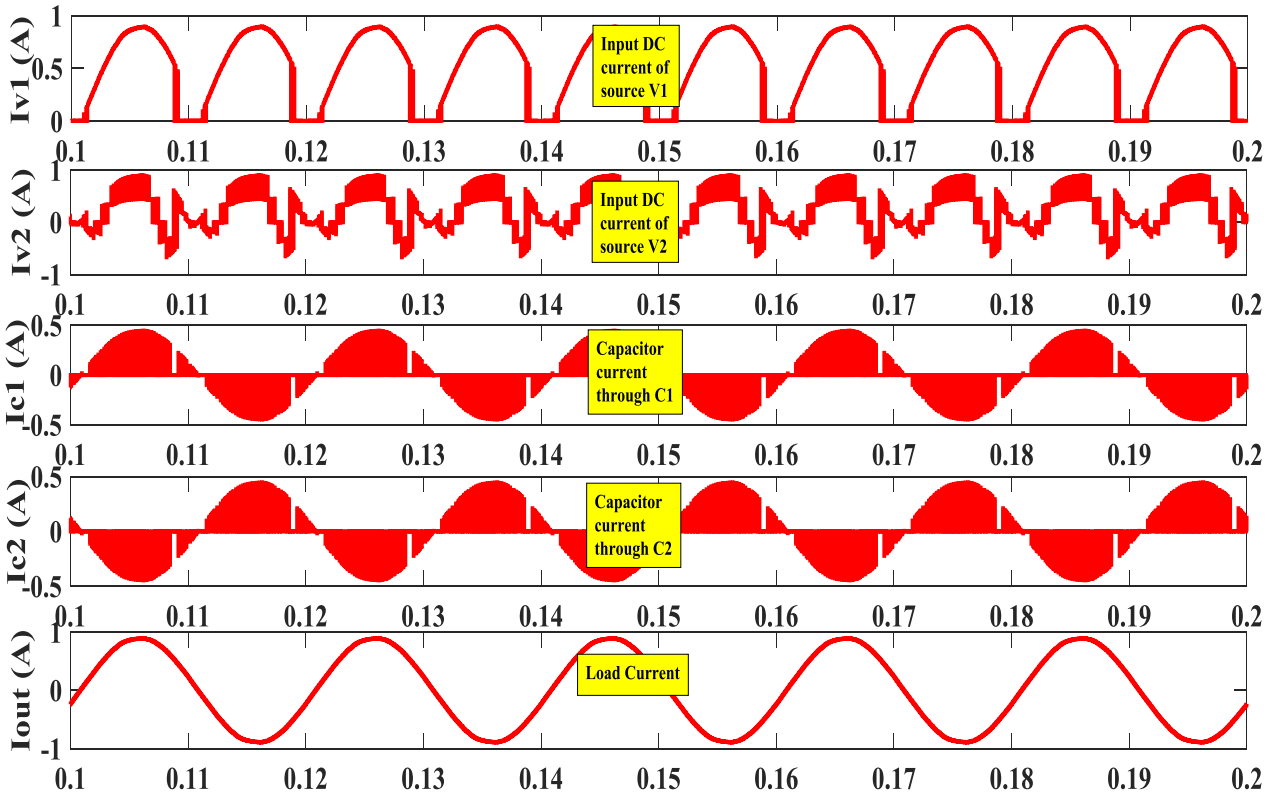


FIGURE 9. Waveforms showing Input DC current for sources V_1 and V_2, Capacitor currents for Capacitors C_1 and C_2, and load current at a load of Z = 150Ω+120mH.

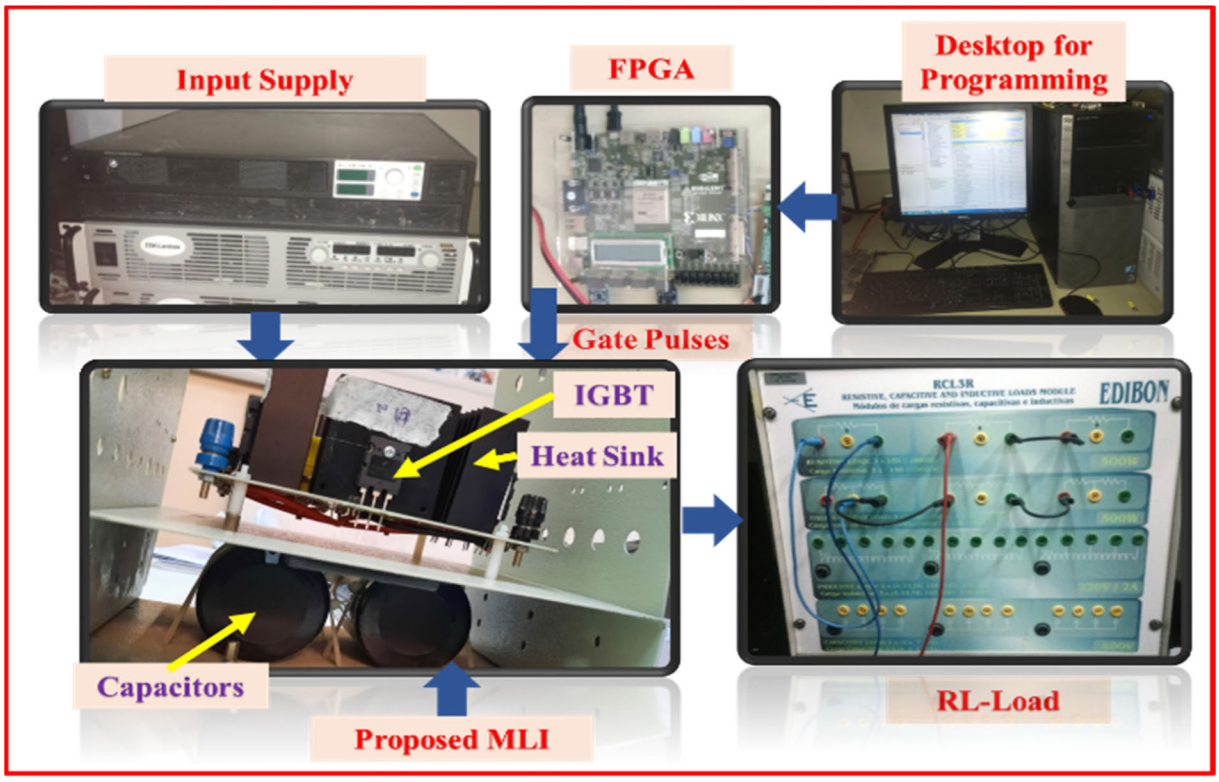


FIGURE 10. Experimental setup.

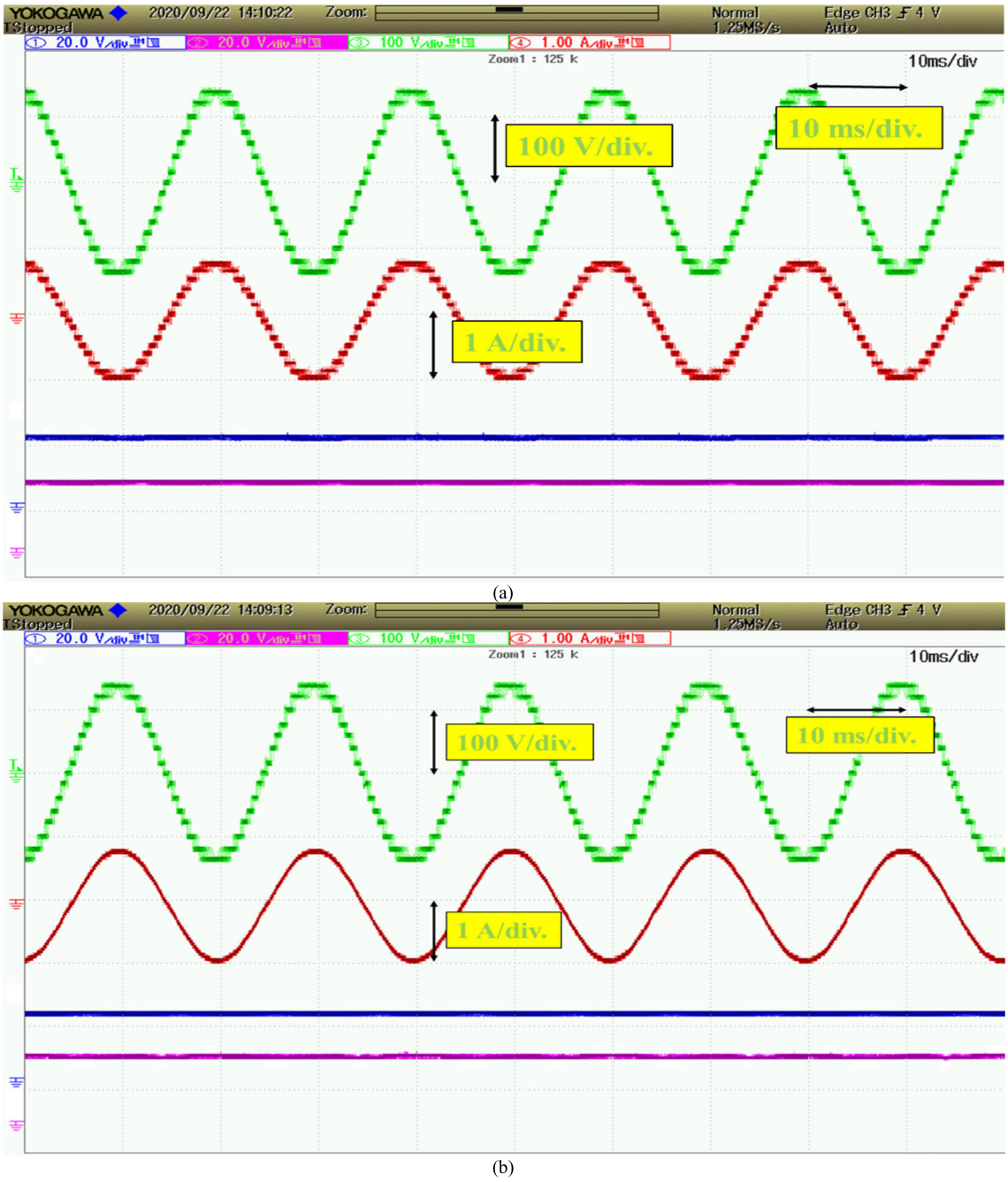


FIGURE 11. (a) Output waveform for a resistive load of 150Ω (b) Output waveform of RL load of Z = 150Ω+120mH.

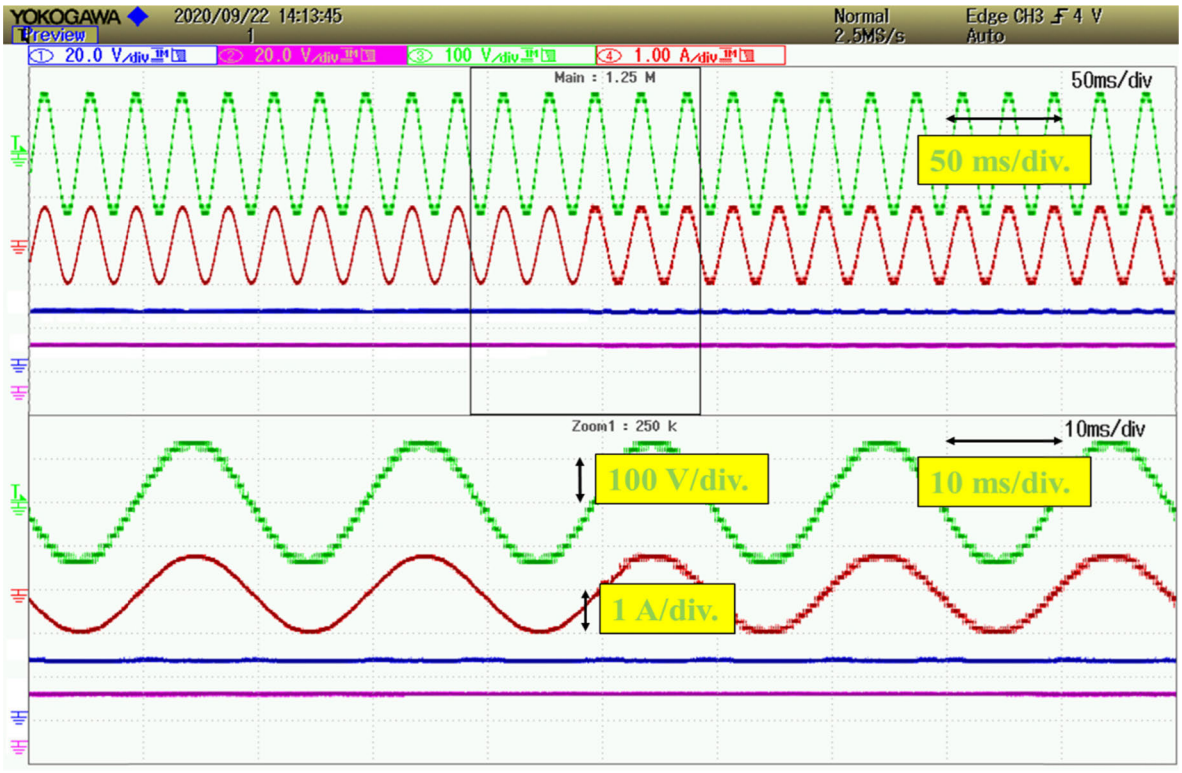
as diodes, switches, and capacitors in the power loss has been given in Fig. 7(b). S9 is the bidirectional switch, as shown in Fig. 1. Both the switches S9_A and S9_B of the bidirectional switch have the same loss. Equal losses are there in the complementary switches since the turn ON and OFF count in a full cycle are equal.

VII. RESULTS AND DISCUSSION

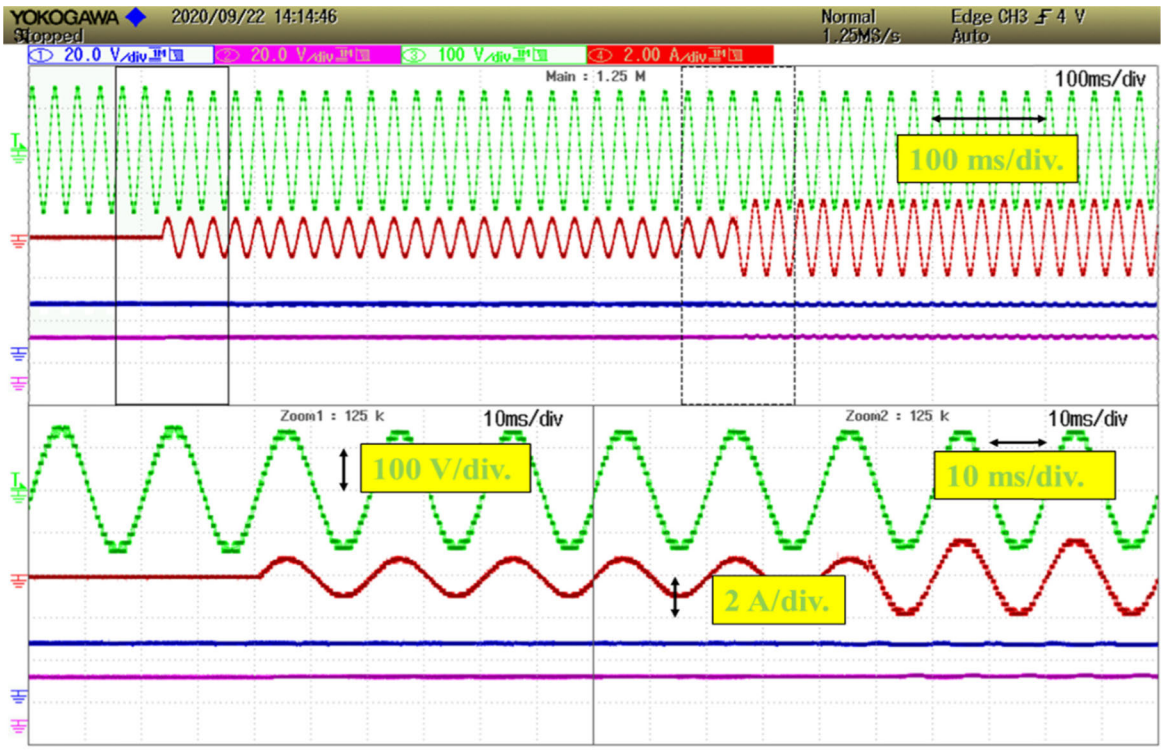
Simulation of the suggested structure is done on Matlab® 2018a. For the verification of the simulation results obtained, results have also been taken on an experimental prototype. The subsequent subsection discusses the simulation and experimental results.

A. SIMULATION RESULTS

For the simulation purpose, DC supplies V_1 and V_2 have values of 100 volts and 20 volts. Both the capacitors used have the same magnitude of 4700 μF with an internal resistance of 0.1Ω. Fig. 8 and Fig. 9 show the different simulation results of the presented structure. Fig. 8(a) expresses the fifteen-level



(a)



(b)

FIGURE 12. (a) Output waveform for dynamic change of load from no load to Z = 150Ω+120mH to resistive load of 150 Ω (b) Output waveform for dynamic.

output waveform for the resistive load of 150 ohms. The output has a peak voltage of 140 V with a step voltage of 20 V. The output voltage and current waveforms for an RL load of Z = 150Ω +120mH are given in Fig. 8(b). Fig. 8(c) and Fig. 8(d) show the output waveform under a dynamic load change from Z = 150Ω+120mH to a resistive

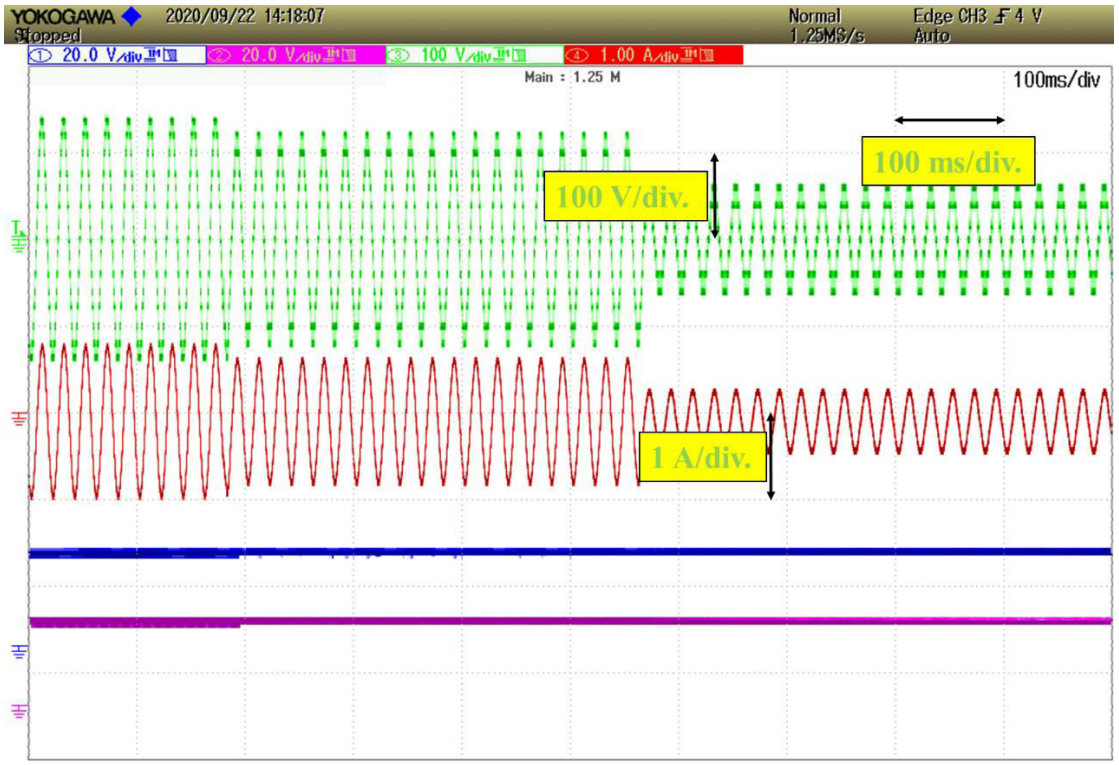


FIGURE 13. Output waveform for dynamic alteration of modulation index.

load of 150 ohms and from Z = 150Ω+120mH to a load of 75 ohms, respectively. Fig. 8(e) shows the output waveform under the dynamic alteration of the modulation index (MI). The output levels obtained is proportional to the MI. Fig. 8(f) depicts the FFT analysis. The figure displays the THD of the output voltage at 7.82%. Fig. 9 shows the current of the input DC sources V_1 and V_2, the current flowing through capacitors C_1 and C2, and load current when an RL load of Z = 150Ω+120mH is taken. Spikes in capacitor current are suppressed, as can be seen in the figure.

B. EXPERIMENTAL RESULTS

To verify the simulation results obtained, an experimental prototype has been developed, as shown in Fig. 10. Fig. 11 to Fig. 13 show similar results obtained experimentally for the same specification of different components. The switch used is Toshiba IGBT GT50J325, and the dSPACE 1104 is used as the controller to generate the required gate signals. For the experimental verification, DC supplies V1 and V2 are taken as 100 volts and 20 volts, respectively. Fig. 11(a) and Fig. 11(b) show the output waveform for a resistive load of 150 ohms and an RL load of Z = 150Ω+120mH, respectively. The output has a peak voltage of 140 V with a step voltage of 20 V. Fig. 12(a) and Fig. 12(b) show the output voltage and current for a dynamic load change from Z = 150Ω+120mH to a load of 150 ohms, and from 0 to Z = 150Ω+120mH to a load of 75 ohms respectively. Fig. 13 shows the output waveforms for the dynamic change in MI. The number of levels decreases proportionally as the modulation index is reduced as can be seen in the waveform.

VIII. CONCLUSION

A new SCMLI structure has been suggested here. The proposed topology can generate fifteen levels per unit, and it can also be extended for getting higher output levels. It has the lowest switch count, and the number of drivers required compared to the recent topologies present in the literature. Capacitor voltage balance is also maintained. A multicarrier level shifted modulation technique has been implemented here. Hardware implementation of the presented structure has been done for the validation of the simulation results at different loading conditions and changing modulation indices. Thus the presented structure can be a viable option for industrial use.

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