IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received June 3, 2021, accepted June 25, 2021, date of publication June 29, 2021, date of current version July 9, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3093508

Design of a Wideband CMOS Balun and Its Application in a Wideband RF Front-End

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This work was supported in part by the National Natural Science Funds of China under Grant 61774035, in part by the Natural Science Foundation of Jiangsu Province under Grant BK20191260, and in part by the Special Major Basic Research Program of Hebei Province under Grant 18960202D.

ABSTRACT This paper presents a 1:2 wideband CMOS balun, and its application for sub-6 GHz wideband front-end. In order to eliminate the amplitude/phase mismatch, the primary and secondary windings are shorted by a transmission line (T-line) for a common ground. The float metal in the primary winding is used for artificial dielectric compensation which further reduce the amplitude imbalance by up to about 0.5 dB. A 2.0-to-3.7 GHz wideband RF front-end is also designed by using the proposed CMOS balun. The balun and RF front-end are fabricated in a 0.13-μm bulk CMOS technology. The bandwidth of the balun with $|S11| < -10$ dB is 2.2-to-5.1 GHz. The fractional bandwidth is large than 79.5%. The corresponding maximum amplitude and phase mismatch is 1.5 dB and 2°, respectively. The measured insertion loss is 4.8-to-5.6 dB from 2.2 to 5.1 GHz.

INDEX TERMS CMOS, balun, transformer, T-line, common ground, artificial dielectric, mismatch compensation, wideband, RF, front-end.

I. INTRODUCTION

Transformer baluns have been widely used in Gilbert mixers, differential amplifiers, phase shifters. They are typically designed to realize the unbalance-to-balance conversions while keeping a minimum insertion loss, and low amplitude and phase mismatch. As can be found in the recently reported publications, there are several well-known baluns such as the Marchand configuration [1]–[4] as well as microstrip [5], branch-line [6] and transformer [7], [8] based structures. Among the available statistics, the Marchand balun is more attractive than others due to its simplicity and well-known wide operating band. An off-chip Marchand balun is modified with a varactor and a series resistor loaded at the central point of the two coupled sections to realize a wide tunable power division ratio and constant phase across 1.2-2.8 GHz band [1]. Silicon-based Marchand balun has been proved to be a competitive candidate for mm-wave applications [3], [4]. However, for sub-6 GHz applications, the coupled spiral transmission lines (T-Line) with the electrical lengths of $\sim\lambda/4$ in the Marchand balun occupies a large chip area, as shown in [2]. [5] reported a microstrip line based on-board balun that can achieve a wide relative bandwidth (92.3%) within the frequency of 1.2-to-3.3 GHz A bandwidth-extended off-chip balun has been demonstrated by using a fully artificial fractal-shaped composite right/left-handed branch line [6]. However, like other PCB-based designs, the reported balun occupies hundreds of mm^2 area.

A miniaturized transformer balun is designed by using the capacitive loading compensation technique with an impressive on-chip performance from 40 to 60 GHz [7]. A K-band transformer balun with a very low amplitude/phase imbalance of 0.13 dB/ 0.4° is employed for a balanced frequency

The associate editor coordinating the review of this manuscript and approving it for publication was Venkata Rajesh Pamula.

doubler to achieve the odd-order harmonic cancellation [8]. However, the reported insertion loss is around 6-10 dB from 7 to15 GHz.

On-chip transformer baluns for sub-6 GHz silicon RFIC design with designed by utilizing interwound metal routing are demonstrated in the paper of [9]–[12]. Transformer balun with the turn ratio of 1:N (N > 1) is needed to transform the impedance from primary to secondary.

An asymmetric-type balun with large turn ratio of 5:1 between the primary and secondary winding is designed by dividing one winding (e.g., the primary) into five individual turns rather than a continuous winding [13]. To form a transformer with the turn ratio of 5:1, those five 1-turn windings are then connected in parallel. However, like most of other asymmetric transformer baluns, asymmetric layout placement will result in a significant imbalance for the amplitude and phase. [14] demonstrates a symmetric transformer with the turn ratio of 1:2 that is constructed with "PSSP" layout placement. Here, the letter "P" represents the primary metal conductor, while the letter "S" represents secondary metal conductor. However, there will have a point with four stacked inductive windings (named as 4Xover) which requires at least three metal conductors cross over each other. The metal conductor at the bottom will significantly increase the imbalance of the transformer due to the parasitic capacitance to the substrate. Although 3D balun [15] with multiple metal conductors shows a compact size of 0.01 mm^2, there still have a phase imbalance of 7°. Active baluns with the small die area can be used for unbalance to balance conversion [16], however, the amplitude and phase mismatch is normally sensitive to the PVT variations.

This paper describes the details of a novel 1:2 transformer balun by using the common ground and artificial dielectric compensation techniques [17]. A wideband RF front-end with the proposed CMOS balun is also designed to provide excellent balanced performance for sub-6 GHz applications. The paper is organized as follows: Section II shows analysis, design and simulation of the proposed balun. Section III depicts the design of the wideband RF front-end. Section IV shows the measurement results of the balun and the RF front-end. Finally, Section V presents the conclusion.

II. ANALYSIS, DESIGN, AND SIMULATION OF THE CMOS BALUN

A. COMMON GROUD COMPENSATION

It is known that four-port transformer balun with a differential excitation exhibits excellent amplitude and phase balance due to its fully symmetric configuration. The S-parameter matrix for four-port transformer balun in a homogeneous medium can be written as [18]:

$$[S] = \begin{bmatrix} 0 & \frac{y}{z} & \frac{x}{z} & 0 \\ \frac{y}{z} & 0 & 0 & \frac{x}{z} \\ \frac{x}{z} & 0 & 0 & \frac{y}{z} \\ 0 & \frac{x}{z} & \frac{y}{z} & 0 \end{bmatrix} \tag{1}$$

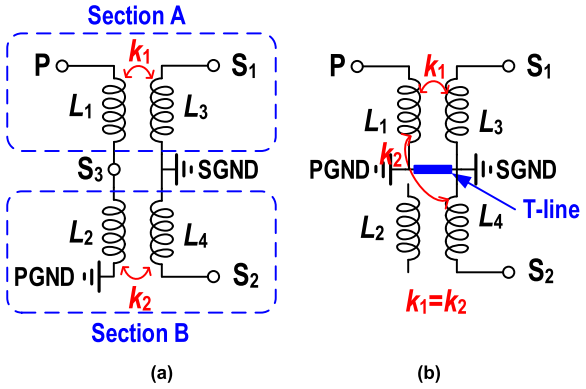

FIGURE 1. Schematic of (a) traditional transformer balun, (b) proposed transformer balun.

where x, y, and z can be expressed as $(1 - k^2)^{1/2}$, $\mathrm{j}k \sin\theta$, and $(1 - k^2)^{1/2} \cos\theta + \mathrm{j} \sin\theta$, respectively. The k represents the coupling factor, and θ denotes the electrical length of the coupled lines. Three-port baluns for unbalance to balance conversion can be generated from four-port transformers. The schematic of traditional transformer balun is shown in Figure 1(a) with mutually nested structure. Here, the inductive windings (L_1~L_4) in transformer balun are surrounded by a wide ground ring that connects to the ground pads to achieve a current returning path (CRP) [13], [19]. For traditional balun, It is difficult to laid the actual grounds of primary (PGND) and secondary (SGND) windings close to each other, and this situation will lead to the different CRPs for primary/secondary windings. As a result, the mutual inductance and the couple factor k_1 of L_1 and L_3 are different from that (k_2) of L_2 and L_4. The difference between k_1 and k_2 will generate the imbalance at the differential output nodes.

Next, we will investigate the 3-port S-parameter matrix with the port s of P, S_1 and S_2 as shown in Figure 1(a). The balun can be divided into two sections. Considering the short boundary condition, the Section A can be modelled as a 3-port S-parameter with the ports of P, S_1, and S_3 and the S-parameter matrix can be expressed as the following equation:

$$[S_A] = \begin{bmatrix} -\frac{y_1^2}{z_1^2} & \frac{x_1}{z_1} & -\frac{x_1 y_1}{z_1^2} \\ \frac{x_1}{z_1} & 0 & \frac{y_1}{z_1} \\ -\frac{x_1 y_1}{z_1^2} & \frac{y_1}{z_1} & -\frac{x_1^2}{z_1^2} \end{bmatrix} \tag{2}$$

where x_1, y_1, and z_1 is written as $(1 - k_1^2)^{1/2}$, $\mathrm{j}k_1 \sin\theta$, and $(1 - k_1^2)^{1/2} \cos\theta + \mathrm{j} \sin\theta$, respectively. The k_1 is the coupling factor of L_1 and L_3. The Section B can be modelled as a 2-port S-parameter with the ports of S_2, and S_3. It's S-parameter matrix can be written as:

$$[S_B] = \begin{bmatrix} -\frac{x_2^2}{z_2^2 - y_2^2} & \frac{y_2}{z_2}\left(1 + \frac{x_2^2}{z_2^2 - y_2^2}\right) \\ \frac{y_2}{z_2}\left(1 + \frac{x_2^2}{z_2^2 - y_2^2}\right) & -\frac{x_2^2}{z_2^2 - y_2^2} \end{bmatrix} \tag{3}$$

where $x_2 = (1 - k_2^2)^{1/2}$, $y_2 = \mathrm{j}k_2 \sin\theta$, $z_2 = (1 - k_2^2)^{1/2} \cos\theta + \mathrm{j} \sin\theta$, and k_2 is the coupling factor of L_2 and L_4. As shown in Eq.(4), at the bottom of the page, the 3-port (P, S_1, and S_2) S-parameter matrix of the transformer balun can be expressed by combining Eq. (2) and (3), as. Note that, when the k_1 is different from the k_2, we can get the equation of $S_{31} \neq -S_{21}$.

According to above analysis, we can conclude that the different CRPs in the traditional transformer balun, which cannot be predefined until layout, will result in the imbalance at the secondary winding. To overcome this issue, a short T-line connects the PGND and SGND node together so as to obtain a common-ground condition for the primary and secondary windings, as referred to the Figure 1(b). As a result, the common-ground condition between the PGND and SGND will force the coupling factor k_1 between L_1 and L_3 to equal with the k_2 between the L_1 and L_4.

B. ARTIFICIAL DIELECTRIC COMPENSATION

Symmetric 1:N transformer balun can be designed with two interwound multi-turn differential inductors [20]. In order to achieve a 1:N (N > 1) transformer balun, the number of turns of secondary winding should be N times than the number of turns primary winding. In order to lay out the 1:N transformer balun, one primary metal conductor is typically followed by N metal conductors.

As shown in Figure 2(a), the primary and secondary windings should be laid with "PSSP" configuration to achieve the turn ratio of 1:2. There will be at least a point named as "4Xover" that four metal conductors must cross each other [14]. As discussed in [14], the typical approach to implement a "4Xover" point is to laid the transformer balun with three metal layers, however, the use of the third metal layers and vias close to the substrate will add more resistance and capacitance. To solve the problem, one or two windings in the "PSSP" configuration can be shorter or longer than the other windings to avoid the "4Xover" point, however, the complicated metal routing will make the transformer balun unsymmetrical and also will increase the mismatch at the balanced output side. Figure 2 (b) shows the layout placement of the 1:2 balun without the "4Xover" point. As can been seen, there is a mismatch between the primary and secondary windings. In real case, the situation can be much more serious than Figure 2(b) due to the complicated design rules in the CMOS technique. In order to overcome the issue, a novel

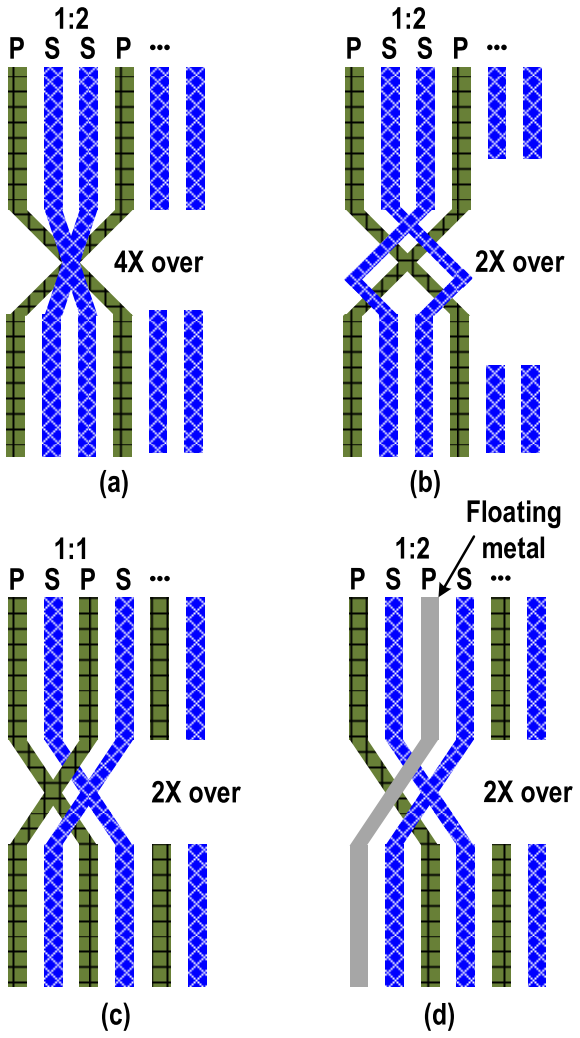

FIGURE 2. Layout placement of in symmetric transformer baluns (a) with turn ratio of 1:2 and "4Xover", (b) with turn ratio of 1:2 and "2Xover", (c) with turn ratio of 1:1, and (d) with turn ratio of 1:2 (proposed).

1:2 transformer balun (Figure 2(d)) is proposed by modifying the traditional 1:1 transformer balun (Figure 2(c)). The transformer balun with a turn ratio of 1:1 normally exhibits excellent balance performance, because only two metal layers are required to cross each other to achieve "2Xover" point. The turn ratio of 1:1 can be transformed to 1:2 by splitting the primary winding into two segments. In our design, we will keep the floating metal in the transformer artificially so as to maintain its geometric symmetry.

$$[S_{\mathrm{balun}}] = \begin{bmatrix} -\left(\frac{y_1^2}{z_1^2} + \frac{x_1^2}{z_1^2}\frac{x_2^2}{z_2^2 - y_2^2}\right) & \frac{x_1 y_2}{z_1 z_2}\left(1 + \frac{x_2^2}{z_2^2 - y_2^2}\right) & -\frac{x_1 y_1}{z_1^2}\left(1 + \frac{x_2^2}{z_2^2 - y_2^2}\right) \\ \frac{x_1 y_2}{z_1 z_2}\left(1 + \frac{x_2^2}{z_2^2 - y_2^2}\right) & -\frac{x_2^2}{z_2^2 - y_2^2} & \frac{y_1 y_2}{z_1 z_2}\left(1 + \frac{x_2^2}{z_2^2 - y_2^2}\right) \\ -\frac{x_1 y_1}{z_1^2}\left(1 + \frac{x_2^2}{z_2^2 - y_2^2}\right) & \frac{y_1 y_2}{z_1 z_2}\left(1 + \frac{x_2^2}{z_2^2 - y_2^2}\right) & -\left(\frac{x_1^2}{z_1^2} + \frac{y_1^2}{z_1^2}\frac{x_2^2}{z_2^2 - y_2^2}\right) \end{bmatrix} \quad (4)$$

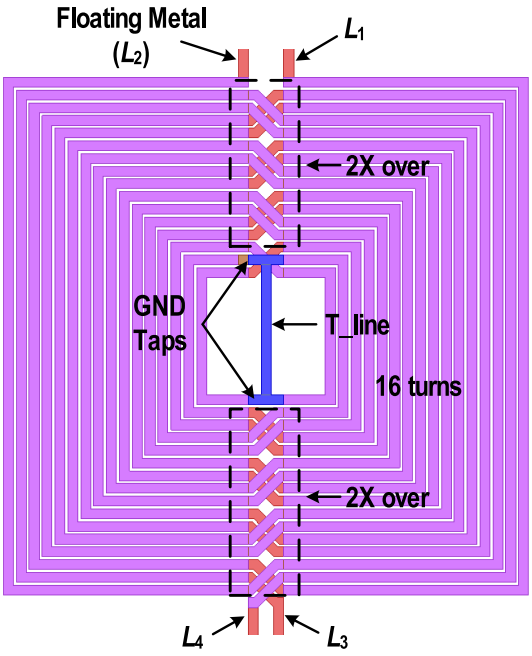

FIGURE 3. Bottom view of the proposed 1:2 transformer balun.

Figure 3 shows the bottom view of the proposed 1:2 transformer balun. It is laid symmetrically with sixteen turns for wideband operation. The balun can be modeled as three mutually nested spiral coils: L_1, L_3 and L_4, and it is implemented using a lateral coupling strategy [21], [22]. The spiral T-line are wound back to themselves to achieve higher coupling coefficient and better size reduction. A symmetrical inductor is split at the center into two segments, which correspond to the inductors of L_1 and L_2, respectively. The secondary windings (L_3 and L_4) are design by another symmetrical inductor. Note that the balun has a unique feature that the ground terminal of L_1 is connected to the center tap of L_3 by using a short T-line and with the L_2 left floating. Thanks to the floating metal conductors, the "4Xover" point (except the GND taps) can be avoided even if only top two metal conductors are used. The common ground technique relaxes the external mismatch caused by different ground potentials. The floating L_2 is embedded into the balun artificially to keep its geometrical symmetry. As a result, a constant effective dielectric coefficient is achieved in this design which can further improve the balance performance.

C. SIMULATION AND COMPARESION

The proposed balun is implemented in a 130-nm bulk CMOS with six metal layers. The spiral coils are built by connecting the top two layers together. The transmission line width is 5-μm and the space between is 1.5-μm. Meanwhile, the cross underpass is implemented by using M_5. To reduce the substrate loss, the ground ring is designed with M_2, and the distance between the ground ring and spiral coils is 50-μm.

To evaluate the proposed imbalance compensation technique, three transformer baluns with the same dimension are designed and simulated by using EM simulator. Figure 4 shows the schematic diagram and layout of the transformer balun with different T-Line and L_2 configurations. An asymmetric balun with the turn ratio of 1:2 is shown in Figure 4(a), it is implemented without using the T-line and L_2 compensation techniques. Then, we add a short T-line to the asymmetric balun to evaluate the T-line compensation effect as shown in Figure 4(b). Finally, the proposed 1:2 balun with simultaneous T-line and L_2 compensation is shown in Figure 4(c).

The simulated amplitude and phase imbalance results are shown in Figure 5 and Figure 6, respectively. As can be seen, without T-line and L_2 compensations, the amplitude imbalance of the balun is up to 5.4 dB at the frequency of 6 GHz. The T-line compensation can significantly reduce the amplitude imbalance by 3 dB at frequency of 6 GHz. It is also observed that the proposed balun features the minimum amplitude mismatch of less than 1.5 dB for 6 GHz range with simultaneous common-ground and artificial-dielectric compensation. Although the advantages of artificial dielectric compensation seem insignificant, the amplitude mismatch can still be improved by up to about 0.5 dB. The proposed balun achieves a phase error of less than 3° from 1 to 6 GHz frequency range. The artificial dielectric compensation with L_2 can further improve the phase balance performance at higher frequencies.

III. WIDEBAND RF FRONT-END

Balun plays an important role in RF front-end designs as it can converts the single-ended signal coming from LNA into a differential signal for double-balanced mixer (DBM). Compared to single-balanced mixer, DBM can offer better RF and LO to RF isolation, and suppress the second-order intermodulation products.

To evaluate the performance of the proposed balun, a wideband RF front-end is design by using the 0.13-μm CMOS technology. Figure 7 shows the schematic of the RF front-end with an inverter-based LNA and a DBM. The first stage of the inverter-based LNA is designed with the inductive source degeneration technique. The small-signal equivalent circuit of the first stage is shown in Figure 8. The load capacitance and the C_{GD} and r_o of M_1 and M_2 have been neglected. Suppose $sg_{m1}L_s \ll 1$ and $sg_{m1}g_{m2}L_s \ll 1$ hold over the low-frequency, which is usually the case [24]. The input impedance Z_{IN} can be represented as follows:

$$Z_{in} = Z_n || Z_f || \frac{1}{sC_{gs2}} \tag{5}$$

$$Z_n = sL_s + \frac{1}{sC_{gs1}} + \omega_T L_s \tag{6}$$

$$Z_f = \frac{1 + sg_{m1}L_s}{g_{m1} + g_{m2} + sg_{m1}g_{m2}L_s} \approx \frac{1}{g_{m1} + g_{m2}} \tag{7}$$

As can be seen, the equivalent input resistance R_{in} can be determined by the $\omega_T L_s || (1/(g_{m1} + g_{m2}))$. Note that, for 50Ω matching, the intrinsic transconductance of M_1 and M_2 is smaller than that of the conventional inverter-based LNA. The R_f can be designed large to meet the noise requirement while

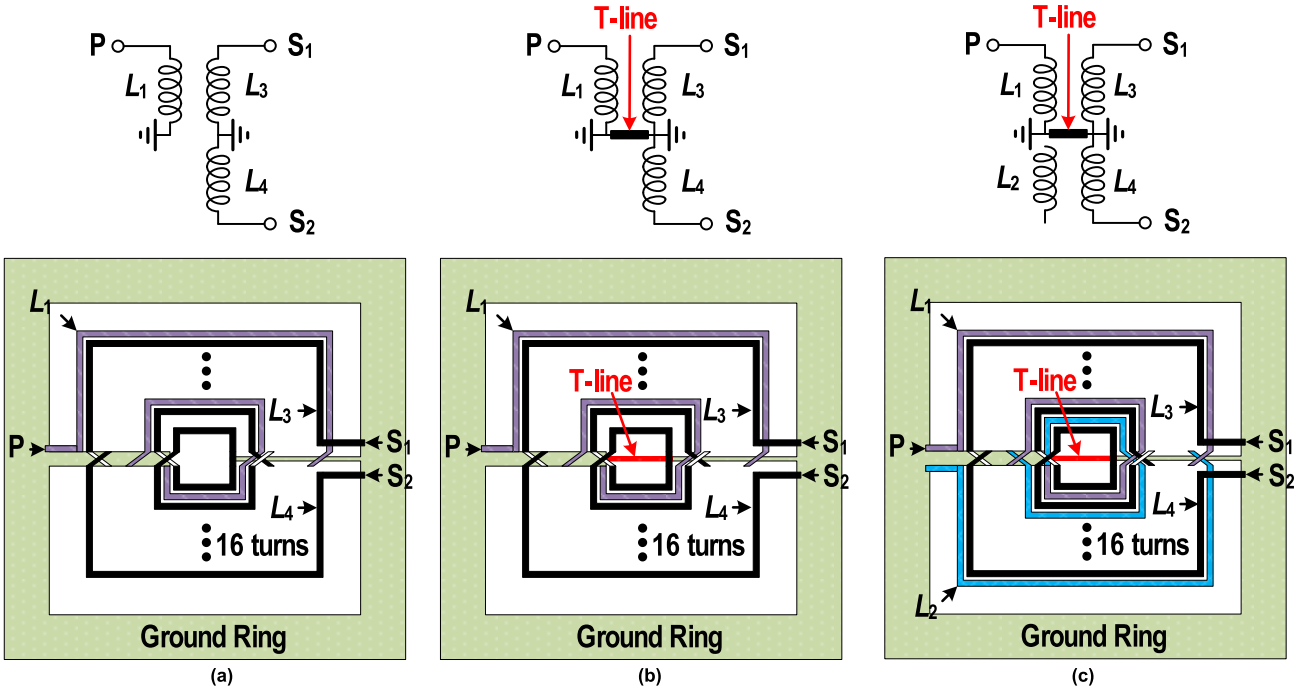

FIGURE 4. Schematic diagram and layout of the transformer balun (a) without T-line and L2, (b) with T-line and without L2, (c) with T-line and L2 (proposed).

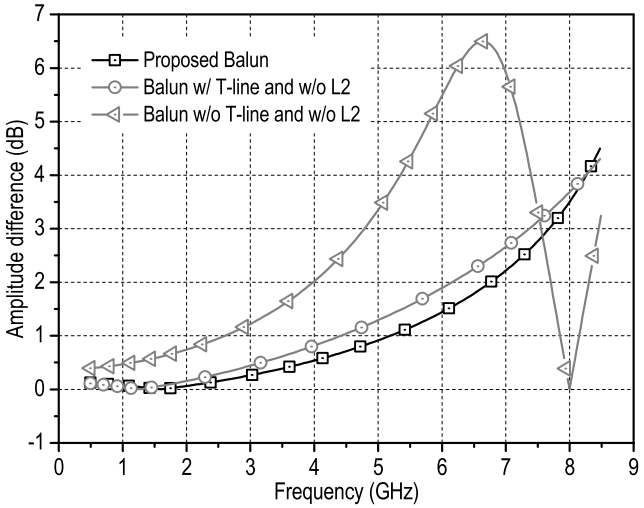

FIGURE 5. Simulated amplitude imbalance.

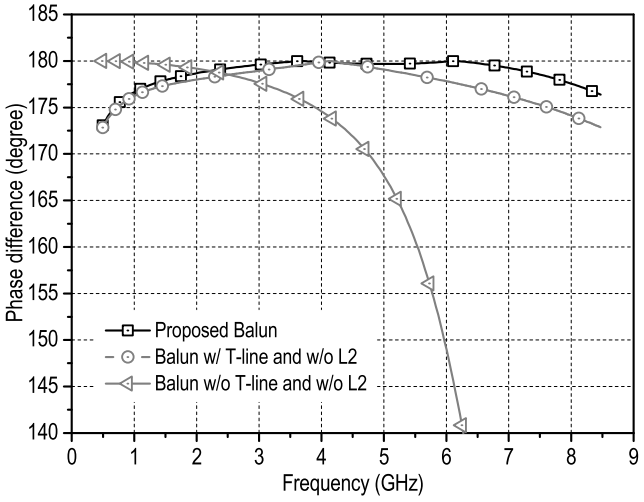

FIGURE 6. Simulated phase imbalance (unwrapped).

TABLE 1. Design parameters of the proposed RF front-end.

M_1	120μm/130nm	M_{11p}, M_{12p}	30μm/130nm
M_2	120μm/130nm	R_f	1 kΩ
M_3	80μm/130nm	R_1	26 Ω
M_4	80μm/130nm	R_2, R_3	10 kΩ
M_5-M_8	42μm/130nm	L_p	6.6 nH
M_9, M_{10}	6μm/130nm	L_s	200 pH
M_{11n}, M_{12n}	48μm/130nm		

ignoring the loading effect. In the second stage, the inductive peaking technique is used to increase the gain and extend the bandwidth by adding L_p at the drain of M_4 [25].

To verify the feasibility of the proposed wideband balun, a DBM with the source-driven and weak-inversion techniques [26] is designed as shown in Figure 7. The mixer topology is also known as the switched-g_m mixer for the low frequency applications [27], [28]. The highly balanced baluns at RF and LO port can suppress the LO leakage and common-mode disturbances by increasing the port-to-port isolation and reducing the second-order intermodulation products. The transconductance (M_1-M_4) works at the subthreshold region with the gate biased at 0.3 V. The active load (M_2 and M_3) is employed to achieve high output impedance as well as large conversion gain (CG). The R_2 and R_3 serve as the

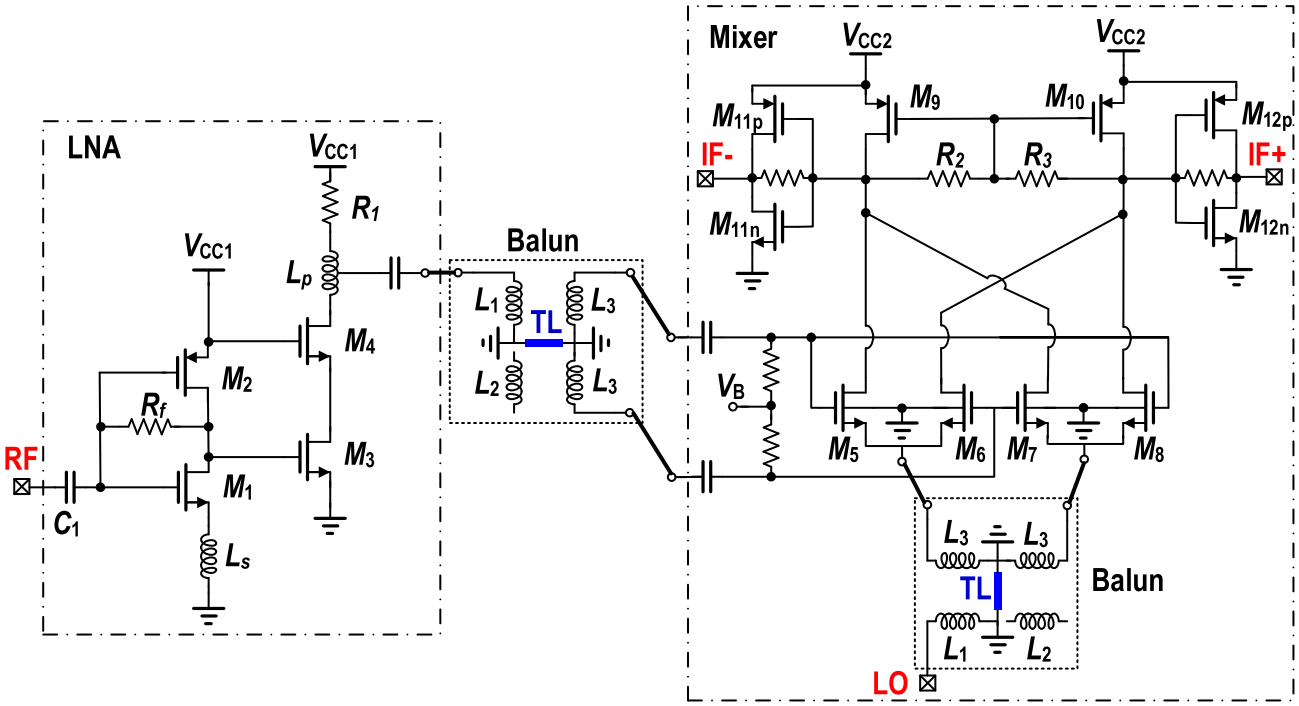

FIGURE 7. Schematic of the RF front-end with the proposed balun.

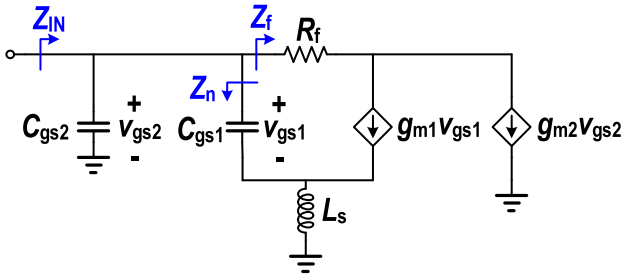

FIGURE 8. Small-signal equivalent circuit of the input stage.

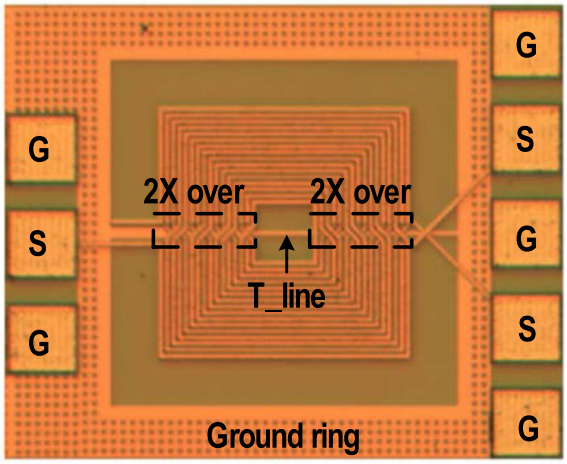

FIGURE 9. Chip die photo of the 1:2 balun.

common-mode feedback. Finally, a self-biased inverter-type buffer (M_{11n}, M_{11p}, M_{12n}, M_{12p}) is designed for the output matching.

IV. MEASUREMENT RESULTS AND DISCUSSION

A. CMOS BALUN

The chip die photo of the proposed transformer balun is shown in Figure 9. The core size of the balun is 0.14 mm^2 without the pads. We perform the n-wafer measurements were by using an Agilent E5071B network analyzer with the on-wafer ground-signal-ground (GSG) and GSGSG probes. As the transformer balun was originally designed for stand-alone use, the parasitic components generated from the pads haven't been de-embedded from the measurement data.

Figure 10 (a) shows the measured S_{21} and S_{11} of the proposed balun with respect to the frequency. The simulated results are also shown here for comparison. The bandwidth of the proposed balun for $S_{11} < -10$ dB is 2.1-to-5.1 GHz with its fractional bandwidth up to 79.5%. The measured insertion loss is 4.8-to-5.6 dB (including 3 dB splitting loss) within the operation frequency range of 2.1-to-5.1 GHz. The measured 3dB-gain bandwidth from the maximum S_{21} is 1.2-to-6.8 GHz. The simulated results are also shown in Figure 10 (a) for comparison. As can be seen, the simulated results agree pretty well with the measured data. The simulated and measured S_{31} curves are not displayed in the figure since they can be directly derived from the S_{21} and amplitude difference curves which are depicted in Figure 10(b).

As shown in Figure 10(b), the measured amplitude imbalance is less than 1.9 dB within the whole 6 GHz range. In the

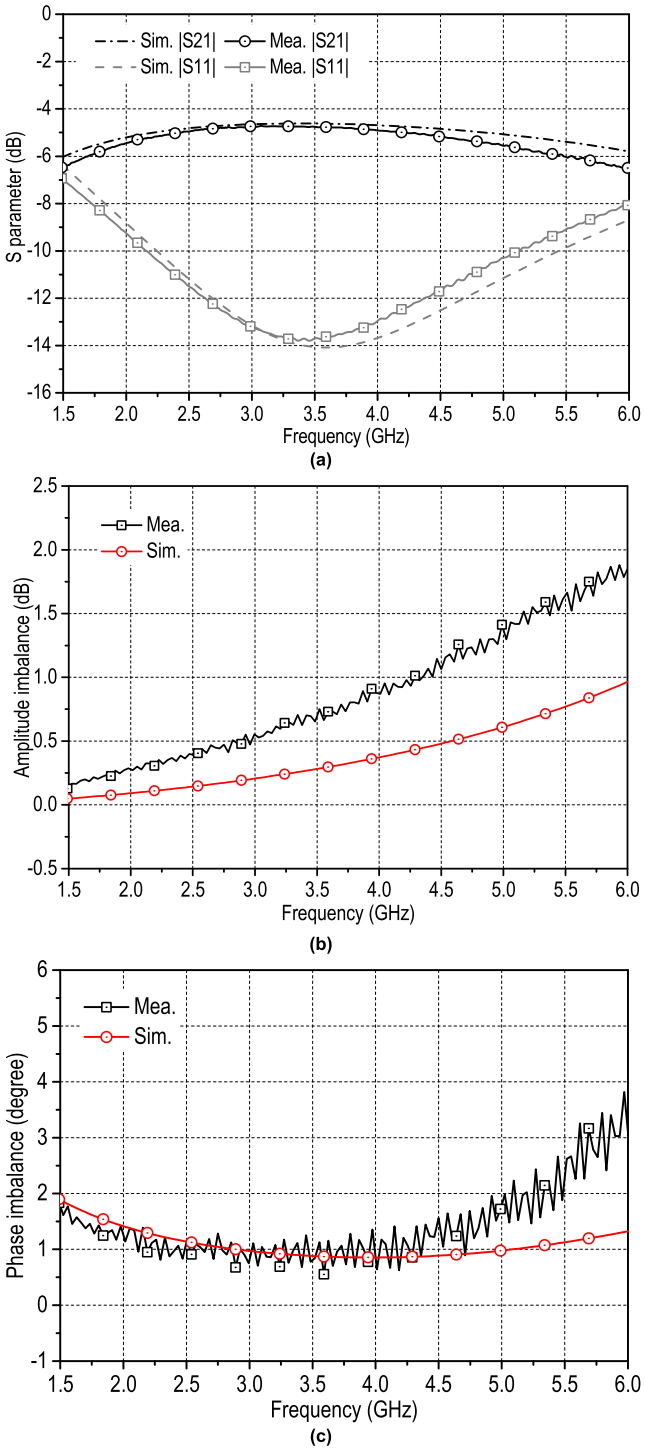

FIGURE 10. Measured and simulated (a) S_{21} and S_{11} of the proposed balun; (b) amplitude imbalance performance; (c) phase (unwrapped) imbalance performance.

frequency range for $S_{11} < -10$ dB, the amplitude imbalance is less than 1.5 dB. It also can be seen from Figure 10(c) that the measured phase imbalance is within 2° range from 2.1-to-5.1 GHz. The mismatch is slightly larger than the simulated results. This is because the test pads have not been

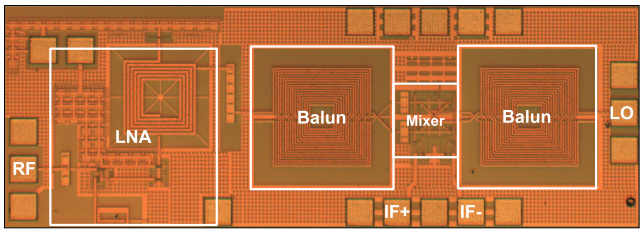

FIGURE 11. Chip die photo of the wideband RF front-end with the proposed transformer balun.

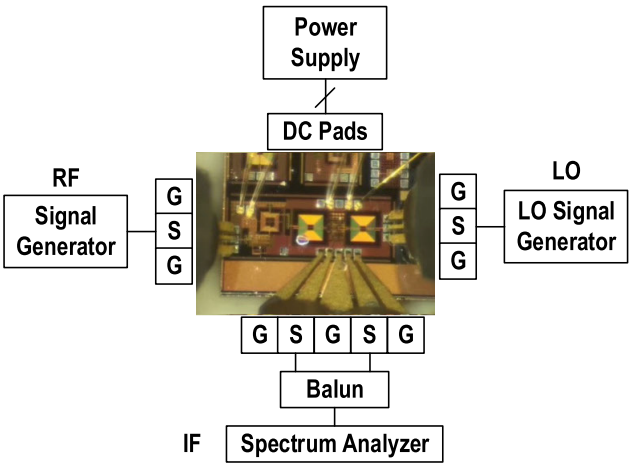

FIGURE 12. Block diagram of the test setup.

embedded from the measured data. Note that, the parasitic capacitance will significantly increase the imbalance when the operational frequency is higher than 6 GHz.

Table 2 summarizes the critical metrics of implemented balun and recently reported state-of-the-art baluns operating in sub-6 GHz band. As can be seen, PCB-based baluns typically show better fractional bandwidth, while they suffer from the relative dimensions. Compared with other works, the proposed balun exhibits the minimum in-band phase error, acceptable amplitude imbalance as well as the compact device size. It also achieves a maximum FBW among the CMOS-based transformer baluns.

B. WIDEBAND RF FRONT-END

The chip die photo of the RF front-end with the proposed transformer balun is shown in Figure 11. The chip area of the RF front-end is 1.7×0.59 mm^2 including pads. The block diagram of the RF front-end test setup is shown in Figure 12. The RF and LO signals are fed by using on-wafer GSG probes, while IF signals are measured through GSGSG probes. The DC pads are wire-bonded to PCB for the DC bias. The measured DC current of LNA and mixer are 11.6 mA and 4 mA from a 1.2 V supply, respectively.

Figure 13 shows that the measured and simulated S_{11} of the RF front-end. The measured S_{11} is -13 dB at 2.5 GHz, and remains lower than -10 dB from 1.6 to 3.9 GHz. Figure 14(a) depicts the measured and simulated CG of the RF front-end

TABLE 2. Performance summary and comparison of the balun.

Ref.	Technology	Freq. @ $\|S_{11}\|$<-10dB [GHz]	FBW* [%]	Amp. imbalance [dB]	Phase imbalance [°]	Size [mm^2]	Relative dimensions#
[1]	PCB	1.2-2.8	80	0.6	9	989	$0.3\lambda_o \times 0.15\lambda_o$
[5]	PCB	1.2~3.3	93.3	0.49	6.5	315	$0.13\lambda_o \times 0.13\lambda_o$
[6]	PCB	1.0-2.3	78.8	1	3.4	884.5	$0.14\lambda_o \times 0.15\lambda_o$
[2]	Silicon-based	1.6-2.6	47.6	0.3	2	2.76	$0.0084\lambda_o \times 0.0164\lambda_o$
[15]	CMOS	6-10$	50	0.6	7	0.01	$0.0027\lambda_o \times 0.0027\lambda_o$
[23]	CMOS	5-6	18.1	1	4	0.06	$0.0092\lambda_o \times 0.0044\lambda_o$
This work	**CMOS**	**2.1-5.1**	**83.3**	**1.5**	**2**	**0.14**	$\mathbf{0.0045\lambda_o \times 0.0045\lambda_o}$

* FBW: BW/f_c, where BW is the frequency range of $|S_{11}|$<-10 dB, and f_c is the center frequency of BW.
$ 3dB-gain bandwidth, S_{11} is not mentioned.
# λ_o: wavelength in free space, $\lambda_o = c/f_c$.

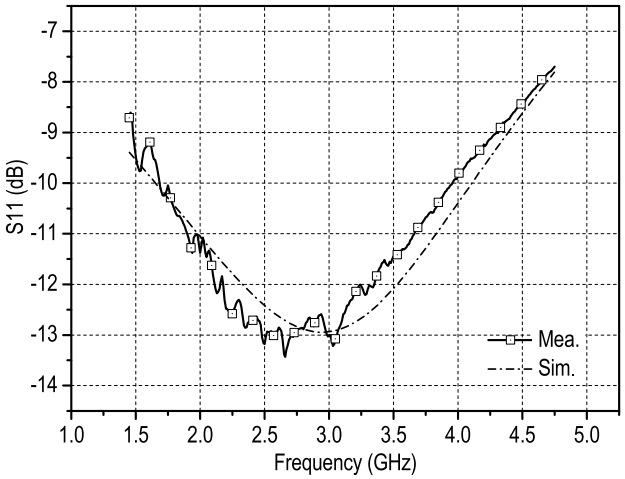

FIGURE 13. Measured and simulated S_{11} of the RF front-end.

versus the RF input frequency with the LO power (P_{LO}) of −3dBm. It shows that the maximum CG is 34.6 dB at 2.7 GHz with the IF of 2.8 MHz. The CG is 33.1 ± 1.5 dB from 2.0 to 3.7 GHz and the corresponding 3 dB RF bandwidth is 1.7 GHz. The measurement result matches well with the trend of simulated one. Figure 14(b) shows that the CG is 32.7±0.5 dB with the IF frequency from 1 to 450 MHz. Figure 14(c) shows the measured CG versus LO power at LO frequency of 2.4 GHz. The RF front-end achieves a maximum CG of 33.6 dB with the LO power of -3 dBm. A 3-dB degradation of the CG is observed when the LO power is reduced to −8.2 dBm.

Figure 15 plots the measured and simulated NF as a function of the IF frequency from 20 to 500 MHz. As can be seen, the RF front-end achieves the NFs of 3.4, 2.7, and 3.0 dB at the frequency of 10, 250, and 450 MHz, respectively. Two-tone tests were performed to measure/simulate the IIP_2 and IIP_3 by applying two RF signals with the equal power level at 2.79 and 2.81 GHz, as shown in Figure 16. The measured/simulated results show that the IIP_3 and IIP_2 of

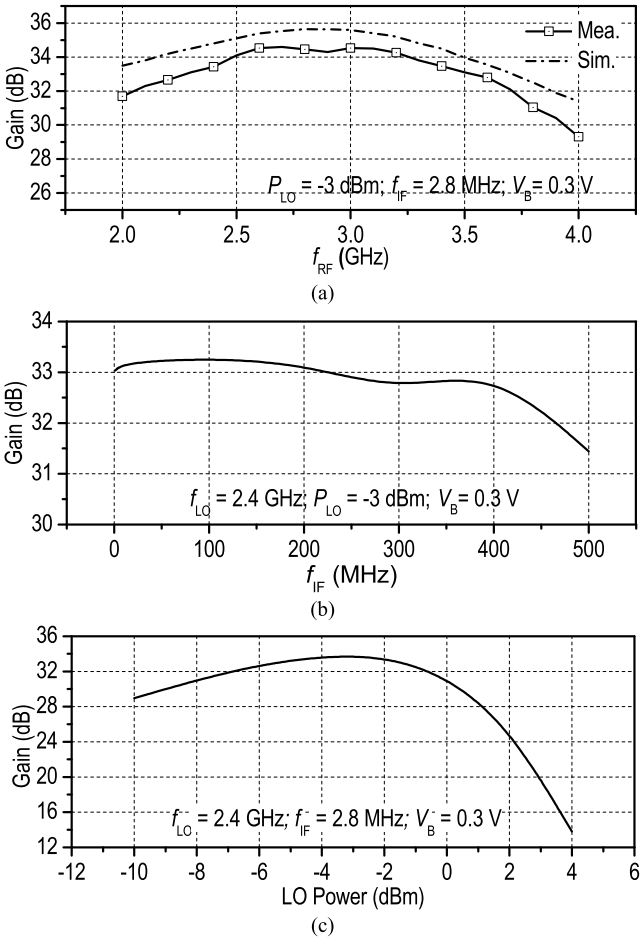

FIGURE 14. Measured CG versus (a) RF frequency, (b) IF frequency, and (c) LO power.

the RF front-end are −19.1 dBm and 36.1 dBm, respectively. Figure 17 shows that measured LO-to-RF isolations is 73.4 dB.

Table 3 summarizes the measured performance and compared with the state-of-the-art RF front-end. Thanks to the

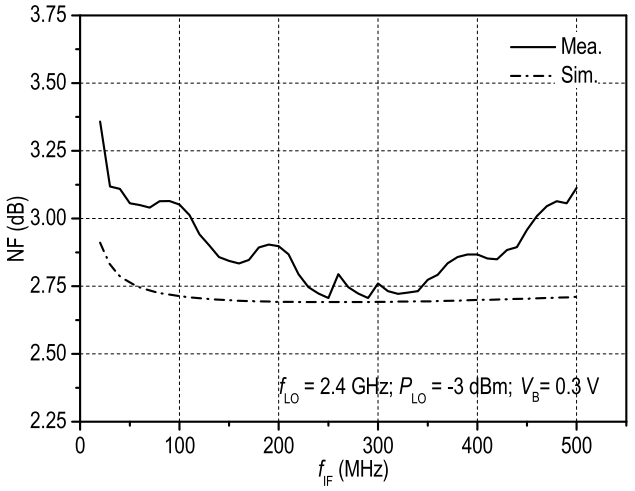

FIGURE 15. Measured NF of the RF front-end.

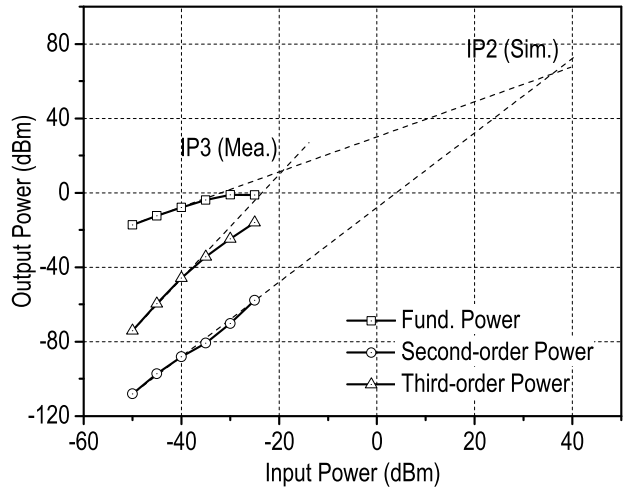

FIGURE 16. Measured IP3 and IP2 with the PLO of −3 dBm.

TABLE 3. Performance summary and comparison of the RF front-end.

Ref.	[29]	[30]	[31]	**This work**
Techn. [nm]	90	180	65	**130**
Freq. [GHz]	4.6-6	0.1-2.5	1.8-2.7	**2.0-3.7**
Peak Gain [dB]	26	30	41-43	**34.6**
NF [dB]	2.7	2.7-4.5	4.1-4.7	**2.7-3.4**
IIP_3 [dBm]	-12	-17.7	-12	**-19.1**
IIP_2 [dBm]	33	N/A	N/A	**36.1***
LO-to-RF ISO. (dB)	62	N/A	N/A	**73.4**
P_{DC} [mW]	21	39.6	21.8	**18.8**

* Simulated result.

wideband balun, the proposed RF front-end achieves better performance in terms of IIP_2, and LO-to-RF isolation without using specific IM_2 cancelling technique.

V. CONCLUSION

A transformer balun with common ground and artificial dielectric compensation techniques is proposed for a 2.0-to-3.7 GHz RF front-end. The chips are fabricated using 0.13-μm bulk CMOS technique. The bandwidth of the balun with $|S11| < -10$ dB is 2.2-to-5.1 GHz, and the fractional bandwidth is large than 79.5%. In the desired bandwidth, the maximum amplitude and phase mismatches are 1.5 dB and 2°, respectively. It also achieves an insertion loss of 4.8-to-5.6 dB from 2.1-to-5.1 GHz. The measurement results show that CMOS balun achieves good input match, low amplitude mismatch as well as high phase accuracy.

ACKNOWLEDGMENT

The authors would like to thank members of Tianjin University and Southeast University of EAST Laboratory for their technical supports.

REFERENCES

[1] H. Zhu and A. M. Abbosh, "Modified wideband Marchand balun with tunable power division ratio and constant phase," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 5, pp. 319–321, May 2016.
[2] Y. J. Yoon, Y. Lu, R. C. Frye, and P. R. Smith, "A silicon monolithic spiral transmission line balun with symmetrical design," *IEEE Electron Device Lett.*, vol. 20, no. 4, pp. 182–184, Apr. 1999.
[3] G. Yang, Z. Wang, Z. Li, Q. Li, and F. Liu, "Balance-compensated asymmetric Marchand baluns on silicon for MMICs," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 6, pp. 391–393, Jun. 2014.
[4] G. Yang, K. Wang, and Z. Wang, "20.8–51 GHz highly balanced CMOS balun," *Electron. Lett.*, vol. 53, no. 17, pp. 1202–1203, Aug. 2017.
[5] Y. F. Geng, W. Wang, X. Chen, L. Han, L. Li, and W. Zhang, "The study and design of a miniaturized microstrip balun with a wider bandwidth," *IEEE Anten. Wireless Propag. Lett.*, vol. 15, pp. 1727–1730, 2016.
[6] H.-X. Xu, G.-M. Wang, X. Chen, and T.-P. Li, "Broadband balun using fully artificial fractal-shaped composite right/left handed transmission line," *IEEE Microw. Wireless Compon. Lett.*, vol. 22, no. 1, pp. 16–18, Jan. 2012.
[7] K. Ma, N. Yan, K. S. Yeo, and W. M. Lim, "Miniaturized 40–60 GHz on-chip balun with capacitive loading compensation," *IEEE Electron Device Lett.*, vol. 35, no. 4, pp. 434–436, Apr. 2014.
[8] S. Chakraborty, L. E. Milner, X. Zhu, L. T. Hall, O. Sevimli, and M. C. Heimlich, "A K-band frequency doubler with 35-dB fundamental rejection based on novel transformer balun in 0.13-μm SiGe technology," *IEEE Electron Device Lett.*, vol. 37, no. 11, pp. 1375–1378, Nov. 2016.
[9] A. M. Niknejad and R. G. Meyer, "Analysis, design, and optimization of spiral inductors and transformers for Si RF ICs," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1470–1481, Oct. 1998.
[10] A. Zolfaghari, A. Chan, and B. Razavi, "Stacked inductors and transformers in CMOS technology," *IEEE J. Solid-State Circuits*, vol. 36, no. 4, pp. 620–628, Apr. 2001.
[11] F. Rotella, G. Tkachenko, and Y. Cheng, "Characterization, design, modeling, and model validation of silicon-wafer M: N balun components under matched and unmatched conditions," in *IEEE RFIC Symp. Dig. Papers*, Jun. 2005, pp. 291–294.
[12] S. Jenei, B. K. J. C. Nauwelaers, and S. Decoutere, "Physics-based closed-form inductance expression for compact modeling of integrated spiral inductors," *IEEE J. Solid-State Circuits*, vol. 37, no. 1, pp. 77–80, Jan. 2002.
[13] J. R. Long, "Monolithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1382, Sep. 2000.
[14] C. Cismaru, Y. Tkachenko, and Y. Cheng, "Characterization, design, modeling, and model validation of silicon on-wafer M: N balun components under matched and unmatched conditions," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1201–1209, May 2006.
[15] W.-Z. Chen, W.-H. Chen, and K.-C. Hsu, "Three-dimensional fully symmetric inductors, transformer, and balun in CMOS technology," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 7, pp. 1413–1423, Jul. 2007.
[16] K. Wang, L. Qiu, J. Koo, R. Ruby, and B. Otis, "Design of 1.8-mW PLL-free 2.4-GHz receiver utilizing temperature-compensated FBAR resonator," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1628–1639, Jun. 2018.

[17] G. Yang, R. Chen, and K. Wang, "A CMOS balun with common ground and artificial dielectric compensation achieving 79.5% fractional bandwidth and <2° phase imbalance," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2020, pp. 1319–1322.
[18] K. Sachse, "The scattering parameters and directional coupler analysis of characteristically terminated asymmetric coupled transmission lines in an inhomogeneous medium," *IEEE Trans. Microw. Theory Techn.*, vol. 38, no. 4, pp. 417–425, Apr. 1990.
[19] H. Wang, L. Zhang, D. Yang, D. Zeng, Y. Wang, and Z. Yu, "Modeling of current-return-path effect on single-ended inductor in millimeter-wave regime," *IEEE Electron Device Lett.*, vol. 32, no. 6, pp. 737–739, Jun. 2011.
[20] M. Danesh and J. R. Long, "Differentially driven symmetric microstrip inductors," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 1, pp. 332–341, Jan. 2002.
[21] K. Wang, B. Otis, and Z. Wang, "A 580-μW 2.4-GHz Zigbee receiver front-end with transformer-coupling technique," *IEEE Microw. Wireless. Compon. Lett.*, vol. 28, no. 2, pp. 174–176, Jan. 2018.
[22] J. Koo, K. Wang, R. Ruby, and B. P. Otis, "A 2-GHz FBAR based transformer coupled oscillator design with phase noise reduction," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 4, pp. 542–546, Aug. 2019.
[23] H.-S. Lee, K. Kim, and B.-W. Min, "On-chip T/R switchable balun for 5-to 6-GHz WLAN applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 1, pp. 6–10, Jan. 2015.
[24] Y.-S. Lin, C.-Z. Chen, H.-Y. Yang, C.-C. Chen, J.-H. Lee, G.-W. Huang, and S.-S. Lu, "Analysis and design of a CMOS UWB LNA with dual-*RLC*-branch wideband input matching network," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 2, pp. 287–296, Feb. 2010.
[25] K. Wang, G. Yang, and Z. Wang, "3-13 GHz Q-enhanced low noise amplifier with optimized inductors utilizing in-phase current returning path technique," *Microw. Opt. Technol. Lett.*, vol. 61, no. 7, pp. 1712–1715, Jul. 2019.
[26] W.-T. Li, H.-Y. Yang, Y.-C. Chiang, J.-H. Tsai, M.-H. Wu, and T.-W. Huang, "A 453-μ/W 53–70-GHz ultra-low-power double-balanced source-driven mixer using 90-nm CMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 5, pp. 1903–1912, May 2013.
[27] E. A. M. Klumperink, S. M. Louwsma, G. J. M. Wienk, and B. Nauta, "A CMOS switched transconductor mixer," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1231–1240, Aug. 2004.
[28] K. Wang, J. Koo, R. Ruby, and B. Otis, "A 1.8 mW PLL-free channelized 2.4 GHz ZigBee receiver utilizing fixed-LO temperature-compensated FBAR resonator," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 372–373.
[29] H.-K. Chiou, K.-C. Lin, W.-H. Chen, and Y.-Z. Juang, "A 1-V 5-GHz self-bias folded-switch mixer in 90-nm CMOS for WLAN receiver," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 6, pp. 1215–1227, Jun. 2012.
[30] J. Han and K. Kwon, "I/Q balance-enhanced wideband receiver front-end for 2G/3G/4G/5G NR cellular applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 6, pp. 1881–1891, Jun. 2020.
[31] L. Liu, K. Zhang, Z. Ren, Z. Lu, and X. Zou, "0.05–2.5 GHz wideband RF front-end exploiting noise cancellation and multi-gated transistors," in *Proc. Asia–Pacific Microw. Conf. (APMC)*, Dec. 2015, pp. 1–3.

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