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Post-Measurement Adjustment of the Coincidence Window in Quantum Optics Experiments

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ABSTRACT We report on an electronic coincidence detection circuit for quantum photonic applications implemented on a field-programmable gate array (FPGA), which records each the time separation between detection events coming from single-photon detectors. We achieve a coincidence window as narrow as 500 ps with a series of optimizations on a readily-available and affordable FPGA development board. Our implementation allows real-time visualization of coincidence measurements for multiple coincidence window widths simultaneously. To demonstrate the advantage of our high-resolution visualization, we certified the generation of polarized entangled photons by collecting data from multiple coincidence windows with minimal accidental counts, obtaining a violation of the Clauser-Horne-Shimony-Holt (CHSH) Bell inequality by more than 338 standard deviations. Our results have shown the applicability of our electronic design in the field of quantum information.

INDEX TERMS Field-programmable gate arrays, quantum information, coincidence counting.

I. INTRODUCTION

The measurement of the arrival time of detections between two or more coincident photons is a fundamental task for many experiments of certification of quantum entanglement, where often Bell's inequalities are used as entanglement witness in the field of quantum information [1]–[7]. Electronic coincidence circuits (ECCs) are employed to determine if detection signals from two (or more) single-photon detectors are close enough in time, by recording a coincidence event if the arrival signals are detected within a time interval τ, usually called the coincidence window. The width of τ is a crucial parameter in such measurements, since in an experiment the detectors present fake detections due to thermal noise, background detections or imperfections in the optical system, which can be detected within τ, leading to accidental coincidence counts. Thus, decreasing the width of τ lowers down the number of accidental coincidences, improving the signal-to-noise ratio. This becomes even more crucial in experiments where high-quality results are needed [5], [6].

Reconfigurable electronic devices such as high-cost field programmable gate arrays (FPGAs) [8], [9] have been proposed to reduce τ to the sub-nanosecond range. However, the temporal uncertainty of the signal generated in the detection of a photon (jitter) in many single-photon detectors [10], implies that a τ with resolution on the order of hundreds of picoseconds is sufficient for coincidence measurements. Thus, low-cost FPGA designs have focused on reducing this

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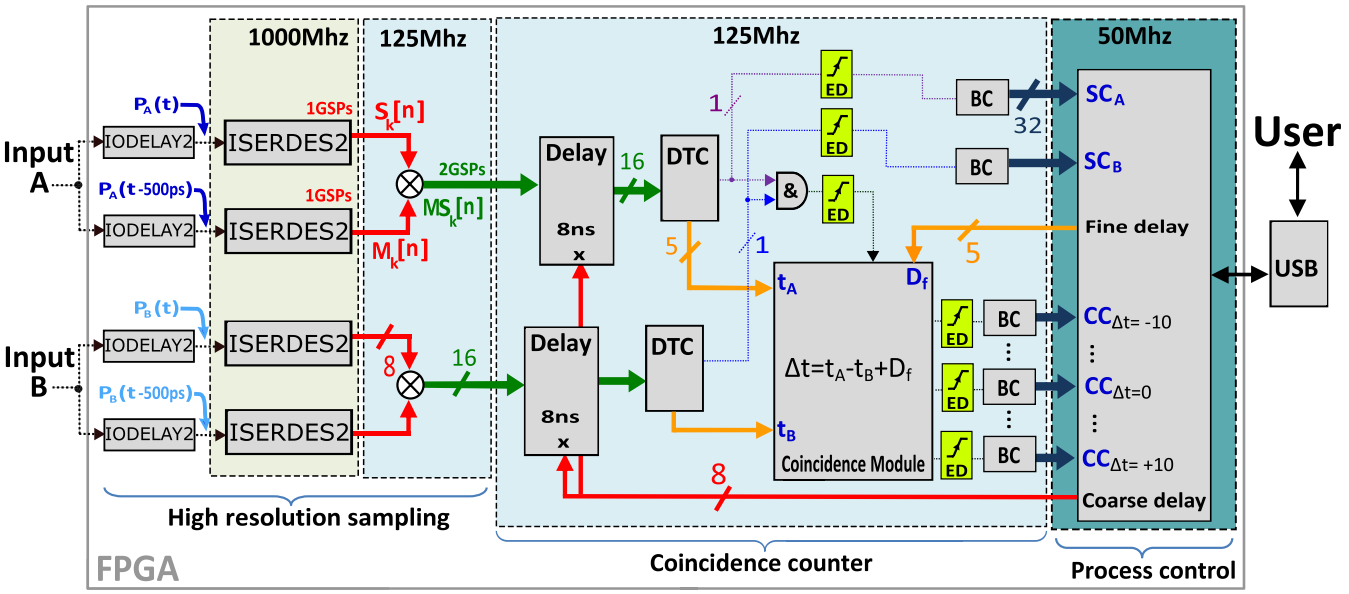

FIGURE 1. ECC architecture synthesized on a Xilinx Spartan-6 FPGA. Two electrical input pulses (A and B) are connected directly to the FPGA. Each pulse is sampled at 1GHz in two tuples: $S_k[n]$ and $M_k[n]$ of 8 bits each. The sampling in $M_k[n]$ is delayed by 500ps with respect to $S_k[n]$ (both provided every 8 ns, corresponding to 125 MHz). then both are merged, generating the 16 bit register $SM_k[n]$, which contains the pulse information sampled at a rate of 2 GS/s. The arrival time of each input is obtained in the digital-to-time converter (DTC) module, whose outputs allow the calculation of the arithmetic difference between arrival times A and B, registering arrivals in coincidence for different detection windows simultaneously. All single (SC) or coincident (CC) counts are accumulated in 32-bit binary counters (BC), which are enabled with an edge detector (ED). The results are shared with a host computer via a USB connection.

parameter with a sequential architecture, where a high speed internal clock is required to improve the resolution of τ, limiting its width to a few nanoseconds [11], [12]. On the other hand, low-cost architectures based on logic gates (combinational coincidence evaluation) have been proposed as coincidence counters by reducing τ to few tens of nanoseconds [13], then improving to sub nanosecond resolution using external circuits [14]. FPGAs using sequential architectures are capable to acquire and transmit electronic signals in the nanosecond regime [15]–[17], integrating arithmetic processes, and providing flow control over different clocks within a single integrated circuit (IC) [18], [19], even being used to manage different quantum information systems, such as quantum routing [20], [21], quantum random generation [22], [23], and quantum key distribution [24]–[26].

In this paper, we present an ECC whose architecture is focused on low-cost sequential architectures, to provide a coincidence window τ in the sub-nanosecond range. This is possible using an Xilinx Spartan-6 FPGA, whose resources allow a sequential architecture capable of a sampling rate of 2 GSPS (gigasample per second) [19]. We obtain an average coincidence window τ of 500±32.1 ps, using an arithmetic process synchronized at 125MHz. With our scheme, we have obtained the temporal information of each coincident signal recorded simultaneously and in real-time over several different coincidence window widths. We demonstrate the precision and usability of the ECC, with which we experimentally certify the generation of polarization-entangled photon pairs of photons through a violation of more than 338 standard deviations of the Clauser-Horne-Shimony-Holt (CHSH) Bell inequality [1]. Finally we show that from the same measured data, we can tune the coincidence window versus the coincidence detection rate depending on the intended application.

This paper is organized as follows: Section II introduces the architecture of the proposed ECC. Section III presents a method to evaluate the ECC performance, obtaining empirical parameters such as τ, jitter and skew. In Section IV, we experimentally certify the generation of polarization entangled photon pairs based on spontaneous parametric down-conversion, demonstrating the accuracy and usability of the ECC presented. Finally, in Section V our work is summarized and concluded.

II. ARCHITECTURE

Figure 1 shows a diagram of the proposed architecture. The process begins at the High resolution sampling stage, where an analog pulse (input A or B) arrives at two input ports. Each port is further divided into two paths, each containing an asynchronous delay line (IODELAY2, [19]), which imposes a time delay of 500 ps between the paths. In the case of input A, the resulting streams on each port ($P_A(t)$ and $P_A(t-500$ ps)) are connected to two synchronized serializers (ISERDES2 [19]), where they are digitized every 1 ns. These ISERDES2 are configured with a 1:8 ratio, generating the 8-bit registers $S_k[n]$ and $M_k[n]$ (please see Fig. 1), which are accessible every 8 ns with a 125MHz clock. To establish that we are now dealing with synchronized discrete times, the subscript k indicates the discrete time associated with that

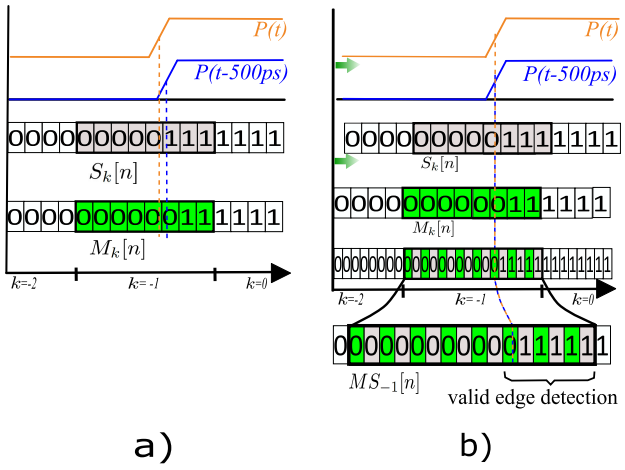

FIGURE 2. High resolution sampling process. a) An input is replicated in two streams, such that one has a delay of 500 ps, generating $P(t)$ and $P(t-500\text{ps})$ respectively. Both are digitized by two 8-bit serial to parallel converters (ISERDES2) at 1 GHz, generating two 8-bit strings $S_k[n]$ and $M_k[n]$ each 125MHz. b) By combining $S_k[n]$ and $M_k[n]$ and interleaving their bits, a 16-bit string $MS_k[n]$ is formed, whose sampling rate is equivalent to 2GS/s over $P(t)$. A valid edge detection in $MS_{-1}[n]$ is defined as a single 0 followed by at least five 1s (please see the text for further details).

particular register, while n represents the bit position within the register, as shown in Fig. 2.a. The same is also performed with respect to input B. The serialization process optimizes most of the resources in the FPGA, such as accumulators and arithmetic operations, evidently reducing dynamic energy consumption by almost two orders of magnitude (comparing the original 2 GHz process vs 125Mhz) [27].

Finally, $S_k[n]$ and $M_k[n]$ are merged every 8 ns, interleaving their bits in order of arrival, producing a new register of 16 bits ($MS_k[n]$), with the process illustrated in Fig. 2.b. Since $S_k[n]$ and $M_k[n]$ are delayed by 500 ps, each reordered bit in $MS_k[n]$ represents sampling every 500 ps (2GS/s), which is processed at the much slower clock of 125 MHz. The internal clocks are adjusted in phase with a phase lock loop (PLL), included in the Spartan 6.

Then, the Coincidence counter module first generates a controlled delay on each 16-bit string (coming from inputs A and B), which is implemented using two variable-length RAM-based shift registers with 8-bit addressing input. Each address bit generates a delay in 8 ns steps, providing a delay between 0 and 2040 ns, which is a coarse delay set by the user (see Fig. 1). With the defined delay, the arrival time of each sample $M_k[n]$ is calculated in the digital-to-time converter (DTC) module. Basically, the DTC assigns a time of arrival value correlated to the detection of a rising edge in the n_{th} bit of $MS_k[n]$. Then, to reduce the chance of false-positives a valid edge detection is defined as a single 0 followed by at least five 1s (...011111...), as shown in Fig. 2.b.

In order to adequately deal with pulses arriving at the first or last slots of the $MS_k[n]$ 16-bit string, we generate an intentional latency expressed through k, where $k = -1$ indicates that the string is out of phase by 8 ns, while $k = -2$ indicates a latency of 16 ns. We then use the following procedure: we form a new 21-bit string called $MS'[n]$ by concatenating the last bit of the string at $k = -2$ with the complete string at $k = -1$, and the first four bits of the current string at $k = 0$.

Then the rising edge position in $MS'[n]$ is written as the 5-bit positive integers t_A^* and t_B^*, which represent the arrival time of the pulses at A and B for the cycle k_j respectively. Valid detection of either time leads to a corresponding single count detection event (SC_A or SC_B) whose accumulation is recorded in a 32-bit counter providing the single count detection rate, which is made available to the user.

In the Coincidence module, the arrival times are re-calculated based on the k_{th} read cycle with the expressions: $t_A = t^*_{A+8ns} \cdot (Nk_A)$ and $t_B = t^*_{B+8ns} \cdot (Nk_B)$, where Nk_A and Nk_B are two binary counters of 5 bits, which increases in each k_{th} read cycle and they are independently reset with a valid detection on each input. These registers allowing us re-calculate asynchronous arrival times for A and B. Then, when valid arrivals are detected in A and B, the arithmetic difference between t_A and t_B will give us a temporal mapping of coincidences for multiple coincidence windows simultaneously:

$$\Delta t = t_A - t_B + D_f, \tag{1}$$

where D_f is a fine adjustable 5-bit delay, with 500 ps precision. All Δt values are recorded in a 32-bit binary counter labeled $CC_{\Delta t}$ and sent to a host computer for user processing through a USB interface (21 such counters are needed in total, for instance, to record the different Δt between -5 ns and 5 ns with 500 ps difference between them). Finally, in a post-process the user can take the sum of the counts from the several $CC_{\Delta t}$ and obtain simultaneous τ measurements, where the width of τ depends on the value of the accumulated Δt. For example if we sum $CC_{\Delta t=0} + CC_{\Delta t=0.5}$ we have the counts over a coincidence window of 1 ns.

III. DESIGN EVALUATION

To evaluate our design, we first define τ as a function of the sampling resolution t_r obtained on each bit of $MS_k[n]$, in the form:

$$\tau = mt_r + d_w, \tag{2}$$

where m is the number of slots that define a window, while d_w represents the total skew noise at a resolution time t_r, as we shown in the Fig. 3.a.

We can define a function when the coincidence window is enabled, based on the delayed time t_d from a trigger detection on A or B, given by:

$$w(t_d) = \begin{cases} 1 & \text{if } 0 \le t_d \le \tau \\ 0 & \text{else} \end{cases}. \tag{3}$$

On the other hand, considering the second arrival time has a stronger influence of the electronic jitter [28] and expressed as a function of a time delay t_d (see Fig. 3.b), then N detection

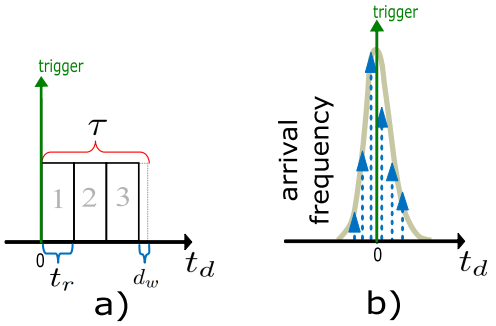

FIGURE 3. Arrival time model. a) Parameters of coincidence windows ($w(t_d)$). b) Stronger influence of the electronic Jitter in arrival time ($g(t_d)$).

events will display a Gaussian variation ($g(t)$) with uncertainty σ and amplitud N', expressed as:

$$g(t_d) = N' e^{-\frac{(t_d)^2}{2\sigma^2}} \tag{4}$$

We define a coincidence count T_{CC}, when $g(t_d)$ is within the coincidence window function $w(t_d)$, as the following convolution between the two functions, for all t_d:

$$T_{CC} = \int_{-\infty}^{\infty} w(t) \cdot g(td - t)dt, \tag{5}$$

The convolution expressed in Eq. 5 can be carried out experimentally using a function generator that is capable of delaying two pulses with a timing resolutions better than t_r. Thus, to avoid solving a Gaussian integral, we make a simple change of variables obtaining $T_{CC} = -\int_{t_d}^{t_d-\tau} g(u)du$. Differentiating with respect to t_d, we obtain:

$$\frac{dT_{CC}}{dt_d} = N' \left\{ e^{-\frac{(t_d)^2}{2\sigma^2}} - e^{-\frac{(t_d-\tau)^2}{2\sigma^2}} \right\}. \tag{6}$$

The expressions in Eq. 6 and Eq. 2 allow us to experimentally measure the parameters τ, σ, t_r and d_w. Therefore, using a Textronix AFG3000 series function generator (with 10 ps of resolution delay time), we have the emulation of T_{CC} varying the delay in steps of 100 ps between two electrical pulses, with rate of 100 kcounts per second, performing the convolution. Thus, we obtain T_{CC} for different coincidence windows as shown in Fig. 4.a.

On the other hand, to measure the parameters mentioned above, we differentiate the results from Fig. 4a and adjust the data with the expression in Eq. 6 (as shown in Fig. 4.b, with a 3ns window as an example), obtaining the values that are presented in Table 1. These results show that the empirical standard deviation of the electronic noise is $\sigma_e = 0.1867 \pm 0.00048$ ns. This deviatios comes from the jitter of the function generator and electronic fluctuation [28]. The empirical time resolution was measured as $t_r = 0.5009$ ns with $d_w = 0.0312$ ns, obtained from Eq. 2 over multiple τ widths ($n = 1, 2, \ldots$).

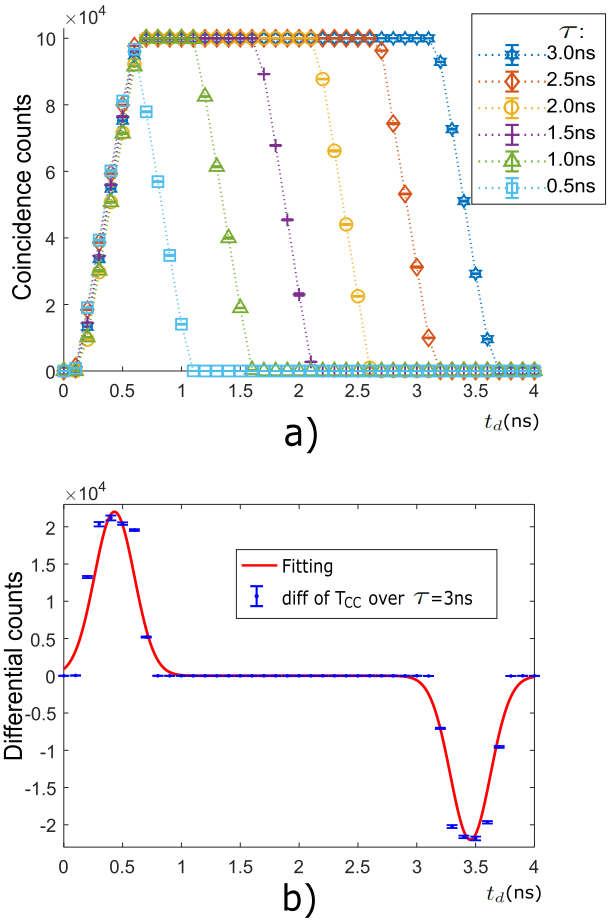

FIGURE 4. Experimental measurements from the proposed ECC obtained using function generator. a) Experimental T_{CC} of simultaneous measurements over various widths of τ. b) Fit of equation 6 on experimental $\frac{dT_{CC}}{dt_d}$ for $\tau = 3ns$.

TABLE 1. Empirical parameters obtained from fitting the experimental measurements with equation 6, and its respective quadratic correlation coefficient (R^2).

n	τ (ns)		σ	R^2
	Design	Empirical		
1	0.5	0.5132 ± 0.0008	0.1879 ± 0.0003	0.9245
2	1	1.0418 ± 0.0037	0.189 ± 0.0001	0.9498
3	1.5	1.5337 ± 0.0008	0.1836 ± 0.0008	0.955
4	2	2.0485 ± 0.0011	0.1844 ± 0.0005	0.951
5	2.5	2.5688 ± 0.0008	0.1873 ± 0.0005	0.9469
6	3	3.0005 ± 0.0031	0.188 ± 0.0007	0.967

IV. POLARIZATION ENTANGLEMENT CERTIFICATION

To demonstrate a practical application and the advantage of the simultaneous multi-width coincidence-windows of our ECC design, we have implemented a photonic experiment to certify two-qubit entanglement using an ultrabright, intrinsically phase-stable photon-pair source based on the spontaneous parametric down-conversion process [6], [29]. The experimental setup is shown in Fig. 5. A 20 mm long, type II non-linear PPKTP crystal placed in a Sagnac interferometer was pumped by a continuous-wave laser operating at 405 nm [30], [31], generating degenerate down-conversion

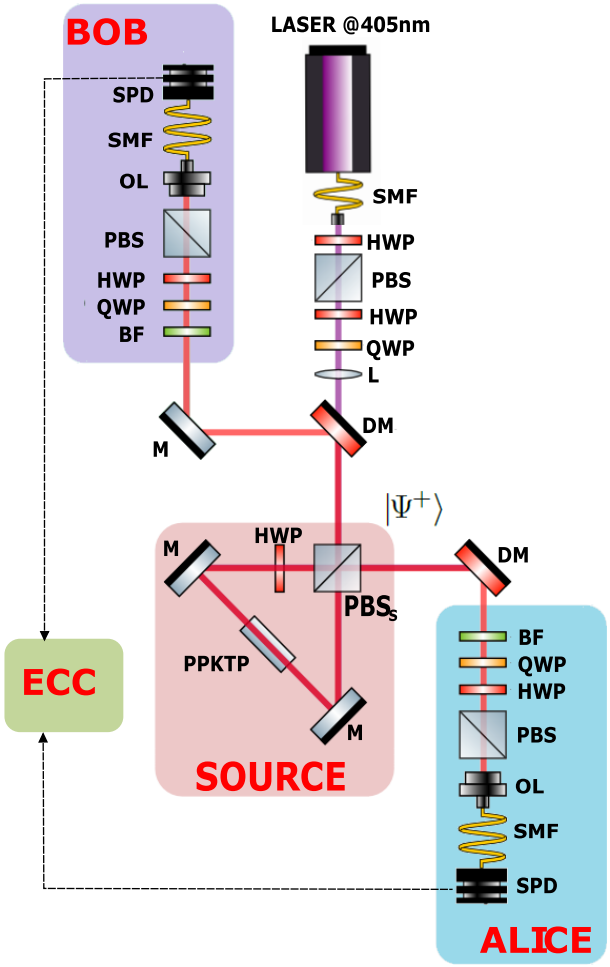

FIGURE 5. Experimental scheme for the ultrabright parametric down-conversion photon-pair source used for testing our ECC. A Sagnac interferometer with a non-linear crystal was used to generate polarization-entangled photons through the down-conversion optical process. M: mirror; PPKTP: periodically poled KTP non-linear crystal; L: 20 cm focal length lens; HWP and QHP: half- and quarter-wave plate; PBS: polarizing beam splitter; DM: dichroic mirror; BF: bandpass filter; SMF: single-mode fiber; SPD: single-photon detector; OL: 10X objective lens; ECC: electronic coincidence circuit. See the main text for more details.

photon pairs at 810 nm in orthogonal polarization modes. Waveplates and a polarizer cube are used to set the pump beam polarization mode to propagate it on the interferometer's reflected and transmitted path. Therefore, photon pairs are generated in the clockwise and counterclockwise direction inside the interferometer. The HWP was set at 45^o to the horizontal, obtaining after the PBS$_S$ the maximally entangled state

$$|\Psi^+\rangle = \frac{1}{\sqrt{2}}(|HV\rangle + |VH\rangle), \tag{7}$$

where $|H\rangle$ ($|V\rangle$) denotes the horizontal (vertical) polarization of the down-converted photon. Dichroic mirrors are placed to remove the remaining pump laser, and Semrock high-quality filters centered at 810 nm (0.5 nm bandpass) are placed at both measurement stages called Alice and Bob (see Fig. 5). Moreover, we follow the numerical model proposed in [32] to maximize the Alice and Bob's coincidence rate. This optimal condition is achieved when $\omega_{SPDC} = \sqrt{2}\omega_p$, where ω_p is the beam waist, and ω_{SPDC} is the waist of the down-converted photons spatial mode at the center of the PPKTP crystal. We used a 20 cm focal length lens (L) for the pump focusing at the crystal's center. Furthermore, to prevent distinguishability between the spatial modes with HV and VH polarization, we couple the generated down-converted photons into single-mode optical fibers (SMF) using 10X objective lens. Thus, ensuring high-quality polarization-entanglement generation.

We certify the polarization entanglement generation evaluating the Clauser-Horne-Shimony-Holt (CHSH) Bell inequality [1], with the aid of our ECC. In the Bell-CHSH scenario, the source distributes the photons to Alice and Bob. Each party can choose among two measurements, denoted by $x, y \in \{0, 1\}$, with binary results $a, b \in \{-1, 1\}$. The CHSH inequality reads

$$S \equiv E(0,0) + E(0,1) + E(1,0) - E(1,1) \leq 2, \tag{8}$$

where $E(x, y) \equiv P(00|xy) - P(01|xy) - P(10|xy) + P(11|xy)$ is the expectation value for both measurements x and y. Here, $P(ab|xy)$ is the joint conditional probability distribution when Alice (Bob) implements the measurement x (y) and obtains the outcome a (b). Quantum theory predicts a violation of this inequality, which its maximum value is $S^{QM} = 2\sqrt{2}$, achieving by a two-qubit maximally entangled state and projective measurements. In our experiment, these projective measurements were implemented in Alice and Bob with a typical polarization analyzer composed of two waveplates and a polarizing beam-splitter (see Fig. 5). PerkinElmer single-photon detectors (SPD) are placed at Alice (Bob) connected to SMFs, recording the arriving photons. This optical configuration allows us to reach two-photon visibility close to 99.7% in the logical and diagonal polarization measurement bases. Besides, considering the SPD quantum efficiency (50% @ 810 nm) and the optical transmission of the filters, polarization controllers, and fiber coupling, we have estimated an overall detection efficiency of 15%.

The ECC records each SPD's output to evaluate the coincidence detection rate (R_{CC}) depending on the circuit's coincidence window τ. However, the accidental counts arising from the electronic and thermal noise affect the experimental value of S. The relation between τ and the accidental coincidence rate R_{Acc} is given by $R_{Acc} = R_A \times R_B \times \tau$, where R_A (R_B) is the single-photon detection rate at the Alice's (Bob's) detector. Thus, smaller values of τ imply smaller accidental coincidence counts. The estimated joint conditional probabilities become more accurate while τ is decreasing, and therefore we can improve the estimation of S adopting lower values of τ. In our experiment, we define eight coincidence windows simultaneously (range from 0.5 to 4 ns) on the ECC to evaluate S. This implies that we can estimate eight joint conditional probabilities at the same time for each joint measurement. For instance, an ECC user can exploit this advantage, selecting a desired τ value after the experiment has done depending on the user's application and needs. The

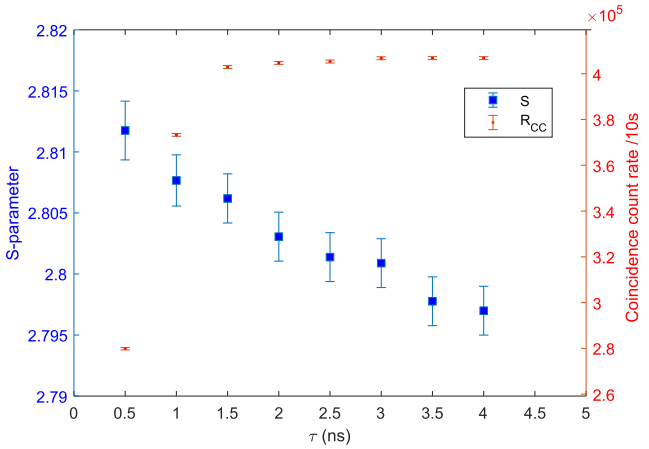

FIGURE 6. Experimental results of the S parameter and the coincidence detection rate (R_{CC}) for multiple coincidence windows τ.

obtained experimental results are shown in Fig. 6. We can observe that the S value on Eq. 8 is improved by reducing the coincidence window τ. For instance, considering one projective measurement (the red line in Fig. 6) with $\tau = 4\,ns$, the coincidence rate is $R_{CC} \approx 410.000$ counts in $10\,s$ of integration. By reducing the coincidence window to $\tau = 0.5\,ns$, the R_{CC} decreases to 280.000 coincidence counts in the same integration time.

The decrease in R_{CC} depends on the jitter of 0.585 ± 0.092 ns in the coincidence counts distribution from both PerkinElmer detectors. This temporal uncertainty is not perceived in coincidence windows greater than 1.5ns, which stabilizes the R_{CC} around 280.000 coincidence counts, however, for shorter coincidence windows the R_{CC} decreases proportionally to the Gaussian function while still increasing the S-parameter.

V. CONCLUSION

We have developed an ECC based on a commercial Spartan 6 FPGA, while allowing the choice of coincident window width to be chosen after the measurement is performed. We achieve a sampling pulse rate of 2 GS/s based on a base clock of only 125 MHz, with a resolution $t_r = 0.5009 \pm 0.0312$ ns. In our design, we process the coincidence counts at the base frequency based on the arithmetic difference between the arrival times of the input pulses. We employed the proposed design on a Bell CHSH inequality violation experiment, obtaining a Bell parameter of $S = 2.8117 \pm 0.0024$ at the narrowest coincidence window of $\tau = 0.5$ ns, corresponding to a violation over 338 standard deviations. Furthermore, our design is scalable to even narrower windows by employing higher-end FPGA chips with higher clocks frequencies. We expect our design to be useful for the efficient characterization of many quantum optics and quantum information experiments.

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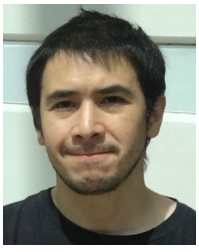

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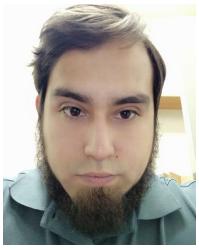

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