Impacts of Grid Voltage Harmonics Amplitude and Phase Angle Values on Power Converters in Distribution Networks

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ABSTRACT Motor drive systems based on diode-rectifier are utilised in many industrial and commercial applications due to their cost-effectiveness and simple topology. However, these diode rectifier-based systems can be affected by power quality and harmonics in distribution networks. Thus, this paper investigates the impact of grid voltage harmonics on the operation of power converters with three-phase diode rectifier using mathematical formulation of the drive voltage and current harmonics based on grid voltage harmonics. Simulation analysis and practical tests have been then carried out to validate the mathematical equations and the impact of grid voltage harmonics on the power converter harmonics. The results illustrate that even a small amount of grid voltage harmonics (around 4%) could significantly impact the input current harmonic contents of the three-phase diode rectifier. It is also shown that the phase-angle of grid voltage harmonics plays a crucial role to improve or deteriorate the input current harmonics of the power converters. In the next step, the optimum condition of grid voltage harmonics to minimise the input current harmonics has been evaluated and verified based on different grid codes. Finally, a harmonic mitigation technique in multi-drive systems using Electronic Inductor is proposed to mitigate the current harmonics at the PCC.

INDEX TERMS Distorted grid, distribution networks, total harmonic distortion, three-phase rectifier, voltage harmonics.

I. INTRODUCTION

In recent years, a higher installation level of nonlinear power electronics-based devices, such as Adjustable Speed Drives (ASDs), computers, and LED lighting, has become noticeable in residential, commercial, and industrial distribution networks [1]. A similar trend can be seen with the penetration level of renewable energy sources, such as solar power [2]. Thus, utility companies have become more concerned about harmonic distortion in the system, which could lead to higher losses, transformer temperature rise, and grid instability issues [3]. It is estimated that more than 40% of the global electrical energy is consumed by motor drives [4].

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This has led manufactures to utilise power electronic-based devices in motor drives, such as ASDs, to improve the efficiency and energy conservation of this significant part of loads [5]. In the literature, researchers have investigated the impact of the increased utilisation of nonlinear loads on the distribution networks. For instance, it has been shown in [6]–[8] that the installation of low quality Compact Fluorescent Lamps (CFLs) could increase the voltage distortion at the medium voltage level and lead to more harmonics-related power loss [8]. The impact of installing residential solar photovoltaic (PV) on the grid voltage distortion has been investigated in [9], [10]. It has been shown in [10] that in a microgrid, which is supplied by a photovoltaic station, replacing 30% of the conventional incandescent lamps by CFL could result in 8% THD_v. The field measurements of

typical residential distribution systems presented in [11] show that the average THD_v was about 4.7% with 45% of the feeders having THD_v above 5%.

Typically, ASDs are designed based on front-end and rear-end power conversion stages, where the Front-end converts the AC voltage to DC, and the Rear-end converts the DC voltage back to the desired AC [12]. A DC-link capacitor is usually employed to maintain a low-ripple DC voltage. Although Voltage Source Inverter (VSI) is commonly utilised in the rear-end [13], different topologies can be used at the front-end stage. In [14]–[16], an active front-end is proposed to improve the quality of the input current by shaping it close to an ideal sinewave signal. However, conventional three-phase Diode Rectifiers (DR) are still used as front-end for a broad range of ASD systems due to their simplicity, reliability, and low cost [17]. Additionally, international standards allow a relatively high level of current Total Harmonic Distortion (THD_i) emitted by three-phase rectifier systems. For instance, according to IEC61000-3-12 Table-4, the THD_i is permitted up to 48% for a system with a current of 16-75 Amps per phase [18]. However, there is still a lack of investigation about the behaviour and harmonic emission of ASDs under the impact of grid voltage distortion.

Authors in [19], [20] have investigated the input current harmonics of ASDs under grid voltage unbalance and sag conditions. A high level of voltage unbalance could lead the conventional three-phase rectifier to operate in single-phase mode, which generates a high amount of current harmonics [20]. In [21], [22], the current harmonics emission of three-phase diode rectifiers has been investigated at the system level. The simulation results in [22] show that the phase-angle of current harmonics is important for harmonic cancellation at the system level. In [23], the power quality issues in mining industry grids have been analysed. It has been shown that the grid impedance influences the current harmonic emission of nonlinear loads. Application of Electronic Inductor (EI) has been proposed in [24], [25] to mitigate the current harmonics in a multi-unit system,. Similarly, it has been shown in [25] that the input current THD_i of a multi-unit system can be dropped to 30% by using EI.

The reviewed literature indicates that there is a research gap in analysis of the impact of grid voltage harmonics on the input current of ASDs with three-phase diode rectifier. Thus, different cases of voltage harmonics at the PCC are considered in this paper to perform a comprehensive analysis in that area. For that aim, first, mathematical formulations of the rectified voltage, inductor current, and input currents in a distorted grid are presented. Then, simulation study and practical experiments are carried out to examine the impact of voltage harmonics on ASD's current harmonics emission. The results show that a small amount of grid voltage harmonics could have a high impact on the generated current harmonics at the drive rectifier input. Finally, a harmonic mitigation technique using EI is proposed to mitigate the current harmonics generated by conventional drives.

The main contributions of the paper can be mentioned as follows:

- Propose a mathematical model to calculate the rectifier voltage and input currents under the distorted grid.
- Evaluate the impact of both magnitude and phase-angle of grid voltage harmonics on the current harmonics emission of a motor drive with three-phase diode rectifier front-end. This is done by considering different scenarios and the permissible voltage harmonics allowed by various international standards.
- Propose a mitigation technique using an Electronic Inductor to reduce harmonics generated by motor drives with conventional three-phase diode rectifier.

This paper is organised as follows: harmonic analysis in the distorted grid is discussed in the next section. Section III then presents the impact of voltage harmonic order, magnitude, and phase-angle on the power converter. Impact of voltage harmonics on the current harmonic emission is then discussed in Section IV. Section V presents a harmonic mitigation technique followed by discussions highlighting the significant outcomes of the work in Section VI. Finally, Section VII concludes the study.

II. HARMONIC ANALYSIS IN A DISTORTED NETWORK
High penetration of nonlinear loads in the distribution network can create voltage harmonics at the PCC due to the interaction between their high level of current harmonics and the network impedance. This voltage distortion could then impact other sensitive loads such as power electronic-based devices. One of these devices is the conventional three-phase diode rectifier with a passive filter, which is a common topology for three-phase ASD systems as shown in Fig. 1 (a). The presence of voltage harmonics at the PCC (shown in Fig. 1 (b)) affects the rectified voltage (v_{rec}) as shown in Fig. 1 (c) for the case of 4% of 7th harmonic with phase-angles 0° and 180° compared with the base case of no harmonics. This change in the rectified voltage can then impact the generated current harmonics. Additionally, voltage harmonics could shift the conductivity of the diode rectifier, which changes the current conduction time at each phase. As a result, the Displacement Power Factor (DPF) of the converter will be impacted. Thus, this section first presents a mathematical formulation for the rectified voltage and then validates them with simulation results. Then, the equations of inductor current and grid currents of the drive are presented and validated by simulation results.

A. MATHEMATICAL FORMULATION OF THE RECTIFIED VOLTAGE
The PCC voltage at a Low Voltage (LV) distribution network with distortion can be presented as the sum of fundamental voltage (V_1) and harmonic voltage (V_h) as shown in Fig. 1 (a). In this study, voltage harmonics magnitudes are considered less than 5% to comply with international standards such as IEEE Std 519, where voltage THD and
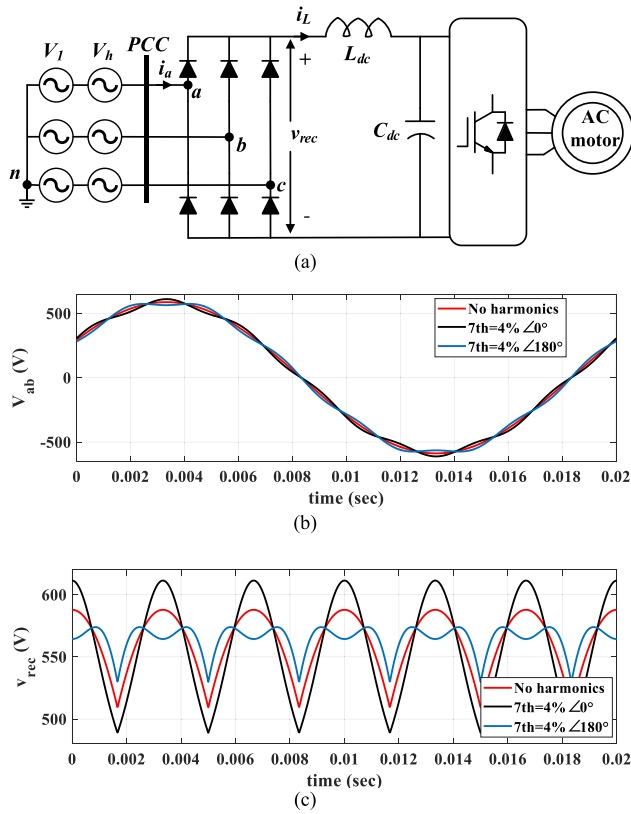
FIGURE 1. Conventional motor drive with diode rectifier under the presence of grid voltage harmonics: (a) circuit diagram, (b) PCC voltage (v_{ab}), and (c) rectified voltage.

individual harmonics are limited to 8% and 5%, respectively [26]. Additionally, to evaluate the impact of harmonic phase-angle, the phase-angle of current or voltage harmonic with respect to the fundamental voltage is used. As defined in IEC 61000-3-12 [18], the positive zero crossing (transition from negative to a positive value) of the fundamental voltage is used as the reference. Thus, the phase "a" voltage at the PCC is as given in (1).

$$v_{an} = V_m \sin{(\omega_0 t)} + \sum_{h=2}^{\infty} V_h \sin{(h\omega_0 t + \theta_h)} \quad (1)$$

where V_m and ω_0 are the peak magnitude and the angular frequency of the fundamental voltage, and V_h and θ_h are the peak
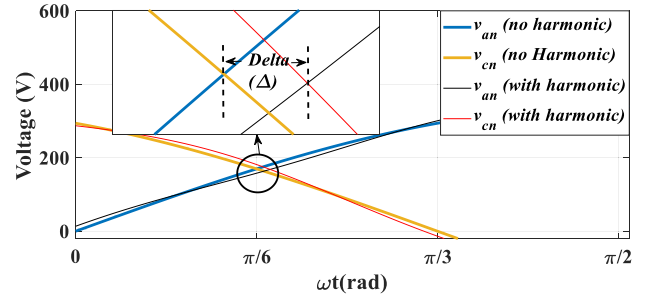

FIGURE 2. The phase delay (Δ) caused by the voltage harmonics phase-angle.

and phase-angle of the voltage harmonic order h. The Fourier series of v_{rec} considering voltage harmonics at the AC-side can then be calculated as given in (2).

$$v_{rec} = A_0 + \sum_{n=1}^{\infty} (A_n \cos{(6n\omega_0 t)} + B_n \sin{(6n\omega_0 t)}) \quad (2)$$

The coefficient A_0 can be calculated as given in (3).

$$A_0 = \frac{3\sqrt{3}V_m}{\pi} cos\Delta + \sum_{h=2}^{\infty} \frac{12V_h}{\pi h}$$
$$\times \sin{\left(\frac{2\pi}{3}h\right)} \sin{\left(\frac{\pi}{6}h\right)} \cos{(h\Delta + \theta_h)} \quad (3)$$

where Δ is the phase delay (measured in radian) caused by the harmonic phase-angle, as shown in Fig. 2. Other coefficients A_n and B_n in (2) can be similarly calculated from (4) and (5), as shown at the bottom of the page. Fig. 2 indicates that the voltage harmonics phase-angle could shift the voltage crossing between phases, which will then shift the conductivity of each phase by Δ. This can also impact the DPF of the converter and the phase-angles of input current harmonics.

To calculate Δ, (6) needs to be first solved to find $\omega_0 t_0$, and then (7) to find Δ.

$$\sqrt{3}V_m \cos{\left(\omega_0 t_0 + \frac{\pi}{3}\right)} +$$
$$+ \sum_{h=2}^{\infty} [2V_h \cos{\left(h\omega_0 t_0 + \theta_h + \frac{h\pi}{3}\right)} \sin{\left(\frac{h\pi}{3}\right)}] = 0 \quad (6)$$

$$\Delta = \omega_0 t_0 - \pi/6 \quad (7)$$

$$A_n = \frac{3\sqrt{3}V_m cos{(n\pi)}}{\pi\left(36n^2 - 1\right)}\left[(6n-1)\cos{(6n\Delta + \Delta)} - (6n+1)\cos{(6n\Delta - \Delta)}\right]$$
$$+ \frac{12}{\pi} \sum_{h=2}^{\infty} V_h cos{(n\pi)} \sin{\left(\frac{2\pi}{3}h\right)} \sin{\left(\frac{\pi}{6}h\right)} \left[\frac{cos{(6n\Delta + h\Delta + \theta_h)}}{6n+h} - \frac{cos{(6n\Delta - h\Delta - \theta_h)}}{6n-h}\right] \quad (4)$$

$$B_n = \frac{3\sqrt{3}V_m cos{(n\pi)}}{\pi\left(36n^2 - 1\right)}\left[(6n-1)\sin{(6n\Delta + \Delta)} - (6n+1)\sin{(6n\Delta - \Delta)}\right]$$
$$+ \frac{12}{\pi} \sum_{h=2}^{\infty} V_h cos{(n\pi)} \sin{\left(\frac{2\pi}{3}h\right)} \sin{\left(\frac{\pi}{6}h\right)} \left[\frac{sin{(6n\Delta + h\Delta + \theta_h)}}{6n+h} - \frac{sin{(6n\Delta - h\Delta - \theta_h)}}{6n-h}\right] \quad (5)$$

B. VALIDATION OF VOLTAGE EQUATION WITH SIMULATION RESULTS

To validate the analytical equation for v_{rec}, the voltage magnitudes calculated from (2) are compared with simulation results in this section. Thus, the system in Fig. 1 (a) has been modelled in MATLAB Simulink, where the PCC voltage is distorted with 4% of the 7th harmonic with a phase-angle of 180°. For this case, Fig. 3 confirms that the time-domain waveforms of v_{rec} in both analytical and simulation results are similar. Thus, the accuracy of (2) to find v_{rec} in a distorted grid is verified. In the next stage, the input and inductor current harmonics of the power converter affected by grid voltage distortions is analytically evaluated.
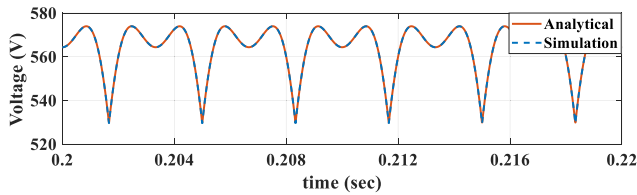

FIGURE 3. Comparison between analytical and simulation waveforms of v_{rec} when 4% of 7th harmonic with 180° phase-angle is present at the PCC voltage.

C. INDUCTOR AND INPUT CURRENTS EQUATIONS

To calculate the phase "a" input current (shown as i_a in Fig. 1 (a)) under the presence of grid voltage harmonics, the inductor current (i_L) must be first calculated. With the practical assumption of Continuous Conduction Mode (CCM) operation, i_L can be calculated in each harmonic frequency by dividing voltage by the inverter harmonic impedance. The impedance seen from the rectifier output at the angular frequency $6n\omega_0(Z_n)$ can be calculated from (8).

$$Z_n = j6n\omega_0 L_{dc} + \frac{R_{Load}}{1 + j6n\omega_0 C_{dc} R_{Load}} \quad (8)$$

where R_{Load} represents the rear-end inverter impedance for low order harmonics, which can be determined based on the load power consumption. As the inductor current harmonic at each frequency is v_{rec} divided by Z_n in that frequency, its Fourier series can be calculated using (2) and (8) as given in (9).

$$i_L = \frac{A_0}{|Z_0|} + \sum_{n=1}^{\infty} \frac{A_n}{|Z_n|} \cos\left(6n\omega_0 t - \theta_{Z_n}\right)$$
$$+ \frac{B_n}{|Z_n|} \sin\left(6n\omega_0 t - \theta_{Z_n}\right) \quad (9)$$

The Fourier series of diodes switching function for phase "a" can be obtained as given in (10).

$$s_{da} = \frac{4}{\pi} \sum_{k=1,3,5\ldots}^{\infty} \frac{\cos\left(k\pi/6\right)}{k} \sin\left(k(\omega_0 t - \Delta)\right) \quad (10)$$

This equation represents a 120° conductivity of i_L seen at the grid-side current of i_a ($i_a = s_{da} i_L$). Thus, the Fourier series of i_a can be calculated by multiplying (9) and (10) as given in (11), as shown at the bottom of the page. It should be noted that the inverter-side current harmonics in Fig. 1 (a) are based on Pulse Width Modulation (PWM) with high switching frequency (5-24 kHz). These high-order harmonics can be neglected in this research as they tend to circulate mainly through the DC-link capacitor. To illustrate, Fig. 4 presents a circuit diagram of a conventional drive, where the inverter-side is represented by the resistor (R_{load}) to model the load power and the current source to model the high-frequency harmonics generated by the inverter PWM switching pattern.

As shown in Fig. 4, this current can be calculated by multiplying load-side currents ($i_{load,a}$, $i_{load,b}$, $i_{load,c}$) by inverter switching functions (s_a, s_b, s_c). Using Fourier series of load currents and switching functions for the case of sine-triangular PWM, i_{inv} has been calculated in [27]. It has been shown that, besides the DC component, represented by R_{Load}, other harmonics of i_{inv} are concentrated around the switching frequency and its multiples which is represented as i_{inv-h}. As can be seen in Fig. 4, the high-frequency components of i_{inv} circulate through the DC-link capacitor C_{dc} with a low high-frequency impedance (shown as "low Z_{HF}") rather than the high-impedance path through the inductor (shown as "high Z_{HF}"). Hence, the impact of high-frequency harmonics of i_{inv} on the grid-side low-order current harmonics can be neglected in this study. Therefore, only R_{load} is considered in (8). In the next section, the accuracy of (9) and (11) in calculating the inductor and grid currents of the power converter in a distorted grid is verified with simulation results.

$$i_a = \frac{4A_0}{\pi |Z_0|} \sum_{k=1,3,5\ldots}^{\infty} \frac{\cos\left(k\pi/6\right)}{k} \sin\left(k(\omega_0 t - \Delta)\right)$$
$$+ \frac{4}{\pi} \sum_{n=1}^{\infty} \sum_{k=1,3,5\ldots}^{\infty} \frac{A_n \cos\left(k\pi/6\right)}{k |Z_n|} \cos\left(6n\omega_0 t - \theta_{Z_n}\right) \sin\left(k(\omega_0 t - \Delta)\right)$$
$$+ \frac{4}{\pi} \sum_{k=1,3,5\ldots}^{\infty} \sum_{n=1}^{\infty} \frac{B_n \cos\left(k\pi/6\right)}{k |Z_n|} \sin\left(6n\omega_0 t - \theta_{Z_n}\right) \sin\left(k(\omega_0 t - \Delta)\right) \quad (11)$$
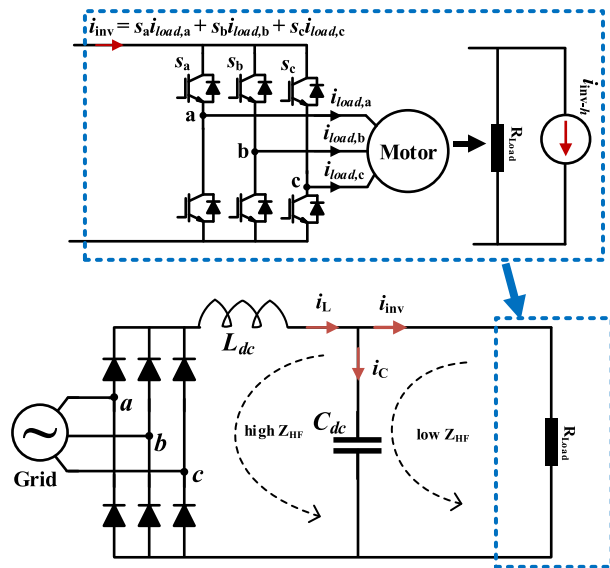
FIGURE 4. A conventional converter with a rear-end inverter, showing low- and high-impedance paths for high-frequency load-side currents circulation.

D. VALIDATION OF CURRENTS EQUATIONS WITH SIMULATION RESULTS

To validate (9) and (11), a comparison of analytical equations with simulation results has been performed, where the grid voltage had a distortion of 4% of the 7th harmonic with 180° phase-angle. In this case, Fig. 5 confirms that the time-domain waveforms of both analytical and simulation results of i_L and i_a are similar. Thus, the accuracy of (9) and (11) to find the currents values is validated and they can be used to evaluate the effect of network voltage harmonics on the converter current harmonics emission. The next
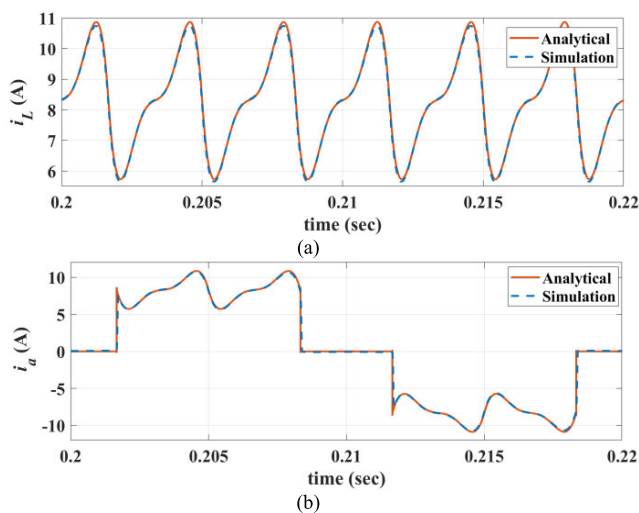

FIGURE 5. Comparison between analytical and simulation time-domain current waveforms: (a) i_L, and (b) i_a.

section investigates the impact of different characteristics of the PCC voltage on the rectified voltage ripple.

III. IMPACT OF PCC VOLTAGE HARMONICS CHARACTERISTICS ON THE RECTIFIED VOLTAGE

The impact of different characteristics of the PCC voltage harmonics including their magnitude, order, and phase-angle on the rectified voltage is investigated in this section.

A. IMPACT OF PCC VOLTAGE HARMONICS ON THE RECTIFIED VOLTAGE

The phase-angle of the PCC voltage harmonics is unpredictable and rely in different aspects such as grid impedance characteristics. Additionally, the current harmonics magnitude and phase-angle generated by the non-linear loads connected to the PCC affect the phase-angle of the PCC voltage harmonics. Therefore, with a fundamental of 240 V and 50Hz, 10 different cases of added distortions to the PCC voltage are considered in this section. The details of voltage harmonics and v_{rec} average values ($V_{rec,avg}$) for all the cases are tabulated in Table 1, where case 1 is with no harmonics for the comparison purpose. From Table 1, the average values of the rectified voltage for all the cases are similar with less than 1% change compare to case 1. Nevertheless, using (2), the ripple magnitude of v_{rec} (V_{ripple}) for all the cases have been calculated as shown in Fig. 6 (a). As can be seen from Fig. 6 (a), although the voltage harmonics at the PCC for all the cases are less than 5% (12 V_{rms}), their impact on V_{ripple} could be significant. It should be noted that any change in the V_{ripple} can also impact the inductor current ripple. Consequently, the AC-side currents harmonics can also be affected as they represent the inductor current with 120° conductivity for each phase.

TABLE 1. Details of Investigated Cases.

Case	PCC Voltage Harmonics (%)	$V_{rec,avg}$ (V)
1	No harmonics	561
2	$V_{h5} = 4\angle 0°$	557
3	$V_{h5} = 4\angle 180°$	566
4	$V_{h5} = 4\angle 90°$	559
5	$V_{h5} = 4\angle 270°$	560
6	$V_{h7} = 4\angle 0°$	558
7	$V_{h7} = 4\angle 180°$	564
8	$V_{h13} = 4\angle 180°$	560
9	$V_{h5} = 2\angle 0°, V_{h7} = 2\angle 180°$	561
10	$V_{h5} = 2\angle 180°, V_{h7} = 2\angle 0°$	562

The changes in V_{ripple} compared with case 1 (ΔV_{ripple}) are shown in Fig. 6 (b). It can be seen from this figure that cases 2, 7, and 9 have the lowest voltage ripple with significant reduction by 56%, 44%, and 52% compared with case 1, respectively. Thus, these cases are expected to have lower input current harmonics due to having lower V_{ripple} compared to case 1. On the other hand, cases 3, 6, and 10 have around 54% higher V_{ripple} compared to case 1. Therefore,
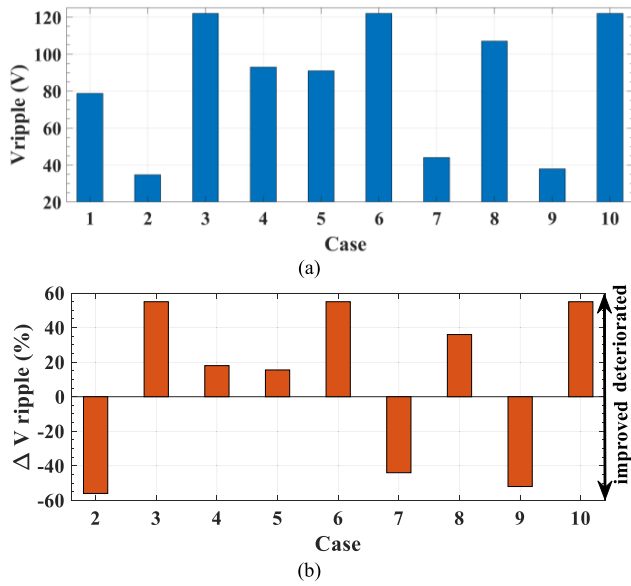
FIGURE 6. Rectified voltage ripple for all the ten cases: (a) the value in each case, (b) percentage change compared to case 1.
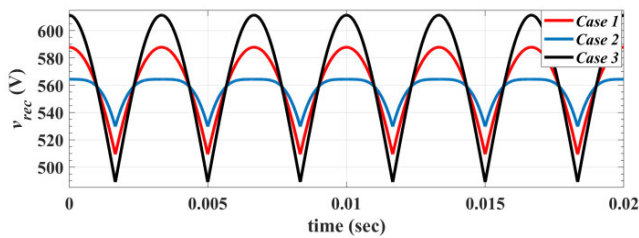

FIGURE 7. The rectified voltage (v_{rec}) for cases 1, 2, and 3.

B. IMPACT OF VOLTAGE HARMONICS PHASE-ANGLE ON DPF

It is worth mentioning that the voltage harmonic phase-angle could also affect the DPF of the converter when Δ is nonzero, which happens at all voltage harmonic phase-angles except 0° and 180°. In this analysis, cases 4 and 5 have voltage harmonic phase-angles of 90° and 270°. Using (7), Δ values are calculated 2.25° and −2.25° for cases 4 and 5, respectively. Thus, both V_{ripple} and DPF are expected to be impacted in these cases by changing the phase-angles of the 5th harmonic. To evaluate that, Fig. 8 shows the simulation signals of i_a in cases 1, 4, and 5. It can be seen that there is a phase shift caused by Δ for cases 4 and 5 compared to case 1. In case 4, due to a positive Δ, the input current is lagging compared to case 1. On the other hand, the input current of case 5 is leading compared to case 1 due to the negative Δ. Consequently, the DPF of case 4 is reduced to 0.970 compared to 0.986 in case 1, while it is improved to 0.994 in case 5. In the next section, the optimum condition of the distorted grid to minimize V_{ripple} is investigated.
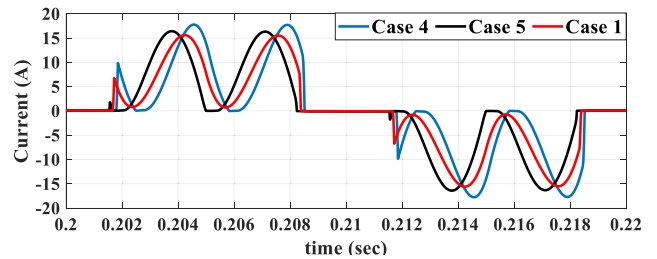

FIGURE 8. Simulation results of i_a waveforms of cases 1, 4, and 5.

C. OPTIMUM V_{ripple} BASED ON GRID CODES

To evaluate the optimum condition of voltage harmonic magnitude, order, and phase-angle, an optimization technique needs to be implemented. The aim of the optimization is to find the minimum and maximum V_{ripple} considering the permissible harmonic levels at the PCC allowed by different international standards. Based on (2), v_{rec} consists of a DC component of A_0 and harmonic components at angular frequencies $6n\omega_0$ with coefficients A_n and B_n as described in (4) and (5). Thus, the harmonic magnitudes can be calculated as given in (12).

$$V_{rec,n} = \sqrt{A_n^2 + B_n^2} \quad n = 1, 2, 3, \ldots \quad (12)$$

The idea to optimize V_{ripple} is to minimize or maximize all the $V_{rec,n}$ values. To illustrate, when all the individual harmonic magnitudes of v_{rec} are minimized (maximized), it is expected that the observed V_{ripple} is also minimized (maximized). The optimization target is to search for a set of grid-side voltage harmonic values (V_h and θ_h) over the permissible limits to minimize (maximize) $V_{rec,n}$, so that V_{ripple} can be minimized (maximized). The objective function (F_{obj}) can then be defined as either $F_{obj-min}$ or $F_{obj-max}$ for

these cases are expected to have the highest level of input current harmonics.

These results show that the level of voltage harmonics at the PCC is similar in all the cases. However, the variation in V_{ripple} is different in each case, which could be related to the voltage harmonic phase-angle. For example, the harmonic distortion is 4% of the 5th harmonic in both cases 2 and 3. However, the difference in their voltage harmonic phase-angles leads to different impact on V_{ripple}. To illustrate that, Fig. 7 presents the rectified voltage for cases 1, 2, and 3.

As can be seen from Fig. 7, in case 2, the voltage ripple is reduced significantly compared to case 1 (34 V versus 78 V), showing a flat peak. In contrast, V_{ripple} of case 3 is considerably higher than case 1 (121 V versus 78 V). Thus, the phase-angle of the 5th harmonic has a significant impact on V_{ripple}. The scenario for the 7th harmonic is the opposite, where V_{ripple} is reduced when the harmonic phase-angle is 180° as shown in Fig. 6 (a) for case 7. The V_{ripple} has dropped to 44 V, which shows a reduction of 44% compared to case 1. In contrast, V_{ripple} increases by around 54% when the harmonic phase-angle is 0° as shown in Fig. 6 (a) for case 6.

minimum or maximum V_{ripple} as given in (13).

$$F_{obj-min} = \sum_n W_n V_{rec,n}^2$$

$$F_{obj-max} = \sum_n -W_n V_{rec,n}^2 \qquad (13)$$

where a constant weight W_n is given to each square $V_{rec,n}$ for prioritization and more flexibility [28]. To find the optimal solution for the objective function, MATLAB optimization function "fmincon" is used. The limits of voltage harmonics magnitudes and phase-angles, and THD_v are set as the constraints based on the grid codes limits. Two international standards IEEE-519 [26] and IEC 61000-3-12 (testing conditions) [18] have been considered in this section to define the harmonics limits as described in Table 2. This table also presents the optimization results for the harmonics magnitudes and phase-angles to minimize or maximize V_{ripple}.

TABLE 2. Voltage Harmonics Limits Based on IEEE and IEC Standards and Their Optimum Values to Minimize or Maximize V_{ripple}.

Standard	V_h	limits	Optimum V_h to minimize V_{ripple}	Optimum V_h to maximize V_{ripple}
IEEE-519	V_{h5}	5%	$5\angle 0°$	$5\angle 180°$
	V_{h7}	5%	$1\angle 180°$	$5\angle 0°$
	V_{h11}	5%	0	$3.2\angle 180°$
	V_{h13}	5%	$1\angle 0°$	$2\angle 180°$
IEC 61000-3-12	V_{h5}	1.5%	$1.5\angle 0°$	$1.5\angle 180°$
	V_{h7}	1.25%	$1.25\angle 180°$	$1.25\angle 0°$
	V_{h11}	0.7%	$0.7\angle 0°$	0
	V_{h13}	0.6%	$0.6\angle 0°$	0

The optimization results of the minimum and maximum V_{ripple} for both standards using calculated harmonics magnitudes and phase-angles in Table 2 are presented in Fig. 9. Figs. 9 (a) and (b) show the v_{rec} waveforms for maximum and minimum V_{ripple} based on the permissible limits in IEEE-519 and IEC 61000-3-12 standards, respectively, and compare them to the case of no harmonics (case 1). Fig. 9 (c) shows the calculated V_{ripple} values, whereas ΔV_{ripple} compared to case 1 is presented in Fig 9 (d). As it can be seen from the figures, the harmonics phase-angle highly impacts the rectified voltage. For IEEE cases, V_{ripple} reaches a maximum of 156% higher than case 1, whereas its minimum is around 70% below case 1. On the other hand, as the permissible harmonic injection is lower in IEC case, ΔV_{ripple} shows less variation compared with case 1. Fig. 9 (d) shows that with IEC harmonics limits, a V_{ripple} of around 40% lower in the minimum case, or 40% higher in the maximum case compared with case 1 can be obtained. To evaluate the impact of grid voltage harmonics on rectifier voltage and power converter currents in a real-world scenario and verify the analytical and simulation results discussed so far, several practical lab tests have been performed and compared to simulation results as presented in the next section.
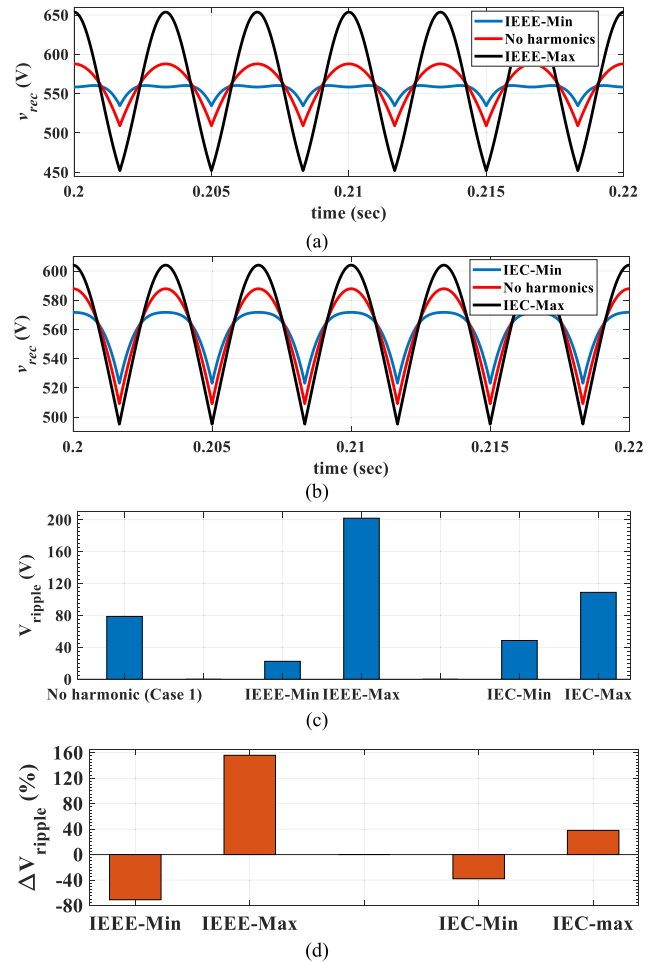

FIGURE 9. v_{rec} waveforms and V_{ripple} under different limits of the grid standards: (a) v_{rec} waveforms for IEEE cases, (b) v_{rec} waveforms for IEC cases, (c) V_{ripple}, (d) ΔV_{ripple} compared to case 1.

IV. IMPACT OF PCC VOLTAGE HARMONICS ON THE CURRENT HARMONICS EMISSION

As it was elaborated in the previous section, voltage harmonics at the PCC can highly impact the rectified voltage. Thus, input current harmonics and THD_i are also expected to be affected as they are related to the rectified voltage ripple. To investigate that, this section evaluates the behaviour of input current harmonics under the presence of PCC voltage harmonics with both simulation results and practical measurements. As the analytical equations were consistent with the simulation results in Section II, the practical measurements in this section are compared with the simulation results for further validation of the analytical results. Hence, a motor drive system with conventional three-phase diode rectifier similar to Fig. 1 (a) has been modelled using Matlab Simulink as shown in Fig. 10. AC voltage sources at different harmonic frequencies have been used to represent the grid distortion at the PCC in that frequency. Additionally, some practical tests were performed in the lab with the setup shown in Fig. 11. A grid simulator is used as the input source of ASD
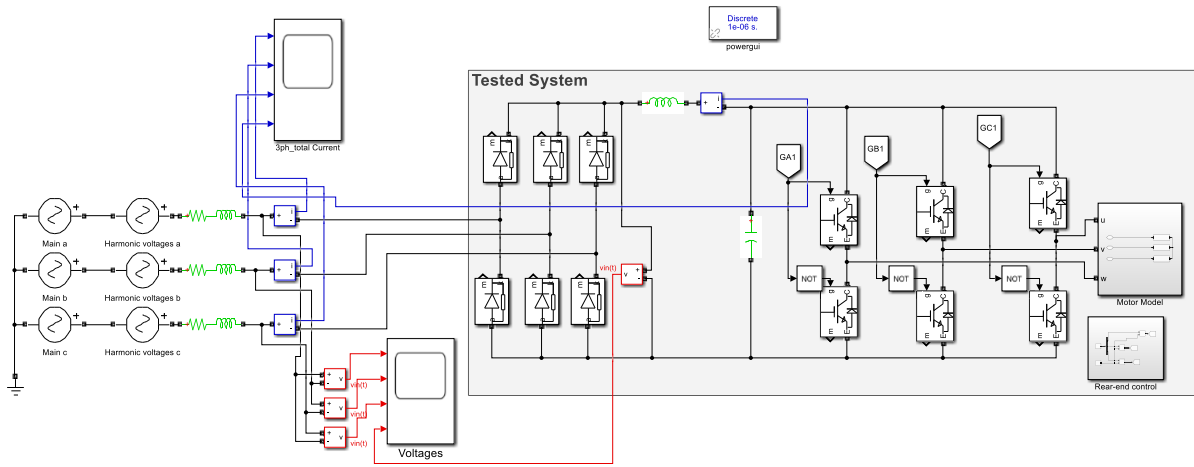
FIGURE 10. Simulink model for the tested ASD under the presence of voltage harmonics at the PCC.

to resemble a distorted grid to evaluate the analysed cases. A motor drive with conventional front-end (bridge diode with DC choke) and inverter rear-end connected to an induction motor coupled with a dc motor is used as the drive setup. Although the rated power of the drive is 7.5 kW, the test is conducted at a load level of 4.5 kW (60%).

A. GRID CURRENT HARMONICS AT DIFFERENT CASES OF PCC VOLTAGE HARMONICS

The 10 cases presented in Table 1 have been first tested using the Simulink model shown in Fig. 10. To validate the simulation results, practical measurements have been then conducted in the lab using the implemented setup shown in Fig. 11. The THD_i comparison of current between the practical measurements and the simulation results for all cases is presented in Fig. 12 which confirms that the THD_i values of phase "a" for all the cases are quite similar in the practical and simulation results. Fig. 12 (b) shows that in cases 2, 7, and 9, the THD_i is reduced significantly by around 45%-50% compared to case 1. On the contrary, the THD_i is increased in cases 3, 6, and 10 by 22%-30% compared
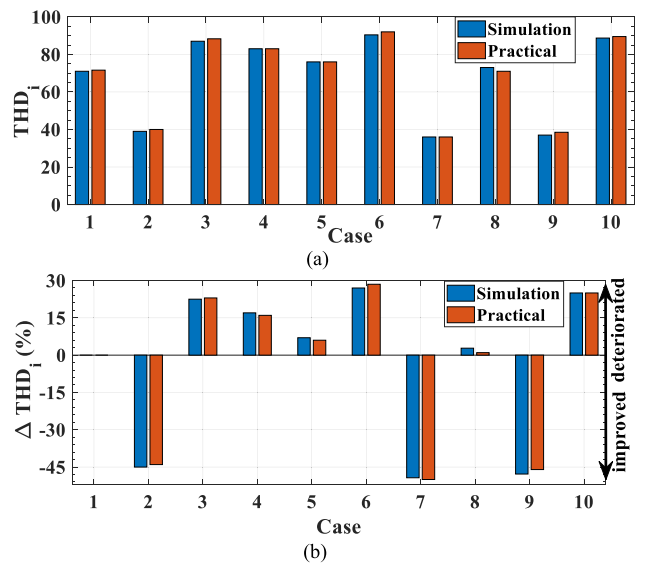

FIGURE 12. THD_i values of i_a for all 10 cases in simulation and practical results: (a) values, (b) percentage change compared to case 1.

to case 1 as can be seen in this figure. These results show that even a small percentage of voltage harmonics at the PCC can profoundly impact the input current harmonics of conventional drives. However, for higher order harmonics (13th or higher), the effect on the current harmonics is not as significant as lower orders (such as 5th and 7th) as shown in Fig. 12 (b) for case 8, where the THD_i is 73% and slightly higher than case 1.

The captured scope waveforms of grid-side currents and v_{rec} in cases 1-3 are presented in Fig. 13 and Fig. 14 for simulation and practical results respectively. These figures validate the consistency of the simulation results with the practical measurements. Moreover, these figures confirm that the phase-angle of the applied voltage harmonic can highly affect the input current shape and THD_i. To illustrate,
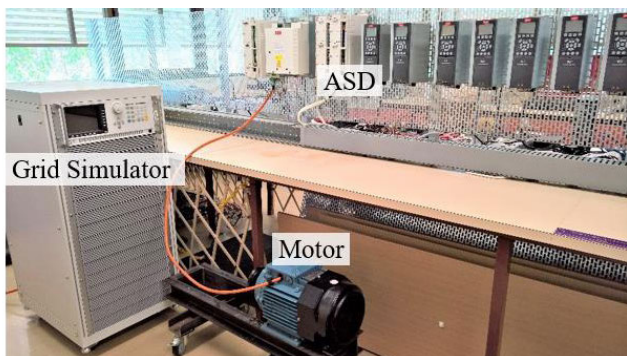

FIGURE 11. Lab setup of the ASD connected to a grid simulator as the distorted voltage source and an induction motor as the load.
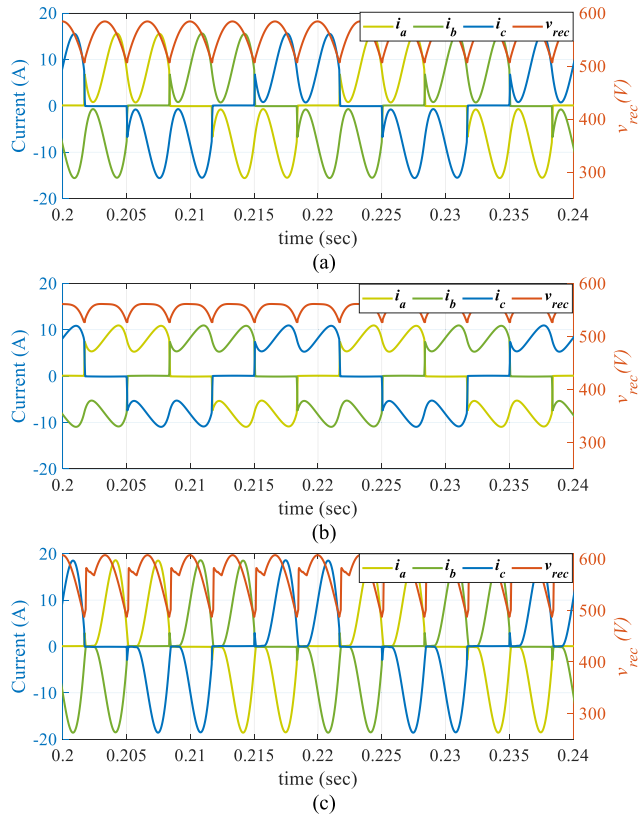
FIGURE 13. Simulation results of the three-phase input currents and v_{rec} in case: (a) 1, (b) 2, and (c) 3.

FIGURE 14. Practical measurements of the three-phase input currents and v_{rec} in cases: (a) 1, (b) 2, and (c) 3.

Fig. 13 (b) and Fig. 14 (b) show v_{rec} and the input three-phase currents of case 2 in both simulation and practical results respectively, where $V_{h5} = 4(\%)\angle 0°$ is added to the fundamental voltage. In this case, V_{ripple} is around 35 V, which is relatively low. Therefore, it can be seen that the input currents also operate at a low ripple, which reduces the THD$_i$ to 40% compared to 71% in case 1. On the other hand, when the voltage is distorted by adding $V_{h5} = 4(\%)\angle 180°$ to the fundamental component as per case 3, V_{ripple} is increased to around 120 V as can be seen in Fig. 13 (c) and Fig. 14 (c) for simulation and practical results respectively. Thus, the input currents operate at Discontinues Conduction Mode (DCM) with a high ripple, and a THD$_i$ of 88%.

B. GRID-SIDE CURRENT HARMONICS IN OPTIMUM CASES OF V_{ripple} BASED ON GRID STANDARDS LIMITS

This section examines the impact of voltage harmonics on current harmonics emission based on the grid codes limits. Hence, the results from Section III.C are applied to the power converter to evaluate the impact of these voltage harmonics on the grid-side current harmonics emission. For that aim, Fig. 15 (a) presents the THD$_i$ of i_a for both IEEE and IEC standards, whereas Fig. 15 (b) presents the THDi change compared to case 1. The results have been obtained from both simulation modelling and practical lab measurements with
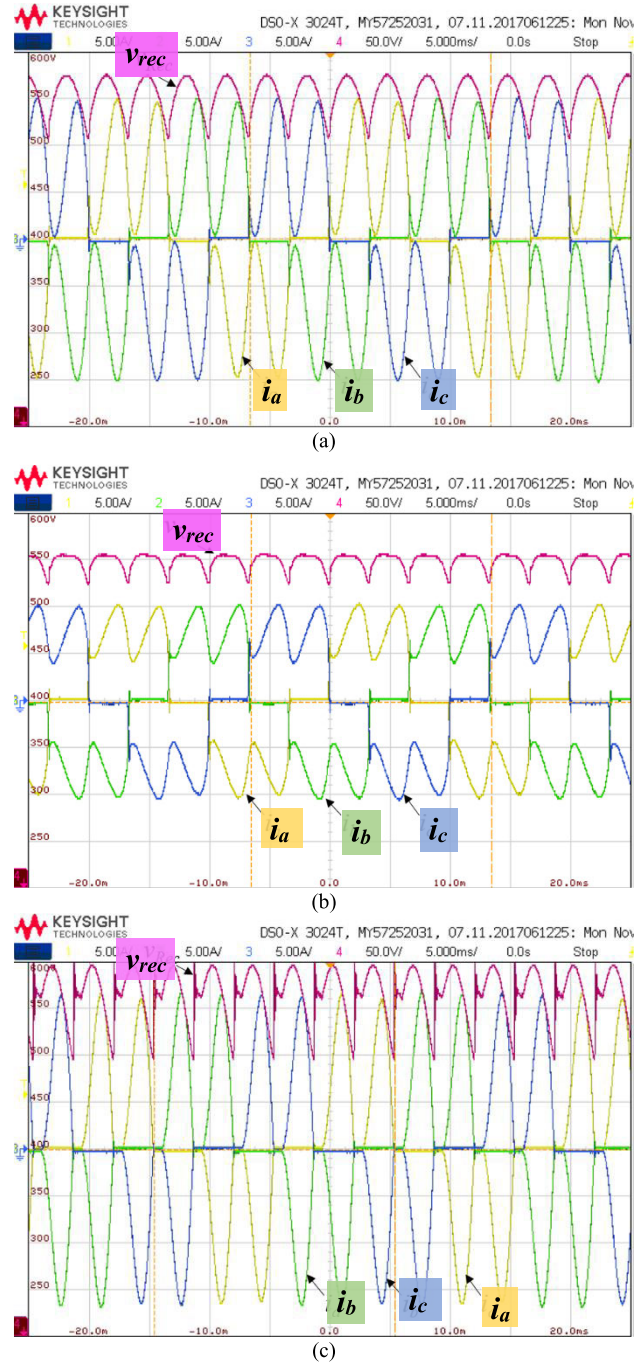
setting the PCC voltage harmonics. It can be seen from this figure that simulation and practical results are quite consistent with small error. The figure also indicates that even under the grid code limits, the impact of voltage harmonics phase-angle on the current harmonics is significant. Based on the limits of the IEEE-519 standard, the THDi can reach a minimum of 50% decrease or a maximum of 40% increase compared to case 1 with the calculated harmonics using the proposed optimisation method. As for the results of IEC 61000-3-12
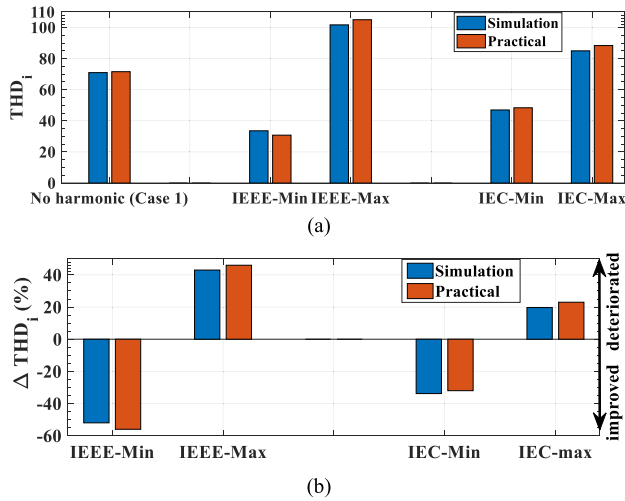
FIGURE 15. Optimum THDi under different grid codes condition in simulation and practical results: (a) values, (b) percentage change compared to case 1.
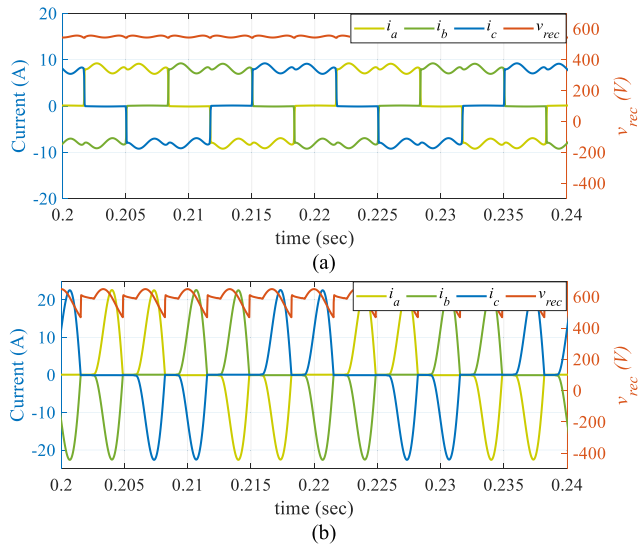

FIGURE 16. Simulation results of the three-phase input currents and v_{rec} in cases: (a) IEEE-Min, (b) IEEE-Max.

FIGURE 17. Practical measurements of the three-phase input currents and v_{rec} in cases: (a) IEEE-Min, (b) IEEE-Max.

voltage harmonic can highly affect the input current shape and THD$_i$.

V. MITIGATION OF CURRENT HARMONICS IN MULTI-DRIVES SYSTEMS

Considering the high impact of the distorted grid on the current harmonic emission of the motor drive with conventional three-phase diode rectifier, in this section a harmonic mitigation technique is proposed to mitigate the high harmonics generated by these type of motor drives. The concept of the proposed technique is based on using an Electronic Inductor (EI) in multi-drive systems to compensate current harmonics generated by the conventional drives, which has been presented in [25]. In contrast to the conventional three-phase diode rectifier, the EI is resilient against the fluctuations of grid harmonics; thus, it can preserve a fixed current harmonic emission, even under the distorted grid condition. Hence, in this section, a system of two units as shown in Fig. 18 (a) is considered to mitigate the harmonics generated by conventional unit (Unit 2).

Fig. 18 (b) shows phase "a" currents of the grid and input of both units. It can be seen that the EI current is a combination of a square-wave and ripple component. This

standard limits shown in Fig. 15 (b), the impact of the voltage harmonics phase-angle on the THDi is still significant, where it can be reduced by 30% or increased by 20% compared to case 1.

The captured scope waveforms of grid-side currents and v_{rec} in IEEE cases are presented in Fig. 16 and Fig. 17 for simulation and practical results, respectively. It can be seen from these figures that, in the case of IEEE-min, the currents waveforms are almost square waves with around 33% THDi, which shows a significant improvement compared to case 1. On the contrast, the currents waveforms in IEEE-max case are operated at DCM with a high THDi around 105%. These figures confirm that, even under the same permissible levels of harmonics (IEEE Std), the phase-angle of the applied
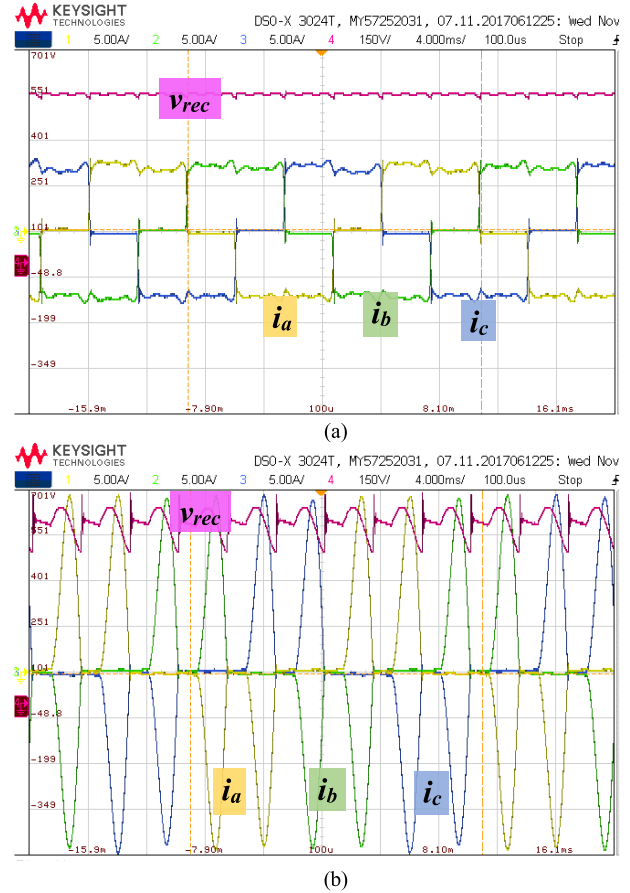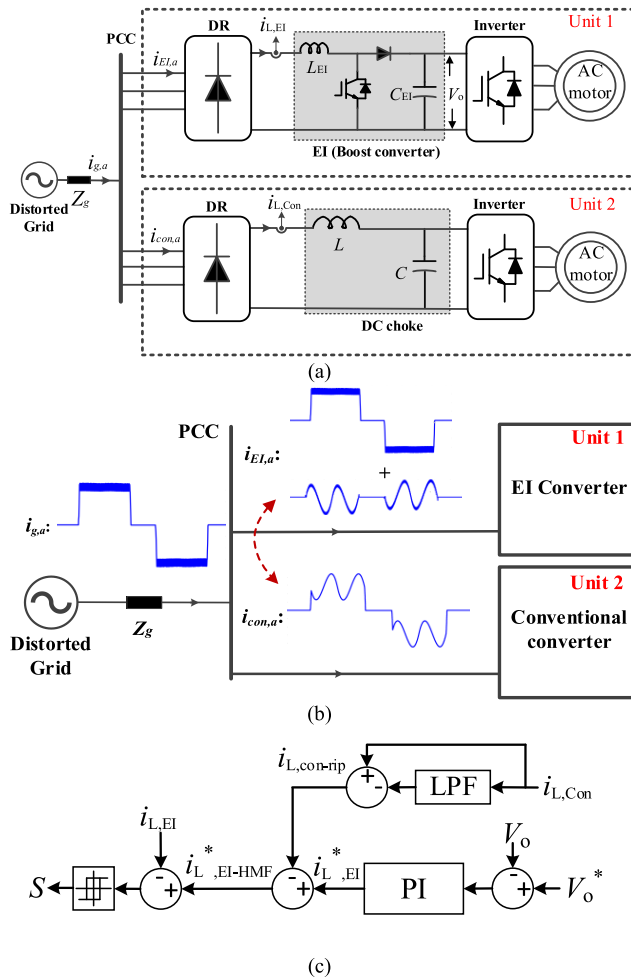
(a)

(b)

FIGURE 18. Proposed harmonic mitigation technique: (a) block diagram of the system showing Unit 1 (U1) equipped with an EI and Unit 2 (U2) with a passive filter (DC choke), (b) current components of the units, (c) the control system with PI and current hysteresis controllers.

(c)

(a)

(b)

FIGURE 19. Simulation results for phase "a" current when U1 mitigates harmonics generated by U2: (a) case 3, (b) IEEE-max case.

ripple component is reverse to the ripple component of Unit 2, so they cancel out each other. Thus, the grid side current can be obtained as a square-wave with a fixed THDi around 30%, which is the lowest THDi that can be observed from three-phase diode rectifier systems. The control concept of the proposed mitigation technique is shown in Fig. 18 (c). In this figure, the inductor current of Unit 2 is measured and then the ripple is subtracted from the current reference of the inductor current of EI unit, which leads the EI to mitigate the ripple of Unit 2. In order to achieve a proper tracking of $i_{L,EI-HMF}^*$ and maintain a desired output voltage of the EI (V_o), a fast and reliable controller is required. Hence, a PI controller is used for the voltage control and a hysteresis controller is adopted as a current controller. The concept of the hysteresis controller is based on regulating the current between the hysteresis bands of the current reference. The hysteresis controller is relatively fast, which makes it suitable for harmonics mitigation function.
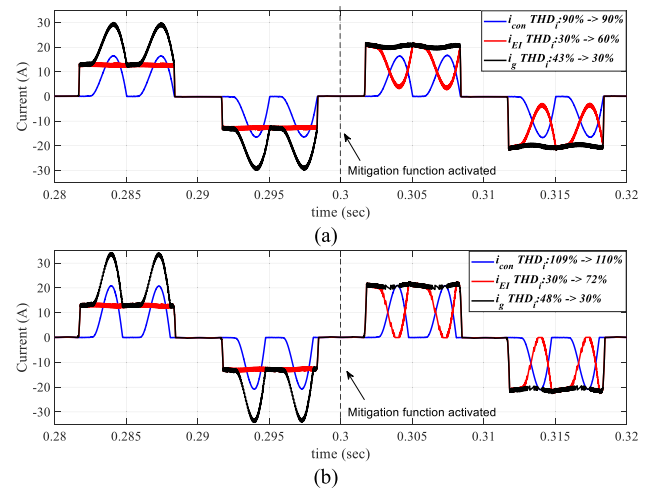
To mitigate the high level of harmonics generated by conventional rectifier under the presence of voltage harmonics at the PCC, Case 3 and IEEE-max case from the previous section are considered here. These two cases have the highest THDi with 90% and 105% respectively. Fig. 19 presents the simulation results for both cases, where the mitigation function of U1 is activated at 0.3 sec. It can be seen from this figure that, after activating the mitigation function, U1 compensates the harmonics generated by U2, which changes the shape of grid side current (i_g) to a square-wave with 30% THDi. Although the THDi of U2 stays around 90% in case 3 as shown in Fig. 19 (a), the THDi of the grid side current is significantly reduced from 43% to 30%. Fig. 19 (b) shows similar results for IEEE-max case, where the grid side current THDi is reduced to 30% compared to 48% before activating the mitigation function. These results confirm the robustness and effectiveness of the EI to mitigate conventional rectifier harmonics.

To show the impact of the proposed harmonics mitigation technique on the primary function of the drive system, the system response to the activation of the mitigation function is analysed. Fig. 20 shows the output voltage (V_o), the inductor current, and phase "a" inverter side current of the EI unit (U1). As it can be seen from the figure, after the mitigation function activated at 0.3 sec, the inductor current start compensating the harmonics of U2. However, the output voltage and inverter side current have not been affected by the activation of the mitigation function. Thus, the proposed technique can mitigate the harmonics generated by U2 while maintaining the desired operation of the motor drive system.

VI. DISCUSSION
Different types of linear and nonlinear loads in distribution networks generate reactive power, network disturbances, and harmonics. High penetration of power electronics converters has the potential to degrade the power quality of
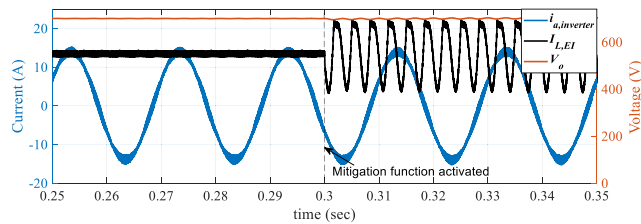
FIGURE 20. Simulation results for output voltage (V_o), inductor current, and phase "a" inverter side current of U1.

grids by introducing harmonics and strong resonances, which pose severe risks to the distribution networks and equipment connected to them. International standardisation committees such as IEC and IEEE have developed different power quality standards such as IEC 61000-3-2 and IEC 61000-3-12 to control harmonic emissions in the grids. However, these standards are defined to control harmonic emission at product level based on test conditions such as setting the grid voltage with or without any background harmonic for any product tests. Other standards such as IEEE 519 are based on demand current at the system level without considering the impact of grid voltage harmonics on power converters. Thus, this paper presents that the impact of the grid voltage harmonics on three-phase diode rectifiers could be significant. Moreover, the power quality of the grid can be predictable based on grid voltage harmonics – amplitude and phase-angle - as the power quality of grids changes due to load variations.

VII. CONCLUSION

In this paper, the impact of grid voltage distortion on power converter current harmonics emission has been investigated. For that aim, ASDs with conventional diode rectifier has been considered to represent the power electronic system. A mathematical formulation of the rectified voltage, inductor current, and input currents of a three-phase diode rectifier is derived under the presence of voltage harmonics at the PCC. Different cases of voltage harmonics are then considered in the analysis to investigate the behaviour of the rectified voltage and the input current harmonics. The results show that the presence of even a small level of voltage harmonics (4%) at the PCC can change the current THD$_i$ by up to 30%. Furthermore, it has been shown that the phase-angle of the voltage harmonics can have a significant impact on the input current harmonics. Depending on the voltage harmonic phase-angle, the same amount of voltage harmonics could improve or deteriorate the rectified voltage ripple and the input current THD$_i$. Moreover, the voltage harmonic phase-angle could create a phase delay (Δ) in the diodes conduction time. A positive Δ impacts the displacement power factor negatively, whereas a negative Δ improves that factor. Finally, a harmonic mitigation technique to compensate the high level of current harmonics using Electronic Inductor (EI) is presented.

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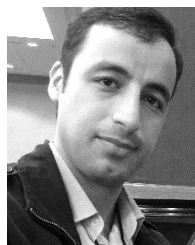
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