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A 0.8V, 152 μW, 433 MHz Mixer-First Receiver with a Self-Adjusted Frequency Tracking Loop

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ABSTRACT This paper presents a 433 MHz low-power receiver utilizing an N-path filter technique and a self-frequency tracking mechanism. Without the front-end amplifier, the mixer-first architecture can reduce power consumption significantly. A self-adjusted frequency tracking loop (SA-FTL) adjusts local oscillator (LO) frequency to approach input RF frequency automatically, thereby enhancing conversion gain and lowering return loss. The receiver, implemented in a 0.18 μm CMOS process, achieves a sensitivity of −80 dBm at a bit error rate (BER) of 10^{-3} and a data rate of 10 kb/s, while consuming 152 μW from a 0.8V voltage supply.

INDEX TERMS Frequency tracking loop, mixer first, N-path filter.

I. INTRODUCTION

Applications of wireless sensor networks (WSNs) are in widespread use in a variety of fields, such as environmental sensing, health care monitoring, and smart cities. These sensor nodes are usually battery-powered and size-constrained. For a wide-range deployment of wireless sensors, the large numbers of relay elements or high transmitter power dissipation significantly increase the cost and maintenance efforts. The sensitivity of receivers is thus considered a key for avoiding excessive transmitter power requirements for long-distance data communication.

To date, several architectures have been proposed to solve these problems. In [1]–[3], the schemes of direct envelope detection introduced sub-μW scale receivers without a mixer and oscillator in the architecture. However, the wide bandwidth and high noise figure cause reduced sensitivity of about −40 dBm. A super-heterodyne two-tone architecture was introduced in [4] to improve sensitivity, and a two-tone signal and envelope detector were used, creating a non-interfering intermediate frequency (IF) signal and reducing the in-band interference. The low IF receiver in [5]–[8] is similar to the uncertain-IF architecture. The receiver can achieve much better sensitivity because of the use of the high-accuracy oscillator and limited bandwidth. Additionally, to overcome frequency drift due to variations in the temperature and supply voltage, a digitally controlled oscillator (DCO) with the calibration of the duty-cycled phase-locked loop (DCPLL) was used. It achieves a high sensitivity but is power-hungry. The subsampling-based receivers in [9], [10] use a precise reference frequency lower than one-tenth of the targeted RF to reduce local oscillator (LO) power dissipation. The primary power consumption comes from the low-noise amplifiers (LNAs) that are used to suppress the noise effects at the following blocks, which enhances sensitivity.

Furthermore, the issue of interference tolerance should be considered. When performing dense network operations, the receivers are susceptible to interference from adjacent channels. Therefore, the receivers must possess immunity against adjacent interference while avoiding low overall performance.

The uncertain-IF heterodyne receiver in [11]–[14] adopts low-accuracy but power-efficient oscillators for frequency conversion. At the same time, it removes the power overhead attributed to phase-locked loops (PLLs). Furthermore, these systems usually pair the passive high-Q filter with a particular process, such as surface acoustic wave (SAW), bulk acoustic wave (BAW), or film bulk acoustic resonator (FBAR),

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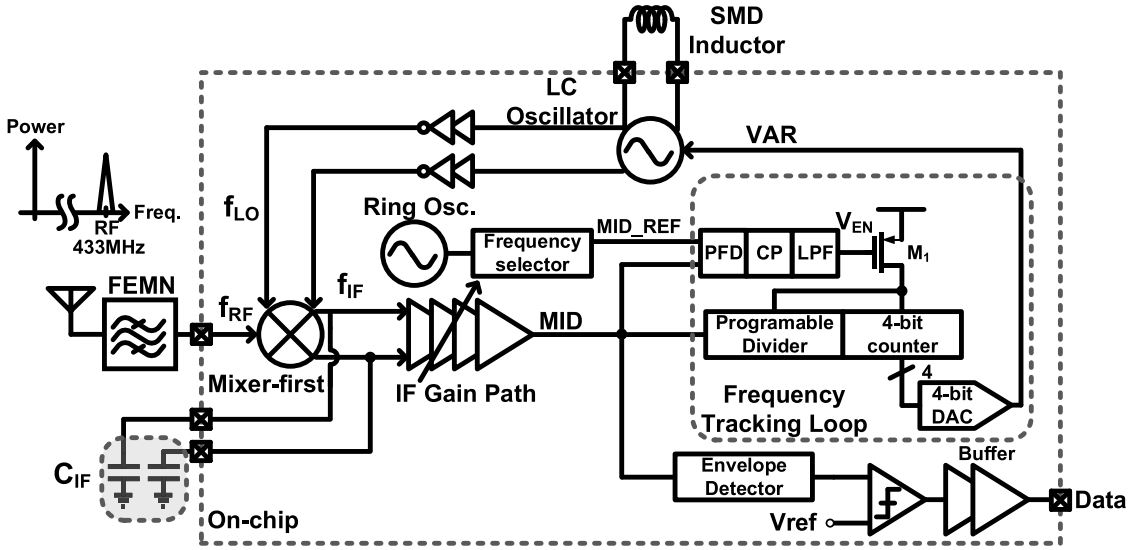

FIGURE 1. Block diagram of a two-path mixer-first receiver with frequency tracking loop.

to provide proper channel filtering at RF and alleviate the requirement for frequency calibration circuits. However, the sensitivity of this scheme is limited by integrated noise thanks to a wide IF bandwidth requirement caused by LO uncertainty.

Therefore, to remove the inaccessible or customized off-chip filter components, the mixer-first architecture was proposed in [15]–[20]. These architectures usually adopt an N-path filter for band selection, and the center frequency is determined by the LO. In addition, the Q factor of the N-path filter can also be defined by the load capacitance. The work in [15] obviates the requirement for a high-Q frequency reference by combining an LC oscillator with an off-chip surface mount device (SMD) inductor (Q is about 25) and a multi-stage high-Q N-path filter while maintaining high sensitivity. The multi-stage filtering architecture increases the complexity of frequency correction, and LO frequency must be accurate enough to avoid filtering out the desired signal.

To ease the requirement of the bulky SAW filter and crystal oscillator, this work presents a single-stage two-path filter while increasing the load capacitance to achieve the same filtering effect as the multi-stage architecture. Simultaneously, this work adopts a frequency tracking loop to adjust frequency correction, directly and automatically following the transmitter carrier signal. This work is designed for a low-power wireless sensor node that monitors slowly changing environmental parameters such as temperature, humidity and pressure.

The remainder of this paper is organized as follows. Section II introduces the concept and system design of the proposed architecture. The chip implementation and experimental results are presented in Section III, and Section IV briefly concludes the paper.

II. DESIGN OF MIXER-FIRST RECEIVER

A. SYSTEM ARCHITECTURE

Fig. 1 shows the architecture of the proposed design. This receiver contains a two-path filter, front-end matching network (FEMN), LC oscillator, frequency tracking loop, IF band gain path, and on–off keying (OOK) demodulator. The mixer down-converts the input signal to a baseband signal for signal amplification and processing. A frequency tracking loop detects any IF frequency error between the targeted RF carrier and the LC oscillator. If the frequency deviates from the desired frequency, which is determined by the frequency selector, the feedback digital-to-analog converter (DAC) controller continuously changes the varactor voltage and adjusts the frequency of the LC oscillator. When the frequency error is small enough, the frequency tracking loop turns off. Then, the system enters the data acquisition mode, where the data signal is amplified and extracted from the received signal. The detailed design of each sub-circuit is described in the following.

B. N-PATH FILTER

To avoid blocking of the receiver due to strong interfering signals, a high-Q band-pass filter is always needed. Although off-chip passive filters can satisfy the requirement of suppressing out-of-band interference, these components also increase the size and cost. An on-chip LC can be implemented, but the Q factor of the inductor below 1 GHz is poor (<10), and the inductor occupies a large chip area. Therefore, an inductor-less tunable N-path filter based on periodically time-variant networks was proposed [21]. The number of filters, N, influences the power consumption and noise of the receiver [22], [23]. In order to reduce the complexity of LO signal distribution and the increased number of drive buffers, an N-path filter with $N = 2$ is adopted in this work. The

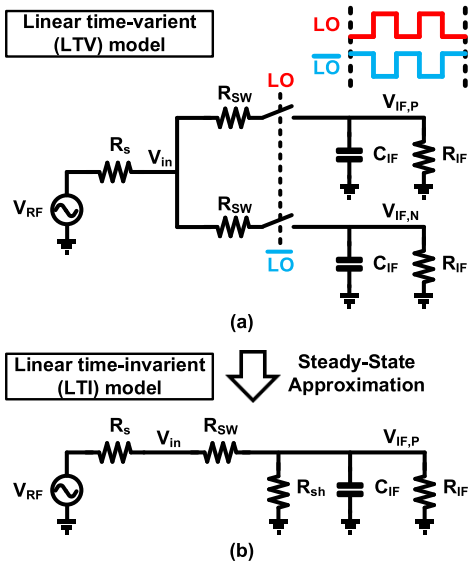

FIGURE 2. Two-path passive mixer model.

two-path passive mixer analysis is based on [15] and [22]. Fig. 2(a) shows the circuit model of a two-path passive mixer. The RF input is modeled as a voltage source connected with a source impedance R_s. The switch is modeled as an ideal switch in series with an on-resistance R_{sw}. R_{IF} and C_{IF} represent the load impedance of the following stage. At the steady state, the linear time-variant (LTV) model can be approximated as a linear time-invariant (LTI) model [23]. The virtual shunt resistance, $R_{sh,n}$, is expressed as detailed in [24]:

$$R_{sh,n} = \frac{2\gamma\,(R_s{+}R_{sw})\,R_{IF}}{2\,(R_s{+}R_{sw})\,(n^2-\gamma)+R_{IF}\,(n^2-2\gamma)},\quad n=1,3,5\ldots \tag{1}$$

where n is the n^{th} LO harmonic. $R_{sh,n}$ represents the input impedance of the IF frequency near a multiple of the LO frequency, and γ is scaling factor [22]. The two-path input impedance of the LTI equivalent model in Fig. 2(b) can be derived as

$$Z_{in} = (n\omega_{LO}+\omega_{IF}) = \left[R_{sw}+\left(R_{sh,n}\,||R_{IF}||\,\frac{1}{jn\omega_{IF}C_{IF}}\right)\right],\quad n=1,3,5\ldots \tag{2}$$

The conversion gain of the two-path filter at the input node is expressed as

$$A_{V,in}\left(\omega_{RF\_in}\right) = \frac{V_{in}\left(\omega_{RF\_in}\right)}{V_{RF}\left(\omega_{RF\_in}\right)} = \frac{Z_{in,fund}\left(\omega_{RF\_in}\right)}{Z_{in,fund}\left(\omega_{RF\_in}\right)+R_s} \tag{3}$$

At the output, the N-path filter performs the low-pass function, which can be expressed as

$$|A_V\,(\omega_{IF})| = \frac{V_{in}\,(\omega_{IF})}{V_{in}\,(\omega_{LO}\pm\omega_{IF})} = \frac{V_{IF,p}\,(\omega_{IF})-V_{IF,n}\,(\omega_{IF})}{V_{in}\,(\omega_{LO}\pm\omega_{IF})} = \frac{A_{Vo}}{\left(1+\left(\frac{\omega_{IF}}{\omega_{BW}}\right)^2\right)^{\frac{1}{2}}}$$

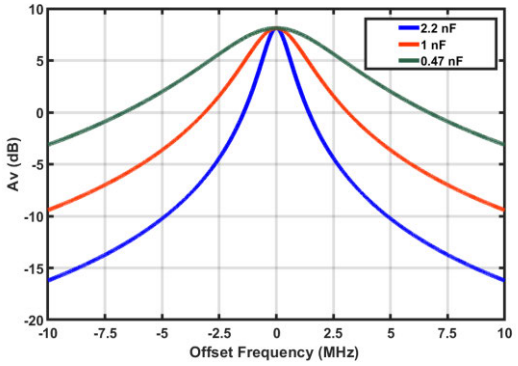

FIGURE 3. The output voltage gain at the IF frequency of the two-path filter.

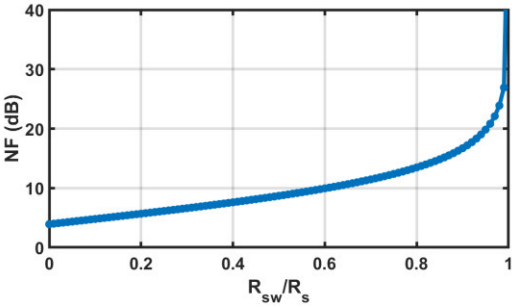

FIGURE 4. The analysis of noise figure with the different Rsw/Rs ratios.

$$A_{Vo} = \frac{8}{\pi}\left(\frac{R_{IF}}{2\,(R_s{+}R_{sw})+R_{IF}}\right)$$
$$\omega_{BW} = \frac{2\,(R_s{+}R_{sw})+R_{IF}}{2\,(R_s{+}R_{sw})\,R_{IF}C_{IF}} \approx \frac{1}{2\,(R_s{+}R_{sw})\,C_{IF}} \tag{4}$$

where A_{v0} is the single-to-differential DC voltage gain, and ω_{BW} is the attenuated 3 dB bandwidth. The analytical results are shown in Fig. 3. The noise figure (NF) of the two-path passive mixer is derived as [15]

$$NF = 10log\left(\sum_{n=1,3,5\ldots}^{\infty}\frac{2\,(R_s{+}R_{sw})}{n^2\,(R_s{-}R_{sw})}\right) \tag{5}$$

From (5), when the ratio of R_{sw}/R_s is close to one, NF increases largely. Fig. 4 depicts the results of NF versus R_{sw}/R_s. The $R_{sw,min}$ from [15] is defined as

$$R_{sw} = (1-4\gamma)\,R_s \approx 0.19R_s = R_{sw,min} \tag{6}$$

The scaling factor γ of the mixer circuit can be derived as 0.203 by using the linear time-varying (LTV) circuit model [22]. Therefore, we set R_{sw} to be 9.5Ω for a conventional R_s of 50Ω. Simultaneously, R_{IF} is set to infinite (input from an amplifier). To characterize the frequency response versus load capacitance, C_{IF} of 0.47 nF, 1 nF, and 2.2 nF, respectively, are simulated. A bandpass function is created by the up-conversion of the frequency response of LPF (C_{IF} and $(R_s{+}R_{sw})$) to a center LO frequency. Previous equations clarify that in order to get a much higher gain and the Q factor, the R_{sw} should be small, and the C_{IF} should be large. In (4), the mixer-first architecture with an N-path filter characterizes

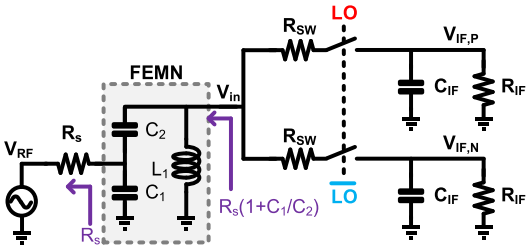

FIGURE 5. The N-path filter and the front-end matching network.

the BPF frequency response generated at the RF input node. The simulated results of the frequency response of a two-path mixer-first architecture are shown in Fig. 3. The BPF characteristics are centered on the LO frequency. The quality factor (Q) can be defined as $f_{LO}/2f_{BW}$.

At $C_{IF} = 2.2$ nF, a 3 dB attenuation at 1 MHz deviation from the LO frequency is achieved. To improve the voltage gain, the source impedance should be large enough. This work adopts an FEMN to boost the source impedance. Fig. 5 shows the schematic of the matching network. The resonant frequency of the FEMN is derived as

$$\omega_C = \sqrt{\frac{1}{L_1 C_T}} = \sqrt{\frac{1}{L_1\left(\frac{C_1 C_2}{C_1+C_2}\right)}} \tag{7}$$

Also, the boosted impedance can be calculated by the equation

$$R_{boosted} = R_S\left(1+\frac{C_1}{C_2}\right)^2 \tag{8}$$

The components, $C_1 = 23$pF, $C_2 = 16$pF, $L_1 = 15$nH, are used in this design. FEMN provides impedance matching, passive voltage gain, and input RF impedance enhancement. The LO frequency is adjusted by a frequency tracking loop to ensure the RF and LO frequencies are close enough to improve conversion gain and signal filtering. After that, the IF stage can be devised in the desired frequency range to provide sufficient voltage gain to enhance sensitivity.

C. SELF-ADJUSTED FREQUENCY TRACKING LOOP (SA-FTL)

For attaining the benefits on interference tolerance and voltage gain of the N-path circuits, the input RF signal should be sampled by an LO signal whose frequency approaches the RF frequency. Most prior works require an accurate external reference frequency to operate the N-path circuit. However, such architectures are unable to respond to the random frequency changes of the RF input signal in time. Without frequency tracking, the uncertainty of IF signal could be out of the bandwidth of baseband amplifiers, resulting in gain degradation, distortion, and low bit-error-rate (BER) in the communication. In this design, the intermediate frequency (IF) is compared with the on-chip reference signal, and then the tracking loop adjusted the LO frequency until the IF is within the desired frequency range. Therefore, the frequency adjustment mechanism on the N-path filter is necessary.

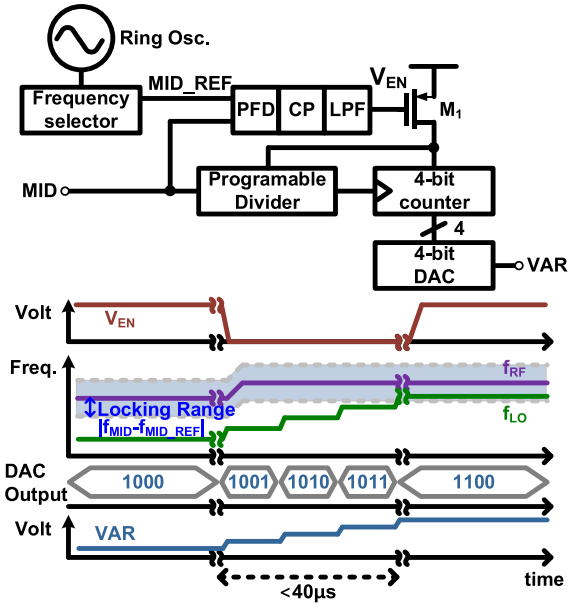

FIGURE 6. Self-Adjusted Frequency tracking loop (SA-FTL).

This work proposes a self-adjusted frequency tracking loop (SA-FTL) to ensure the down-converted IF frequency within the band-pass baseband amplifier bandwidth of 500 kHz $\sim$ 1 MHz. Fig. 6 shows the architecture of the frequency tracking loop. The SA-FTL is composed of a ring oscillator with a frequency selector, phase detector, charge pump, programmable divider, 4-bit up counter, and 4-bit DAC. The programmable divider is applied for the clock of a 4-bit up-counter and reducing the power consumption of the back-end digital circuit. IF frequency (MID) first is compared with a reference frequency of FTL (MID_REF) from the ring oscillator. The frequency difference is detected by the PFD and converted to a DC voltage using a charge pump. The voltage determines whether it continues to adjust up/down the frequency of LC oscillator by changing the bias voltage to the varactor. The negative feedback loop ensures the LO tracks the input RF frequency to improve the interference rejection ratio (IRR).

Moreover, the operation of SA-FTL includes two modes: frequency tracking mode and data acquisition mode. When the IF carrier frequency f_{MID} is larger than the reference f_{MID_REF}, the gate voltage of M_1, V_{EN}, decreases, and M_1 thus turns on, enabling the programmable divider and 4-bit counter. The 4-bit counter and DAC continuously update the bias voltage to the varactor until the LO is close to the RF frequency. Eventually, the IF carrier frequency f_{MID} is smaller than the reference IF carrier frequency, f_{MID_REF}, and V_{EN} becomes high, inactivating the programmable divider and 4-bit counter. At that point, the frequency of the LC oscillator is maintained, and the system enters the data acquisition mode. The operation of the frequency tracking loop is shown in Fig. 7. The relation between f_{RF} and f_{LO} is derived from (9) and (10):

$$|f_{RF} - f_{LO}| = f_{IF} = f_{MID} \leq f_{MID\_REF} \tag{9}$$

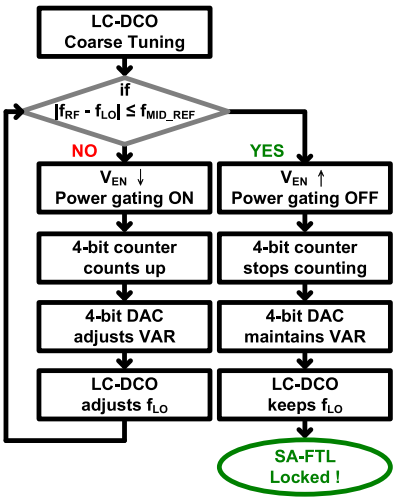

FIGURE 7. The methodology of frequency tracking in the SA-FTL.

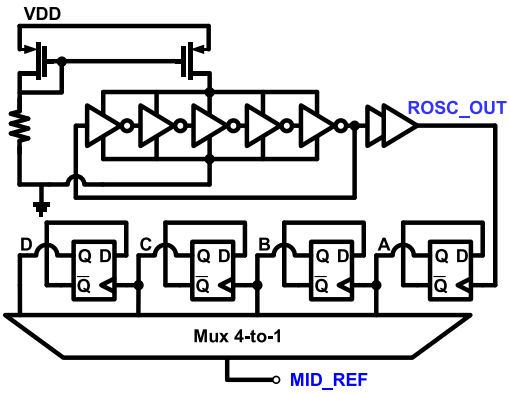

FIGURE 8. Architecture of ring oscillator and frequency selector.

$$f_{RF} \pm f_{MID} = f_{LO} \tag{10}$$

Thus, the frequency loop adjusts the VCO frequency through the 4-bit DAC, and the VCO frequency continuously changes until $f_{MID} \leq f_{MID\_REF}$. In Fig. 8, a five-stage ring oscillator is chosen in the frequency tracking loop and creates a 2 MHz reference signal. In order to alleviate the effects of PVT variation in the ring oscillator and to adjust the appropriate IF reference frequency MID_REF, the frequency selector is employed. The frequency selector is added as a frequency divider providing /2, /4, /8 frequency to overcome large frequency deviations over the PVT variations. The MID_REF signal decides the maximal frequency deviation between LO and RF frequency.

D. IF BAND GAIN AND DEMODULATION PATHS

Following the N-path filter is the IF band gain path, which is used to amplify the down-converted signal after the N-path filter. Fig. 9 shows the architecture of the IF gain path.

In order to accommodate the different input power levels, the IF chain consists of a differential pre-amplifier, variable gain amplifier (VGA), a differential-to-single-ended amplifier, and an envelope detector. The gain stages offer a more than 90 dB voltage gain within the bandwidth of 100 kHz while only consuming 40 μA. For high trans-conductance efficiency (g_m/id), the input transistors in the IF stage is sized (40 μm/0.4 μm) and operates in the subthreshold region. The pre-amplifier provides a gain of 15 dB.

The VGA is adapted to different input signal power levels for avoiding signal saturation in a broad dynamic range. Its architecture is shown in Fig. 9. The gain of the VGA is controlled by a 3-bit ($D_0 \sim D_2$) binary-weighted capacitor array in a range between C_F/C_0 and $C_F/(C_0+C_1+C_2)$. In this design, the value of C_0, C_1 and C_2 is 0.43 pF, 0.86 pF and 1.72 pF, respectively. The voltage conversion gain of two-stage VGAs is controlled by a 3-bit adjuster, $D_0 \sim D_2$, offering a variable gain from 7 to 48 dB, and bandwidth from 100 kHz to 500 kHz. The final stage of the IF band gain path is the differential signals to a single-ended converter that provides an additional 34 dB voltage gain.

E. DATA ACQUISITION PATH WITH ENVELOPE DETECTOR AND COMPARATOR

The blocks following the IF chain are the demodulation path and the frequency tracking loop. In the demodulation path, the Dickson charge pump [25] is used for envelope detection, and a comparator converts the analog signal to the digital pattern. Fig. 10 shows the architecture of the demodulation path. The rectifier uses MOSFET as a diode.

The turn-on voltage of a diode-connected MOSFET is almost equal to the threshold voltage (V_{th}) of a MOSFET. When the input signal, V_{MID}, is at the negative half cycle, the current flows through M_1 to charge the capacitor C_C, and the voltage of the C_C bottom plate is $-V_{th}$. When V_{MID} is at the positive half cycle, the bottom plate voltage becomes $2V_{MID}-V_{th}$ due to the fixed voltage difference between the two plates of C_C, and the resulting output voltage (ED_OUT) is $2V_{MID}-2V_{th}$. An amplified waveform is generated at ED_OUT, which is compared with COMP_REF. After passing through the inverter buffer, a series of data are generated at V_o.

F. DIGITAL CONTROL LC OSCILLATOR

The LC oscillator controls the center frequency of the N-path filter, causing the LO to track the targeted RF frequency. The improvement of phase noise and frequency accuracy from using an LC oscillator rather than a ring oscillator reduces the reciprocal mixing effects of in-band interferers. Fig. 11 shows the architecture of the digital control LC oscillator (LC-DCO) using a surface-mounted inductor. At initial, the 5-bits coarse tuning capacitor bank digitally controls LC-OSC to set LO frequency less than f_{MID_REF}. Then, the frequency tracking path controls the voltage of the varactor, VAR. When the SA-FTL detects the input RF frequency changes, the DAC updates VAR voltage for adjusting LO frequency until frequency differences are smaller than a 300 kHz offset. Fig. 12 shows the simulation results of DAC-controlled oscillator frequency in each step. The tracking range from 431.1 MHz to 434.5 MHz covers the

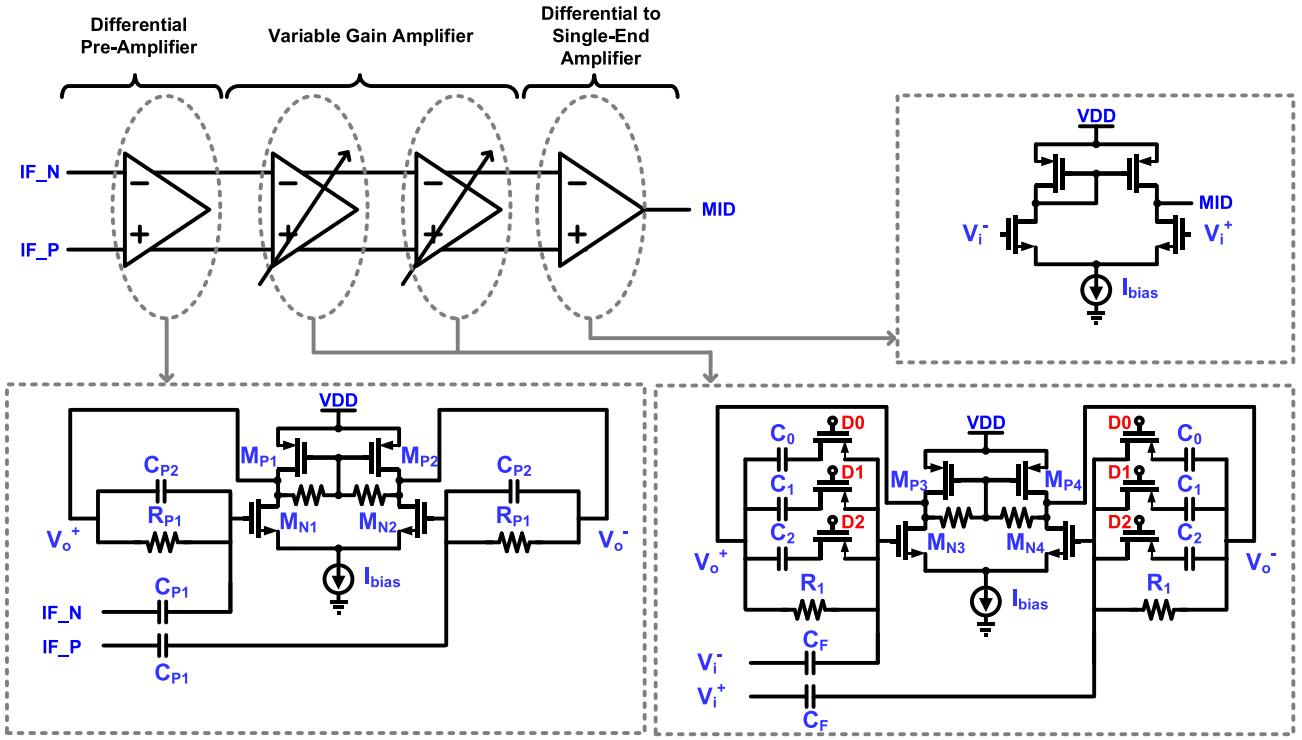

FIGURE 9. IF band gain path.

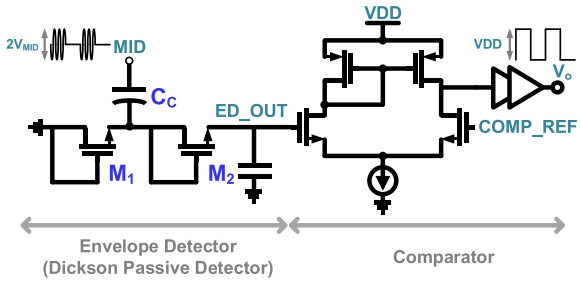

FIGURE 10. Data acquisition path with envelope detector and comparator.

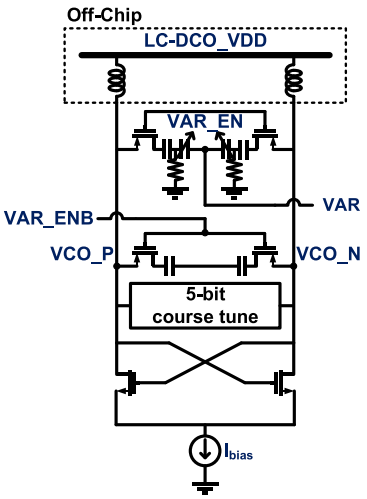

FIGURE 11. Digital control LC oscillator.

3dB attenuation bandwidth of two-path filter centered at 433 MHz. Fig. 13(a) shows the schematic of the PFD [26], which compares the phases and frequencies of the reference signal (MID_REF) and feedback signal (MID), and generates UP and DN signals to control the CP. In order to reduce the effects of the periodic glitch, additional digital logic gates are added. Fig. 13(b) shows the schematic of the CP [27] and LPF. The nonlinearity of the CP is mainly attributed to the UP/DN current mismatch and dead zone phenomena [28], [29]. Conventionally, the dead zone problem can be addressed by adding the delay chain at the reset of the PFD.

Also, to alleviate the current mismatch problem, two transistors, M_6 and M_{13}, are employed in the CP. These transistors compensate for the channel-length modulation effect of the UP/DN current mirror dynamically via negative feedback.

The last part is used for IF carrier extraction. If the power transistor (M_1, Fig. 6) is still turned on, the counter continuously counts the IF carrier to drive the 4-bit DAC that controls the varactor voltage in the LC oscillator. Also, a counter is added to avoid a random error due to the sudden frequency change. Fig. 14 shows the architecture of the DAC. The DAC is 4-bit, and its voltage range is from 10 mV to 580 mV. When the output of counter D3∼D0 is "0000," the oscillator frequency is the highest.

III. IMPLEMENTATION AND MEASUREMENT RESULTS

Fig. 15 shows the chip micrograph of the proposed receiver. It consists of the low-drop output (LDO) regulator, the IF

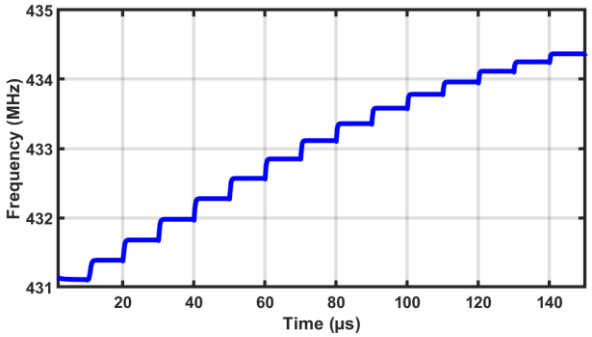

FIGURE 12. VCO frequency adjustment by variable DAC input.

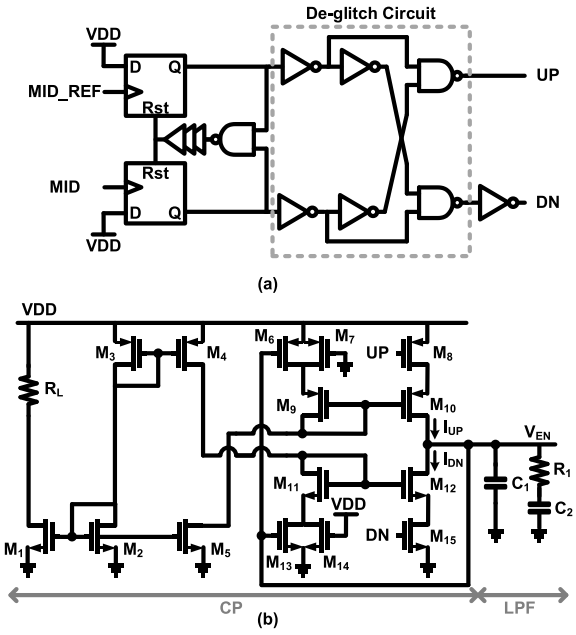

FIGURE 13. (a) PFD (b) CP and LPF.

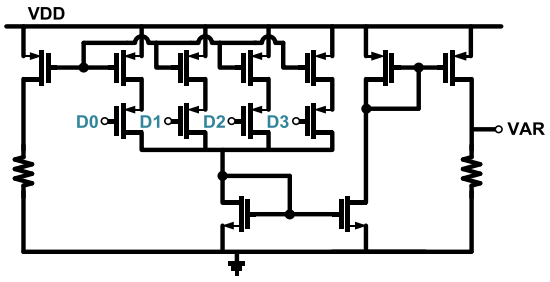

FIGURE 14. The 4-bit digital-to-analog converter (DAC) and its behavior.

band gain path, N-path filter, data acquisition path, LC oscillator, and the frequency tracking loop. The chip was fabricated in a 0.18 μm CMOS process, and the active core area, including LDO, is 1.4 mm^2 (the active core area is 0.86 mm^2). The chip is mounted and tested on the printed circuit board. The measured $|S_{11}|$ of the FEMN is presented in Fig. 16(a), where a 2.2 nF (C_{IF}) off-chip SMD capacitor is chosen. The design achieves $|S_{11}|$ of −15.29 dB at 433 MHz. When

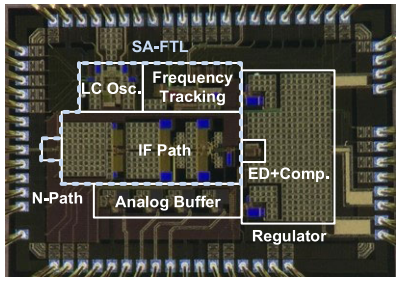

FIGURE 15. Chip micrograph.

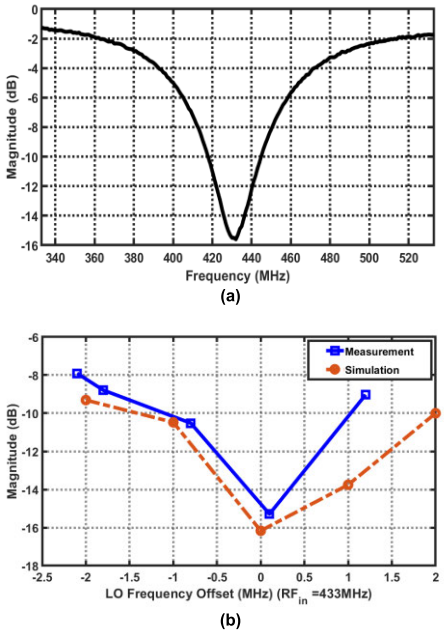

FIGURE 16. (a)S11; (b) the effect of the local oscillator (LO) offset on S11.

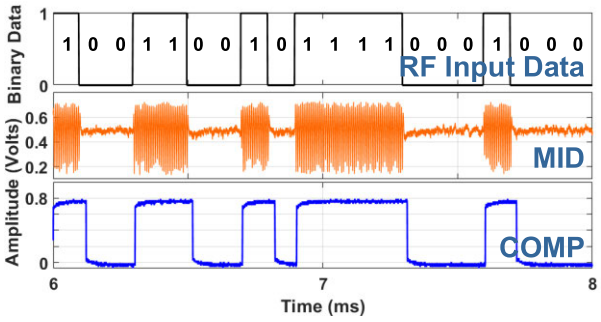

FIGURE 17. Measured time-domain response.

the LO frequency is far from the input RF frequency, $|S_{11}|$ degrades. The effect of LO offset from the RF carrier on $|S_{11}|$ is shown in Fig. 16(b). We set codes at the DAC input to set an initial frequency of the LC VCO. From the measurement, at a 2.2 MHz LO offset frequency from the center frequency, $|S_{11}|$ increases from −15.8 dB to −8 dB. Therefore, frequency tracking is necessary for improving power transfer and voltage gain. Fig. 17 shows the measured output waveform at an input of −80 dBm 433 MHz data-modulated signal at a

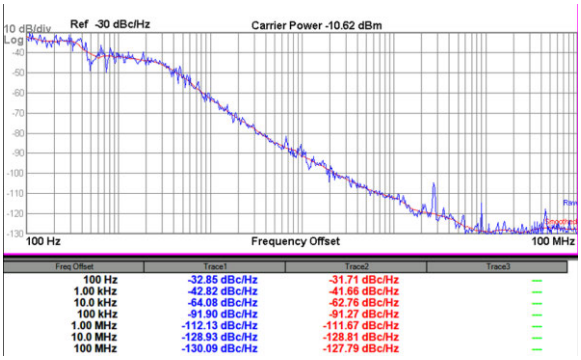

FIGURE 18. Measured LC digital control oscillator (LC-DCO) phase noise.

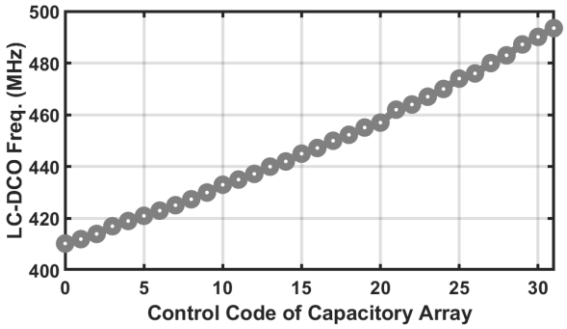

FIGURE 19. 5-bit coarse-tuning of LC-DCO.

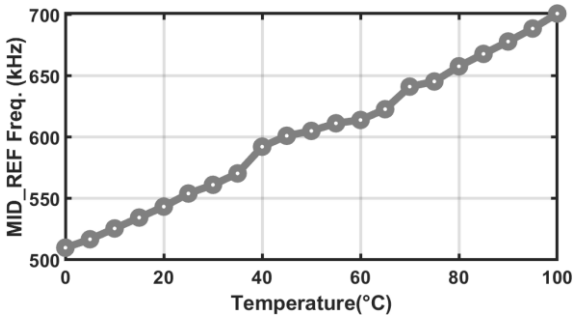

FIGURE 20. Frequency vs. temperature of ROSC.

10 kbps data rate. The MID signal is measured through an on-chip analog buffer. The oscillator frequency and phase noise are measured by a spectrum analyzer. Fig. 18 shows the phase noise measurement result of LC-DCO. At 433 MHz, the measured phase noise is −112 dBc/Hz at 1 MHz offset. The measured tunable frequency changes of the 5-bits capacitor bank are shown in Fig. 19. The tunable frequency range is from 410.3 MHz to 493.5 MHz. Fig. 20 shows the measured RO frequency deviations over temperature. The frequency changes from 509.9 to 700.9 kHz in a temperature range of 0∼100°C. The ring oscillator is used to set the accuracy between LO and RF frequency and in this frequency range, the N-path mixer gain and filtering degrade insignificantly.

Fig. 21(a) shows the waveforms of the frequency tracking loop. In the diagram, a programmable input RF frequency is adjusted from 434 MHz to 431 MHz at a 1 MHz step. The

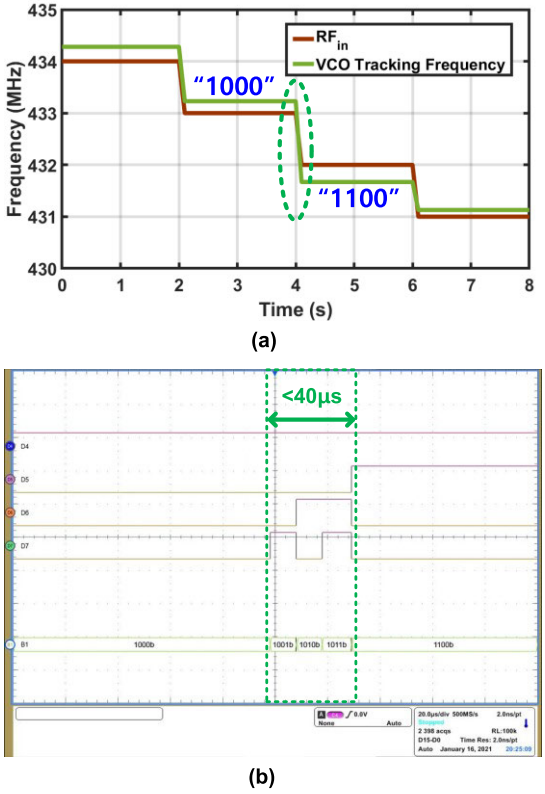

FIGURE 21. (a) The measured frequency tracking condition (b) FTL response time measured by the digital code conversion.

DAC output codes are measured by a digital oscilloscope and depicted in Fig. 21(b). The transitions of the digital codes show the response time from "1000" to "1100" is less than 40 μs (the x-axis scale is 20.0 μs/div of the window and D_4 is MSB). Fig. 22(a) shows the time-domain waveform of the frequency calibration path under the condition that the IF frequency MID is larger than MID_REF. The frequency detector activates the power-gating transistor, and hence, the control code of the DAC continuously changes to correct the LC oscillator frequency. The spectrum (Fig. 22(b)) of frequency tracking, recorded using "Max-hold" function, shows that the LC oscillator continuously changes the operating frequency until it approaches 434.38 MHz. Fig. 23(a) shows the time-domain waveform of the frequency calibration path under the condition that the IF frequency MID is less than or equal to the reference frequency MID_REF. In this state, the frequency detector turns off the power-gating transistor and maintains the constant control code of the DAC. The frequency tracking is performed automatically when frequency deviation occurs. The output spectrum of the LC oscillator is shown in Fig. 23(b). Fig. 24(a) shows the sensitivity of the proposed receiver, which is measured at a modulated input signal with the OOK PN9 pseudo-random bit sequences (PRBS). The bit error rate (BER) is characterized by the output waveform converted by the comparator. The measured sensitivity is −80 dBm for 10 kbps and −78.5 dBm for 20 kbps at a BER of 10^{-3}. As the data rate increases to

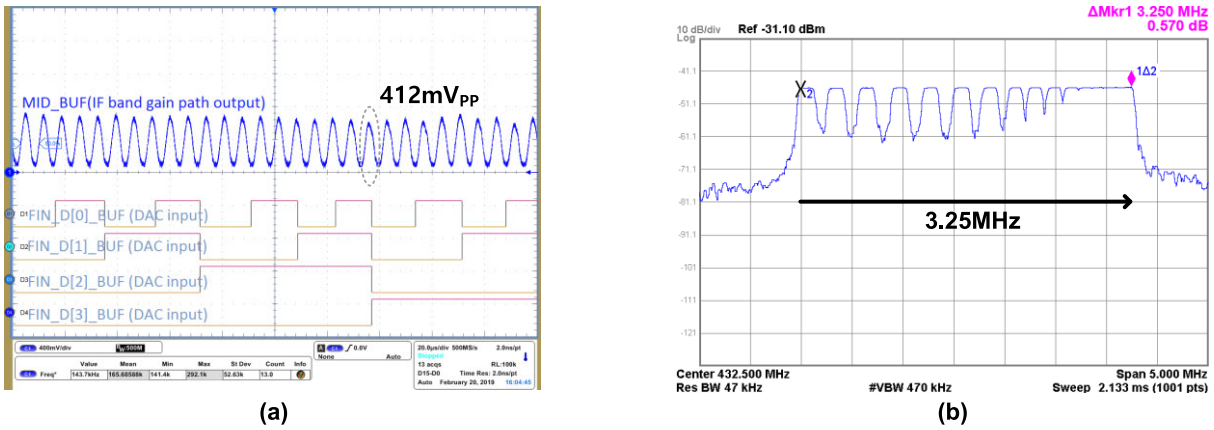

FIGURE 22. (a) Time-domain (high-Z load) (b) frequency-domain at MID > MID_REF (tracking) (50Ω load).

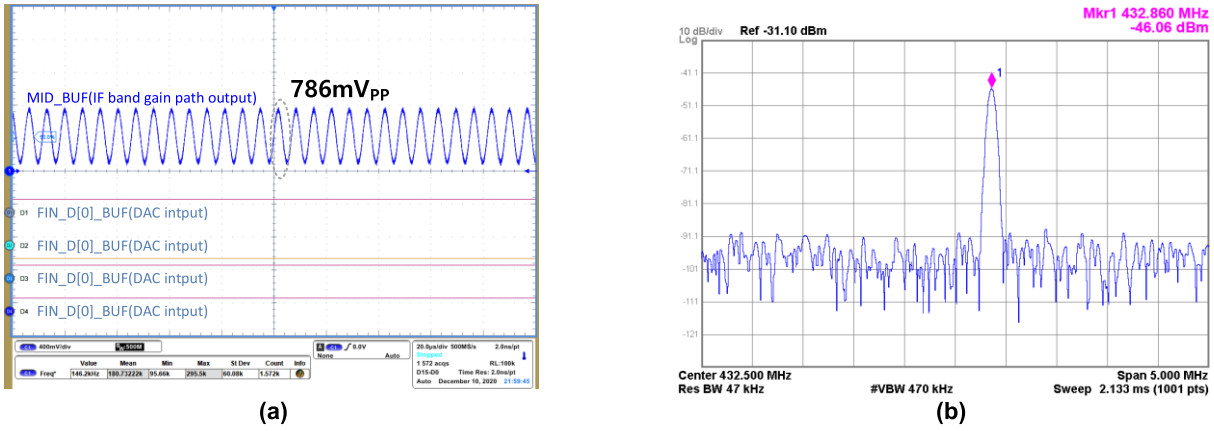

FIGURE 23. (a) Time-domain (high-Z load) (b) frequency-domain at MID≤ MID_REF (locked) (50Ω load).

TABLE 1. Performance summary and comparisons.

	[1]	[6]	[12]	[19]	[20]	[30]	This Work
CMOS Technology (nm)	130	90	65	65	180	180	180
Architecture	Envelope Detector	Low-IF	Heterodyne	Mixer-First with Two-Step Down-Conversion	Mixer-First	Multiple-Gated LNA	Mixer-First with Frequency Tracking
External Components	Resonant Tank RF Input	Resonant Tank RF Input	FBAR	External Clock and Off-chip RF Filter	FEMN	ADC and MCU	FEMN and SMD Inductor
Voltage Supply (V)	1.2	0.75	0.7	0.85	1.2	0.45	0.8
Power Consumption (μW)	0.098	126	180	335	2190*4	129*5	152
LO Generation	–	Ring-OSC	Ring-OSC	ROSC with FLL	Quadrature Ring-OSC	Clock gen.	LC-DCO
Modulation	OOK	FSK	OOK	FSK	ASK	OOK/FSK	OOK
Carrier Frequency (MHz)	915	868/915	2400	5800	403/433	402~405	433
Data Rate (Kbps)	100	1~50	1000	31.25	20	50/120	10
Sensitivity @ 10^{-3} BER (dBm)	−41	−65	−67	−72	−72/−73	−55	−80
Active Area (mm^2)	1.82	–	0.49*3	0.228	2.46	3.3	0.86*3
FoM *6	161	150	164	151	141	140	158

*1 Excluding bond-pads; *2 Excluding bulk acoustic wave (BAW); *3 Active core area; *4 Including transmitter power consumption; *5 Sleep mode.
*6 FoM = -Sensitivity - 10*log (Power Consumption / Data rate)

20 kbps, the envelope detector limits the response due to the constrained bandwidth and degrades the sensitivity by 1.5 dB. Fig. 24(b) shows the measured BER when the frequency tracking loop locked and unlocked. Compared to the

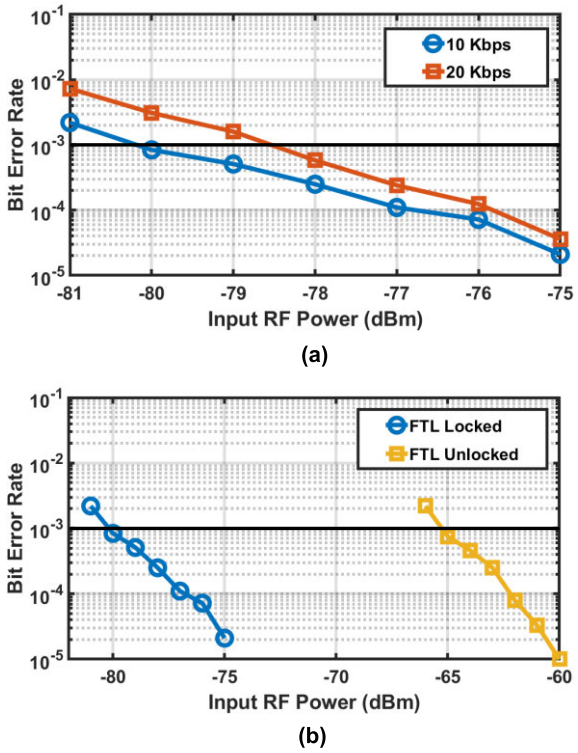

FIGURE 24. (a) BER (b) BER with FTL Locked and Unlocked.

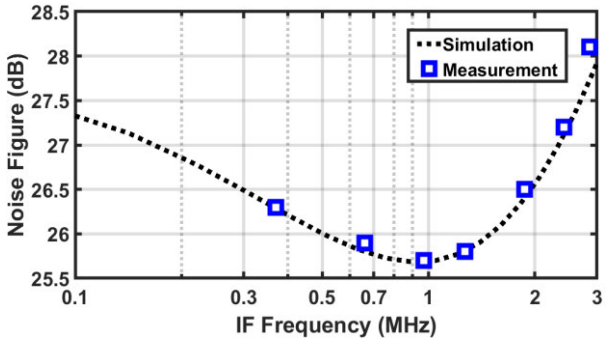

FIGURE 25. Noise figure comparison of simulated and measured results.

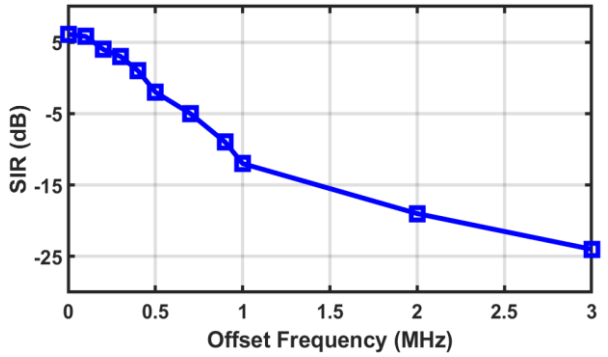

FIGURE 26. Signal-to-interference ratio.

unlocked condition, the design at locked condition improves the sensitivity by 15dB, which agrees with the gain improvement by the N-path mixer. Fig. 25 shows the simulated and measured noise figure. The measured noise figure is 25.8 dB at 970 kHz offset. The effect of flicker noise and down-converted harmonics generated by the LO square clock signal is folded on the spectrum. NF increases by 1.5 dB at low IF because of the influence of flicker noise, and NF degrades at high IF due to the bandwidth limits of the IF gain stages. Fig. 26 shows the measured result of the signal-to-interference ratio (SIR), the interference tolerance from the signal. SIR of 5 dB means the signal needs to be larger than interference by 5 dB for correct demodulation. When interference moves far from the RF signal frequency, the interference is attenuated due to the band-pass characteristics of the mixer-first architecture. The design achieves SIR of −24 dB at a 3 MHz offset.

Table 1 summarizes the performance of the proposed receiver and the comparison with the state-of-the-art. Compared with other sub-GHz works, the proposed mixer-first receiver achieves a good compromise between sensitivity and power consumption.

IV. CONCLUSION

In this paper, a low-power mixer-first OOK with SA-FTL receiver was proposed. With the use of an N-path filter and automatic frequency tracking mechanism, the system can achieve high sensitivity, low return loss, and high conversion gain. The proposed 433 MHz receiver consumes 152 μW from a supply of 0.8 V and achieves −80 dBm sensitivity at a 10 kb/s data rate with a BER of 10^{-3}, a 15 dB improvement by turning on the tracking loop. The SIR is −24 dB at a 3 MHz offset. The proposed receiver is designed for low power consumption and low deployment density of wireless sensor nodes in an Internet of Things application.

ACKNOWLEDGMENT

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