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A New Asymmetric Cascaded Multilevel Converter Topology With Reduced Voltage Stress and Number of Switches

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This work did not involve human subject or animals in its research.

ABSTRACT This paper presents a new structure of a multilevel inverter with fewer components, which is suitable for renewable energy sources and industrial loads applications. The structure has three unequal input sources and ten switches that can generate a 15-level output voltage. Furthermore, it can be connected in cascade for increasing, even more, the number of levels and output voltage. The main feature of the proposed inverter is its very low harmonic distortion at the output voltage and current due to the control method, which is based on the nearest level control method for generating a high-quality output voltage. A typical application of this inverter is in solar cells and wind turbines. Both simulations in Matlab/Simulink and experimental results in a scaled-down prototype validate the proposed theoretical analysis.

INDEX TERMS Multilevel inverter, cascading converters, low harmonics, losses, distortion.

I. INTRODUCTION

Multilevel inverters are applicable in medium voltage and high power applications such as electrical motor drives, energy storage systems, reactive power compensators, and flexible AC transmission systems (FACTS) [1], [2]. Nabae first introduced these inverters in 1975, which are comprised of a series combination of multiple neutral point clamped (NPC) three-level full-bridge converters [3], [4]. Multilevel inverters can be categorized into three groups: NPC inverters [4], flying capacitor (FC) multilevel inverters [5], and multilevel inverters with cascaded H-full bridges (CHB) [6].

As the most common NPC and FC inverters' failures are related to the unbalanced DC link voltage and the high stress on switches, researchers have focused on CHB converters by providing different structures. These structures can be compared in various aspects, such as the number of levels, the number of DC sources, the number of switches, and the total standing voltage (TSV) [7], [8].

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Another method to produce multilevel converters is using modules, thus multi-modular converters (MMCs) arise. A DC source with two switches can generate a level of this multilevel converter, so it can be considered as a module [9]. If these modules are connected in series, a greater number of levels can be reached. In addition, an auxiliary circuit, such as an H-bridge, can turn these positive levels to negative ones. Thus, a sinusoidal voltage output with no DC component can be obtained [10]. The main drawback is that the switches in the H-bridge circuit must tolerate high voltage stress.

Multilevel converters usually produce a sinusoidal waveform with small output voltage steps. An output voltage step is a DC voltage, which can be added or subtracted to track a sinusoidal waveform. Thus, any multilevel converter's main goals are to minimize the number of components and produce an output voltage with the highest number of levels to reduce the Total Harmonic Distortion (THD) of the output signal.

In order to achieve that, an attractive solution is to use asymmetric DC sources [11], [12]. If asymmetric DC sources are used, the voltage stress in each switch is different. The TSV is defined as the maximum voltage applied to each switch during the off state. The lower the TSV, the lower

the power losses in the switches. In order to reduce voltage stress, an enhanced H-bridge with different DC sources has been proposed in [13]. However, for improving the voltage and current quality, the converters require more levels; so the number of switches increases. Due to that, in general, cost, conduction and switching losses and complexity of the control system increase, and reliability reduces. Many structures have been introduced to increase the number of voltage levels, in order to improve the system's performance [13], [14], [16].

Asymmetrical CHB multilevel inverter (CHB-MLI) topologies have been introduced to increase the number of levels by connecting different non-equal voltage DC sources [13]–[15]. The main drawback is that the switches' stresses are not the same. The voltage stress on switches connected to the highest DC input voltage will be higher than that on switches connected to the lowest DC input voltage. Unbalanced loss sharing among switches will cause varying high temperatures for switches. In addition, unequal voltage stresses mean different voltage ratings will be used for switches, which results in a higher cost. Other modified topologies based on CHB have been proposed to improve the output voltage quality [16], [17], but the advantages of the CHB, such as simplicity, simple construction, simple control, and modularity, are lost.

Cascaded structures have also drawn attention because of their advantages compared to the prior topologies, such as simpler control structure and absence of diodes and capacitors for generating more levels in high power applications [14], [15]. On the contrary, cascaded structures have some disadvantages, such as the need for multiple DC power sources for each base unit to generate more voltage levels [17], [18].

New structures for multilevel inverters such as hybrid and asymmetrical cascaded multilevel structures have recently appeared to decrease the number of input DC voltage sources [19], [20]. However, these structures need specific algorithms to determine the amount of DC voltage sources. Furthermore, the presence of too many switches is not cost-effective. Although the rated voltage of switches may be low in these multilevel inverters, the fact that each switch requires a separate driver and protection circuit increases the cost and complexity of the circuit notably [21].

This paper proposes a new structure that aims to reduce construction costs and increase power quality. The proposed structure is analized in two parts: single basic unit and cascaded of basic units. The single basic unit needs three DC sources and only ten switches, which can produce a sinusoidal output with 15 levels. This way, the proposed single unit offers a great tradeoff between the number of DC sources, number of switches, and the number of levels, thus producing a very low distortion in the output port. This inverter can be widely used as an interface for renewable energy sources and high-voltage overhead distribution lines [13], [14]. In addition, several single basic units can be connected in cascade to reach a higher voltage range and a greater number of levels because the cascaded units can have different DC input voltages and thus can create additional voltage levels

TABLE 1. Switching states of the proposed basic unit.

S_1	S_2	S_3	S_4	S_5	S_6	T_1	T_2	T_3	T_4	V_{out}
1	0	0	0	0	0	1	1	0	0	E_1
0	0	0	0	1	1	1	0	1	0	E_2
1	0	0	0	0	0	0	0	1	1	E_3
0	0	0	0	1	1	1	1	0	0	E_1+E_2
1	0	0	0	0	0	0	1	0	1	E_1+E_3
0	0	0	0	1	1	0	0	1	1	E_2+E_3
0	0	0	0	1	1	0	1	0	1	E_1+E_2+E_3
0	1	0	0	0	0	0	0	1	1	-E_1
0	0	1	1	0	0	0	1	0	1	-E_2
0	1	0	0	0	0	1	1	0	0	-E_3
0	0	1	1	0	0	0	0	1	1	-E_1-E_2
0	1	0	0	0	0	1	0	1	0	-E_1-E_3
0	0	1	1	0	0	1	1	0	0	-E_2-E_3
0	0	1	1	0	0	1	0	1	0	-E_1-E_2-E_3
1	0	0	0	0	0	1	0	1	0	0

The paper is structured as follows. The description and analysis of the basic unit are given in Section II. Section III describes the nearest level control (NLC) as the proposed control method. Section IV describes how to connect the basic units to create a cascaded structure. Section V compares the proposed cascaded multilevel inverter with several cascaded multilevel inverters that have been presented in the literature. The simulation and experimental results are investigated and presented in Section VI. Finally, the conclusions are shown in Section VII.

II. DESCRIPTION AND ANALYSIS OF THE BASIC UNIT

The basic unit of the proposed method is illustrated in Fig. 1.a for single-phase system and can be extended to produce three-phase system by using three basic units one per phase. The basic structure consists of ten switches: six bidirectional switches (S_1, S_2, T_1, T_2, T_3, T_4), which block the current in the two directions (details of the bidirectional switches are shown in Section II.C), and four unidirectional switches (S_3, S_4, S_5, S_6). It has three inputs, E_1, E_2, and E_3, which must be isolated among each other to ensure the proper operation of the converter. The ratio between the DC sources must be:

$$E2 = 2E1 \quad \& \quad E3 = 2E2 \tag{1}$$

in order to minimize of the total harmonic distortion (THD) of the output voltage. The basic structure is shown in Fig. 1.a, its output voltage has 15 levels: seven positive, seven negative voltage levels and one zero-voltage level. Table 1 shows the state of the switches and the corresponding output voltage. Fig. 1.c shows an application of the multilevel converter using several renewable energy sources as power inputs. This is one of the methods to produce the three independent sources, where a DC link is used and then independent

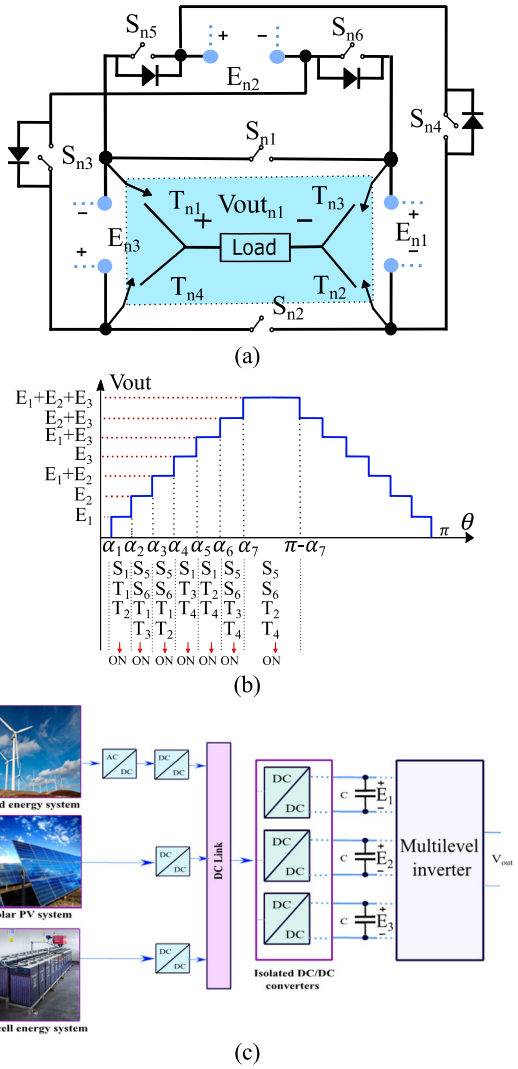

FIGURE 1. Proposed 15-level multilevel converter: (a) basic unit, (b) Switching pattern, (c) Application for renewable sources [18].

TABLE 2. Switching angles ($0 < t < T/2$).

digre	α_1	α_2	α_3	α_4	α_5	α_6	α_7
α_i	4.09°	12.37°	20.92°	30.00°	40.00°	51.78°	68.21°
$Sin(\alpha_i)$	0.071	0.214	0.357	0.5	0.642	0.785	0.928
$Cos(\alpha_i)$	0.997	0.976	0.934	0.866	0.766	0.618	0.371

DC/DC converters provides the input DC sources. Another possibility is a direct connection of PV panels using the strategy of (1). This means that, if the PV panels are equal, the ones connected to E_1 are half of the panels connected to E_2 and a quarter of the panels connected to E_3.

A. OPERATION PRINCIPLE

Table 1 shows the switches' operation versus output voltage. For example, according to Table 1, when S_1, T_1, and T_2 turn on with the rest of the switches off,, the output voltage becomes E_1, when S_2, T_1, and T_2 turn on output voltage becomes $-E_3$, and so on. Switches are controlled in order not to have any conducting diodes that can short-circuit the DC sources. Fig. 1.b shows the switching pattern that the controller of the inverter produces using a sinusoidal reference. It shows which of the inputs (E_1, E_2 or E_3) are selected to have a signal close to a sinusoidal waveform in the output port. The voltage difference between the multilevel output signal and the sinusoidal signal is the source of THD and must be minimized.

Fig. 2 shows the current path at eight different modes, which are detailed at Table 1. The other switching modes can be obtained using Table 1. The switches must be switched on and off, avoiding short-circuit in the inputs and following the reference signal. In order to create a sinusoidal waveform, the switching pattern must change according to the control presented in Section III. The transition from one state to the next one is done at the transition angles, $\alpha_1, \alpha_2, \ldots, \alpha_N$, which are shown in Fig. 3 and Table 2. Notice that during a whole cycle, which lasts 20ms (50Hz), the converter changes its output 28 times using the 15 levels. The total amount of commutations including all of the switches in one cycle can be extracted using Fig. 2 and Table 1. It gives 100 commutations per cycle including all of the switches, so the switching losses is low.

B. CURRENT THROUGH THE SWITCHES

In order to evaluate power losses and to select the switches, the current through the switches during the on-state must be calculated. Particularly, the average and the RMS current rating are needed. In the proposed multilevel inverter, the waveform of output current can be considered sinusoidal by assuming the high number of levels. The current waveforms through the diodes and switches are depicted in Fig 3. By assuming a constant temperature, the average current can be calculated by:

$$I_{ave}(S_n) = \frac{1}{T}\int_0^T i_{(t)}dt. \tag{2}$$

For example, the average current for switch S_1 is calculated below:

$$\begin{aligned} I_{ave}(S_1) &= \frac{1}{T}\int_0^T I_{(t)}dt \\ &= \frac{2}{2\pi}\left[\int_0^{\alpha_2} I_m sin\theta d\theta + \int_{\alpha_4}^{\alpha_6} I_m sin\theta d\theta\right] \\ &= \frac{I_m}{2\pi}\left[-2\left[cos\theta|_0^{\alpha_2} + cos\theta|_{\alpha_4}^{\alpha_6}\right]\right] \\ &= \frac{I_m}{\pi}\left[1 + cos\alpha_4 - cos\alpha_2 - cos\alpha_6\right] \end{aligned} \tag{3}$$

where α_2, α_4 and α_6 are the angles of the sinusoidal waveform that start and end a conductive period for S_1 and I_m is the peak of the output current. These angles are shown in Fig. 3 and Table 2, and correspond to the case of the converter working at the maximum power with the minimum THD. The angles

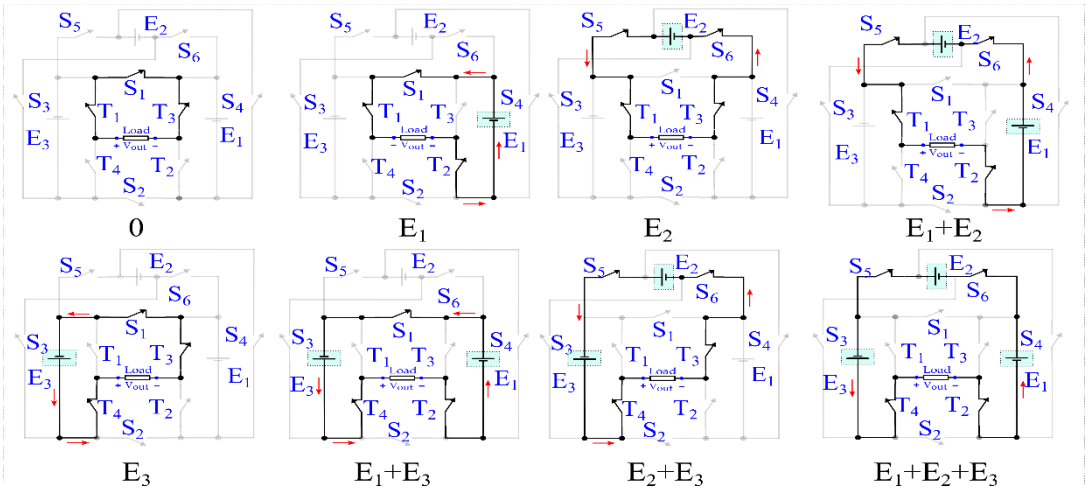

FIGURE 2. Current path and state of switches (0<t<T/4).

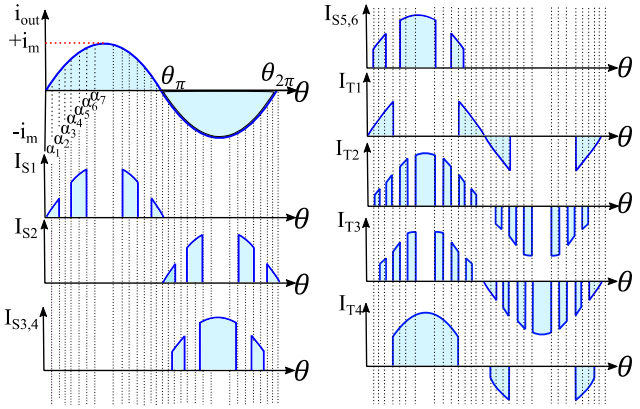

FIGURE 3. Current waveforms through the switches.

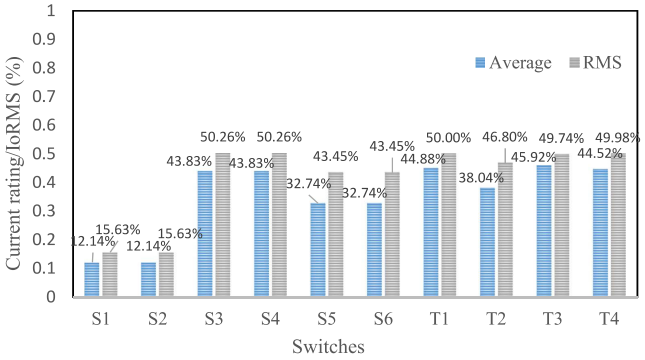

FIGURE 4. Current rating for the switches in the proposed structure normalized with the output RMS current.

can be obtained by:

$$\alpha_j = sin^{-1}\left(\frac{2j-1}{2N_{level}}\right), \quad \text{for } j = 1, \ldots, (N_{level}-1)/2 \tag{4}$$

where N_{level} is the number of levels of the output voltage ($N_{level} = 15$). For the first quadrant, seven angles exist in the proposed converter. The angles in the other quadrants can be obtained using the symmetric properties of the sinusoidal signal.

The average current is computed only in the first quarter of the period and is multiplied by two due to the signal symmetry. The value of I_m can be obtained by:

$$I_m = \frac{Vo_{max}}{\sqrt{R_L^2 + X_L^2}} = \frac{Vo_{max}}{|Z_L|} \tag{5}$$

where R_L, X_L are resistance and reactance of the load, respectively. Vo_{max} is the peak of the output voltage.

Fig. 4 shows the current rating of the switches normalized with the output RMS current. For example, for the average current of S1, using (3), the rating is:

$$\frac{I_{ave}\,(S_1)}{I_{rms}\,(output)} = \frac{I_{ave}\,(S_1)}{I_m(output)/\sqrt{2}} = 12.14\% \tag{6}$$

The RMS current for each of the switches:

$$I_{RMS}\,(S_n) = \sqrt{\frac{1}{T}\int_0^T i_{(t)}^2 dt}. \tag{7}$$

Similarly to the average current, the RMS was calculated and normalized for every switch, as shown in Fig. 4. As the ratings are different for each switch, it is possible to select the switch according to these values to optimize cost, power rating and thermal design for implementing the prototype. According to Fig. 4, the switches can be divided into two categories. S_3, S_4, S_5, S_6, T_1, T_2, T_3, and T_4 have an average current around 40% of the output RMS current, and S_1 and S_2 switches have only around 10% of the output RMS current.

C. CALCULATION OF POWER LOSSES

As in any other converter, semiconductor power losses can be divided in conduction and switching losses. Conduction

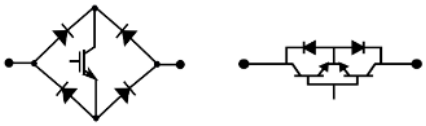

FIGURE 5. Bidirectional switches: (a) Bridge of diodes with single IGBT, (b) Double IGBT structure.

losses occur when the switch is on and depend on the current through the switches. Switching losses exist during turn-on and turn-off transitions and they are proportional to the switching frequency. For this particular modulation the switching frequency is very low, so switching losses are extremely low, which is very favorable for high power applications.

Bidirectional switches can be done in different ways. Fig. 5.a shows a diode bridge with a single switch that is able to control current in both directions. This switch topology consists of four ultra-fast diodes with a controllable unidirectional switch. The advantage of this switch is that it has a simple construction and requires only one switch, for example, one insulated-gate bipolar transistor (IGBT), and the blocking voltage is shared between two diodes and one IGBT. However, the conduction losses are due to two voltage drops in the diodes and one IGBT saturation voltage.

A structure which reduces the voltage drop is shown in Fig. 5.b. This structure has only two IGBTs, so only one saturation voltage and one forward voltage drop in the diode. Therefore this structure has reduced conduction losses. Besides, the two IGBTs can be triggered using the same driver; this means that to have a bidirectional switch instead of a unidirectional switch does not add complexity in the driver and control stages, so the cost is not increased. The first topology was used for calculating the losses in the following section thus it imposes a maximum limit on power losses; other configurations will reduce the power losses and can be easily calculated following the same approach.

1) CONDUCTION LOSSES

Conduction losses can be calculated using the on-voltage drop in the switch:

$$\begin{aligned} \mathrm{P_{Cond}} &= \frac{1}{T}\int_{\mathrm{t+T}}^{\mathrm{T}} V_{on}(t)\cdot I(t)dt \\ &= \frac{V_{SAT}}{T}\int_{\mathrm{t+T}}^{\mathrm{T}} |i(t)|\,dt + \frac{r_{on}}{T}\int_{\mathrm{t+T}}^{\mathrm{T}} i^2(t)dt \\ &= V_{SAT}I_{AVEABS} + r_{on}I_{RMS}^2 \end{aligned} \tag{8}$$

where $\mathrm{V_{on}(t)}$ is the on-voltage drop, i(t) is the current through the switch and $\mathrm{r_{on}}$ is the on-resistance. In bidirectional switches, $\mathrm{V_{on}(t)}$ has the same sign as the current through the switch, so the average absolute current must be used, $\mathrm{I_{AVEABS}}$. The total conducting losses is the sum of the losses in each switch. Thus, using (8) and switching intervals of section II.B, the total conducting losses are:

$$\begin{aligned} P_{cond}\,(Total) &= \sum_{i=1}^{10} P_{Con}\,(Si) = (0.459)\,(V_T + 2V_D)\,I_m \\ &\quad + (5.87\cdot 10^{-3})\,(R_T + 2R_D)\,\frac{{I_m}^2}{2}, \end{aligned} \tag{9}$$

where $\mathrm{V_T}$ and $\mathrm{R_T}$ are the saturation voltage and on-resistance of the IGBT, $\mathrm{V_D}$ and $\mathrm{R_D}$ are the forward voltage drop and on-resistance of one diode. The losses per switch are illustrated in Fig. 6.a as the percentage of the total conductive losses. It can be seen that the $\mathrm{S_3}$, $\mathrm{S_4}$, $\mathrm{S_5}$, $\mathrm{S_6}$, $\mathrm{T_1}$, $\mathrm{T_2}$, $\mathrm{T_3}$, and $\mathrm{T_4}$ switches dissipate 94% of conduction losses.

2) SWITCHING LOSSES

The switching losses are the energy losses during the transition (from on to off and vice versa) multiplied by the switching frequency. In order to estimate the energy losses, the current and voltage profiles can be linearized during the transition [22]. Thus, the energy losses for the on-transition and off-transition:

$$E_{on} = \int_0^{t_{on}} v_{(t)}i_{(t)}dt = \frac{V_{switch}It_{on}}{2}, \tag{10}$$

$$E_{off} = \int_0^{t_{off}} v_{(t)}i_{(t)}dt = \frac{V_{switch}It_{off}}{2}, \tag{11}$$

where $\mathrm{t_{on}}$ and $\mathrm{t_{off}}$ are the duration of the switching transition, v(t) and i(t) are the voltage and current during the transition. I is current through the switch at the beginning of the off-transition and at the end of the on-transition, and $\mathrm{V_{switch}}$ is the voltage across the switch at the beginning of the on-transition and at the end of the off-transition. Following the same approach as in conducting losses, the total switching losses are:

$$\begin{aligned} P_{sw}\,(Total) &= \frac{1}{T}\left[\sum_{i=1}^{10}\left(E_{off\,(Si)} + E_{on(Si)}\right)\right] \\ &= (25.1)\,E1\frac{\Delta t}{T}I_m. \end{aligned} \tag{12}$$

where it is considered that $\mathrm{t_{off}} = \mathrm{t_{on}}\Delta\mathrm{t}$. The distribution of total switching losses is illustrated in Fig. 6.b. Finally, based on conducting and switching losses, the efficiency can be calculated as:

$$\eta_{eff} = \frac{P_{out}}{P_{in}} = \frac{1}{1 + \frac{P_{con}(Total)+P_{sw}(Total)}{P_{out}}} \tag{13}$$

where

$$P_{out} = \frac{7E1I_m}{2} = 3.5E1I_m, \tag{14}$$

for the maximum power and voltage. The efficiency is:

$$\begin{aligned} \eta_{eff} = \frac{1}{1 + (7.17)\,\Delta t/T + (0.1311/E1)\,(V_T + 2V_D)} \\ + (0.00838/E1)\,(R_T + 2R_D)\,I_m, \end{aligned} \tag{15}$$

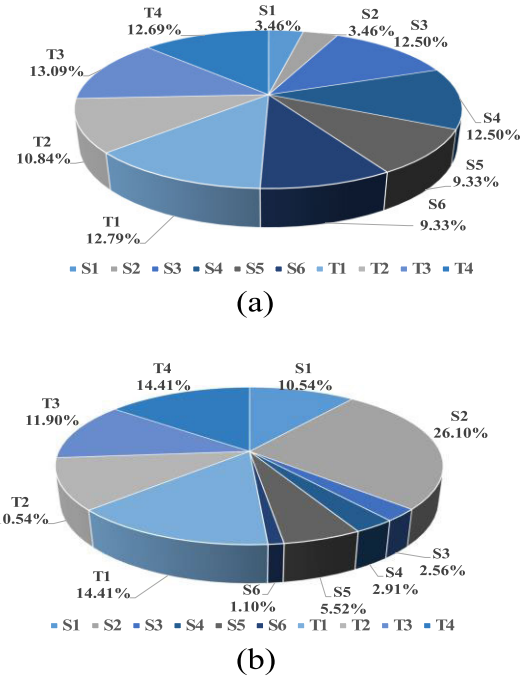

FIGURE 6. Losses of switches in the proposed structure, (a) Conductive losses. (b) Switching losses.

For example, $E_1 = 50V$, which means a maximum output voltage of 350V and Im=100A, considering Δt=1us, T=20ms, and $V_T + 2V_D = 3.5V$ $R_T + 2R_D = 90m\Omega$, the maximum efficiency is 99%, and the conduction losses are dominant. Improving the switches can produce even better efficiency.

3) SIMULATION RESULTS

The following parameters are considered to calculate the efficiency of the proposed module: $V_T = 1.5V$, $V_D = 1V$, $R_T = 0.033\Omega$, $R_D = 0.06\Omega$, $t_{on} = t_{off} = \Delta t = 1\mu s$, $Vo_{rms} = 56V$, Pout=65W and f = 50Hz, $E_1 = 12V$. The load is series RL = 48Ω+125 μH. These parameters were selected in order to compare with the experimental results. The basic unit (Fig. 1.a) was simulated in MATLAB/Simulink. The converter's output voltage is a sinusoidal signal at 50 Hz. This converter has 28 transitions in each period (20ms), as shown in Fig. 1.b. The simulated efficiency is 94.2%, which matches the theoretical calculations.

The THD is defined as:

$$THD = \frac{\sqrt{\sum_{h=2,3,4,5,\ldots}^{\infty} V_{oh}^2}}{V_{o1}} = \sqrt{\left(\frac{V_{o,rms}}{V_{o1}}\right)^2 - 1}, \quad (16)$$

where h is the harmonic order, h = 1 is corresponds to the main frequency. As the waveform is completely symmetric, the even harmonics are zero. V_{oh} and V_{o1} are the hth-order harmonic and fundamental harmonic RMS values of the output voltage waveform. Furthermore, V_{orms} is the total RMS value of the output voltage. V_{o1} and $V_{o,rms}$ can be calculated

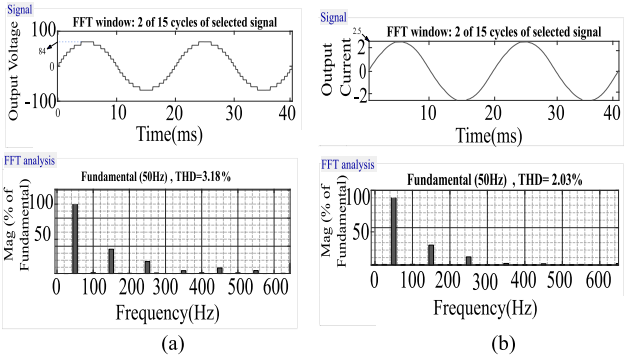

FIGURE 7. Simulation results (a) Output voltage. (b) Output current.

using:

$$V_{o,rms}^2 = \frac{4E1^2}{2\pi}\left(-\alpha_1 - 3\alpha_2 - 5\alpha_3 - \ldots - (2n-1)\,\alpha_n - (2N_{level}-1)\,\alpha_{\frac{Nlevel-1}{2}} + \left(\frac{N_{level}-1}{2}\right)^2 \frac{\pi}{2}\right) \quad (17)$$

and, if the number of levels is large, the first harmonic can be estimated as:

$$V_{o1} = \left(\frac{N_{level}-1}{2}\right)\frac{E1}{\sqrt{2}}. \quad (18)$$

By considering (16)-(18), it is observed that the THD value depends on the switching angles and the number of levels. It is clear that if the number of levels is increased, the output waveform will be similar to a sinusoidal waveform, and the THD value will decrease. Fig. 7. shows the simulation results for output voltage and current with the proposed structure. The THD value for voltage and current is 3.18% and 2.03%. The THD of the current is slightly lower than the THD of the voltage because the R-L load acts as a filter.

III. CONTROL MODULATION METHOD

Several modulation techniques have been analyzed and applied to multilevel converters, such as Carrier-Based (CB) PWM, Selective Harmonic Elimination (SHE) PWM, and Space Vector (SV) PWM. CBPWM needs various carrier signals to achieve gate pulses and causes higher switching losses. In SVPWM, the algorithm's complexity will increase as the number of levels at the output rises. Likewise, using SHEPWM, the estimation of switching angles becomes very complex as the number of levels increases [22]–[24].

The nearest level control (NLC) is a low switching frequency PWM method [25], where the calculation time is reduced. So, it is a simple control algorithm attractive for a high number of levels.

The nearest output voltage level, $vlevel_n$ can be determined as:

$$vlevel_n = round(v_{ref}/E_1), . \quad (19)$$

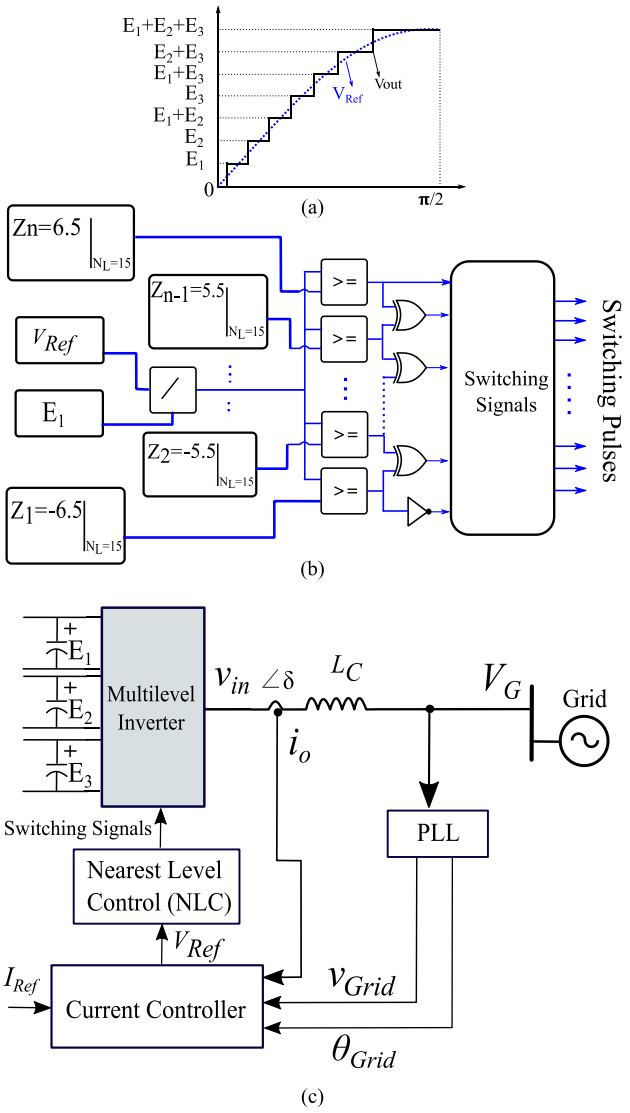

FIGURE 8. Nearest level control (NLC) with (a) sampled reference voltage and (b) simplified NLC implementation (c) Control block diagram of the grid-connected inverter.

TABLE 3. Output voltage of proposed cascade multilevel converter topology ($0<\omega t<\pi/2$).

State	Switching pattern	Output voltage
1	S_{11}, T_{11}, T_{31}, S_{12}, T_{12}, T_{32}	0
2	S_{11}, T_{11}, T_{21}	E_{11}
3	S_{51}, S_{61}, T_{11}, T_{31}	E_{21}
4	S_{51}, S_{61}, T_{11}, T_{21}	$E_{11}+E_{21}$
5	S_{11}, T_{31}, T_{41}	E_{31}
6	S_{11}, T_{21}, T_{41}	$E_{31}+E_{11}$
7	S_{51}, S_{61}, T_{11}, T_{21}	$E_{31}+E_{21}$
8	S_{51}, S_{61}, T_{11}, T_{41}	$E_{11}+E_{21}+E_{31}$
9	S_{11}, T_{11}, T_{21}, S_{12}, $T1_1$, T_{32}	$E_{12}+E_{11}$
.	.	.
.	.	.
.	.	.
62	S_{51}, S_{61}, T_{21}, T_{41}, S_{52}, S_{62}, T_{32}, T_{42}	$E_{12}+E_{13}+E_{32}+E_{22}+E_{12}$
63	S_{51}, S_{61}, T_{11}, T_{41} , S_{52}, S_{62}, T_{12}, T_{42}	$E_{11}+E_{21}+E_{31}+E_{12}+E_{22}+E_{32}$

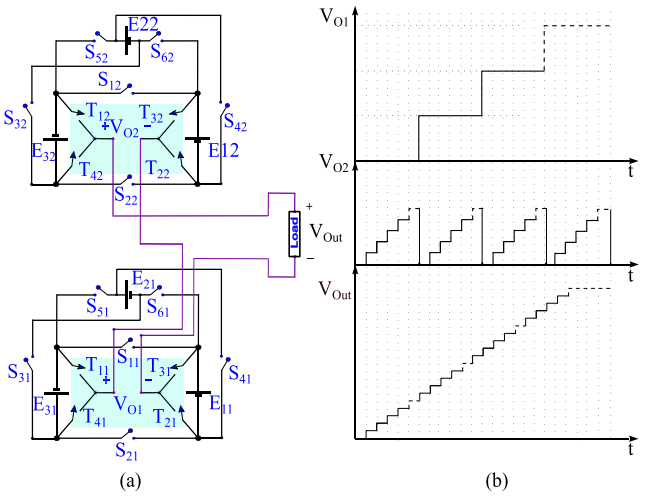

FIGURE 9. (a) Cascaded structure with two stages of the proposed converter. (b) Output voltage for each stage and total output voltage.

where v_{ref} is the reference voltage and E_1 is the lowest level, and (19) gives the nearest integer. Fig. 8 shows the scheme of a simplified NLC implementation. The level is chosen in order to be as close as possible to the reference signal (Fig.8.a).

Fig. 8.b shows the control diagram in order to select the proper level, where

$$z_n = n - 7.5 \quad for\ n = [1, 2, \ldots (N_L - 1)]. \qquad (20)$$

The reference signal, v_{ref}=V sin (ωt), is divided by E1, and then after many comparisons, the proper level is selected.

The comparators must also turn on the switching pattern of the highest level that satisfies the condition, which is why the x-or gates are added. Once the switching pattern is selected, the switching signal block generates the proper signals.

Although the focus of the paper is to present the new topology, it is of interest to show the grid connection. Fig. 8.c shows how the inverter can be connected to the grid. The control loop is a traditional dq-frame current controller with a PLL as is shown. The coupling inductor (L_C) avoids high currents and aids to proper track the output current. The current controller compares the current reference (I_{Ref}) with the measurement current (i_o) and sends the output voltage signal (V_{Ref}) to the NCL controller to adjust the triggering angles α_n in order to have the proper inverters' output voltage (v_{in}).

IV. CASCADING OF THE PROPOSED STRUCTURE

In order to reach higher voltages, increase the power rating, as well as the number of voltage levels, and decrease the voltage stress on power semiconductors in multilevel inverters, a cascaded structure is proposed. The cascading technique is useful in photovoltaic and grid-tied systems due to the PV energy system's capability of synthesizing stepped AC

output voltage from several DC sources. However, due to the unequal DC inputs, the complexity of control increases, particularly for solar application including partial shaded conditions.

Fig. 9.a shows the proposed cascaded structure with two stages. Fig. 9.b shows part of the output voltage for each stage(V_{O1}, V_{O2}) and the total output voltage (V_{Out}). The cascaded structure's switching pattern, which has 63 states to produce a positive cycle, is shown in Table 3. In a cascaded structure, every basic unit's switch pattern is different from each other because it has a different value in its output voltage. Moreover, Table 3 shows the output voltage as a function of the switching state. The output voltage of the cascaded structure is the sum of every unit stage. Thus,

$$V_{out} = V_{o1} + V_{o2} + \cdots + V_{oN} \tag{21}$$

where $V_{o1}, V_{o2}, \ldots, V_{oN}$ are the output voltages of every single unit connected in series. The maximum output voltage is:

$$V_{o,max} = E_{11} + E_{21} + E_{31} + E_{12} \ldots + E_{3N} \tag{22}$$

where the first index is the DC source in each stage (1,2 and 3) and the second index is the number of stages from 1 to N. Two algorithms are described for determining the values of the cascaded structure DC input sources.

Algorithm 1 (Equal DC Input Sources): In this algorithm, the values of DC sources in each unit are the same:

$$E_{1i} = E_{2i} = E_{3i} = Vdc. \tag{23}$$

The number of output voltage levels, including positive, negative, and zero states are:

$$N_{Levels} = 6i + 1 \quad i = 2, 3, 4, \ldots, N \tag{24}$$

where i is the number of stages. The maximum amplitude of the output voltage is:

$$V_{o,max} = 3iVdc \quad i = 2, 3, 4, \ldots, N \tag{25}$$

Using this algorithm, there are many independent DC sources, but all of them have the same output voltage, which reduces the complexity of the auxiliary DC side.

Algorithm 2 (Non-Equal DC Input Sources): The DC sources of each basic unit are non-equal in the second algorithm. For the first unit, the DC sources are determined as follows (1):

$$E_{11} = VdcE_{21} = 2E_{11}, \quad E_{31} = 2E_{21}, \tag{26}$$

for the second stage

$$E_{12} = \frac{E_{11}}{8}, \quad E_{22} = 2E_{12}, \; E_{32} = 2E_{22}. \tag{27}$$

This algorithm extracts all the advantages of the basic unit presented in Section II. Moreover, if the structure has more than two stages, for k-th stage

$$E_{1k} = \frac{E_{1(k-1)}}{8}, \quad E_{2k} = 2E_{1k}, \; E_{3k} = 2E_{2k}. \tag{28}$$

TABLE 4. Comparison of several cascaded multilevel topologies (N_L = Number of levels).

	Number of switches	Number of diodes	Number of DC links / sources	TSV*xVdc
CHB	$2(N_L - 1)$	$2(N_L - 1)$	$(N_L - 1)/2$	$2(N_L - 1)$
NCML[9]	$N_L + 3$	$N_L + 3$	$(N_L - 1)/2$	$3(N_L - 1)$
2CLHB[10]	$N_L + 1$	$N_L + 1$	$(N_L - 1)$	$2(N_L - 1)$
CSMLI[11]	$N_L + 1$	$N_L + 1$	$(N_L - 1)/2$	$2(N_L - 1)$
K-Type[17]	$14\left(\frac{N_L - 2}{12} + 1\right)$	$14\left(\frac{N_L - 2}{12} + 1\right)$	$2\left(\frac{N_L - 2}{12} + 1\right)$	$32\left(\frac{N_L - 2}{12} + 1\right)$
ST-Type[27]	$12 \log_{17} N_L$	$12 \log_{17} N_L$	$4 \log_{17} N_L$	$5\left(\frac{N_L - 1}{2}\right)$
Novel H-Bridge [14]	$2 \log_2 N_L + 1$	$2 \log_2 N_L + 1$	$\log_2\left(\frac{N_L + 1}{2}\right)$	$2(N_L - 1)$
Proposed Structure using Fig. 5.a	$3 \log_2 N_L$	$12 \log_2 N_L$	$\frac{9}{10} \log_2 N_L$	$17(N_L - 1)/20$

The number of output voltage levels can be calculated as follows:

$$N_{Levels(i)} = 2\left[8\left(\frac{N_{Levels(i-1)} - 1}{2}\right) + 7\right] + 1$$
$$i = 2, 3, 4, \ldots, k \quad \text{is the number of stages,} \tag{29}$$

where $N_{Levels(1)} = 15$. For example, to determine the output voltage levels of two stages in the cascaded structure, we have:

$$i = 2, \quad N_{Levels(1)} = 15 \rightarrow N_{Levels(2)} = 127 levels. \tag{30}$$

The maximum output voltage is

$$V_{o,max} = \left(\frac{N_{Levels(i)} - 1}{2}\right) Vdc. \quad i = 2, 3, 4, \ldots, k. \tag{31}$$

These two algorithms have some advantages and drawbacks. In the equal input sources algorithm, switching losses are low because the number of transitions within a period are reduced about 20 times for the two stage case compared to the non-equal sources algorithm (28 transitions vs. 255 transitions). However, the non-equal case transitions occur at different voltages, so some units have higher switching losses than others due to the differences in the input DC sources. To conclude the 2nd algorithm has much more levels, so much lower THD, with slightly more un-equally distributed switching losses, and much higher complexity in the input DC side in order to produce more different DC levels. According to the application and the available inputs, the proper algorithm must be chosen, reminding that the dominant losses are the conducting losses.

V. COMPARISON OF PROPOSED STRUCTURE WITH OTHER TOPOLOGIES

The proposed cascaded multilevel inverter is compared with several cascaded multilevel inverters that have been presented in the literature. Table 4 compares the number of

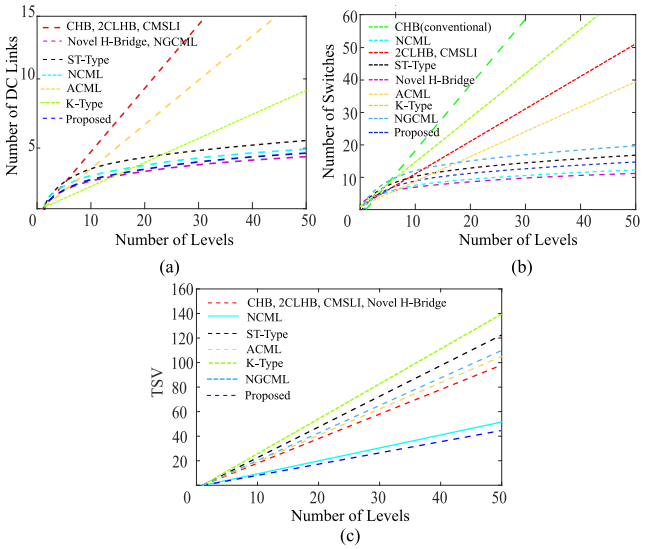

FIGURE 10. Comparative studies: The number of (a) DC links, (b) switches, and (c) TSV in terms of the number of levels.

switches, diodes, DC voltage sources (or DC links), and TSV, which indicates the maximum blocking voltage across each semiconductor device. The second algorithm presented in Section IV was used for comparison.

Table 4 includes the conventional cascaded H-bridge converter (CHB), multilevel DC links (NCML) [9], two capacitor links H-bridge (2CLHB) [10], crossing switch multilevel inverter (CSMLI) [11], Novel H-Bridge [14], K-Type [17], and square T-Type topology (ST-Type) inverter presented in [27]. The number of switches, the number of DC links and TSV are reduced down to $3\log_2 N_L$, $\frac{9}{10}\log_2 N_L$ and $17(N_L-1)/20$ respectively, for the proposed structure. On the other hand, in the proposed structure, the number of diodes is more than other topologies because a bridge of diodes with a single IGBT has been used as a bidirectional switch (Fig. 5.a).

Fig. 10.a compares the number of DC voltage sources in the proposed topology with other cascaded multilevel inverters, in terms of the number of levels. It shows that the proposed cascaded inverter needs a lower number of DC voltage sources than CHB, 2CLHB [10], and CMSLI [11] (which have the same number) and the ACML [13], K-Type [17] and ST-Type [27]. The number of DC voltage sources is similar in the proposed topology, NGCML [31], and novel H-Bridge [14]. This comparison shows that the proposed converter has a low number of isolated DC inputs.

Fig. 10.b compares the number of switches in the proposed topology with other cascaded multilevel inverters. It is clear that the proposed topology requires lower number of switches compared with most of the mentioned topologies, except for Novel H-Bridge and NCML. In Fig. 10.c, it can be seen that the proposed structure has the lowest TSV compared to other references.

Table 5 shows a comparison of several multilevel topologies. It can be seen that the proposed topology offers better characteristics than the other structures.

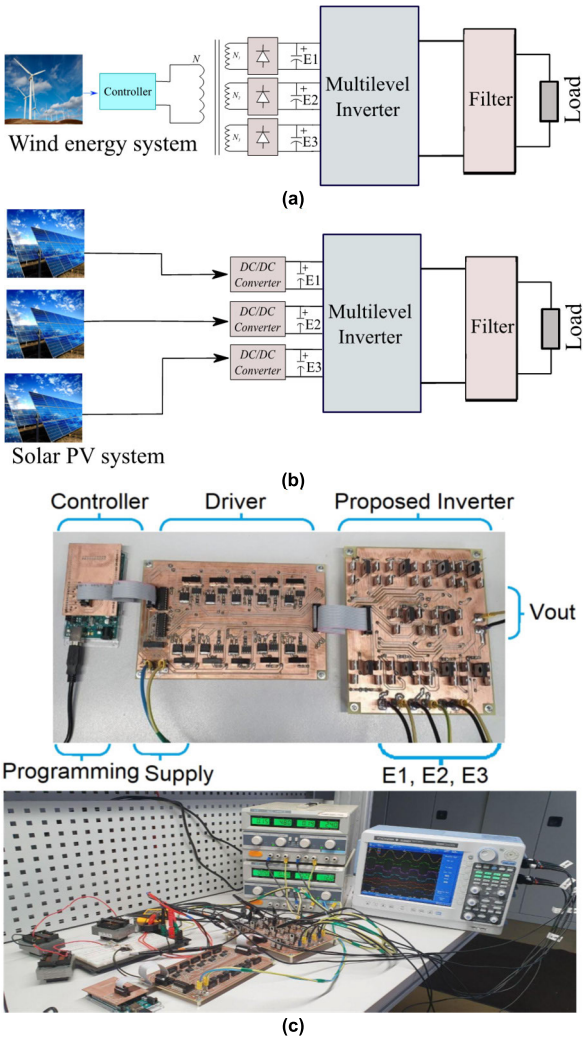

FIGURE 11. Hardware to create multiple DC sources (a) Multi tap transformer, (b) DC/DC converters [19], [28], (c) Prototype of the proposed structure.

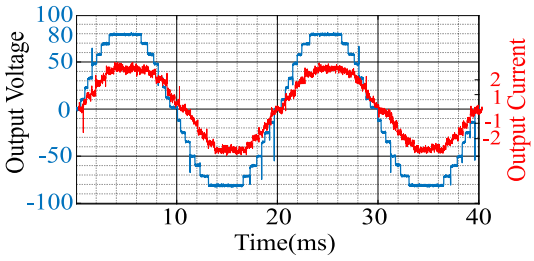

FIGURE 12. Experimental results: Output voltage (blue) and Output current (red).

VI. EXPERIMENTAL RESULTS

Experiments on a real prototype, based in Fig. 1.a, were conducted. Fig. 11.c shows the prototype, and Table 6 lists the converter's main components. The prototype has three parts: the first one is the control part, which is based on the Atmel SAM3X8E ARM Cortex-M3 microcontroller. In this controller, Table 1 is used for programming and generating the

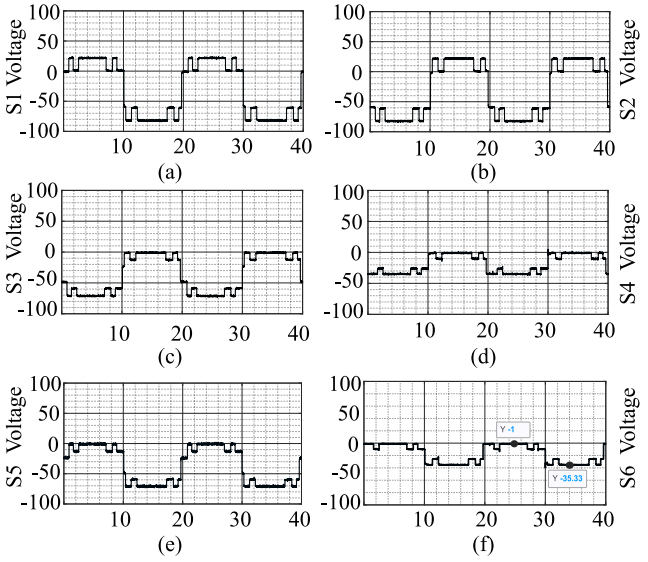

FIGURE 13. Experimental results: voltage on (a) S1, (b) S2, (c) S3, (d) S4, (e) S5, and (f) S6 switches.

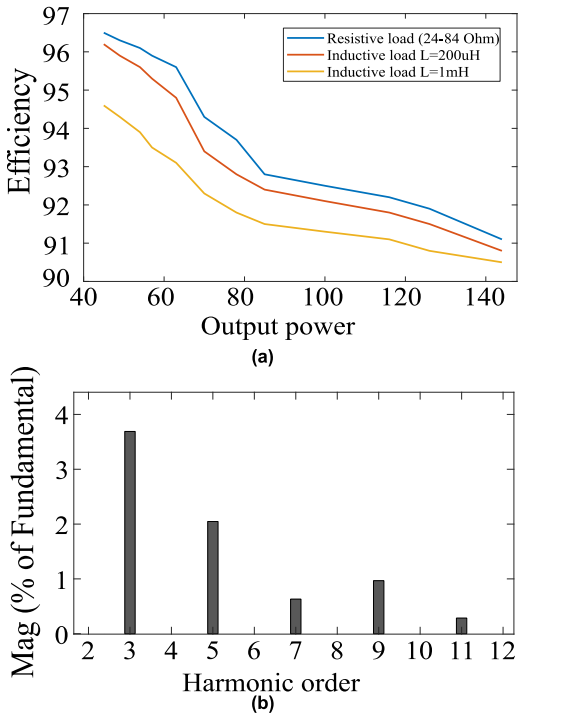

FIGURE 14. Experimental results: (a) Measured efficiency against output power at different loads, (b) Measured FFT of the output voltage.

signals to trigger the switches in order to obtain a sinewave in the output. The second part is the driver stage, which includes isolation and negative bias. The last part is the power section, containing the proposed structure to convert DC voltage sources to AC voltage on the load. This part needs isolated DC inputs.

The optimal methods to generate DC inputs are isolated DC/DC converters and multi tap transformer [19], [28]–[30].

TABLE 5. Comparison of several multilevel topologies (Low(L), Medium(M), High(H)).

	METHOD OF CONTROL	THD	Efficiency	TSV	Losses
NCML[9]	FUNDAMENTAL FREQUENCY SWITCHING	M	M	H	M
2CLHB[10]	PWM	L	M	L	M
CSMLI[11]	FUNDAMENTAL FREQUENCY SWITCHING	M	H	L	L
ST-Type[27]	NEAREST LEVEL CONTROL	L	H	H	L
K-Type[17]	NEAREST LEVEL CONTROL	M	H	H	L
ACML[13]	SELECTIVE HARMONIC ELIMINATION	L	M	H	M
Novel H-Bridge [14]	PWM	L	M	L	M
NGCML[31]	SPWM	H	M	H	M
Proposed Structure using Fig. 6.a	NEAREST LEVEL CONTROL	L	H	L	L

TABLE 6. Experimental components.

Components	Type
Power Stage	**Proposed Inverter**
Voltage source(DC)	12, 24, 48 V
Diode	RURP860
IGBT	FGH40N60SFDTU
Capacitor	T491C225M035AT
Load	Variable resistor from R=[24-84]Ohm, L=[200-1000]μH
Gate drive	HCPL3120

Fig. 11.a shows how to provide DC sources using a multi-winding transformer and rectifying units; so only one source is needed, and Fig. 11.b shows a similar approach using DC/DC converters, where multiple sources can be connected.

Fig. 12 shows the experimental results for output voltage and current. There are some voltage spikes during the switching processes due to the switches' dead time; during a small time interval, bidirectional switches are off, so the current flows through a snubber circuit. The magnitude of the peaks depends on the amplitude of the load current and the snubber design. Due to the voltage drop on switches, the maximum output voltage is close to 80V instead of 84V. In the experiments, the voltage spikes induce some noise in the current probe as well, which is not really present in the circuit.

Fig. 13 shows the voltages on the S1, S2, S3, S4, S5, and S6 switches. Based on Fig. 13, it is possible to calculate the voltage stress on each switch. For example, in Fig. 13.a and 13.d, the voltage stresses for S1 and S4 are 84V and 36V.

Fig. 14.a shows the measured efficiency versus output power at different loads. When the output power increases, the efficiency decreases mainly due to the conduction losses.

Fig. 14.b shows the FFT of the measured output voltage. It can be seen that the output voltage contains many harmonics but low in magnitude. The results correspond to the maximum power for the load in Table 6. Both efficiency and THD are in concordance with the theoretical analysis and simulation results. The theoretical analysis predicts an efficiency of 94%, while experimental results show 93.8% at 65W. The simulated THD was 3.18% for the output voltage at maximum power, while in the prototype, it was 4.5%. The difference can be attributed to the switches' dead times. For higher voltage applications, efficiency can be much higher because the voltage drops in the diodes and switches do not increase with the output voltage, so the ratio between voltage drops in switches and the output signal is reduced and efficiency increases.

VII. CONCLUSION

A new topology for multilevel inverter was described in this paper for renewable energy sources and industrial loads applications. The basic unit of the proposed topology can generate 15 levels with a reduced number of components and three DC inputs. The low number of components leads to a reduction in size, a simple control strategy, and high efficiency. The conduction and switching losses of the proposed 15-level inverter operating under the nearest level modulation technique were determined theoretically.

The paper also suggests a cascade connection of basic units leads to achieving more output voltage levels.

The proposed topology was compared with many other multilevel topologies. As a result, it shows the advantages of less TVS, reduced number of switches, and fewer DC sources. The comparison results indicate that the cascaded structures could overcome some of the disadvantages of other topologies, which reveals that the proposed topology significantly reduces the number of DC links and power switches compared to CHB, 2CLHB, and CSMLI.

Finally, the proposed structure has the lower number of DC-link sources, TSV, and THD among the mentioned topologies. Theoretical analysis were verified by simulation and experimental results in a 15-level inverter prototype.

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