

Received June 2, 2021, accepted June 21, 2021, date of publication June 25, 2021, date of current version July 5, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3092439

Event Circular Waits and Their Analysis via Petri Nets

XING FAN¹, BENYUAN YANG¹, AND HESUAN HU^{1,2}, (Senior Member, IEEE)

¹School of Mechano-Electronic Engineering, Xidian University, Xi'an, Shaanxi 710071, China

²State Key Laboratory for Manufacturing Systems Engineering, Xi'an Jiaotong University, Xi'an, Shaanxi 710054, China

Corresponding author: Hesuan Hu (huesuan@gmail.com)

This work was supported in part by the National Natural Science Foundation of China under Grant 61973242, Grant 61573265, and Grant 61203037; in part by the Fundamental Research Funds for the Central Universities under Grant K7215581201, Grant K5051304004, and Grant K5051304021; in part by the New Century Excellent Talents in University under Grant NCET-12-0921; in part by the Academic Research Fund Tier 1 by Ministry of Education in Singapore under Grant 2014-T1-001-147; in part by the Academic Research Fund Tier 2 by Ministry of Education in Singapore under Grant MOE2015-T2-2-049; and in part by the Major Fundamental Research Program of the Natural Science Foundation of Shaanxi Province under Grant 2017ZDJC-34.

This work did not involve human subjects or animals in its research.

ABSTRACT Deadlock control of automated manufacturing systems has been widely investigated in recent decades. According to classical Coffman theory, resource circular wait (RW) is viewed as a necessary condition for deadlocks to occur. However, the fact is not as simple as so. Counterexamples are presented to show that RWs do not necessarily appear together with deadlocks. Event circular waits (EWs) are proposed as an alternative to represent a fundamental necessary condition of deadlocks. First, we present the formal definitions of EWs in a type of Petri nets, i.e., weighted augmented marked graphs (WAMGs), and show that EWs are more general and essential than RWs in describing the cause of deadlocks. Second, we show a new classification of siphons, i.e., types I, II, III, and IV, and illustrate the relationship between undermarked siphons and EWs in the WAMGs. Third, we show that EWs are more efficient than RWs for deadlock avoidance since deadlocks can be avoided earlier at a specified marking by using EWs rather than RWs. Several examples are given to clarify the theory throughout this paper.

INDEX TERMS Event circular waits, Petri nets, siphons, deadlock avoidance.

I. INTRODUCTION

Due to the continuous improvement of requirements for products, automated manufacturing systems (AMSs) emerge with the assistance of computer science and automatic control technologies. AMSs are widely used in industrial field since they not only facilitate industry automation but also promote diversified production. With the gradual realization of electrification and informatization, the potential for AMSs is enormous.

Deadlocks are particularly important problems in large-scale AMSs because they may destroy the stable performance of AMSs [4], [16], [17], [20], [21], [28], [29]. Deadlocks can lead some processes to indefinitely wait, which prevents them from moving forward and directly cause a sharp decline in productivity

The associate editor coordinating the review of this manuscript and approving it for publication was Her-Terng Yau.

[1], [7], [8], [10], [16]–[18], [20], [38]. Moreover, a process unnecessarily using the scrambled resources can be blocked by these processes in stagnation. In the worst case, a whole system may fall into a deadlock [5], [23], [24], [34]–[36], [39]–[41]. Therefore, deadlock problems should be solved in both design and application of AMSs.

Resource circular wait (RW) refers to a circular chain consisting of several processes, where each of these processes is waiting for resources held by the next process in this circular chain. Based on Coffman theory, RW is treated as one of four necessary conditions for deadlocks to occur. In accordance with this statement, there must be an RW if there exists a deadlock. Conversely, there will be no deadlock if no RW appears. Hence, the most widely used method for deadlock prevention is to break RWs through manual intervention. Specifically, the phenomenon that a process is waiting for resources is allowed to appear, while the circular chain of these waiting processes is prevented by establishing the

priority of resource allocation. However, almost all existing works assume default RW conditions [2], [21] are the cause of deadlocks, namely, some processes require some resources held by others that will never be released. This claim is certainly true in most resource-sharing systems due to the competition for limited resources among multiple processes. However, in some concrete systems, e.g., non-resource allocation systems, such behavior cannot be found. This implies that RWs are not always suitable for describing the cause of deadlocks. This motivates us to explore a more general and essential cause of deadlocks.

In this paper, we propose a different kind of circular wait, namely, event circular waits (EWs). EWs can substitute RWs as an alternative necessary condition for a deadlock to occur. Our approach and its main contributions are elaborated as follows.

First, we propose the definition of EWs in weighted augmented marked graphs (WAMGs). An EW is an event circular chain where each event waits for the next event in the chain to execute. EWs are more general than RWs since EWs can describe some situations causing deadlocks that cannot be explained by RWs. Furthermore, we illustrate under what conditions an EW can occur in a net system.

Second, we explore the relationship between undermarked siphons and EWs since both siphons and EWs in PNs are employed as the structural characteristics of deadlock. Before that, we show a new classification of siphons in the WAMGs. We illustrate the characteristic of four types of siphons of WAMGs. A necessary and sufficient condition is established between undermarked siphons and EWs.

Third, we investigate the application of EWs for deadlock avoidance. We show that EWs occur before RWs starting from a specified state; and EWs and RWs are generated simultaneously only in a few cases. Based on this fact, we show that deadlocks can be avoided earlier at a specified state by using EWs rather than RWs. Then, an effective approach to avoiding deadlocks is proposed based on EWs.

The remainder of this paper is organized as follows. Section II introduces the definitions of PNs. Section III proposes the definition of EWs and a new classification of siphons, and illustrates the relationship between undermarked siphons and EWs in the WAMGs. Section IV presents a method based on EWs to avoid deadlocks. Section V summarizes this paper and elaborates future work.

II. PRELIMINARIES

Let $\mathbb{N} = \{0, 1, 2, \dots\}$ be the set of non-negative integers and $\mathbb{N}^+ = \{1, 2, \dots\}$ be the set of positive integers. Given $n \in \mathbb{N}^+$, then let $\mathbb{N}_n = \{1, 2, \dots, n\}$ be the set of integers from 1 to n .

A. PNs DEFINITIONS

A PN is $N = (P, T, F, W)$ where P is a set of places, T is a set of transitions, $F \subseteq (P \times T) \cup (T \times P)$ is a set of directed arcs, and $W: (P \times T) \cup (T \times P) \rightarrow \mathbb{N} = \{1, 2, \dots\}$, such that $P \cup T \neq \emptyset$, $P \cap T = \emptyset$, and $W(x, y) = 0$ if $(x, y) \notin F$. $W(x, y)$ is undefined if $x, y \in P$ or $x, y \in T$. A marking of N

is a mapping $M: P \rightarrow \mathbb{N}^{|P|}$. It can be represented by tokens located at various places. $M(p)$ (resp., $M_0(p)$) indicates the number of tokens in p at M (resp., M_0). M_0 denotes the initial marking. (N, M_0) is a net system with an initial marking M_0 .

The preset of a node $x \in P \cup T$ is defined as $\bullet x = \{y \in P \cup T \mid (y, x) \in F\}$. Its postset $x^\bullet = \{y \in P \cup T \mid (x, y) \in F\}$. ${}^{(n)}x$ (resp., $x^{(n)}$) is the n -order preset (resp., n order postset) of x . N is a marked graph if $W: F \rightarrow \{1\}$ and $\forall p \in P, |\bullet p| = |p^\bullet| = 1$. N is strongly connected if there exists a directed path from every node to every other node in $P \cup T$.

t is enabled at M , denoted by $M[t]$, if $\forall p \in \bullet t, M(p) \geq W(p, t)$. Given a marking M , t can fire if it is enabled at M . M' is reachable from M , denoted by $M[\sigma] M'$, if there exists a firing sequence $\sigma = \langle t_1, t_2, \dots, t_n \rangle$ such that $M[t_1] M_1 \dots [t_n] M'$. $\vec{\sigma}$ is a $|T|$ -dimensional firing count vector where $\vec{\sigma}(t)$ states the number of t 's appearances in σ . Precisely, this evolution can be described by $M' = M + [N] \cdot \vec{\sigma}$. The set of all markings reachable from M_0 is denoted by $R(N, M_0)$. It follows a necessary reachability condition, i.e., $M = M_0 + [N] \cdot \vec{\sigma}$. When $|\sigma| = 1$, we have $M[t] M'$, implying t 's firing at M can lead to M' . $t \in T$ is live under M_0 if $\forall M \in R(N, M_0), \exists M' \in R(N, M), M'[t]$ holds. t is dead at $M \in R(N, M_0)$ if $\nexists M' \in R(N, M)$ so that $M'[t]$ holds. Deadlock markings include partially and totally dead ones. $M \in R(N, M_0)$ is a totally deadlock marking if $\forall M' \in R(N, M), \forall t \in T, \neg M'[t]$, where $M \neq M_0$. (N, M_0) is deadlock-free if $\forall M \in R(N, M_0), \exists t \in T, M[t]$. It is livelock if it is deadlock-free and $\exists t \in T$ so that t is dead at $M \in R(N, M_0)$. The marking M which indicates a livelock is said to be a partially deadlock marking.

A nonempty set $S \subseteq P$ (resp., $Q \subseteq P$) is a siphon (resp., trap) if $\bullet S \subseteq S^\bullet$ (resp., $Q^\bullet \subseteq \bullet Q$). A strict minimal siphon is a siphon containing neither other siphons nor traps except itself. A siphon is undermarked at M if $\exists t \in S^\bullet$ such that t is dead at M .

A P - (resp., T -) vector is a column vector $I: P$ (resp., $J: T$) $\rightarrow \mathbb{Z}$ indexed by P (resp., T), where \mathbb{Z} is the set of integers. A P -vector $I \neq \mathbf{0}$ becomes a P -invariant if $[N]^T \cdot I = \mathbf{0}$, where $\mathbf{0}$ means a vector of zeros. By $I \geq \mathbf{0}$, we mean that $\forall p \in P, I(p) \geq 0$ and $\exists p \in P, I(p) > 0$. A P -invariant is called a P -semiflow if $I \geq \mathbf{0}$. $\|I\| = \{p \in P \mid I(p) \neq 0\}$ is called the support of I . A P -semiflow I (resp., T -semiflow J) is said to be minimal if there exists no other P -semiflow I' (resp., T -semiflow J') such that $\|I\| \supset \|I'\|$ (resp., $\|J\| \supset \|J'\|$).

B. WAMGs

Definition 1: A WAMG is a PN $N = (P, T, F, W)$ such that:

- 1) $P = P_0 \cup P_A \cup P_R$, in which P_0 is a set of idle places such that $P_0 = \bigcup_{i \in \mathbb{N}_K} \{p_{0i}\}$; P_A is a set of activity places such that $P_A = \bigcup_{i \in \mathbb{N}_K} \{P_{A_i}\}$. $\forall i, j \in \mathbb{N}_K, i \neq j, P_{A_i} \cap P_{A_j} = \emptyset$; and $P_R = \bigcup_{i \in \mathbb{N}_L} \{r_i\}$ is a set of resource places. $\forall p \in P_0 \cup P_A, |p^\bullet| = |\bullet p| = 1$;
- 2) $T = T_A = \bigcup_{i \in \mathbb{N}_K} \{T_i\}$, $\forall i \in \mathbb{N}_K, T_i \neq \emptyset$, and $\forall i, j \in \mathbb{N}_K, i \neq j, T_i \cap T_j = \emptyset$;

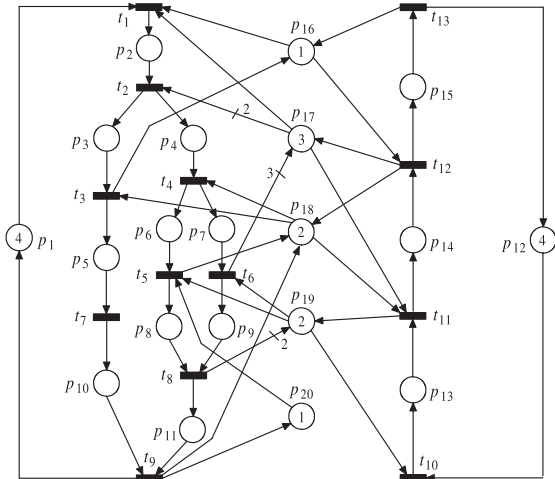


FIGURE 1. A WAMG.

- 3) $F = \bigcup_{i \in \mathbb{N}_K} \{F_i\} = F_0 \cup F_A \cup F_R$, in which $F_0 \subseteq (P_0 \times T_A) \cup (T_A \times P_0)$, $F_A \subseteq (P_A \times T_A) \cup (T_A \times P_A)$, and $F_R \subseteq (P_R \times T_A) \cup (T_A \times P_R)$;
- 4) For each $i \in \mathbb{N}_K$, $\bar{N}_i = N \setminus (\{p_{0_i}\} \cup P_{A_i}, T_i, F_i)$ is a strongly connected marked graph such that every circuit includes p_{0_i} ;
- 5) $\forall r \in P_R, \exists$ a unique minimal P -semiflow $X_r \in \mathbb{N}^{|P|}$ such that $\{r\} = \|X_r\| \cap P_R, P_0 \cap \|X_r\| = \emptyset, P_A \cap \|X_r\| \neq \emptyset$, and $X_r(r) = 1$; and
- 6) $X_r(p)$ is not necessarily binary, i.e., $\exists f \in F_R \subseteq (P_R \times T_A) \cup (T_A \times P_R)$ such that $w(f) \geq 1$.

Definition 2: M_0 is said to be an acceptable initial marking of N such that:

- 1) $\forall p_0 \in P_0, M_0(p_0) \geq 1$;
- 2) $\forall p \in P_A, M_0(p) = 0$;
- 3) $\forall r \in P_R, \forall p \in P_A, M_0(r) \geq X_r(p)$, where X_r is r 's minimal P -semiflow; and
- 4) $M_0(r) \geq \sum_{p \in P_\Sigma} X_r(p)$, where all p in P_Σ can use r simultaneously at a state.

Fig.1 exemplifies an acceptably marked WAMG, where $P_0 = \{p_1, p_{12}\}, P_{A_1} = \{p_2 - p_{11}\}, P_{A_2} = \{p_{13} - p_{15}\}, P_R = \{p_{16} - p_{20}\}, T_1 = \{t_1 - t_9\}$, and $T_2 = \{t_{10} - t_{13}\}$. There are 5 P -semiflows corresponding to the resource places, i.e., $X_{p_{16}} = p_2 + p_3 + p_{15} + p_{16}, X_{p_{17}} = p_2 + 3 \cdot p_4 + 3 \cdot p_7 + p_{14} + p_{17}, X_{p_{18}} = p_5 + p_6 + p_{10} + p_{14} + p_{18}, X_{p_{19}} = p_8 + p_9 + p_{13} + p_{19}$, and $X_{p_{20}} = p_8 + p_{11} + p_{20}$.

Definition 3: A transition $t \in T$ is resource disabled at $M \in R(N, M_0)$ iff $\bullet t \cap P_R \neq \emptyset$ and $\exists r \in \bullet t \cap P_R$ such that $M(r) < W(r, t)$. A transition t is process disabled at $M \in R(N, M_0)$ iff $\bullet t \cap (P_0 \cup P_A) \neq \emptyset$ and $\exists p \in \bullet t \cap (P_0 \cup P_A)$ such that $M(p) = 0$.

Definition 4: If a transition $t \in T$ can be fired by $r \in P_R$ and the resources in r are occupied after t is fired, then t holds the resources in r .

Definition 5: $\forall i \in \mathbb{N}_{n-1}, \langle x_1, x_2, \dots, x_n \rangle$ is said to be a path in PNs such that $x_{i+1} \in x_i^\bullet$, where $\forall x \in \{x_1, x_2, \dots, x_n\}, x \in P \cup T$. The path from x_1 to x_n is said to be an elementary path.

Definition 6: $\langle x_1, x_2, \dots, x_n \rangle$ is a circuit if: 1) all nodes except x_1 and x_n are different; and 2) it is an elementary path and $x_1 = x_n$. The circuit is generally represented by C , while the circuit containing node x is denoted as $C(x)$. The support of the circuit C is denoted as $\|C\|$.

Definition 7: Let U represent a T -invariant. If \exists an elementary circuit C_U such that $\|U\| = \|C_U\| \cap T, C_U$ is called a circuit derived from a T -invariant U . A T -invariant U can derive multiple circuits.

Definition 8: The set of holders of $r \in P_R$ is the support of a P -semiflow X_r without r , i.e., $H(r) = \|X(r)\| \setminus \{r\}$.

Definition 9: A process connector (PC) refers to the activity places between two consecutive transitions in the same process, if $\exists p \in t^\bullet \cap \bullet t'$ such that $p \in P_A$, then p is said to be a process connector between t and t' , denoted as $PC(t, t')$.

III. EVENT CIRCULAR WAITS AND NEW CLASSIFICATION OF SIPHONS IN WAMGS

In this section, two novel definitions are introduced, i.e., event circular waits and new classification of siphons in the WAMGs. Further, the relationship between undemarked siphons and EWs is illustrated in the WAMGs.

A. EVENT CIRCULAR WAITS

Generally speaking, circular waits considered in existing literature refer to RWs from a process perspective. The stagnation of several processes in a circular state is attributed to the improper resource allocation among processes. However, this claim is not always true. In this paper, event circular waits (EWs) are proposed as an alternative to represent the necessary condition of deadlock.

Definition 10: An event path (EP) is an ordered transition sequence $\langle t_1, t_2, \dots, t_n \rangle$ such that: 1) $\{t_1, t_2, \dots, t_n\} \subseteq T$; and 2) $\forall i \in \mathbb{N}_{n-1} = \{1, 2, \dots, n-1\}, \bullet t_i \cap t_{i+1}^\bullet \neq \emptyset$.

Definition 11: An event circuit (EC) is an EP $\langle t_1, t_2, \dots, t_n \rangle$, where all nodes are different except $t_1 = t_n$.

Definition 12: Given a WAMG $N = (P, T, F, W)$, a resource circular wait (RW) at $M \in R(N, M_0)$ is an ordered resource place sequence $\langle r_1, r_2, \dots, r_n \rangle$ such that:

- 1) $r_1, r_2, \dots, r_n \in P_R$, and $r_1 = r_n$;
- 2) $\forall i \in \mathbb{N}_{n-1} = \{1, 2, \dots, n-1\}, \bullet r_{i+1} \cap r_i^\bullet \neq \emptyset$; and
- 3) $\forall i \in \{1, 2, \dots, n\}, \exists t \in T$ such that $r_i \in \bullet t \cap P_R$ and $M(r_i) < W(r_i, t)$.

Definition 13: Given a WAMG $N = (P, T, F, W)$, an event circular wait (EW) at $M \in R(N, M_0)$ is an EP $\langle t_1, t_2, \dots, t_n \rangle$, such that:

- 1) $t_1 \in EC_x$ (the x th EC in an EW) and $t_n \in EC_y, x, y \in \mathbb{N}^+$;
- 2) $\forall i \in \{1, 2, \dots, n\}, t_i$ is disabled at M ; and
- 3) $\forall i \in \{1, 2, \dots, n\}, \nexists EP' \langle t_a, t_b, \dots, t_c, t_i \rangle$ such that $M(\bullet t_a) \neq 0, \exists M [t_a, \dots, t_b, \dots, t_c] M'$ and $M' [t_i]$.

Remark 1: According to Definition 13, the existence of a circular chain can be explained from the view of transitions. Each transition in an EC is waiting for the execution of its previous transition. Although EWs are defined in WAMGs,

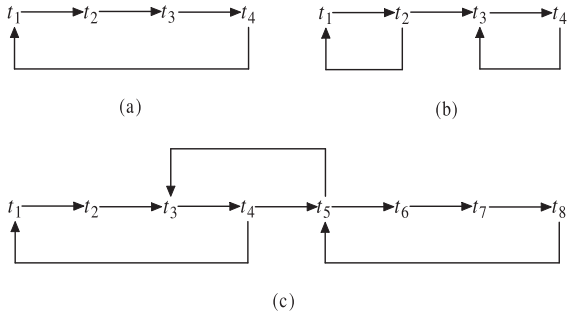


FIGURE 2. Three types of EWs. (a) An EWA, (b) an EWB, and (c) an EWC.

the applicable scope of EWs is larger than WAMGs. In other words, EWs can not only explain the deadlocks in WAMGs, but also explain the deadlocks in other PNs.

Definition 14: There are three types of EWs in terms of structure as follows:

- Type A: $\exists \langle t_1, t_2, \dots, t_n \rangle$ such that $\langle t_1, t_2, \dots, t_n, t_1 \rangle = EC$. This case is denoted as EWA.
- Type B: $\exists \langle t_1, t_2, \dots, t_n \rangle$ such that $\langle t_1, t_2, \dots, t_n \rangle \supseteq EC_1 \cup EC_2 \cup \dots \cup EC_m, m \in \mathbb{N}^+, \text{ and } \forall x, y \in \{1, 2, \dots, m\}, EC_x \cap EC_y = \emptyset$. This case is denoted as EWB.
- Type C: $\exists \langle t_1, t_2, \dots, t_n \rangle$ such that $\langle t_1, t_2, \dots, t_n \rangle \supseteq EC_1 \cup EC_2 \cup \dots \cup EC_m, m \in \mathbb{N}^+, \text{ and } \exists x, y \in \{1, 2, \dots, m\}, EC_x \cap EC_y \neq \emptyset$. This case is denoted as EWC.

Fig. 2 depicts the examples of three types of EWs, respectively. Fig. 2(a) shows an EWA including 4 transitions and all transitions belong to the same EC $\langle t_1, t_2, t_3, t_4, t_1 \rangle$; Fig. 2(b) illustrates an EWB also including 4 transitions but these transitions belong to two different ECs $\langle t_1, t_2, t_1 \rangle$ and $\langle t_3, t_4, t_3 \rangle$, and there are no common transitions between these two ECs; and Fig. 2(c) shows an EWC including 8 transitions and these transitions belong to three different ECs $\langle t_1, t_2, t_3, t_4, t_1 \rangle, \langle t_3, t_4, t_5, t_3 \rangle, \text{ and } \langle t_5, t_6, t_7, t_8, t_5 \rangle$, and there exist common transitions among these ECs, namely, these ECs are intersecting or adjacent from the structure perspective.

Next, we show that EWs are more general and essential than RWs in describing the cause of deadlocks via several examples.

First, we illustrate that the deadlocks in some systems can be explained only by EWs, rather than by RWs, via the examples in Figs. 3(a) and (b).

Example 1: As shown in Fig. 3(a), a partial deadlock can occur since the token in the place p_1 can only transfer either from the place p_1 to the place p_2 or from the place p_2 to the place p_1 , while the other parts of this system are blocked. From the perspective of EWs, two EWs $\langle t_4, t_5 \rangle$ and $\langle t_3, t_5 \rangle$ exist. t_5 , which cannot be fired owing to the insufficient tokens of p_2 , is waiting for t_4 to fire, while t_4 is waiting for t_5 to fire. Similar, t_5 , which cannot be fired due to the insufficient tokens of p_1 , is waiting for t_3 to fire, while t_3 is waiting for t_5 to fire. However, RWs fail to describe the cause of the partial deadlock in Fig. 3(a) due to this net system is a non-resource allocation system. We specify the process in Fig. 3(a) as $\langle p_1, t_2, p_2, t_1, p_1 \rangle, \langle p_1, t_5, p_3, t_3, p_1 \rangle, \text{ and}$

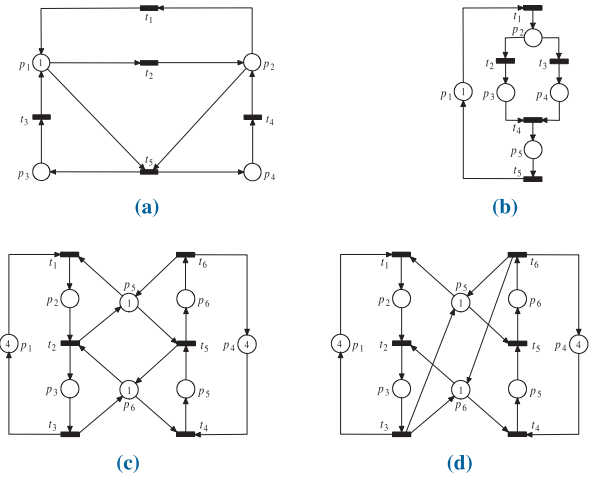


FIGURE 3. Four example PNs.

$\langle p_2, t_5, p_4, t_4, p_2 \rangle$. It is clear that RWs are inadequate to describe the deadlock in Fig. 3(a) since there exists no resource place.

Example 2: Fig. 3(b) shows a separate process that contains two subprocesses $\langle t_1, p_2, t_2, p_3, t_4, p_5, t_5 \rangle$, and $\langle t_1, p_2, t_3, p_4, t_4, p_5, t_5 \rangle$. Under the assumption that there is only one token in p_1 , only one transition between t_2 and t_3 possesses the ability to fire after the firing of t_1 since there exists a conflict between t_2 and t_3 . However, no matter which one fires, the system will eventually fall into a deadlock since t_4 can never be enabled. Since there is only one independent process in this example and no competition for resources exists, the cause of deadlock cannot be explained by RWs. However, an EW $\langle t_5, t_4, t_2, t_1 \rangle$ exists. Thus, we can easily describe the deadlock via EWs.

Then, we show that although both RWs and EWs can be used to describe the cause of deadlocks, EWs are much more essential than RWs via the examples in Figs. 3(c) and (d).

Example 3: In Fig. 3(c), t_2 is dead after the firings of t_1 and t_4 due to the lack of resources in p_6 . In this case, p_2 and p_5 hold the resources required by each other and wait for each other to release. From the perspective of RWs, an RW $\langle p_5, p_6 \rangle$ causes the deadlock. From the perspective of EWs, an EW $\langle t_2, t_5 \rangle$ results in the same deadlock in which t_2 and t_5 are resource disabled.

Example 4: Fig. 3(d) shows the similar example as Fig. 3(c) except that its resource allocation logic is much more complex than that of Fig. 3(c). In Fig. 3(d), t_2 is also dead after the firings of t_1 and t_4 due to the lack of resources in p_6 . From the view of RWs, the deadlock is caused by the RW $\langle p_5, p_6 \rangle$. It can be observed that the above conclusion is the same as that in Fig. 3(c) from the RWs perspective. Although the structures of the PNs in Figs. 3(c) and (d) are different, the deadlocks can be explained by the same RW. However, from the perspective of EWs, the EW $\langle t_2, t_6, t_5, t_3 \rangle$ causes the deadlock in Fig. 3(d) in which t_2 and t_5 are resource disabled while t_3 and t_6 are process disabled. This is different from the cause of deadlock in Fig. 3(c) from the EWs perspective.

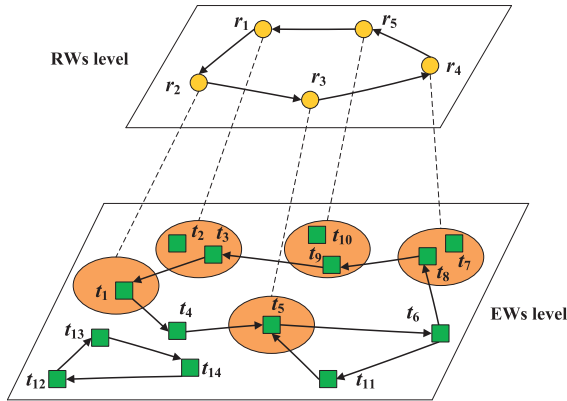


FIGURE 4. Different views of circular waits causing deadlocks.

In contrast to RWs, EWs can illustrate the causes of deadlocks more concretely and accurately. In other words, EWs provide a more essential and specific description of deadlocks than RWs do.

The main difference between RWs and EWs in describing circular waits causing deadlocks are depicted in Fig. 4. From a high-level view, i.e., from the RWs perspective, deadlocks occur because of the circular waits among resources shared by different processes. In contrast, from a low-level view, i.e., from the EWs perspective, deadlocks are caused by the circular waits among transitions in the processes. On the one hand, RWs show a superficial cause of a deadlock, while EWs illustrate the fundamental reason for each deadlock. On the other hand, EWs are more general than RWs since EWs can describe some situations causing deadlocks that cannot be explained by RWs. Therefore, EWs are more general and essential than RWs in describing deadlocks.

Based on the above discussions, two important lemmas are presented as follows to show the relationship between RWs and EWs. If there exists an RW, then there must be an EW; however, an EW does not necessarily correspond to an RW.

Lemma 1: If there exists an RW, then there must be an EW.

Proof: Let $N = (P, T, F, W)$ be a WAMG. Suppose that there exists an RW $\langle r_1, r_2, \dots, r_K \rangle$ among $\bar{N}_1, \bar{N}_2, \dots, \bar{N}_K$. \bar{N}_1 holds the resources in r_1 while waiting for r_2 , and \bar{N}_2 holds the resources in r_2 while waiting for r_3, \dots, \bar{N}_K holds the resources in r_K while waiting for r_1 , where $r_1, r_2, \dots, r_K \in P_R$. From the EWs perspective, this situation can be described as follows: $\exists t_{1x} \in T_1, x \in \mathbb{N}_{|T_1|}$, such that t_{1x} waits for $t_{2y} \in T_2, y \in \mathbb{N}_{|T_2|}$, $\exists t_{2y} \in T_2$ such that t_{2y} waits for $t_{3z} \in T_3, z \in \mathbb{N}_{|T_3|}, \dots, \exists t_{K-1m} \in T_{K-1}, m \in \mathbb{N}_{|T_{K-1}|}$, such that t_{K-1m} waits for $t_{Kn} \in T_K, n \in \mathbb{N}_{|T_K|}$, and $\exists t_{Kn} \in T_K$ such that t_{Kn} waits for $t_{1x} \in T_1$. Namely, an EW $\langle t_{1x}, t_{2y}, \dots, t_{Kn} \rangle$ exists. Therefore, if there exists an RW, then there must be an EW.

Lemma 2: If there exists an EW, then there does not necessarily exist an RW.

Proof: Let $N = (P, T, F, M_0)$ be a WAMG. Suppose that $\exists t_{ix}, t_{ix+1} \in T_i, x \in \mathbb{N}_{|T_i|}, \exists r \in P_R$ such that $r \in \bullet t_{ix} \cap \bullet t_{ix+1}$. t_{ix} fires several times with the aid of the resources in r but

t_{ix+1} cannot fire owing to $M(r) < W(r, t_{ix+1})$ after the firing of t_{ix} . $\exists t_{ix+2} \in T_i$ such that $t_{ix+2} \in t_{ix+1}^\bullet, \dots, \exists t_{ix+n-1} \in T_i$ such that $t_{ix+n-1} \in t_{ix+1}^{(n-2)}, \exists t_{ix+n} \in T_i$ such that $t_{ix+n} \in \bullet r \cap t_{ix+1}^{(n-1)}$, where $\{x, x+1, \dots, x+n-1, x+n\} \in \mathbb{N}_{|T_i|}, \forall j \in \{1, 2, \dots, K\}, j \neq i, \forall t_{jy} \in T_j, y \in \mathbb{N}_{|T_j|}, t_{jy}$ is live under M_0 . Based on the assumption, there exists an EW $\langle t_{ix+n}, t_{ix+n-1}, \dots, t_{ix+2}, t_{ix+1} \rangle$ in \bar{N}_i . However, there exists no RW since an RW must occur among different processes. Therefore, if there exists an EW, then there does not necessarily exist an RW.

Based on Lemmas 1 and 2, we present the following theorem to illustrate the relationship between EWs and deadlocks.

Theorem 1: Let $N = (P, T, F, M_0)$ be a WAMG. \exists an EW at $M \in R(N, M_0)$ iff \exists a deadlock at M .

Proof: Given a WAMG, we prove that there exists an EW at M iff there exists at least one dead transition at M .

- **Necessity.** Suppose that there exists an EW $\langle t_1, t_2, \dots, t_n \rangle, \forall i \in \{1, 2, \dots, n\}, t_i$ is disabled at M and $\nexists EP' \langle t_a, t_b, \dots, t_c, t_i \rangle$ such that $M(\bullet t_a) \neq 0, \exists M \langle t_a, \dots, t_b, \dots, t_c \rangle M'$ and $M' \langle t_i \rangle$. According to Definition 13, each EW consists of several ECs. It can be indicated that each transition in an EC is vainly waiting for the execution of its previous transition. $\forall t \in \{t_1, t_2, \dots, t_n\}$ such that t is dead at M . Hence, a deadlock occurs at M .
- **Sufficiency.** Suppose that $t_1 \in T$ is a dead transition at M , which implies that $\exists p \in \bullet t_1 \cap P$ such that $M(p) < W(p, t_1)$. Furthermore, $\exists t_2 \in \bullet p \cap T$ such that t_2 is a dead transition. Owing to the strong connectivity of WAMGs, there exist paths between transitions t_1 and t_2 that can reach each other. Repeat the above steps. A circular chain of dead transitions can be obtained when $\exists t_n \in t_1^\bullet \cap T$ such that t_n is a dead transition, where $\{1, 2, \dots, n\} \in \mathbb{N}_{|T|}$. Namely, $\forall i \in \{1, 2, \dots, n\}, t_i$ is disabled at M and $\nexists M' \in R(N, M)$ such that $M' \langle t_i \rangle$, which implies that $\nexists EP' \langle t_a, t_b, \dots, t_c, t_i \rangle$ such that $M(\bullet t_a) \neq 0, \exists M \langle t_a, \dots, t_b, \dots, t_c \rangle M'$ and $M' \langle t_i \rangle$. Hence, an EW $\langle t_1, t_2, \dots, t_n \rangle$ can be constructed.

Next, we show that under what conditions can an EW occur in a WAMG.

Lemma 3: Let $M_0 \langle \sigma \rangle M$. $\vec{\sigma}$ is a T -invariant of N , then $M = M_0$.

Proof: Trivial, see [26].

Theorem 2: Let $N = (P, T, F, M_0)$ be a WAMG. \exists an EW at $M \in R(N, M_0)$ iff N is irreversible.

Proof: We prove that \exists an EW at M iff $M_0 \notin R(N, M)$.

- **Necessity.** Since there exists an EW at M , there is at least one dead transition at M in accordance with Theorem 1. Suppose $t \in T_i, i \in \{1, 2, \dots, K\}$, is a dead transition at M , and N is reversible, i.e., $\forall M \in R(N, M_0), M_0 \in R(N, M)$. Since N is a WAMG, $\forall i \in \{1, 2, \dots, K\}, \bar{N}_i$ is a strongly connected marked graph such that every circuit includes p_{0i} . This indicates that a path from p_{0i} to t can be obtained. Since N is acceptably marked, there exists no disabled transition at M_0 and there is a firing sequence σ , containing the transitions in the path from p_{0i} to t , that can reach a new marking $M' \in R(N, M_0)$ such that $M' \langle t \rangle$.

Since $M_0 \in R(N, M)$, t is enabled at M . This is in contradiction with the hypothesis [29].

- Sufficiency. Suppose N is irreversible and there exists no dead transition at M , i.e., $\forall t \in T$, t is enabled at M , which is denoted as $M[t]$. Since the WAMG is acceptably marked, there exists no disabled transition at M_0 . Based on the Definitions 5-7, there exists a T -semiflow $\vec{\sigma}$ in the WAMG, where $\vec{\sigma} = \vec{\sigma}_0 + \vec{\sigma}_1$, such that $M_0[\sigma_0]M$, i.e., $M = M_0 + [N] \cdot \vec{\sigma}_0$, and $M[\sigma_1]M'$, i.e., $M' = M + [N] \cdot \vec{\sigma}_1$. On the basis of $M = M_0 + [N] \cdot \vec{\sigma}_0$ and $M' = M + [N] \cdot \vec{\sigma}_1$, we obtain $M' = M_0 + [N] \cdot \vec{\sigma}$. Since $\vec{\sigma}$ is a T -semiflow, $M' = M_0$ according to Lemma 3. Replacing M' by M_0 in state equation $M' = M + [N] \cdot \vec{\sigma}_1$, we have $M_0 = M + [N] \cdot \vec{\sigma}_1$, i.e., $M_0 \in R(N, M)$, indicating that N is reversible. This is in contradiction with the hypothesis. Therefore, there exists a dead transition at M . According to Theorem 1, if there is a dead transition at M , then there is an EW at M .

B. NEW CLASSIFICATION OF SIPHONS IN WAMGs

Event circular waits (EWs) are employed as the structural characteristic of deadlock from a transition perspective. Nevertheless, from the viewpoint of place, there exists another structural characteristic of deadlock, i.e., siphons, which are widely used to solve deadlocks by preventing siphons from being undermarked [3], [6], [9], [11]–[14], [19]. Next, we illustrate the relationship between siphons and EWs.

Consider a siphon S in a simple net system, such as a system of simple sequential processes with resources (S^3PR) and a system of sequential systems with shared resources (S^4R). Let $S_R = S \cap P_R$ and $S_A = S \cap P_A$, such that $S_A \subseteq H(S_R)$. However, not all siphons in WAMGs conform to this feature. Thereby, a new classification of siphons is explored.

Definition 15: Let S be a siphon:

- 1) S is said to be of Type I if $\forall p \in S_A$, $p \in H(S_R)$, and $\forall r \in S_R$, $\exists p \in S_A \cap H(r)$;
- 2) S is said to be of Type II if $\exists p \in S_A \setminus H(S_R)$, and $\forall r \in S_R$, $\exists p \in S_A \cap H(r)$;
- 3) S is said to be of Type III if $\forall p \in S_A$, $p \in H(S_R)$, and $\exists r \in S_R$, $\nexists p \in S_A \cap H(r)$; and
- 4) S is said to be of Type IV if $\exists p \in S_A \setminus H(S_R)$, and $\exists r \in S_R$, $\nexists p \in S_A \cap H(r)$.

A siphon S as $S = S_{A1} \cup S_{A2} \cup S_{R1} \cup S_{R2}$, where $S_{A1} = \{p \mid p \in S_A \wedge p \in H(S_R)\}$, $S_{A2} = S_A \setminus S_{A1}$, $S_{R1} = \{r \mid H(r) \cap S_{A1} \neq \emptyset\}$, and $S_{R2} = S_R \setminus S_{R1}$.

Consider the weighted augmented marked graphs (WAMGs) (N, M_0) shown in Fig. 1. There are 25 siphons involved in the WAMG, as shown in Table 1, in which S_{11} , S_{12} , S_{13} , S_{14} , S_{16} , S_{20} , S_{21} , S_{22} , S_{23} , S_{24} and S_{25} are Type I siphons. Take S_{11} as an example, $S_{11} = \{p_5, p_9, p_{10}, p_{15}, p_{16}, p_{18}, p_{19}\}$, in which $S_A = \{p_5, p_9, p_{10}, p_{15}\}$ and $S_R = \{p_{16}, p_{18}, p_{19}\}$. $\forall p \in S_A$, $p \in H(S_R)$, i.e., $p_5, p_9, p_{10}, p_{15} \in H(S_R)$. $\forall r \in S_R$, $\exists p \in S_A \cap H(r)$, i.e., for p_{16} , $\exists p_{15} \in H(p_{16})$; for p_{18} , $\exists p_5, p_{10} \in H(p_{18})$; for p_{19} , $\exists p_9 \in H(p_{19})$. In S_{11} , $S_{A1} = S_A = \{p_5, p_9, p_{10}, p_{15}\}$ and $S_{R1} = S_R = \{p_{16}, p_{18}, p_{19}\}$.

$S_2, S_4, S_6, S_7, S_8, S_9$ and S_{10} are Type II siphons. Take S_2 as an example, $S_2 = \{p_9, p_{11}, p_{14}, p_{18}, p_{19}\}$, in which $S_A = \{p_9, p_{11}, p_{14}\}$ and $S_R = \{p_{18}, p_{19}\}$. $\exists p \in S_A \setminus H(S_R)$, i.e., $\exists p_{11} \in S_A$ such that $p_{11} \notin H(S_R)$. $\forall r \in S_R$, $\exists p \in S_A \cap H(r)$, i.e., for p_{18} , $\exists p_{14} \in H(p_{18})$; for p_{19} , $\exists p_9 \in H(p_{19})$. In S_2 , $S_{A1} = \{p_9, p_{14}\}$, $S_{A2} = S_A \setminus S_{A1} = \{p_{11}\}$, $S_{R1} = S_R = \{p_{18}, p_{19}\}$.

S_{15}, S_{17}, S_{18} and S_{19} are Type III siphons. Take S_{15} as an example, $S_{15} = \{p_5, p_{10}, p_{15}, p_{16}, p_{18}, p_{20}\}$, in which $S_A = \{p_5, p_{10}, p_{15}\}$ and $S_R = \{p_{16}, p_{18}, p_{20}\}$. $\forall p \in S_A$, $p \in H(S_R)$, i.e., $p_5, p_{10}, p_{15} \in H(S_R)$. $\exists r \in S_R$, $\nexists p \in S_A \cap H(r)$, i.e., for p_{20} , $\nexists p \in S_A$ such that $p \in H(p_{20})$. In S_{15} , $S_{A1} = S_A = \{p_5, p_{10}, p_{15}\}$, $S_{R1} = \{p_{16}, p_{18}\}$, $S_{R2} = S_R \setminus S_{R1} = \{p_{20}\}$.

S_1, S_3 and S_5 are Type IV siphons. Take S_1 as an example, $S_1 = \{p_9, p_{11}, p_{15}, p_{16}, p_{18}, p_{19}\}$, in which $S_A = \{p_9, p_{11}, p_{15}\}$ and $S_R = \{p_{16}, p_{18}, p_{19}\}$. $\exists p \in S_A \setminus H(S_R)$, i.e., $\exists p_{11} \in S_A$ such that $p_{11} \notin H(S_R)$. $\exists r \in S_R$, $\nexists p \in S_A \cap H(r)$, i.e., for p_{18} , $\nexists p \in S_A$ such that $p \in H(p_{18})$. In S_1 , $S_{A1} = \{p_9, p_{15}\}$, $S_{A2} = S_A \setminus S_{A1} = \{p_{11}\}$, $S_{R1} = \{p_{16}, p_{19}\}$, $S_{R2} = S_R \setminus S_{R1} = \{p_{18}\}$.

- 1) The siphon of Type I can be derived when $S_{A2} = \emptyset$ and $S_{R2} = \emptyset$, i.e., $S = S_{A1} \cup S_{R1}$. Type I usually appears in S^3PR and S^4R . In such systems, $|\bullet t| = |t\bullet| = 1$, $\bullet t \cap P_A = \{p\}$ and $\{r\} \subseteq t\bullet \cap P_R$. If $\{p, r\} \in S$, then $p \in H(r)$.
- 2) When the siphon is of Type II, $S_{R2} = \emptyset$, i.e., $S = S_{A1} \cup S_{A2} \cup S_{R1}$. The occurrence of Type II is attributed to the synchronizations of WAMGs. This is a main characteristic that is different from state machines. Since multiple places can point to the same transition, there exists the case that several places belong to a siphon even though these places do not use the resources contained in the siphon. S_{A2} usually appear as a chain of $p \in P_A$, and these places are mostly in parallel processes. Assume that $\exists p_{ji} \in S_{A1}$ such that $p_{j1}^\bullet = \bullet p_{j2}$, $p_{j2}^\bullet = \bullet p_{j3}$, \dots , $p_{ji-1}^\bullet = \bullet p_{ji}$ and $p_{j1}, p_{j2}, \dots, p_{ji} \in S_{A1}$, where $j \in \mathbb{N}_K$ and $i \in \mathbb{N}_{|PT_j|}$. Two situations are presented to clarify S_{A2} . 1) $\forall \bullet p_{j1} \in S_{R1}^\bullet$, $\exists t \in \bullet S_{R1}$ such that $t \in S_{A2}^\bullet$. 2) If $\exists p_{j1} \notin S_{R1}^\bullet$, then $\exists t \in \bullet S_{A1}$ such that $t \in S_{A2}^\bullet$.
- 3) For the siphon of Type III, $S_{A2} = \emptyset$, i.e., $S = S_{A1} \cup S_{R1} \cup S_{R2}$. The occurrence of Type III is the connection between resources and processes in WAMGs. There exists not only $t \in \bullet S_{R1}$ satisfying $S_{A1} \in \bullet t$ in certain processes, but also $t \in \bullet S_{R1}$ in other processes such that $\nexists p \in S_{A1}$, $p \in \bullet t$. Therefore, S_{R2} can be introduced if $\exists t \in \bullet S_{R1}$ such that $t \in S_{R2}^\bullet$. Assume that $\exists p_{ji} \in S_{A1}$ such that $p_{j1}^\bullet = \bullet p_{j2}$, $p_{j2}^\bullet = \bullet p_{j3}$, \dots , $p_{ji-1}^\bullet = \bullet p_{ji}$ and $p_{j1}, p_{j2}, \dots, p_{ji} \in S_{A1}$, where $j \in \mathbb{N}_K$ and $i \in \mathbb{N}_{|PT_j|}$. 1) $\forall \bullet p_{j1} \in S_{R1}^\bullet$, $\exists t \in \bullet S_{R1}$ such that $t \in S_{R2}^\bullet$. 2) If $\exists p_{j1} \notin S_{R1}^\bullet$, then $\exists t \in \bullet S_{A1}$ and $\exists t \in \bullet S_{R1}$ such that $t \in S_{R2}^\bullet$.
- 4) For the siphon of Type IV, each component is not empty, i.e., $S = S_{A1} \cup S_{A2} \cup S_{R1} \cup S_{R2}$. Type IV is a combination of Type II and Type III with both S_{A2} and S_{R2} . In different situations, the post-transitions of S_{A2} and S_{R2} are utilized to complement the pre-transitions of different components. Assume that $\exists p_{ji} \in S_{A1}$ such

TABLE 1. Description of the siphons for the WAMG in Fig. 1.

i	S	S_{A_1}	S_{A_2}	S_{R_1}	S_{R_2}	T
1	{ $p_9, p_{11}, p_{15}, p_{16}, p_{18}, p_{19}$ }	{ p_9, p_{15} }	{ p_{11} }	{ p_{16}, p_{19} }	{ p_{18} }	IV
2	{ $p_9, p_{11}, p_{14}, p_{18}, p_{19}$ }	{ p_9, p_{14} }	{ p_{11} }	{ p_{18}, p_{19} }	{ \emptyset }	II
3	{ $p_8, p_{11}, p_{15}, p_{16}, p_{18}, p_{19}$ }	{ p_8, p_{15} }	{ p_{11} }	{ p_{16}, p_{19} }	{ p_{18} }	IV
4	{ $p_8, p_{11}, p_{14}, p_{18}, p_{19}$ }	{ p_8, p_{14} }	{ p_{11} }	{ p_{18}, p_{19} }	{ \emptyset }	II
5	{ $p_7, p_9, p_{11}, p_{15}, p_{16}, p_{18}, p_{20}$ }	{ p_{11}, p_{15} }	{ p_7, p_9 }	{ p_{16}, p_{20} }	{ p_{18} }	IV
6	{ $p_7, p_9, p_{11}, p_{14}, p_{18}, p_{20}$ }	{ p_{11}, p_{14} }	{ p_7, p_9 }	{ p_{18}, p_{20} }	{ \emptyset }	II
7	{ $p_6, p_7, p_9, p_{11}, p_{15}, p_{16}, p_{18}$ }	{ p_6, p_{15} }	{ p_7, p_9, p_{11} }	{ p_{16}, p_{18} }	{ \emptyset }	II
8	{ $p_6, p_7, p_9, p_{11}, p_{14}, p_{18}$ }	{ p_6, p_{14} }	{ p_7, p_9, p_{11} }	{ p_{18} }	{ \emptyset }	II
9	{ $p_6, p_8, p_{11}, p_{15}, p_{16}, p_{18}$ }	{ p_6, p_{15} }	{ p_8, p_{11} }	{ p_{16}, p_{18} }	{ \emptyset }	II
10	{ $p_6, p_8, p_{11}, p_{14}, p_{18}$ }	{ p_6, p_{14} }	{ p_8, p_{11} }	{ p_{18} }	{ \emptyset }	II
11	{ $p_5, p_9, p_{10}, p_{15}, p_{16}, p_{18}, p_{19}$ }	{ p_5, p_9, p_{10}, p_{15} }	{ \emptyset }	{ p_{16}, p_{18}, p_{19} }	{ \emptyset }	I
12	{ $p_5, p_8, p_{10}, p_{15}, p_{16}, p_{18}, p_{19}$ }	{ p_5, p_8, p_{10}, p_{15} }	{ \emptyset }	{ p_{16}, p_{18}, p_{19} }	{ \emptyset }	I
13	{ $p_9, p_{14}, p_{17}, p_{19}$ }	{ p_9, p_{14} }	{ \emptyset }	{ p_{17}, p_{19} }	{ \emptyset }	I
14	{ $p_8, p_{14}, p_{17}, p_{19}$ }	{ p_8, p_{14} }	{ \emptyset }	{ p_{17}, p_{19} }	{ \emptyset }	I
15	{ $p_5, p_{10}, p_{15}, p_{16}, p_{18}, p_{20}$ }	{ p_5, p_{10}, p_{15} }	{ \emptyset }	{ p_{16}, p_{18} }	{ p_{20} }	III
16	{ $p_5, p_6, p_{10}, p_{15}, p_{16}, p_{18}$ }	{ p_5, p_6, p_{10}, p_{15} }	{ \emptyset }	{ p_{16}, p_{18} }	{ \emptyset }	I
17	{ $p_3, p_9, p_{15}, p_{16}, p_{17}, p_{19}$ }	{ p_3, p_9, p_{15} }	{ \emptyset }	{ p_{16}, p_{19} }	{ p_{17} }	III
18	{ $p_3, p_8, p_{15}, p_{16}, p_{17}, p_{19}$ }	{ p_3, p_8, p_{15} }	{ \emptyset }	{ p_{16}, p_{19} }	{ p_{17} }	III
19	{ $p_5, p_{10}, p_{14}, p_{18}, p_{20}$ }	{ p_5, p_{10}, p_{14} }	{ \emptyset }	{ p_{18} }	{ p_{20} }	III
20	{ p_4, p_7, p_{14}, p_{17} }	{ p_4, p_7, p_{14} }	{ \emptyset }	{ p_{17} }	{ \emptyset }	I
21	{ p_9, p_{13}, p_{19} }	{ p_9, p_{13} }	{ \emptyset }	{ p_{19} }	{ \emptyset }	I
22	{ $p_3, p_4, p_7, p_{15}, p_{16}, p_{17}$ }	{ p_3, p_4, p_7, p_{15} }	{ \emptyset }	{ p_{16}, p_{17} }	{ \emptyset }	I
23	{ p_8, p_{13}, p_{19} }	{ p_8, p_{13} }	{ \emptyset }	{ p_{19} }	{ \emptyset }	I
24	{ $p_5, p_9, p_{10}, p_{14}, p_{18}, p_{19}$ }	{ p_5, p_9, p_{10}, p_{14} }	{ \emptyset }	{ p_{18}, p_{19} }	{ \emptyset }	I
25	{ $p_5, p_8, p_{10}, p_{14}, p_{18}, p_{19}$ }	{ p_5, p_8, p_{10}, p_{14} }	{ \emptyset }	{ p_{18}, p_{19} }	{ \emptyset }	I

that $p_{j_1}^\bullet = \bullet p_{j_2}, p_{j_2}^\bullet = \bullet p_{j_3}, \dots, p_{j_{i-1}}^\bullet = \bullet p_{j_i}$ and $p_{j_i}, p_{j_2}, \dots, p_{j_i} \in S_{A_1}$, where $j \in \mathbb{N}_K$ and $i \in \mathbb{N}_{|PT_j|}$. 1) $\forall \bullet p_{j_1} \in S_{R_1}^\bullet, \exists t \in \bullet S_{R_1}$ such that $t \in S_{R_2}^\bullet$ and $\exists t \in \bullet S_{R_2}$ such that $t \in S_{A_2}^\bullet$. 2) If $\exists p_{j_1} \notin S_{R_1}^\bullet$, then $\exists t \in \bullet S_{A_1}$ such that $t \in S_{R_2}^\bullet, \exists t \in \bullet S_{R_2}$ such that $t \in S_{A_2}^\bullet$ and $\exists t \in \bullet S_{A_1}$ such that $t \in S_{A_2}^\bullet$.

Theorem 3: Consider a WAMG (N, M_0) and $M \in R(N, M_0)$. \exists an EW at M iff \exists an undermarked siphon S at M .

Proof: We prove that a WAMG (N, M_0) contains an EW at M iff there exists a undermarked siphon S at M .

- Necessity. Since (N, M_0) contains an EW at M , there exists at least one event circuit $EC_1 \langle t_1, t_2, \dots, t_n, t_1 \rangle$ at M . A set $P_1 = \langle p_1, p_2, \dots, p_n \rangle$ can be constructed such that $p_1 \in \bullet t_1 \cap t_2^\bullet, p_2 \in \bullet t_2 \cap t_3^\bullet, \dots, p_n \in \bullet t_n \cap t_1^\bullet$. For $t \in P_1^\bullet$, there are two cases:
 - Case 1) $\exists i \in \{1, 2, \dots, n\}, \exists t \in p_i^\bullet$ such that $t \notin EC_1$ and $\forall t \in \bullet p_i$ such that $t \in EC_1$. Therefore, P is a siphon since $\bullet P \subseteq P^\bullet$ holds.
 - Case 2) $\exists i \in \{1, 2, \dots, n\}, \exists t \in \bullet p_i$ such that $t \notin EC_1$, According to Definition 13, t belongs to the other event circular wait. Therefore, $\exists EC = EC_1 \cup EC_2 \cup \dots \cup EC_m$ and $P = P_1 \cup P_2 \cup \dots \cup P_m, (m \geq 2)$.

For $t \in P^\bullet$, repeat above steps. There are two cases which are similar to Case 1) and Case 2). In the most

complicated case, all places can constitute a maximal set P . After removing some redundant places that do not affect other places, the remaining places can constitute a strict minimal undermarked siphon [11], [18], [27]. By selecting a specific dead transition t , all the places in P are sequentially checked. For a clear description, let $S = P - \{p\}$. Based on the definition of undermarked siphon, if $p \in \bullet t, p$ is temporarily reserved in the strict minimal siphon to be sought. If $p \notin \bullet t$, it is necessary to verify whether the remaining places can still constitute a siphon after removing p . There are two cases. Case 1) S is still a siphon, which means that the removal of p does not affect the remaining places. This situation occurs due to $\forall t \in \bullet P \cap p^\bullet$ such that $t \in S^\bullet$, indicating that p is not a necessary element of a strict minimal undermarked siphon. Case 2) S is no longer a siphon since $\bullet S \subseteq S^\bullet$ does not hold. $\exists t \in \bullet P \cap P^\bullet$ such that $t \notin S^\bullet$, which means that the removal of p will cause other places to be removed. Hence, p is an element that constitutes a strict minimal siphon. $\forall p \in P$, repeat above steps. Select the places that are temporarily reserved in P to ensure that at least one is retained in the strict minimal siphon. A strict minimal undermarked siphon can be obtained.

- Sufficiency. If $\exists S$ at M such that S is undermarked, then $\exists t \in T$ at M such that t is dead. In accordance with Theorem 1, an EW exists at M .

Note that the statement that \exists an EW at M iff \exists an undermarked siphon S at M proved in Theorem 3 indicates that an undermarked siphon S is obtained according to an EW at M and an EW can be deduced based on an undermarked siphon S at M , which does not mean that both elements of S and EW correspond to each other. In the sequel, we show the basic relationships between the EWs and the corresponding undermarked siphons (S_C s). In other words, we illustrate the relationships between the places that correspond to the dead transitions in EWs and the places that are involved in the undermarked siphons S_C s. The dead transitions in EWs can be classified into two types, i.e., resource disabled and process disabled. Based on Definition 15, we assume that $S_C = S_{CA} \cup S_{CR} = S_{CA_1} \cup S_{CA_2} \cup S_{CR_1} \cup S_{CR_2}$. The relationships are explained as follows via two cases:

- Case 1) If a dead transition in an EW is process disabled, i.e., $\exists p \in P_A, t \in P^\bullet$ is dead due to $M(p) = 0$, then p acts as a PC between two dead transitions and $p \notin H(S_{CR})$ and $p \in S_{CA_2}$.
- Case 2) If a dead transition in an EW is resource disabled, i.e., $\exists r \in P_R, t \in r^\bullet$ is dead due to $M(r) < W(r, t)$, then $r \in S_{CR}$. Since resources in a WAMG can be shared by different processes, t and t' that is being waited by t can be in the same process or in different processes.
 - Case 2.1) If $t \in T_i$ and $t' \in T_j$, ($i, j \in \mathbb{N}_K$ and $i \neq j$), then $r \in S_{CR_1}$ and $\forall p \in t^\bullet \cap H(r)$ such that $p \in S_{CA_1}$. If $\exists p_{ij} \in S_{CA_1}, i \in \mathbb{N}_K$ and $j \in \mathbb{N}_{|P_i|}$, such that $t = \bullet p_{i1}, p_{i1} = \bullet p_{i2}, p_{i2} = \bullet p_{i3}, \dots, p_{ij-1} = \bullet p_{ij}$, then $p_{i1}, p_{i2}, \dots, p_{ij} \in S_{CA_1} \subseteq H(S_{CR_1})$.
 - Case 2.2) If $t, t' \in T_i, i \in \mathbb{N}_K$, then $r \in S_{CR_2}$ and $\forall p \in t^\bullet$ such that $p \notin S_C$.

Here, $p \in S_{CA_1}$ in Case 2.1 ensures that $t' \in S_C^\bullet$. However, this is not necessary in Case 2.2. We show that $t' \in S_C^\bullet$ according to the following cases: Case a) if t' is resource disabled by r' such that $t' \in \bullet r' \cap r'^\bullet$, then $t' \in \bullet S_C \cap S_C^\bullet$; and Case b) if t' is process disabled by p' , then $p' \in S_{CA_2}$ such that $t' \in \bullet r' \cap p'^\bullet$, i.e., if $\exists p' \in \bullet t'$ such that $M(p') = 0$, then $t' \in \bullet S_C \cap S_C^\bullet$. Since $p \in t^\bullet \cap \bullet t'$ and $t' \in S_C^\bullet$, p is not an unnecessary element for S_C , i.e., $p \notin S_C$ in Case 2.2. If p is in S_C , then S_C is not a strict minimal siphon. This is contrary to Theorem 3.

Note that a dead transition in an EW can be both process disabled and resource disabled. Under such a circumstance, the activity places and resource places that are related to the transition are categorized as the elements of S_{CA_1} and S_{CR_1} , respectively, based on the principle that the places that correspond to the dead transitions in EWs are first mapped in the places of Type I S_C s, and then those of Type II, Type III, and Type IV S_C s, respectively.

Next, we elaborate on several specified relationships between the classifications of EWs, i.e., EWA, EWB, and EWC, and that of S_C s, i.e., Type I, Type II, Type III, and Type IV, according to above discussions, along with several illustrative examples.

Consider the WAMG in Fig. 1. We denote $T_1 = \{t_1, t_2, \dots, t_9\}$ and $T_2 = \{t_{10}, t_{11}, t_{12}, t_{13}\}$. The initial marking in Fig. 1 is

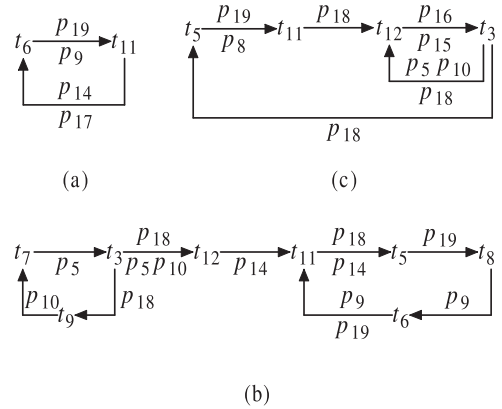


FIGURE 5. Three example event circular waits. (a) $\{t_6, t_{11}\}$, (b) $\{t_9, t_7, t_3, t_{12}, t_{11}, t_5, t_8, t_6\}$, and (c) $\{t_5, t_{11}, t_{12}, t_3\}$.

set as $M_0 = [4 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 4 \ 0 \ 0 \ 0 \ 1 \ 3 \ 2 \ 2 \ 1]$. The WAMG in Fig. 1 can reach a totally deadlock marking $M = [3 \ 1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 2 \ 2 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1]$. In the sequel, we assume that all EWs for the WAMG in Fig. 1 is obtained at M if no other statement is given. To facilitate the readers' understanding, we label the resource places corresponding to the transitions in an EW outside the EW, and resource holders or process connectors corresponding to the transitions in an EW inside the EW, in the following examples. Assume that a dead transition t in an EW is waiting for another transition t' . If t is resource disabled, i.e., $\exists r \in \bullet t \cap t'^\bullet$ such that $M(r) < W(r, t)$, then r is a resource place that is marked outside the EW. $\forall p \in H(S_{CR}) \cap t^\bullet, p$ is a resource holder which is marked inside the EW. For process disabled t , the process connector $p \in \bullet t \cap t'^\bullet$ is marked inside the EW.

(1) If an EWA is an RW, then the EWA correspond to a Type I S_C .

Example 5: An EWA $\{t_6, t_{11}\}$ is shown in Fig. 5(a). Since there is a resource competition that occurs between p_{17} and p_{19} , the deadlock can also be explained by an RW $\langle p_{17}, p_{19} \rangle$. Since t_6 is dead due to $M(p_{19}) < W(p_{19}, t_6)$ and t_{11} is dead due to $M(p_{17}) < W(p_{17}, t_{11})$, t_6 and t_{11} are resource disabled and $p_{19}, p_{17} \in S_{CR_1}$. Because $p_9 \in t_6^\bullet \cap H(p_{19})$ and $p_{14} \in t_{11}^\bullet \cap H(p_{17}), p_9, p_{14} \in S_{CA_1}$. Hence, we obtain Type I $S_C = \{p_9, p_{14}, p_{17}, p_{19}\}$.

(2) Not only EWAs but also EWBs and EWCs can correspond to the Type I siphons.

Example 6: Assume that the structure of the WAMG in Fig. 1 remains unchanged whereas the initial marking is changed to $M_0 = [4 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 4 \ 0 \ 0 \ 0 \ 1 \ 3 \ 1 \ 2 \ 1]$. There exists a totally deadlock marking $M' = [3 \ 0 \ 1 \ 0 \ 0 \ 1 \ 1 \ 0 \ 0 \ 0 \ 2 \ 2 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1]$. An EWB can be derived at M' as shown in Fig. 5(b). Since t_3 is dead due to $M(p_{18}) < W(p_{18}, t_3)$, t_{11} is dead due to $M(p_{18}) < W(p_{18}, t_{11})$, and t_6 is dead due to $M(p_{19}) < W(p_{19}, t_6)$, t_3, t_{11} and t_6 are resource disabled and $p_{18}, p_{19} \in S_{CR_1}$. Because $p_5 \in t_3^\bullet \cap H(p_{18}), p_{10} \in t_3^{(3)} \cap H(p_{18}), p_{14} \in t_{11}^\bullet \cap H(p_{18})$, and $p_9 \in t_6^\bullet \cap H(p_{19}), p_5, p_9, p_{10}, p_{14} \in S_{CA_1}$. Since $t_5, t_8 \in T_1, p_8 \in t_5^\bullet$ such that p_8 is not in any undermarked siphon that corresponds to the

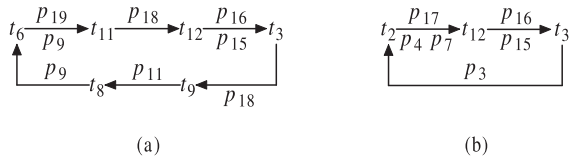


FIGURE 6. Two example event circular waits. (a) $\{t_6, t_{11}, t_{12}, t_3, t_9, t_8\}$ and (b) $\{t_2, t_{12}, t_3\}$.

EWB. Since t_7, t_8, t_9, t_{12} are process disabled, $\exists p_5 \in t_3^\bullet \cap \bullet t_7$, $\exists p_9 \in t_6^\bullet \cap \bullet t_8$, $\exists p_{10} \in t_7^\bullet \cap \bullet t_9$, and $\exists p_{14} \in t_{11}^\bullet \cap \bullet t_{12}$ such that $p_5 \in PC(t_3, t_7)$, $p_9 \in PC(t_6, t_8)$, $p_{10} \in PC(t_7, t_9)$, and $p_{14} \in PC(t_{11}, t_{12})$. Furthermore, $p_5 \in H(p_{18}) \cap PC(t_3, t_7)$, $p_9 \in H(p_{19}) \cap PC(t_6, t_8)$, $p_{10} \in H(p_{18}) \cap PC(t_7, t_9)$, and $p_{14} \in H(p_{18}) \cap PC(t_{11}, t_{12})$. Hence, we obtain Type I $SC = \{p_5, p_9, p_{10}, p_{14}, p_{18}, p_{19}\}$.

Example 7: An *EW* is shown in Fig. 5(c). Since t_5 is dead due to $M(p_{19}) < W(p_{19}, t_5)$, t_{12} is dead due to $M(p_{16}) < W(p_{16}, t_{12})$ and t_3 is dead due to $M(p_{18}) < W(p_{18}, t_3)$, t_5, t_{12} , and t_3 are resource disabled and $p_{19}, p_{16}, p_{18} \in SC_{R1}$. Because $p_8 \in t_5^\bullet \cap H(p_{19})$, $p_{15} \in t_{12}^\bullet \cap H(p_{16})$, $p_5 \in t_3^\bullet \cap H(p_{18})$, and $p_{10} \in t_3^{(3)} \cap H(p_{18})$, $p_5, p_8, p_{10}, p_{15} \in SC_{A1}$. Since $t_{11}, t_{12} \in T_2$ and $p_{14} \in t_{11}^\bullet$, p_{14} is not in any undermarked siphon that corresponds to the *EW*. Hence, we obtain Type I $SC = \{p_5, p_8, p_{10}, p_{15}, p_{16}, p_{18}, p_{19}\}$.

(3) *EWAs* can correspond to not only Type I SCs but also Type II, Type III and Type IV SCs .

Example 8: We illustrate that *EWAs* correspond to Type IV SCs since Type IV is a combination of Type II and Type III. There is an *EWA* shown in Fig. 6(a). Since t_6 is dead due to $M(p_{19}) < W(p_{19}, t_6)$ and t_{12} is dead due to $M(p_{16}) < W(p_{16}, t_{12})$, t_6 and t_{12} are resource disabled and $p_{19}, p_{16} \in SC_{R1}$. Because $p_9 \in t_6^\bullet \cap H(p_{19})$ and $p_{15} \in t_{12}^\bullet \cap H(p_{16})$, $p_9, p_{15} \in SC_{A1}$. Since $t_3, t_9 \in T_1$ and $t_{11}, t_{12} \in T_2$, t_{11} is dead due to $M(p_{18}) < W(p_{18}, t_{11})$, and t_3 is dead due to $M(p_{18}) < W(p_{18}, t_3)$, t_3 and t_{11} are resource disabled and $p_{18} \in SC_{R2}$. $p_5 \in t_3^\bullet$ and $p_{14} \in t_{11}^\bullet$ such that p_5 and p_{14} are not in any undermarked siphon that corresponds to the *EWA*. Since t_9 is process disabled, $\exists p_{11} \in t_8^\bullet \cap \bullet t_9$, $p_{11} \in PC(t_8, t_9)$ such that $p_{11} \in SC_{A2}$. Hence, we obtain Type IV $SC = \{p_9, p_{11}, p_{15}, p_{16}, p_{18}, p_{19}\}$.

A special case is presented as follows.

(4) Assume that $t \in r^\bullet$ is dead due to $M(r) < W(r, t)$. $\exists p \in r^\bullet$ such that $p \notin H(r)$. There must be a transition $t' \in p^\bullet$ such that t' is dead owing to $M(p) = 0$. p behaves as a resource holder in SC , i.e., $\exists r' \in SC$ such that $p \in H(r')$, essentially p acts as a process connector.

Example 9: In the *EW* as shown in Fig. 6(b), t_2 is dead due to $M(p_{17}) < W(p_{17}, t_2)$ and $p_3 \in t_2^\bullet$ such that $p_3 \notin H(p_{17})$. Furthermore, $t_3 \in p_3^\bullet$ such that t_3 is dead due to $M(p_3) = 0$. Even if p_3 behaves as a $H(p_{16})$, it is actually a $PC(t_2, t_3)$ in $SC = \{p_3, p_4, p_7, p_{15}, p_{16}, p_{17}\}$.

IV. A NEW METHOD BASED ON EVENT CIRCULAR WAITS FOR DEADLOCK AVOIDANCE

Since deadlocks can degrade the stability and operating efficiency of the systems, it is crucial to avoid deadlocks as

soon as possible [15], [22], [27], [30]–[33], [37]. Although many technologies, such as the look-ahead strategy, have been proposed to deal with deadlocks, there is little work for in-depth exploration of how long a deadlock will occur from a specified marking. This makes the current methods too aggressive, i.e., they explore too many reachable markings, from the *RWs* perspective.

Theorem 1 proposed above provides the sufficiency and necessity condition between *EWs* and the liveness of *PNs*. Therefore, deadlocks can be avoided via *EWs*. In this section, we show that deadlocks can be avoided earlier at a specified marking by using *EWs* rather than *RWs*, indicating that *EWs* are much more efficient than *RWs* for deadlock avoidance. Then, an effective approach to avoid deadlocks is proposed based on *EWs*.

We will compare the avoidance efficiency by using *EWs* and *RWs* in the following two cases. The case in Lemma 4 shows that there exists an ordered transition sequence. Each transition is waiting for a transition in other processes. The cases in Lemma 5 shows that there exists an ordered transition sequence, at least one of which is waiting for a transition in the same process.

Lemma 4: Let $N = (P, T, F, W)$ be a *WAMG*. $\exists t_{1i} \in T_1$, $i \in \mathbb{N}_{|T_1|}$, such that t_{1i} holds the resources in r_1 while waiting for r_2 , $\exists t_{2j} \in T_2$, $j \in \mathbb{N}_{|T_2|}$, such that t_{2j} holds the resources in r_2 while waiting for $r_3, \dots, \exists t_{kk} \in T_K$, $k \in \mathbb{N}_{|T_K|}$, such that t_{kk} holds the resources in r_K while waiting for r_1 at $M \in R(N, M_0)$, where $r_1, r_2, \dots, r_K \in P_R$, then an *EW* $\langle t_{1i}, t_{2j}, \dots, t_{kk} \rangle$ and an *RW* $\langle r_1, r_2, \dots, r_K \rangle$ generate simultaneously at $M \in R(N, M_0)$.

Proof: Based on the assumption that t_{1i} is waiting for t_{2j}, \dots, t_{kk} is waiting for t_{1i} , an *EW* $\langle t_{1i}, t_{2j}, \dots, t_{kk} \rangle$ exists; meanwhile, since $t_{1i}, t_{2j}, \dots, t_{kk}$ are all resource disabled and belong to different processes, an *RW* $\langle r_1, r_2, \dots, r_K \rangle$ can be obtained.

Example 10: As shown in Fig. 5(a), $t_6 \in T_1$ is waiting for $t_{11} \in T_2$ to release the resources in p_{19} , and $t_{11} \in T_2$ is waiting for $t_6 \in T_1$ to make the resources in p_{17} sufficient. Since both t_6 and t_{11} are resource disabled and are located in different processes, an *EW* $\langle t_6, t_{11} \rangle$ and an *RW* $\langle p_{19}, p_{17} \rangle$ are formed simultaneously.

Lemma 5: Let $N = (P, T, F, W)$ be a *WAMG*. $\exists t_{ix}, t_{ix+n} \in T_i$, $i, n \in \mathbb{N}^+$, $x, \dots, x+n \in \mathbb{N}_{|T_i|}$, such that t_{ix+n} is waiting for t_{ix} or t_{ix} is waiting for t_{ix+n} at $M \in R(N, M_0)$, then \exists an *EW* but \nexists an *RW* at M .

Proof: Based on the assumption, we then prove this lemma by the following two cases:

- Case 1) t_{ix+n} is waiting for t_{ix} due to $M(p_{ia}) = 0, \dots, M(p_{ia+n}) = 0$, where $p_{ia} \in t_{ix}^\bullet \cap \bullet t_{ix+1}, \dots, p_{ia+n-1} \in t_{ix+n-1}^\bullet \cap \bullet t_{ix+n}$, $a, \dots, a+n-1 \in \mathbb{N}_{|P_i|}$. $\exists t_{jy} \in T_j$, $j \in \mathbb{N}^+$, $y \in \mathbb{N}_{|T_j|}$, t_{jy} is resource disabled and waiting for $t_{kz} \in T_k$, $k \in \mathbb{N}^+$, $z \in \mathbb{N}_{|T_k|}$, t_{kz} is resource disabled and waiting for t_{mn} , $m \in \mathbb{N}^+$, $n \in \mathbb{N}_{|T_m|}$, \dots, t_{ix+n} is process disabled and waiting for $t_{ix+n-1}, \dots, t_{ix+1}$ is process disabled and waiting for t_{ix} , and t_{ix} is resource disabled and waiting for t_{jy} , i.e., all resource competitions occur

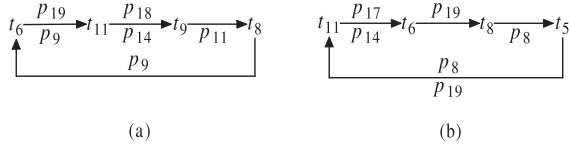


FIGURE 7. Two example event circular waits. (a) (t_6, t_{11}, t_9, t_8) and (b) (t_{11}, t_6, t_8, t_5) .

among different processes. Since $\exists t_{ix+1}, \dots, t_{ix+n} \in T_i$ such that $t_{ix+1}, \dots, t_{ix+n}$ are process disabled, RWs do not exist. However, an EW $\langle t_{jy}, t_{kz}, t_{mn}, \dots, t_{ix+n}, \dots, t_{ix+1}, t_{ix} \rangle$ can be constituted at M .

- Case 2) t_{ix} is waiting for t_{ix+n} due to $M(r) < W(r, t)$, where $r \in t_{ix+n}^\bullet \cap t_{ix}^\circ$. $\exists t_{jy} \in T_j, y \in \mathbb{N}_{|T_j|}, t_{jy}$ is resource disabled and waiting for $t_{kz} \in T_k, k \in \mathbb{N}^+, z \in \mathbb{N}_{|T_k|}, t_{kz}$ is resource disabled and waiting for $t_{mn}, m \in \mathbb{N}^+, n \in \mathbb{N}_{|T_m|}, \dots, t_{ix}$ is resource disabled and waiting for t_{ix+n} , and t_{ix+n} is waiting for a transition in the same process or other processes, \dots , and t_{ix} is resource disabled and waiting for t_{jy} . Note, only the resource competition between different processes can constitute an RW. Since $t_{ix}, t_{ix+n} \in T_i$, there exists no RW under this situation. However, an EW $\langle t_{jy}, t_{kz}, t_{mn}, \dots, t_{ix}, t_{ix+n} \rangle$ can be constituted at M . no matter whether they are process disabled or resource disabled.

Example 11: As shown in Fig. 7(a), $t_6 \in T_1$ is waiting for $t_{11} \in T_2$ to release the resources in p_{19} and $t_{11} \in T_2$ is waiting for $t_9 \in T_1$ to make the resources in p_{18} adequate. Both t_6 and t_{11} are resource disabled while t_9 and t_8 are process disabled. The competition of t_6 and t_{11} for resource p_{19} and the competition of t_{11} and t_9 for resource p_{18} occur between different processes. Since t_9 and t_8 are process disabled, there exists no resource wait between t_9 and t_8 or t_8 and t_6 . Obviously, EWs are formed before RWs in such cases.

Example 12: Fig. 7(b) shows an EW, where both t_{11} and t_6 are resource disabled. The competition of t_{11} and t_6 for resource p_{17} exists between different processes, while the competition of t_6 and t_8 for resource p_{19} exists between the same process. An RW cannot be formed but an EW can. Clearly, EWs generate before RWs in such cases.

Remark 2: Lemma 4 illustrates the case that both EWs and RWs are formed simultaneously. Only in this case, can an EW and an RW have the same efficiency when avoiding deadlocks. Lemma 5 illustrates the case when EWs occur before RWs, indicating that EWs are much more efficient than RWs in avoiding deadlocks.

Lemma 6: Consider a WAMG (N, M_0) . If there exists an EW at $M \in R(N, M_0)$ and $\exists t \in T$ such that $t \notin$ any EW, then N is partially deadlocked and M is a partially deadlock marking.

Proof: According to Theorem 1, each EW consists of several dead transitions. If $\exists t \in T$ such that $t \notin$ any EW at M , then t is live. Therefore, N is partially deadlocked and M is a partially deadlock marking.

Lemma 7: Consider a WAMG (N, M_0) . If there exists an EW at $M \in R(N, M_0)$ and $\forall t \in T$ such that $t \in$ an EW, then N is totally deadlocked and M is a totally deadlock marking.

Proof: Since $\forall t \in T$ such that $t \in$ an EW, $\forall t \in T$ such that t is dead. Therefore, N is totally deadlocked and M is a totally deadlock marking.

Theorem 4: Deadlocks can be avoided earlier at a specified marking by using EWs in contrast to RWs

Proof: Let $N = (P, T, F, W)$ be a WAMG. According to the structure of a WAMG, we prove this proposition by the following two cases:

- Case 1) There is only one process in a WAMG, i.e., for $i \in \{1\}, \bar{N}_i = N \setminus (\{p_{0i}\} \cup P_{A_i}, T_i, F_i)$ is a strongly connected PN. M is a deadlock marking, i.e., $\exists t \in T_i, i \in \{1\}$, such that t is dead at $M \in R(N, M_0)$. When avoiding deadlock marking M at a given marking $M_x \in R(N, M_0)$, since the deadlock occurs only in \bar{N}_i , there exists an EW at M , but not an RW.
- Case 2) There are several processes in a WAMG, i.e., for each $i \in \mathbb{N}_K, \bar{N}_i = N \setminus (\{p_{0i}\} \cup P_{A_i}, T_i, F_i)$ is a strongly connected PN. A deadlock marking $M \in R(N, M_0)$ can be a partially deadlock marking or a totally deadlock marking. According to Lemmas 6 and 7, there are two cases:

- Case 2.1) M is a totally deadlock marking, i.e., $\forall t \in T$ such that t is dead at M . We suppose that \exists EW at $M' \in R(N, M_0)$ and \exists RW at $M'' \in R(N, M_0)$. There are three cases:

- * Case 2.1.1) If $M', M'' \in R(N, M_0)$ are two partially deadlock markings, which eventually reach M .
- * Case 2.1.2) If $M'' = M, M' \in R(N, M_0)$ is a partially deadlock marking, which eventually reaches M .
- * Case 2.1.3) If $M' = M'' = M$.

Assume that an EW exists at M' and an RW exists at M'' when avoiding deadlock markings at a given marking $M_x \in R(N, M_0)$. According to Lemmas 4 and 5, $\exists \sigma', \sigma'' \in T$ such that $M_x [\sigma'] M'$ and $M_x [\sigma''] M''$, then $|\sigma'| \leq |\sigma''|$.

- Case 2.2) M is a partially deadlock marking, i.e., $\exists t \in T_i, i \in \mathbb{N}_K$, such that t is dead at M . We suppose that \exists EW at $M' \in R(N, M_0)$ and \exists RW at $M'' \in R(N, M_0)$.

- * Case 2.2.1) $\forall t \in T_j, j \in \mathbb{N}_K$ and $i \neq j$, such that $M [t]$ holds.
- * Case 2.2.2) $\exists t \in T_j, j \in \mathbb{N}_K$ and $i \neq j$, such that t is dead at $M \in R(N, M_0)$. If $M', M'' \in R(N, M_0)$ are two partially deadlock markings, which eventually reach M .
- * Case 2.2.3) If $M'' = M, M' \in R(N, M_0)$ is a partially deadlock marking, which eventually reaches M .
- * Case 2.2.4) If $M' = M, M'' \in R(N, M)$.
- * Case 2.2.5) If $M' = M'' = M$.

In Case 2.2.1, when avoiding deadlock marking M at a given marking $M_x \in R(N, M_0)$, since the deadlock occurs only in \bar{N}_i instead of \bar{N}_j , there

exists an *EW* at M , but not an *RW*. In Case 2.2.2, Case 2.2.3, Case 2.2.4 and Case 2.2.5, when avoiding deadlock markings at a given marking $M_x \in R(N, M_0)$. According to Lemmas 4 and 5, $\exists \sigma', \sigma'' \in T$ such that $M_x [\sigma'] M'$ and $M_x [\sigma''] M''$, then $|\sigma'| \leq |\sigma''|$.

Next, we propose an approach to avoiding deadlocks via EWs.

First, a control law $f(M, t): \{t \mid M [t]\} \rightarrow \{0, 1\}$ of any marking $M \in R(N, M_0)$ is shown as follows: if the firing of t needs to be prevented, we set $f(M, t) = 0$; otherwise, we set $f(M, t) = 1$.

Then, we present the detailed procedures of our deadlock avoidance policy.

Consider a certain marking M in which deadlocks are to be avoided. If there is an *EW* at $M' \in R(N, M)$, then M' is a deadlock marking and the firing sequences from M to M' are forbidden. More specifically, given the current marking M ,

$$f(M, t) = \begin{cases} 0, & \text{if } \forall t \in T, \text{ such that } M [t]M', \\ & \text{where an EW exists at } M'; \\ 1, & \text{otherwise.} \end{cases} \quad (1)$$

The above procedure then repeats after the execution of the next marking.

Algorithm 1 is proposed to calculate a set of transitions that lead to no deadlock markings at $M \in R(N, M_0)$. The main steps of Algorithm 1 and its time complexity are summarized as follows.

First, we obtain all enabled transitions by traversing all transitions at M . Since there are at most $|T|$ transitions, the computation complexity of this step is $O(|T|)$. Then, we detect EWs at $M' \in R(N, M)$ via the following 5 steps:

- 1) Step 1 (Lines 9-11): Obtain a set of all disabled transitions at M' (denoted as T_1) by traversing all transitions. The computation complexity of this step is $O(|T|)$;
- 2) Step 2 (Lines 12-14): Obtain a set of transitions which satisfy the condition 3) of Definition 13 at M (denoted as T_2). All reachable markings need to be traversed in the worst case, thus the computation complexity of this step is $O(|R(N, M)|)$;
- 3) Step 3 (Line 15): Obtain a set of the event paths which consist of the transitions in T_2 (denoted as Γ) by the Depth First Search (DFS) Algorithm. Suppose that there are s directed arcs in a PN, $s \in \mathbb{N}^+$. The main step is to determine the paths between any two transitions in T_2 . Paths between $|T_2|^2$ pairs of nodes should be calculated at M . When calculating the path between two nodes, each place needs to be traversed to check whether it is connected to each transition. Similarly, each transition must be traversed to check whether it is connected to each place. Two directed arcs are then obtained, such that one is from a place to a transition and the other is from a transition to a place, forming a complete process. The complexity of this process is $O(|T| \cdot |P|)$. Nodes can be added to a path

Algorithm 1: Calculation of a Set of Transitions That Lead to No Deadlock Markings at M

```

1 Input: A WAMG  $N = (P, T, F, W)$  and a marking  $M$ ;
2 Output: A set of transitions that lead to no deadlock
  markings at  $M$ ;
3  $EP^f$ : the first transition in an event path  $EP$ ;
4  $EP^l$ : the last transition in an event path  $EP$ ;
5 for  $i = 1; i \leq |T|; i++$  do
6   if  $\forall p \in \bullet t_i, M(p) \geq W(p, t_i)$  then
7      $M [t_i] M', EW = T_1 = T_2 = \Gamma = \Delta = \emptyset$ ; for  $j =$ 
8        $1; j \leq |T|; j++$  do
9         if  $\exists p \in \bullet t_j, M'(p) < W(p, t_j)$  then
10           $T_1 = T_1 \cup t_j$ ;
11         for  $j = 1; j \leq |T_1|; j++$  do
12          if  $t_j$  satisfies the condition 3) of
13            Definition 13; then
14               $T_2 = T_2 \cup t_j$ ;
15          Obtain event paths which consist of the
16            transitions in  $T_2$  by DFS Algorithm and denote
17            as  $\Gamma = \{EP_1, EP_2, \dots, EP_m\}$ ;
18          Obtain event circuits which consist of the
19            transitions in  $T_2$  by DFS Algorithm and denote
20            as  $\Delta = \{EC_1, EC_2, \dots, EC_n\}$ ;
21          for  $j = 1; j \leq |\Gamma|; j++$  do
22            if  $EP_j^f \in EC_x \subseteq \Delta, EP_j^l \in EC_y \subseteq \Delta, x, y \in$ 
23               $\{1, 2, \dots, n\}$  then
24                 $EW = EW \cup EP_j$ ;
25            if  $EW = \emptyset$  then
26               $f(M, t_i) = 1, T_E = T_E \cup t_i$ ;
27            else
28               $f(M, t_i) = 0$ ;

```

if there exist connections between two nodes. Then, subsequent nodes are traversed. In the worst case, all the directed arcs need to be traversed in a PN when looking for a path, which means that the process with a complexity of $|T| \cdot |P|$ needs to be performed $s/2$ times. Therefore, the total computation complexity of this step is $O(|T_2|^2 \cdot (|T| \cdot |P|)^{s/2})$.

- 4) Step 4 (Line 16): Obtain a set of the event circuits which consist of the transitions in T_2 (denoted as Δ) by the Depth First Search Algorithm. When calculating an event circuit, each node needs to be traversed so as to determine whether it is connected to other nodes. Since there are $|T| + |P|$ nodes in total, the computation complexity of this step is $O(|T| + |P|^{(|T|+|P|)})$;
- 5) Step 5 (Line 17-23): Calculate EWs at M' and determine a set of transition that can be fired at M (denoted as T_E). All event paths in Γ need to be traversed, so the time complexity is $O(|\Gamma|)$.

TABLE 2. Reachable markings for the WAMG in Fig. 1.

M_i	Marking	M_i	Marking
M_0	[4 0 0 0 0 0 0 0 0 0 0 4 0 0 0 2 3 2 2 1]	M_{12}	[3 0 0 1 1 0 0 0 0 0 0 4 0 0 0 2 0 1 2 1]
M_1	[3 1 0 0 0 0 0 0 0 0 0 4 0 0 0 1 2 2 2 1]	M_{13}	[3 0 0 0 1 1 1 0 0 0 0 4 0 0 0 2 0 0 2 1]
M_2	[2 2 0 0 0 0 0 0 0 0 0 4 0 0 0 0 1 2 2 1]	M_{14}	[3 0 0 0 1 0 1 1 0 0 0 4 0 0 0 2 0 1 1 0]
M_3	[2 2 0 0 0 0 0 0 0 0 0 3 1 0 0 0 1 2 1 1]	M_{15}	[3 0 0 0 1 0 0 1 1 0 0 4 0 0 0 2 3 1 0 0]
M_4	[2 2 0 0 0 0 0 0 0 0 0 2 2 0 0 0 1 2 0 1]	M_{16}	[3 0 0 0 1 0 0 0 0 0 1 4 0 0 0 2 3 1 2 0]
M_5	[2 2 0 0 0 0 0 0 0 0 0 2 1 1 0 0 0 1 1 1]	M_{17}	[3 0 0 1 0 0 0 0 0 1 0 4 0 0 0 2 0 1 2 1]
M_6	[2 2 0 0 0 0 0 0 0 0 0 1 2 1 0 0 0 1 0 1]	M_{18}	[3 0 0 0 0 1 1 0 0 1 0 4 0 0 0 2 0 0 2 1]
M_7	[2 2 0 0 0 0 0 0 0 0 0 3 0 1 0 0 0 1 2 1]	M_{19}	[3 0 0 0 0 0 1 1 0 1 0 4 0 0 0 2 0 1 1 0]
M_8	[3 0 1 1 0 0 0 0 0 0 0 4 0 0 0 1 0 2 2 1]	M_{20}	[3 0 0 0 0 0 0 1 1 1 0 4 0 0 0 2 3 1 0 0]
M_9	[4 0 0 0 0 0 0 0 0 0 0 3 1 0 0 2 3 2 1 1]	M_{21}	[3 0 0 0 0 0 0 0 0 1 1 4 0 0 0 2 3 1 2 0]
M_{10}	[3 1 0 0 0 0 0 0 0 0 0 3 1 0 0 1 2 2 1 1]	M_{22}	[2 2 0 0 0 0 0 0 0 0 0 3 1 0 0 0 1 2 1 1]
M_{11}	[3 0 1 1 0 0 0 0 0 0 0 3 1 0 0 1 0 2 1 1]		

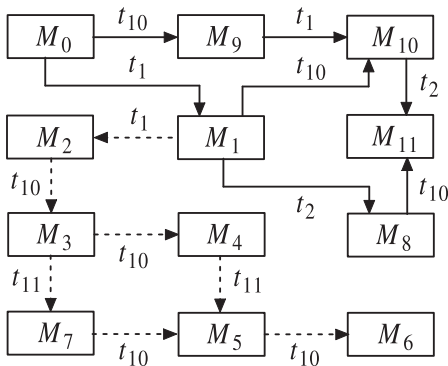


FIGURE 8. Partial reachability graph of the WAMG in Fig. 1 including $M_0 - M_{11}$.

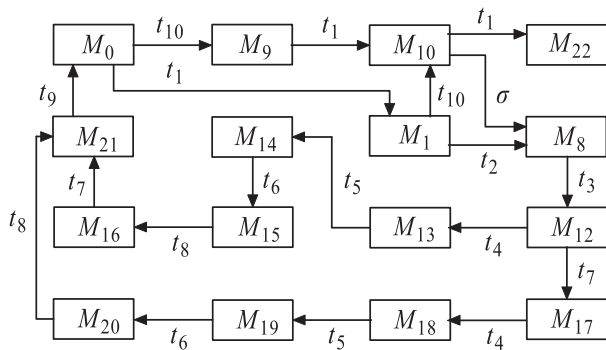


FIGURE 9. Partial reachability graph of the WAMG in Fig. 1 including $M_0 - M_1, M_8 - M_{10}$, and $M_{12} - M_{22}$.

In summary, the overall computation complexity of Algorithm 1 is $O(|T| \cdot |T_2|^2 \cdot (|T| \cdot |P|)^{s/2})$.

We now implement the proposed deadlock avoidance policy by the WAMG in Fig. 1. Assume that the structure of the WAMG in Fig. 1 remains unchanged whereas the initial marking is changed to $M_0 = [4 0 0 0 0 0 0 0 0 0 0 4 0 0 0 2 3 2 2 1]$.

A partial reachability graph of the WAMG is shown in Fig. 8, and the reachable markings are shown in Table 2.

Assume the net system is at M_1 . There are three transitions t_1, t_2 and t_{10} that can be fired at M_1 . It is necessary to predict whether the EWs exist at the markings reachable from M_1 after the execution of t_1, t_2 or t_{10} . If t_1 is fired, the WAMG can reach M_2 , which contains an EW $\langle t_2, t_6 \rangle$; if t_2 is fired, it can reach M_8 that does not contain any EW; and if t_{10} is fired, it can reach M_{10} that does not contain any EW. Therefore, $f(M_1, t_1) = 0, f(M_1, t_2) = 1$, and $f(M_1, t_{10}) = 1$. The firing of t_1 is forbidden which is represented by a dotted arrow. And the firing of t_2 and t_{10} are permitted, which are represented by solid arrows. In case such an EW $\langle t_2, t_6 \rangle$ at M_2 is not avoided beforehand, the system will eventually reach an RW $\langle p_{17}, p_{19} \rangle$ at a totally deadlock marking M_6 after 4 transitions. Clearly, the deadlock can be avoided earlier at M_1 by using EWs compared with RWs, indicating that EWs are much more efficient than RWs for deadlock avoidance. A partial reachability graph of the WAMG is shown in Fig. 9, it can be found that $M_0 \in R(N, M_1)$. After the firing of t_1 is forbidden at M_1 , there exist two firing sequences $\sigma_1 = \langle t_3, t_4, t_5, t_6, t_8, t_7, t_9 \rangle$ and $\sigma_2 = \langle t_3, t_7, t_4, t_5, t_6, t_8, t_7 \rangle$ such that $M_1 [t_2] M_8 [\sigma_1] M_0, M_1 [t_2] M_8 [\sigma_2] M_0, M_1 [t_{10}] M_{10} [\sigma] M_8 [\sigma_1] M_0$, and $M_1 [t_{10}] M_{10} [\sigma] M_8 [\sigma_2] M_0$, where $\sigma = \langle t_{10}, t_{11}, t_{12}, t_{11}, t_{13}, t_{12}, t_2, t_{13} \rangle$.

V. CONCLUSION

This paper proposes a new type of circular wait, namely, EWs, as an alternative to RWs that were treated as one of four necessary conditions for a deadlock. EWs are shown and proven to be more general and essential than RWs in WAMGs. We illustrate the relationship between EWs and deadlocks and show the conditions under which an EW can occur in PNs. This is critical of deadlock control of network systems. Since both siphons and EWs in PNs are employed as the structural characteristic of deadlock, we study the relationship between EWs and undermarked siphons in WAMGs. A necessary and sufficient condition is established between undermarked siphons and EWs. Finally, EWs are used to

avoid deadlocks. We show that deadlocks can be avoided earlier at a specified marking by using EWs rather than RWs, indicating that EWs are much more efficient than RWs for deadlock avoidance. In future research, the application scope of EWs for deadlock avoidance should be further expanded.

REFERENCES

- [1] F. Basile, R. Cordone, and L. Piroddi, "Integrated design of optimal supervisors for the enforcement of static and behavioral specifications in Petri net models," *Automatica*, vol. 49, no. 11, pp. 3432–3439, Nov. 2013.
- [2] E. G. Coffman, M. Elphick, and A. Shoshani, "System deadlocks," *ACM Comput. Surveys*, vol. 3, no. 2, pp. 67–78, Jun. 1971.
- [3] C. Chen and H. Hu, "Liveness-enforcing supervision in AMS-oriented HAMGs: An approach based on new characterization of siphons using Petri nets," *IEEE Trans. Autom. Control*, vol. 63, no. 7, pp. 1987–2002, Jul. 2018.
- [4] C. Chen and H. Hu, "Static and dynamic partitions of inequalities: A unified methodology for supervisor simplification," *IEEE Trans. Autom. Control*, vol. 64, no. 11, pp. 4748–4755, Nov. 2019.
- [5] C. Chen and H. Hu, "Time-varying automated manufacturing systems and their invariant-based control: A Petri net approach," *IEEE Access*, vol. 7, pp. 23149–23162, 2019.
- [6] F. Chu and X.-L. Xie, "Deadlock analysis of Petri nets using siphons and mathematical programming," *IEEE Trans. Robot. Autom.*, vol. 13, no. 6, pp. 793–804, Dec. 1997.
- [7] V. Deverakonda and R. S. Sreenivas, "On a sufficient information structure for supervisory policies that enforce liveness in a class of general Petri nets," *IEEE Trans. Autom. Control*, vol. 60, no. 7, pp. 1915–1920, Jul. 2015.
- [8] N. Du and H. Hu, "A robust prevention method for automated manufacturing systems with unreliable resources using Petri nets," *IEEE Access*, vol. 6, pp. 78598–78608, 2018.
- [9] J. Ezpeleta, J. M. Colom, and J. Martinez, "A Petri net based deadlock prevention policy for flexible manufacturing systems," *IEEE Trans. Robot. Autom.*, vol. 11, no. 2, pp. 173–184, Apr. 1995.
- [10] A. Giua, C. Seatzu, and F. Basile, "Observer-based state-feedback control of timed Petri nets with deadlock recovery," *IEEE Trans. Autom. Control*, vol. 49, no. 1, pp. 17–29, Jan. 2004.
- [11] H. Hu and Z. Li, "An optimal-elementary-siphons-based iterative deadlock prevention policy for flexible manufacturing systems," *Int. J. Adv. Manuf. Technol.*, vol. 38, nos. 3–4, pp. 309–320, Aug. 2008.
- [12] H. Hu, M. Zhou, Z. Li, and Y. Tang, "An optimization approach to improved Petri net controller design for automated manufacturing systems," *IEEE Trans. Autom. Sci. Eng.*, vol. 10, no. 3, pp. 772–782, Jul. 2013.
- [13] H. Hu and Y. Liu, "Supervisor simplification for AMS based on Petri nets and inequality analysis," *IEEE Trans. Autom. Sci. Eng.*, vol. 11, no. 1, pp. 66–77, Jan. 2014.
- [14] H. Hu, Y. Liu, and L. Yuan, "Supervisor simplification in FMSs: Comparative studies and new results using Petri nets," *IEEE Trans. Control Syst. Technol.*, vol. 24, no. 1, pp. 81–95, Jan. 2016.
- [15] H. Hu, R. Su, M. Zhou, and Y. Liu, "Polynomially complex synthesis of distributed supervisors for large-scale AMSs using Petri nets," *IEEE Trans. Control Syst. Technol.*, vol. 24, no. 5, pp. 1610–1622, Sep. 2016.
- [16] H. Hu, M. Zhou, Z. Li, and Y. Tang, "Deadlock-free control of automated manufacturing systems with flexible routes and assembly operations using Petri nets," *IEEE Trans. Ind. Informat.*, vol. 9, no. 1, pp. 109–121, Feb. 2013.
- [17] H. Hu and M. Zhou, "A Petri net-based discrete-event control of automated manufacturing systems with assembly operations," *IEEE Trans. Control Syst. Technol.*, vol. 23, no. 2, pp. 513–524, Mar. 2015.
- [18] Y. Huang, M. Jeng, X. Xie, and S. Chung, "Deadlock prevention policy based on Petri nets and siphons," *Int. J. Prod. Res.*, vol. 39, no. 2, pp. 283–305, Jan. 2001.
- [19] Z. Li and M. Zhou, "Elementary siphons of Petri nets and their application to deadlock prevention in flexible manufacturing systems," *IEEE Trans. Syst., Man, Cybern. A, Syst. Humans*, vol. 34, no. 1, pp. 38–51, Jan. 2004.
- [20] Z. Li, G. Liu, H. Michael, and M. Zhou, "Erratum to deadlock prevention based on structure reuse of Petri net supervisors for flexible manufacturing systems," *IEEE Trans. Syst., Man, Cybern. Syst.*, vol. 43, no. 2, p. 474, Mar. 2013.
- [21] Z. Li, N. Wu, and M. Zhou, "Deadlock control of automated manufacturing systems based on Petri nets—A literature review," *IEEE Trans. Syst., Man, Cybern. C, Appl. Rev.*, vol. 42, no. 4, pp. 437–462, Jul. 2012.
- [22] J. Luo, Z. Liu, and M. Zhou, "A Petri net based deadlock avoidance policy for flexible manufacturing systems with assembly operations and multiple resource acquisition," *IEEE Trans. Ind. Informat.*, vol. 15, no. 6, pp. 3379–3387, Jun. 2019.
- [23] J. Luo and K. Nonami, "Approach for transforming linear constraints on Petri nets," *IEEE Trans. Autom. Control*, vol. 56, no. 12, pp. 2751–2765, Dec. 2011.
- [24] J. Luo, H. Ni, W. Wu, S. Wang, and M. Zhou, "Simultaneous reduction of Petri nets and linear constraints for efficient supervisor synthesis," *IEEE Trans. Autom. Control*, vol. 60, no. 1, pp. 88–103, Jan. 2015.
- [25] Z. Ma, Y. Tong, Z. Li, and A. Giua, "Basis marking representation of Petri net reachability spaces and its application to the reachability problem," *IEEE Trans. Autom. Control*, vol. 62, no. 3, pp. 1078–1093, Mar. 2017.
- [26] T. Murata, "Petri nets: Properties, analysis and applications," *Proc. IEEE*, vol. 77, no. 4, pp. 541–579, Apr. 1989.
- [27] J. Park and S. A. Reveliotis, "Deadlock avoidance in sequential resource allocation systems with multiple resource acquisitions and flexible routings," *IEEE Trans. Autom. Control*, vol. 46, no. 10, pp. 1572–1583, Oct. 2001.
- [28] E. Salimi and R. S. Sreenivas, "On invariant-based monitors that enforce liveness in a class of partially controlled general Petri nets," *IEEE Trans. Autom. Control*, vol. 60, no. 10, pp. 2825–2830, Oct. 2015.
- [29] F. Tricas, F. García-Vallés, J. M. Colom, and J. Ezpeleta, "A Petri net structure-based deadlock prevention solution for sequential resource allocation systems," in *Proc. IEEE Int. Conf. Robot. Autom.*, Barcelona, Spain, Apr. 2005, pp. 271–277.
- [30] N. Viswanadham, Y. Narahari, and T. L. Johnson, "Deadlock prevention and deadlock avoidance in flexible manufacturing systems using Petri net models," *IEEE Trans. Robot. Autom.*, vol. 6, no. 6, pp. 713–723, Dec. 1990.
- [31] N. Wu, "Deadlock avoidance in AGV system using colored Petri net model," *Int. J. Prod. Res.*, vol. 40, no. 1, pp. 223–238, 2002.
- [32] N. Wu and M. Zhou, "Avoiding deadlock and reducing starvation and blocking in automated manufacturing systems," *IEEE Trans. Robot. Autom.*, vol. 17, no. 5, pp. 657–668, Oct. 2001.
- [33] N. Wu, M. Zhou, and G. Hu, "One-step look-ahead maximally permissive deadlock control of AMS by using Petri nets," *ACM Trans. Embedded Comput. Syst.*, vol. 12, no. 1, pp. 10:1–10:23, Jan. 2013.
- [34] X. Xie and M. Jeng, "ERCN-merged nets and their analysis using siphons," *IEEE Trans. Robot. Autom.*, vol. 15, no. 4, pp. 692–703, Aug. 1999.
- [35] K. Xing, F. Wang, M. C. Zhou, H. Lei, and J. Luo, "Deadlock characterization and control of flexible assembly systems with Petri nets," *Automatica*, vol. 87, pp. 358–364, Jan. 2018.
- [36] K. Xing, M. Zhou, F. Wang, H. Liu, and F. Tian, "Resource-transition circuits and siphons for deadlock control of automated manufacturing systems," *IEEE Trans. Syst., Man, Cybern. A, Syst. Humans*, vol. 41, no. 1, pp. 74–84, Jan. 2011.
- [37] Y. Yang and H. Hu, "Implementation of distributed control of hierarchical assembly systems via extended critical places," *IEEE Access*, vol. 7, pp. 182937–182950, 2019.
- [38] X. Yin and S. Lafortune, "Synthesis of maximally permissive supervisors for partially-observed discrete-event systems," *IEEE Trans. Autom. Control*, vol. 61, no. 5, pp. 1239–1254, May 2016.
- [39] Y. Zhou, H. Hu, Y. Liu, and Z. Ding, "Collision and deadlock avoidance in multirobot systems: A distributed approach," *IEEE Trans. Syst., Man, Cybern. Syst.*, vol. 47, no. 7, pp. 1712–1726, Jul. 2017.
- [40] Y. Zhou, H. Hu, Y. Liu, S.-W. Lin, and Z. Ding, "A distributed approach to robust control of multi-robot systems," *Automatica*, vol. 98, pp. 1–13, Dec. 2018.
- [41] Y. Zhou, H. Hu, Y. Liu, S.-W. Lin, and Z. Ding, "A distributed method to avoid higher-order deadlocks in multi-robot systems," *Automatica*, vol. 112, pp. 1–13, Feb. 2020.



XING FAN received the B.S. degree in automation from the Shaanxi University of Science and Technology, Xi'an, China, in 2015. She is currently pursuing the Ph.D. degree in control theory and control engineering with Xidian University. Her research interests include discrete event systems and their supervisory control techniques, Petri nets, and automated manufacturing systems.



BENYUAN YANG received the B.S. degree in logistics engineering from the Tianjin College, University of Science and Technology Beijing, Tianjin, China, in 2014, and the M.S. degree in logistics engineering from the University of Science and Technology Beijing, in 2017. He is currently pursuing the Ph.D. degree in control theory and control engineering with Xidian University, Xi'an, China. His research interests include discrete event systems and their supervisory control techniques, Petri nets, automated manufacturing systems, business process management, and distributed control techniques.



HESUAN HU (Senior Member, IEEE) received the B.S. degree in computer engineering and the M.S. and Ph.D. degrees in electro-mechanical engineering from Xidian University, Xi'an, China, in 2003, 2005, and 2010, respectively.

He is currently a Professor with Xidian University and also with Nanyang Technological University, Singapore, and a Researcher with Xi'an Jiaotong University, Xi'an. He holds over 30 issued and filed patents in his fields of expertise.

He has over 130 publications in journals, book chapters, and conference proceedings in the above areas. His current research interests include discrete event systems and their supervisory control techniques, Petri nets, automated manufacturing systems, multimedia streaming systems, autonomous vehicles, cyber security, and artificial intelligence.

Prof. Hu was a recipient of many national and international awards, including the Franklin V. Taylor Memorial Award for Outstanding Papers from the IEEE SMC Society, in 2010, and the finalist of the Best Automation Paper from the IEEE ICRA Society, in 2013, 2016, and 2017, respectively. He has been an Associate Editor of the *IEEE Control Systems Magazine*, *IEEE Robotics and Automation Magazine*, *IEEE TRANSACTIONS ON AUTOMATION SCIENCE AND ENGINEERING*, and *Journal of Intelligent Manufacturing*. He was on the editorial board over ten international journals.

• • •