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High-Efficiency High Voltage Hybrid Charge Pump Design With an Improved Chip Area

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ABSTRACT A hybrid charge pump was developed in a 0.13-μm Bipolar-CMOS-DMOS (BCD) process which utilised high drain-source voltage MOS devices and low-voltage integrated metal-insulator-metal (MIM) capacitors. The design consisted of a zero-reversion loss cross-coupled stage and a new self-biased serial-parallel charge pump design. The latter has been shown to have an area reduction of 60% in comparison to a Schottky diode-based Dickson charge pump operating at the same frequency. Post-layout simulations were carried out which demonstrated a peak efficiency of 38% at the output voltage of 18.5 V; the maximum specified output voltage of 27 V was also achieved. A standalone serial-parallel charge pump was shown to have a better transient response and a flatter efficiency curve; these are preferable for time-sensitive applications with a requirement of a broader range of output currents. These findings have significant implications for reducing the total area of implantable high-voltage devices without sacrificing charge pump efficiency or maximum output voltage.

INDEX TERMS Charge pump, high-voltage, hybrid, BCD, small-area, cross-coupled, serial-parallel.

I. INTRODUCTION

Since the inception of the first transistor device many decades ago, the continuous miniaturization of transistor size has been the primary driving force of CMOS manufacturers. Smaller devices permit lower operating voltages, which enable power savings, and allows the conception of ultra-low-power devices. Though this is generally true for digital processors and memory devices, the same cannot be said for analog circuits. In particular, analog front-ends (AFEs) for sensors and actuators depend on physical limits of the driven device and naturally-occurring signals. This poses a contradictory requirement for electronic devices where miniaturisation and low power consumption are essential. Systems such as wearable and implantable medical devices and point-of-care diagnostic tools use state-of-the-art CMOS technology nodes to reduce their form factor, but the in-built sensors often require voltages significantly larger than the nominal supply voltage. Portable ultrasound front-ends, SPAD (single photon avalanche diode) imagers and electrical neuro-stimulator devices are good examples of a high voltage supply created locally in order to drive the sensor or actuator, while the rest of the analog/digital processing is done with a much lower supply voltage. Hence, in these systems, it is essential to integrate a low-area, high-efficiency charge pump along with the AFE.

A high excitation voltage is fundamental in many ultrasound applications that utilise the piezoelectric effect. Achieving the required image quality is often possible only through a high amplitude driving pulse and/or high DC bias voltages in capacitive micromachined ultrasonic transducer (CMUT) devices. For ultrasound applications in ultra-low form factor devices, such as capsule endoscopy [1], intracardiac echocardiography (ICE) [2] and other handheld devices [3], a bulky switched-inductor approach for voltage amplification is not feasible. Hence, a low-area charge pump is a logical choice. Similarly, autofluorescence imaging using SPADs is now being explored in endoscopes [4] and capsule applications [5]. Such systems rely on reverse biasing an array of diodes and then counting discrete avalanche breakdown

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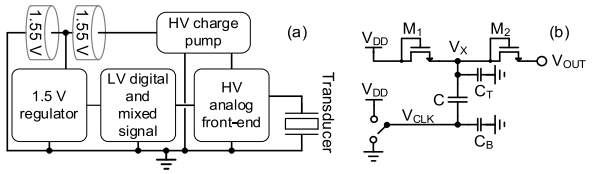

FIGURE 1. a) A generic block diagram of an IoT sensor/actuator running from two standard 1.55 V coin cells. b) A basic single-stage Dickson charge pump circuit diagram.

events triggered by single photons. The diode breakdown voltage varies significantly with technology and design, but voltages above 20 V are not uncommon [5], [6]. Another example of high voltage generation is found in both implanted and external environments in neurostimulation and sensing applications, in cases where area and power limitations are extremely strict. Here the voltage requirement can vary widely in the range 5 – 30 V depending on the electrode impedance and stimulation strength (μA - mA).

For biologically implantable and IoT applications power is usually generated by lower voltage coin cell batteries. A 1.55 V silver-oxide battery is a standard choice that has a high power-density-to-weight ratio and can tolerate high current loads. However, amplifying this voltage to up to 20 V would significantly impact the efficiency of the voltage conversion. In the proposed system (Figure 1(a)), two coin-cell batteries, connected in series, are used to provide 3.1 V as an input to the charge pump, effectively halving the required number of stages in the charge pump. At the same time, 1.55 V supply can be used to power lower voltage digital and analog domains.

Standard nanometre-scale technology can be used to reach output voltages as high as 36 V [7] but this is possible only for small output currents. Another option is to use Bipolar-CMOS-DMOS (BCD) [8] technology which incorporates high-voltage capabilities but usually comes with higher manufacturing costs. Consequently, there is a need for area-saving designs, which maintain high efficiency and current requirements to counterbalance increased costs per silicon area.

In this paper, we present a fully integrated hybrid charge pump implemented in a 0.13-μm BCD process. An efficient and fast-transient charge pump was conceived by incorporating cross-coupled and serial-parallel charge pumps operating at different frequencies. Voltages across all flying capacitors were kept under 6 V which permitted the use of metal-insulator-metal (MIM) capacitors instead of metal-oxide-metal (MOM) capacitors throughout the design. The capacitive density of MOM capacitors were 1.22 fF/μm^2 whilst using metal layers M1-M5; MIM capacitors were implemented in layers M5-M6 and were determined by the technology to have a capacitance of 1.5 fF/μm^2. By utilising low-voltage capacitors, an effective area-saving of 60% for the 6 – 30 V charge pump stages was achieved.

The paper is organised as follows: Section II introduces the basic principles of a charge pump and the main areas of consideration for an optimal charge pump design; Section III presents the architecture and operating principles of an area-efficient hybrid charge pump design. In Section IV, measurement and post-layout simulation results are discussed and, finally, Section V guides the reader through an analysis of the results and possible hybrid charge pump alterations to meet different system requirements.

II. CHARGE PUMP THEORY OF OPERATION

A charge pump is a device used to boost a supply voltage. The underlying principle of every charge pump is based on rapidly charging and discharging a capacitor resulting in the potential at the top plate being a discrete value multiplier of the supply voltage.

Figure 1(b) shows a simplified diagram of a generic single-stage Dickson charge pump design where M_1 and M_2 are diode-connected nMOS devices [9]. The charge pump is driven by a single clock with an amplitude of V_{DD}. During phase one, when V_{CLK} is low, capacitor C is charged to (V_{DD}–V_T) through M_1, where V_T is the threshold voltage of a diode-connected MOS device. During phase two, V_{CLK} goes to V_{DD}, boosting the voltage at node V_x to (2*V_{DD}-V_T). Consequently, M_2 starts to conduct current, and the output is charged to 2*(V_{DD}-V_T). The operation is then continuously repeated with the capacitor being discharged to the output every half-period.

By including parasitic capacitances charged every cycle, a full expression for the output voltage at zero output current can be written as [10]:

$$V_{out} = V_{DD}\left(1 + N\frac{C}{C + C_{par}}\right) - (N+1)\,V_T \qquad (1)$$

where N is the number of stages, C is capacitor value (generally called the flying capacitor), C_T is the parasitic capacitance and V_T is the threshold voltage of a switch. It is important to note that the parasitic capacitance C_B, present at the bottom plate of the flying capacitor, is closer to the conductive layers underneath it and is significantly larger than the top plate parasitic capacitance. This contributes to an increase in the overall power consumption and affects the transient response seen at the V_{CLK} node; however, only C_T is in parallel to the main capacitor C, seen at the node V_X. As a result, only parasitic capacitance C_T contributes to V_{OUT} losses.

It is evident from Equation (1) that, in order to optimise the performance of any charge pump, the diode drop has to be eliminated and the parasitic capacitance must be minimised. Other issues stemming from this implementation are also present. For example, due to an increase in the source voltage at every stage, a body effect causes the threshold voltage of an nMOS transistor to increase until the pumping efficiency of the charge pump is degraded [11].

Minimisation of parasitic effects can be achieved by choosing MIM capacitors which are further away from the substrate; however, this is usually not viable for high-voltage applications, and MOM capacitors must be used. Eliminating the diode drop can be achieved through active switching of

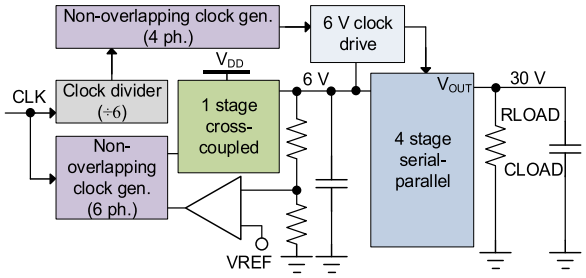

FIGURE 2. System diagram of the proposed hybrid charge pump.

the nMOS using an auxiliary circuit; however, this becomes complicated for non-linear type charge pumps, in which the amplification factor is non-linearly proportional to the number of pumping stages [12]. The body effect can be eliminated by appropriate biasing techniques; here butting the source and body is the preferred option in a triple-well process [13]. Integration of these approaches leads to the highest efficiency and output voltage results. A design which implements all of the techniques whilst using high-efficiency, cross-coupled and self-biased serial-parallel charge pumps is presented in the following sections.

III. A HYBRID CHARGE PUMP ARCHITECTURE

This section describes the overall make-up of the charge pump to achieve high voltage generation, above 20 V, from two serially-connected 1.55 V coin-cell batteries operating as a 3.1 V input voltage source. It then discusses the final circuit implementation to provide a continuous unregulated output current.

A. CONTINUOUS OPERATION CHARGE PUMP

The overall design of a hybrid charge pump can be seen in Figure 2. It consists of two sub-pumps: a single-stage, regulated cross-coupled pump and a four-stage serial-parallel pump. Initially, the supply voltage is doubled to a value of 6 V which is used to source both the input and the clock of the serial-parallel stages. This has multiple functions. Firstly, it has been observed in the simulations that the efficiency of subsequent serial-parallel pumping stages is proportional to the input voltage and reaches its highest value at an input of 6 V. The resistivity of switches does not change with varying input voltage and does not play a meaningful role in efficiency when operating in slow switching mode (i.e., the switching period is significantly larger than time constants from capacitances and resistances of integrated components and interconnects). However, a higher input voltage results in a larger amount of charge stored and then transferred from the flying capacitors, consequently increasing the efficiency. Secondly, the serial-parallel charge pump operates non-symmetrically: the current draw is much higher half of the time (charging phase) than it is in the output stage. A regulated cross-coupled stage adjusts for the difference in load requirements, improves the overall charge pump efficiency and ensures that the voltage does not exceed the 6 V limit. Thirdly, the number of stages is cut in half by doubling the clock voltage, and the transient response of the output voltage is faster. This is particularly important in applications where the system must boost the input voltage promptly after a prolonged standby period. Finally, a voltage of at least 5 V is often required to drive the high-voltage laterally-diffused MOS (LDMOS) switches used in other parts of a chip – the regulated output eliminates the need for an additional charge pump.

The design uses 5 V transistors for lower voltage operating regions and high-voltage transistors with a drain-source tolerance of up to 28 V elsewhere. The gate length of the 5 V MOS devices was extended to increase their maximum voltage tolerance by 10%, from 5.5 V up to 6 V. The capability for this increase was confirmed by tests beforehand by the foundry. The first doubler stage operates at a clock base frequency of 20 MHz and uses two 30 pF MIM capacitors, whilst the second sub-pump is driven by a clock of 2.5 MHz (six times slower) and uses a 15 pF MIM capacitor per stage. A 20 pF MOS capacitor was included between the two charge pump stages to smooth voltage spikes caused by charge redistribution from serial-parallel stage switches.

The overall operation of the hybrid charge pump can be explained by analysing the two sub-pumps separately.

B. THE CROSS-COUPLED CHARGE PUMP

For the first stage, a cross-coupled charge pump was chosen due to its high efficiency, as reported in previous work [13]. A generic cross-coupled charge pump (Figure 3) [14]–[16] (has two complementary branches operating in opposite phases, each actively controlling the switches of the other. Under stable conditions, the operation of the charge pump is as follows. Clock Φ_A is high and Φ_B is low; node V_A is at 2^*V_{DD}, connected to the output through M_{P2}. At the same time, node V_B is charged to V_{DD} through M_{N1} whilst M_{P1} is off. One node is being charged by the input whilst the other one is supplying current to the output. In the next phase, the voltages of clocks Φ_A and Φ_B alternate and the cycle is repeated in a mirrored manner. In comparison to a Dickson charge pump, the cross-coupled implementation eliminates the diode drop across stages and improves output voltage ripple due to the two pumping branches operating in parallel. In a way similar to a Dickson design, dynamic body biasing and other techniques can be applied to ensure reliability as the number of stages increases.

The main drawback of the basic cross-coupled design is the reverse charge flow [17]. During clock transitions, both n-type and p-type devices are turned on simultaneously for a short time (Figure 3, timing diagram). As a result, a path for reverse charge flow from the output to the top capacitor nodes and from the nodes to the input exists. Previous work has shown that by including a non-overlapping period between the two main phases and adding two additional phases to control the nMOS and pMOS transistors separately, any reverse flow conditions can be prevented, increasing efficiency significantly [18]–[20].

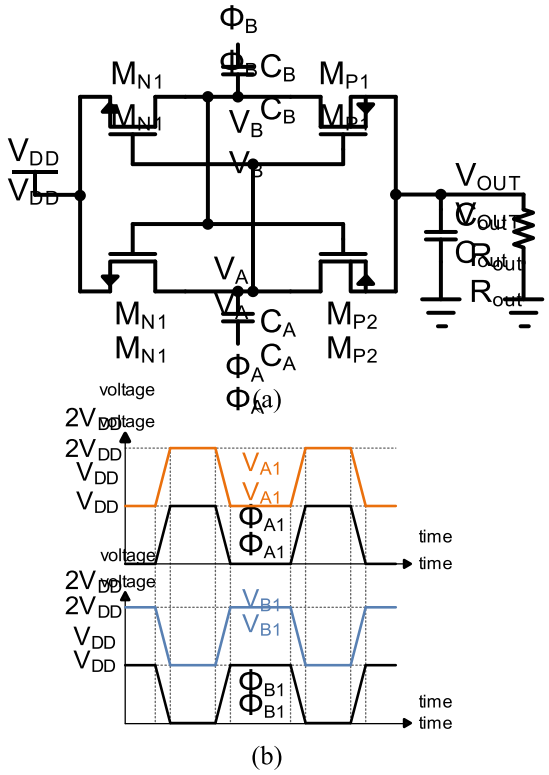

FIGURE 3. Zero reversion loss cross-coupled charge pump schematic (a) and timing diagram (b).

C. ZERO REVERSION LOSS CROSS-COUPLED STAGE

The cross-coupled charge pump used in this design is a cross-coupled doubler with an auxiliary circuit, presented previously by Kim *et al.* [21]. It operates with a four-phase non-overlapping clock scheme which ensures that each switch in the main pumping branch is controlled separately (Figure 4). A secondary cross-coupled charge pump circuit (M_{N3}, M_{N4}, C_{C1}, C_{C2}) is used to level-shift the control signals for the nMOS up by V_{DD}. Assuming steady-state operation, the signal Φ_{A1} in the bottom charging path is initially low, which turns on M_{P1}; Φ_{A2} is high, which turns on M_{N2}, and V_{A1} is charged to V_{DD}. At the same time, in the top path Φ_{B1} is high, i.e. V_{B1} is at 2^*V_{DD} and connected to the output through M_{P1}; M_{N1} is turned off by the low clock signal Φ_{B2} and voltage V_{B2} is at V_{DD}. On the next transition, Φ_{A2} goes low first and disables M_{N2} which puts node V_{A1} into a high-impedance state. Clock Φ_{A1} goes high which boosts V_{A1} to 2^*V_{DD} and turns M_{P1} off. Clock Φ_{B1} then goes low and the voltage at node V_{B1} drops by V_{DD}, which turns M_{P2} on and the charge starts to flow from C_A to the output. Finally, Φ_{B1} goes high and turns M_{N1} on, and capacitor C_B is recharged to V_{DD}. The cycle is inverted for the second part of the operational routine. The switching logic ensures that the charge always flows from the input to a flying capacitor and from the capacitor to the output. The auxiliary capacitors are approximately 10x smaller than the main charge pump and, together with the additional switches, incur minimal area and power losses.

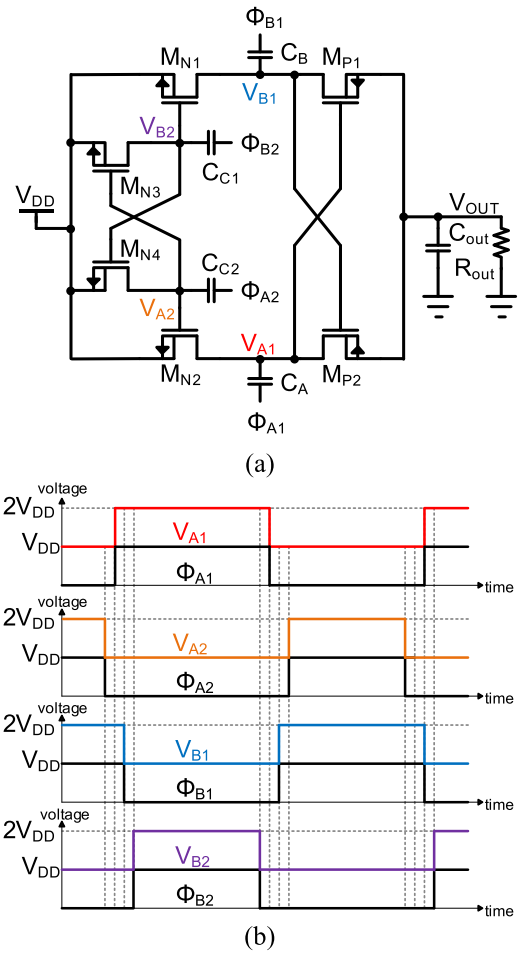

FIGURE 4. Zero-reversion loss cross-coupled charge pump schematic (a) and timing diagram (b).

The capacitive level shifter can be used to control both pMOS and/or nMOS switches. It was used to control nMOS devices in the present design for two reasons. Firstly, the quantity of charge required to drive a gate in a MOS device is proportional to the gate capacitance and must be large enough to push it into saturation. An nMOS device is much smaller than a pMOS device for the same conductivity at an equal overhead voltage. Furthermore, the high control signal for a pMOS device must be close to the output voltage of 2^*V_{DD} to fully turn it off, whereas a level-shifted signal can turn on an nMOS device effectively as long as the driving voltage is above $V_{DD} + V_{thNMOS}$. As the main pump capacitors are large and the voltages across them already vary between V_{DD} and 2^*V_{DD}, it is logical to use them to drive the pMOS device of an adjacent branch whilst using the auxiliary circuit to control the nMOS switches.

D. SERIAL-PARALLEL CHARGE PUMP

A simplified diagram of a serial-parallel charge pump [22] can be seen in Figure 5. In contrast to cross-coupled and Dickson charge pumps, the serial-parallel operation is asymmetric: during the charging phase, switches S_A are turned on

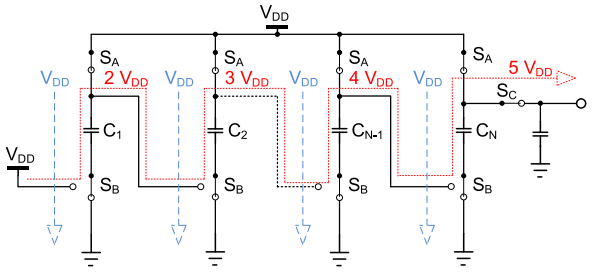

FIGURE 5. Simplified serial-parallel charge pump schematic.

and S_B are connected to ground: all capacitors are charged to V_{DD} in parallel. During the output phase, switches S_A are disconnected, S_B of the first stage is connected to V_{DD} and the remaining S_B are connected to each previous stage, forming a serially connected chain of capacitors. A current flows from V_{DD} to C_1, from C_1 to C_2, etc. to the output. The voltage at each node is proportional to the stage number and high V_{DS} tolerant switches are required. In contrast, the maximum voltage across any flying capacitor is never higher than V_{DD} and, thus, low-voltage MIM capacitors can be used.

The proposed design, Figure 6, incorporates a self-biasing technique. Normally, high-voltage MOS devices can tolerate V_{DS} up to 36 V but are limited to a maximum of 5.5 V gate-source voltage. Due to high voltage swings equal to N^*V_{DD}, where N is the number of pumping stage, a complex biasing scheme would be required to ensure reliable operation [23]. This would increase both the area and power losses. As a better alternative, an auxiliary charge pump (M_{A1-3}, C_0) is used to drive the high-side switches M_{B1-4}. The gate of the inter-stage switch M_{B6} is biased by V_{DDSP} and the switches M_{B7-8} are biased by their preceding stages; low-side switches M_{B6-12} are controlled by a 3.1 V clock. The auxiliary charge pump is cross-coupled to the first stage of the serial-parallel pump: during start-up, all high-side switches conduct current through their body diodes and pre-charge capacitors C_{0-4} to (V_{DD}-V_{diode}); no other start-up circuit is required. The only disadvantage of this operation is the existence of a body (M_{B4}) and Schottky (D_2) diodes between V_{DD} and V_{OUT} which results in a static current if the charge pump is disabled for a long period.

The clock diagram of the serial-parallel pump can be seen in Figure 6. V_{DDSP} is supplied by a cross-coupled charge pump with value of 2^*V_{DD}. Clocks Φ_{A1}, Φ_{B1}, Φ_X and Φ_Y are non-overlapping to remove crowbar currents through switches $M_{A2/3}$ and $M_{B5/9-11}$; Φ_X and Φ_Y are boosted into the range $V_{DD} - 2^*V_{DD}$ to control high-side switches. Under steady-state conditions, the charge pump operates as follows. During the charging phase, clocks Φ_{X1} and Φx are low and Φ_{Y1} is high. V_{SP0} is boosted to 2^*V_{DDSP} – this enables M_{B1-4} and nodes V_{SP1-4} are charged to V_{DDSP}. In turn, node V_{SP1} has voltage V_{DDSP} and M_{A1} is disabled. On the next clock transition, the boosted signal Φ_X goes high to V_{DDSP} and Φ_{Y1} goes low: the bottom plates of C_0 and C_{1-4} are disconnected from the supply and the ground

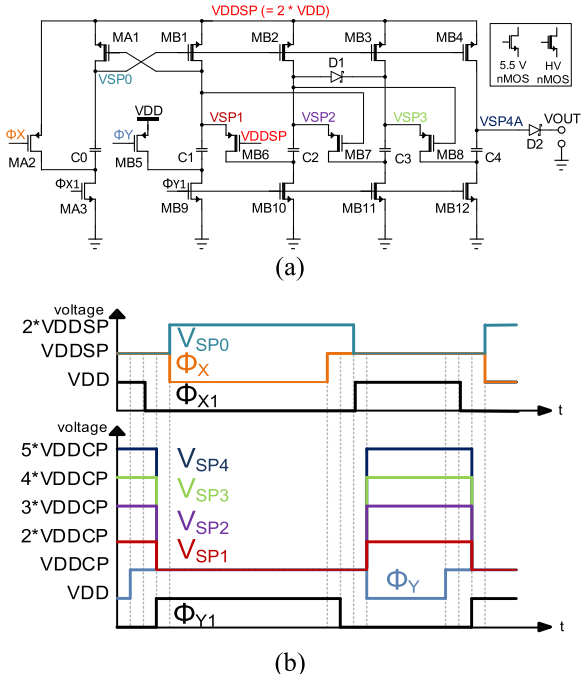

FIGURE 6. Proposed serial-parallel charge pump schematic (a) and timing diagram (b).

node accordingly. Clock Φ_{X1} then goes high which pulls the M_{B1-4} gate voltage down to V_{DDSP}, disabling the switches in the process. Finally, Φ_Y goes down to V_{DD} and M_{B5} starts charging bottom plate of C_2. As a result, voltage V_{SP1} starts rising until it reaches $V_{DDSP} + V_{THP}$ and M_{B6} starts to conduct current. The voltage at V_{SP2} then starts increasing, following the voltage at node V_{SP1}. The gate voltage of M_{B7} follows V_{SP1} and M_{B7} starts conducting when V_{SP2} is equal to $V_{SP1}+ V_{THP}$. The same principle applies to nodes V_{SP3} and V_{SP4} until V_{SP4} is boosted to 5^*V_{DDSP} and the current flows to the output. On the next clock transition, clocks Φ_Y and then Φ_{Y1} go high to V_{DDSP} and V_{DD} respectively and discharge all the capacitors simultaneously. Afterwards, clock Φ_{X1} goes low, followed by Φ_X and the recharge cycle is repeated.

Two Schottky diodes were used in the design. The first diode was placed between charge pump stages two and three. During the transition between the charging and output phases, a small delay exists, caused by the time required to turn the inter-stage pMOS switches on. As a result, the voltage at node V_{SP2A} rises significantly faster than the voltage at stage V_{SP3A} and the source-gate voltage across M_{B8} can reach more than a 6 V difference, which would cause reliability issues in the long term. The additional diode D_1 between the two stages solves the issue by conducting the current intermittently.

The second diode was used as an output pass device. An actively switched MOSFET with a high-voltage level shifter could be used in place of the diode to eliminate the voltage drop. This would increase the output voltage sourcing capability, but the efficiency improvement would be marginal

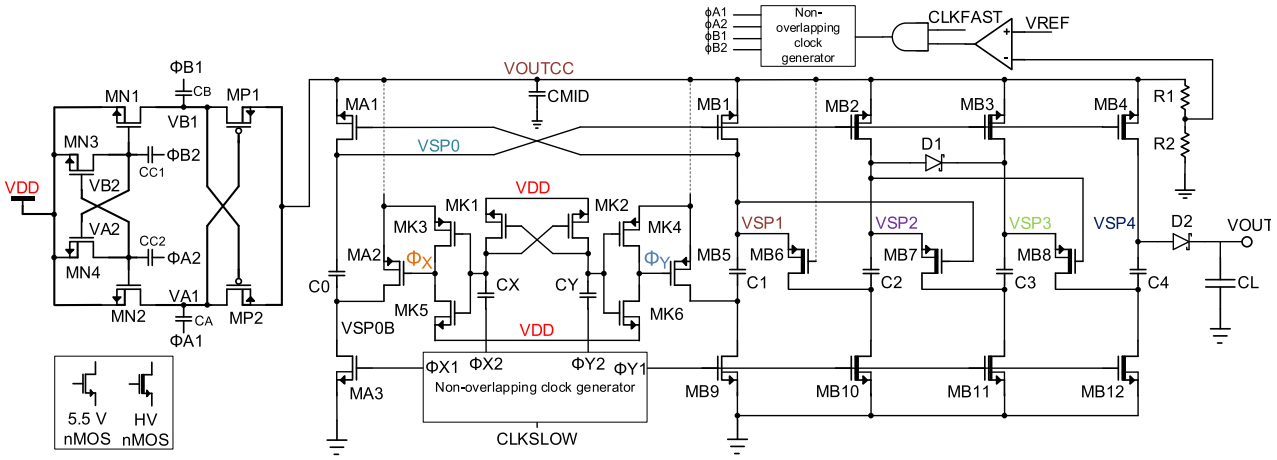

FIGURE 7. Proposed hybrid charge pump schematic.

and would be negated by the power consumption in the auxiliary circuit controlling the switch.

The overall charge pump design can be seen in Figure 7. An additional cross-coupled circuit with an inverter to boost Φ_X and Φ_Y is shown. Only four phases are shown to drive the cross-coupled stage, although clock signals Φ_{A1} and Φ_{B1} both have two additional phases, each controlling high and low side switches of the clock driver output separately to reduce energy losses caused by crowbar currents.

The main concern of the hybrid charge pump is that some of the nMOS switches in both stages of the charge pump are forward biased in the conduction phase; specifically on the start-up, when all capacitors are discharged, this leads to a VDD drop across source-body connection which can turn on the parasitic BJT and cause detrimental operational issues. Hence, measurements were done from a fabricated cross-coupled stage first. These results are included with the simulations of the serial-parallel and the overall hybrid charge pump to show that the proposed circuit operates as intended and its performance does not degrade over time.

The regulation scheme used in the design is based on pulse-skip modulation [24] and regulates the cross-coupled stage. A voltage divider using resistors R_1 and R_2 is used to extract a fraction of the voltage V_{OUTCC}. It is then compared to a reference signal of 1.25 V and the result is used as an input to gate the clock signal CLKFAST. It drives the non-overlapping signal generator, producing the signals that control the cross-coupled stage. The charge pump circuit is disabled and skips several clock pulses until the output voltage decreases due to the output load. A latched comparator was used to prevent multiple transitions of its output when close to the desired voltage V_{REF}.

E. PARASITIC EFFECTS

The main disadvantage of a serial-parallel charge pump is its sensitivity to parasitic effects. Tanzawa [20] has shown analytically that linear charge pumps, such as the Dickson and cross-coupled designs, perform better than other topologies, such as serial-parallel or exponential [25] designs, especially under higher parasitic effect conditions. It has also been shown that charge pump losses due to parasitic effects are proportional to the number of pumping stages and are limited to a maximum of four or five in serial-parallel topologies [21]. An optimization method for the serial-parallel topology by tapering flying capacitor sizes was presented in [22]; however, it could not be confirmed by circuit-level simulations in the present work. As a result, a linear charge pump is the best option for the majority of integrated voltage multipliers. However, when it comes to fully integrated applications, parasitic effects are highly dependent on the capacitor devices used. A linear pump requires the use of high-voltage MOM capacitors which have been shown to have high parasitic capacitances, reaching over 8% for a metal 2 – metal 4 implementation [10]. Even if a higher metal layer count is utilised, the capacitance per unit area of the MOM device is usually significantly lower than the MIM type [23], which is usually implemented in the uppermost layers of the chip. Furthermore, the area occupied by a MOM capacitor is unusable for routing, whereas a MIM capacitor can fit above the switches and interconnect, significantly reducing the overall chip area. This leads to the conclusion that a low-voltage serial-parallel charge pump stage can be a better alternative for low-area, fully-integrated applications.

F. NON-OVERLAPPING CLOCK GENERATOR

The non-overlapping clock generators used in present work are shown in Figure 8. Two versions of the generator - four-phase and six-phase - were used. The goal of the generator circuit was to ensure a sufficient delay between driving signals, preventing crowbar currents in the clock driver and reverse charge flow in the pump itself. Previous works have incorporated non-overlap generators based on voltage-controlled delay cells as well as an inverter chain-based delay approach [19]. However, these designs can

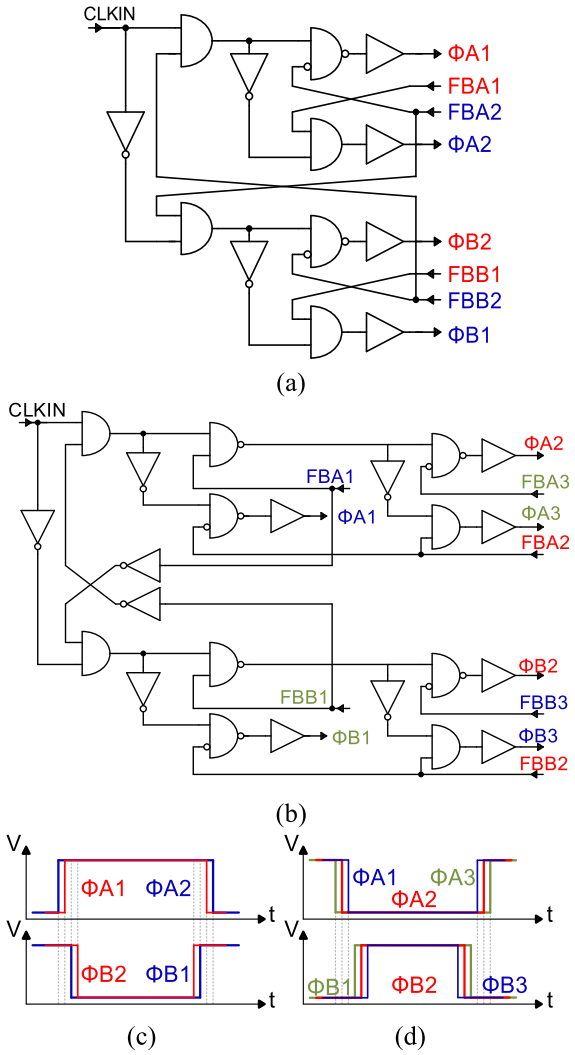

FIGURE 8. Non-overlapping signal generator circuits: four-phase (a), six-phase (b) and their timing diagrams: four-phase (c) and six-phase (d).

have high power losses and suffer from sub-optimal clock signals due to process, voltage and temperature variation if caution is not exercised in the design layout.

The present design relies on two parameters: internal delays of digital cells and a feedback mechanism. The clock is based on a conventional non-overlapping clock circuit using NAND gates with additional nested loops inside, as well as adjustments for falling-rising edge priority logic. The delay between phases relies fully on the internal delays of the logic elements and was observed to be below a nanosecond if the output (ΦA1, Φ2, etc.) and feedback (FBA1, FBB1, etc.) nodes were shorted. Testing across all PVT corners showed no stability issues in the circuit whilst dead-time periods remained small.

IV. DICKSON CHARGE PUMP

A standard Dickson charge pump [26] was engineered as a comparative design to the serial-parallel one. The charge pump was implemented using high voltage, low drop-out

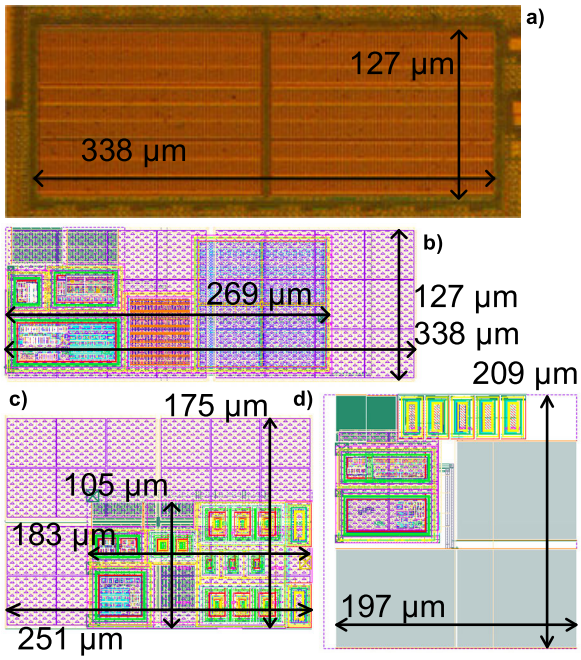

FIGURE 9. Macrograph of the cross-coupled voltage doubler (a); layout views of cross-coupled (b), serial-parallel (c) and Dickson (d) charge pumps.

voltage Schottky diodes with a diode drop of 0.4 V. The design gave a 2 V output loss and a 100 μW power loss at a 50 μA output current. Although different design techniques could solve the diode drop issue, it would be at the cost of increased area and power consumption in the auxiliary circuit. As a result, a Schottky-based design was chosen for comparison.

The Dickson charge pump was driven by the same non-overlapping clock circuitry as the serial-parallel charge pump. The design used a MIM capacitor for the first stage (operational range 6 - 12 V; placed above the switching circuitry) and high voltage MOM capacitors which occupied layers M1 – M5 for the other stages. This approach used the maximum number of metal layers available and resulted in approximate capacitance per unit area of 1.22 fF/μm^2 and a total capacitance per stage of 10 pF.

V. RESULTS

The following section covers the results obtained from post-layout simulations as well as measurement results for the cross-coupled charge pump. Figure 9 shows the image of the cross-coupled charge pump and the layout view of serial-parallel and Dickson charge pumps. The main advantage of the serial-parallel charge pump is the area preservation which comes from placing the full switching circuitry under the 5 V MIM flying capacitors. This also allows the remaining space under the capacitors to be used for regulation circuitry, on-chip base clock generation and any other circuits that are to be implemented together with the charge pump. In contrast, the same circuitry would occupy additional area around the Dickson design. Empty space is also

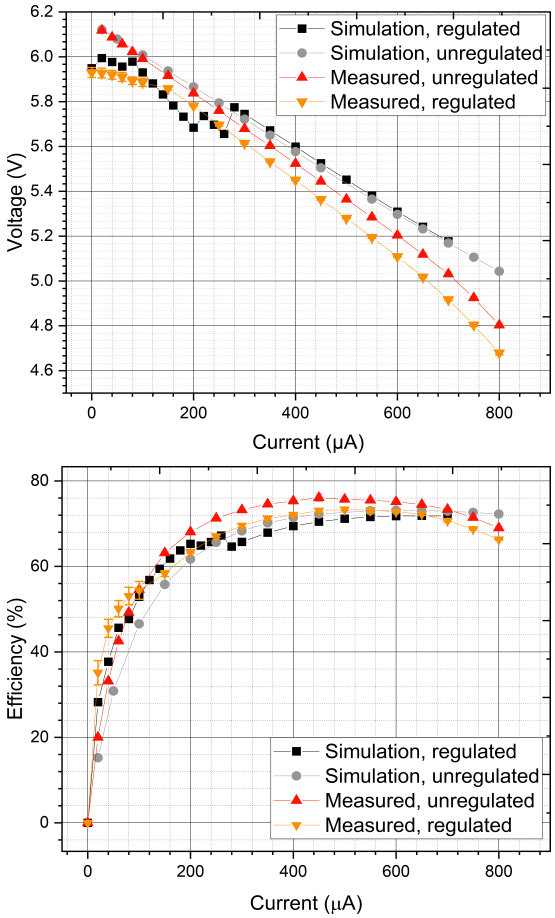

FIGURE 10. Output voltage and power efficiency of the cross-coupled stage.

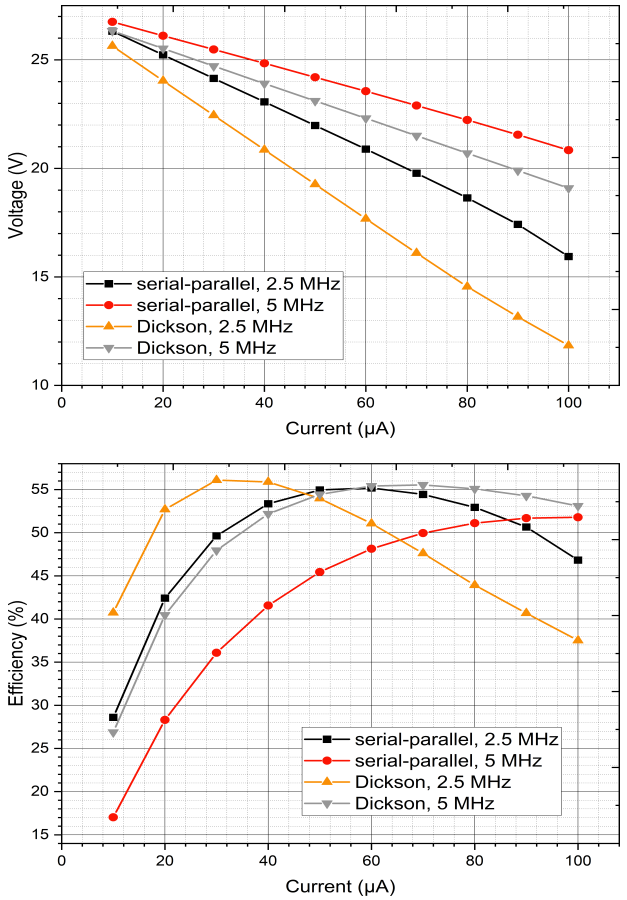

FIGURE 11. Four stage serial-parallel and Dickson charge pumps' output voltage and power efficiency curves.

available under the cross-coupled charge pump stages; a large portion is occupied by the MOS capacitor which could be removed in exchange for lower long-term reliability of the circuit.

The total area of the cross-coupled voltage doubler pump (CCVD) is 0.042 mm^2 and the total area of the serial-parallel charge pump is 0.044 mm^2. The area of the Dickson charge pump is 0.0411 mm^2 i.e. it is 6.6% smaller. However, by considering the free area available under the flying capacitors for a serial-parallel design, an equivalent of 0.025 mm^2 area saved (60 % of total Dickson charge pump design) can be achieved. Without a MOScap, the area available under the cross-coupled stage is also 0.025 mm^2. As a result, if the total empty area available under the MIM capacitors is utilised, the total effective area of the hybrid charge pump is 0.036 mm^2.

The CCVD was fabricated, and its output voltage and efficiency were measured at 15 MHz for three circuits for up to 800 μA of output current. The results are shown in Figure 10. The maximum efficiency is 76% at 450 μA output current for the unregulated version and 73.3% at 500 μA for the regulated one. The regulated version output was limited to 5.93 V and showed an improved efficiency for the output currents up to 100 μA. A higher discrepancy in the measurements at low currents between circuits was observed for the regulated version which can be attributed to the variation of the control circuit. A dip in the output voltage and efficiency can be observed between output currents of 100 μA and 300 μA. This is because, with a small output capacitor of 20 pF and an increasing output current, an increasingly larger ripple is created due to pulse-skip regulation. This reduces calculated values of the average output voltage and efficiency. When the current increases further, the regulatory circuit is disabled and the output voltage changes to an unregulated mode – the efficiency drops, but output voltage increases.

To investigate the issue of the parasitic BJT existing in the fabricated CCVD, a hundred start-up conditions were carried out at a minimum output current, and the measurements were taken before and after the procedure. The maximum average difference between the two sets of measurements was 0.19% for efficiency and 0.005 V for the output voltage. Furthermore, the difference polarity varied across data point pairs which indicated a random error rather than a degrading trend in the measurements.

Figure 11 shows the efficiency and output voltage results of the serial-parallel and Dickson charge pumps, both powered by a 6 V supply. The serial-parallel design shows

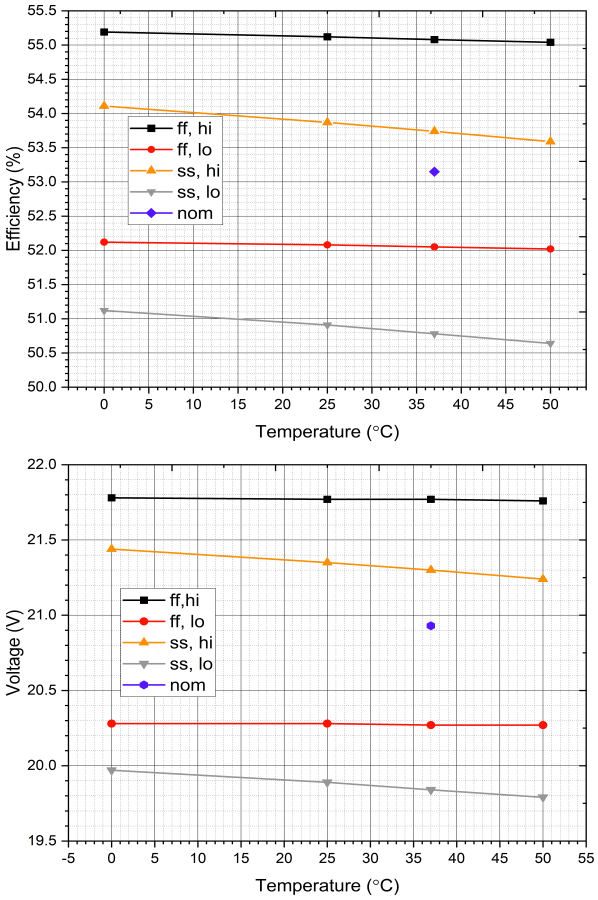

FIGURE 12. Post-layout corner simulation results.

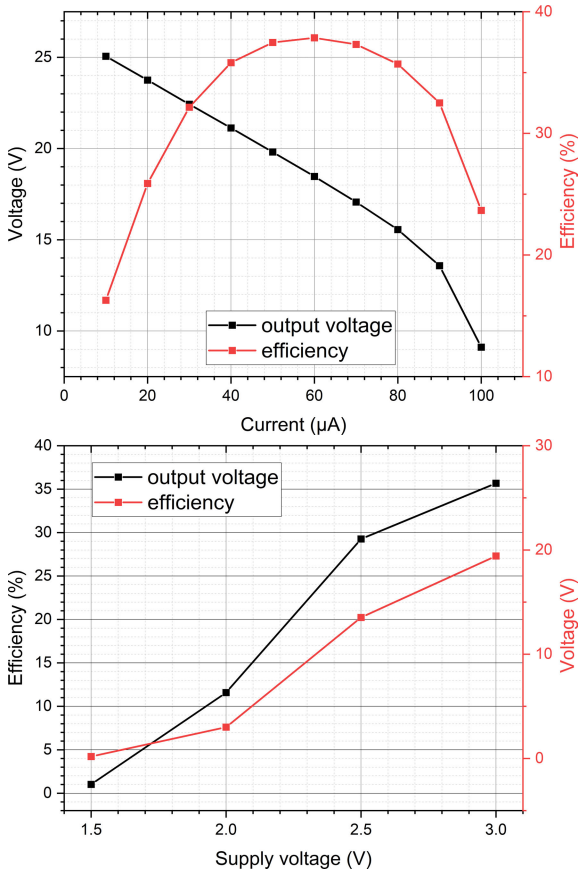

FIGURE 13. Output voltage and power efficiency of a serial-parallel charge pump (top); its output voltage dependency on the input voltage at 50 μA output current (bottom) graphs.

much better output voltage capability at the same operational frequency. The difference in the maximum efficiency of the designs was within the bounds of error, although a greater discrepancy between the two circuits was present when operating at 5 MHz. It is important to note that the efficiency characteristics of a serial-parallel charge pump at 2.5 MHz coincided well with Dickson charge pump operation at 5 MHz. At double the frequency the power consumption of the clock source increases and the non-overlapping signal generator power consumption doubles. Thus, the overall power consumption of the serial-parallel charge pump is lower than that of a Dickson design for the same output voltage at a similar output current.

The serial-parallel charge stage was further analysed across corners of interest. The analysis was carried out for the maximum efficiency point, $I_{OUT} = 60\ \mu A$. The simulation was done for fast-fast (ff) and slow-slow (ss) active device parameters in combination with lowest (lo) and highest (hi) value passive devices across the temperature range relevant for biomedical applications (0 - 50°C). The results are shown in Figure 12, where ''nom'' stands for the nominal corner result at body temperature of 37°C. The lowest efficiency was observed at the ''ss, lo'' corner, at which resistivity of the switches increases and pumping capacitance is the lowest. The difference between the nominal and this (ss, lo) corner was around 2.4% in efficiency and 1.1 V drop in output voltage at 37°C, translating to 4.5% and 5.3% relative changes respectively. The variation in passive component value affected the performance of the circuit to some degree, but the effect was constant across the temperature range of interest. A decrease in output voltage and efficiency with an increase in temperature is present across all corners and is most evident for the 'ss' corner pair. The overall performance across corners is within the acceptable limit, especially for biomedical applications where temperature is a reasonably stable parameter.

Finally, a process and mismatch Monte-Carlo simulation (random sampling) was carried out for 100 samples for the nominal corner at 37°C. The mean of the output voltage was found to be 20.2 V with a maximum standard deviation (σ) of 235 mV whilst the mean of efficiency was found to be 54% with $\sigma = 0.5\%$; the variation due to random process and mismatch is significantly lower than that of process corners and demonstrates the robustness of the design.

The simulation results of the power efficiency and output voltage of the hybrid charge pump, together with its output voltage dependency on the input voltage – all at nominal corner – can be seen in Figure 13. The maximum efficiency of 38% for the hybrid charge pump simulation is

TABLE 1. Comparison of regulated high-voltage charge pumps. Values in brackets for this work indicate the effective area calculations of the design.

Reference	**This Work**	[7]	[29]	[30]	[31]	[32]
Output voltage (V)	**26**	36 (up to 100)	19.6	28	17.7	16
Load Current (µA)	**60**	20	150	-	-	25
Technology	**0.13-µm BCD**	65-nm CMOS	0.18-µm CMOS	0.25 -µm CMOS	0.13-µm CMOS	0.35-µm CMOS
Supply voltage (V)	**3.1**	2.5	3.3	2.5	1.8	2.5
Switch Device	**PMOS/NMOS**	PMOS/NMOS/ Polysilicon Diode	PMOS/NMOS	Polysilicon Diodes	PMOS/NMOS	PMOS/NMOS
Number of Stages	**1+4 (CC+SP)**	12	11	12	12	6
Stage Capacitor (pF)	**30 / 15**	8	1.2	10	1.4	1.5
Frequency (MHz)	**20 / 2.5**	4	50	1	100	30
Efficiency @ I_{LOAD} (%)	**42%**	49%	34%	-	-	34
Area (mm^2)	**0.086 (0.036)**	0.18	0.063	-	0.175	0.069
VCE (%) *	**86.8**	81.8	53.9	86.4	81.9	91.4
Output power density (mW/mm2) **	**12.9 (30.8)**	2.8	38	-	-	3.9

*** Where VCE (voltage conversion efficiency) = V_{OUT}(real)/V_{OUT}(ideal) = V_{OUT}(real)/((n+1)*V_{DD}), where V_{OUT} is the output voltage of the charge pump, V_{DD} is supply voltage and N is the number of charge pump stages** [26]
**** Based on output current and voltage values at the peak efficiency.**

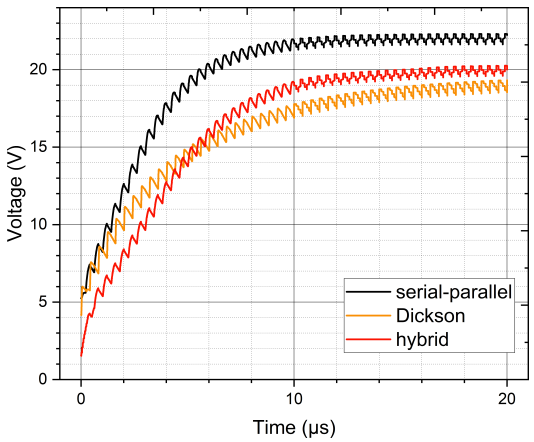

FIGURE 14. Transient start-up response.

lower than the 43% product of the standalone cross-coupled (78%) and serial-parallel (55%) designs. This is attributed to the fact that the input of the serial-parallel stages is not a perfect voltage source: supply voltage drops under higher output current conditions, which leads to the drop in the overall efficiency when the two designs are used in series.

The transient responses of serial-parallel, Dickson and hybrid charge pumps operating at 2.5 MHz and at a constant output current of 50 μA are shown in Figure 14. From an ideal 6 V supply, the serial-parallel charge pump can reach 90% of the steady state level in 5.625 μs whilst the hybrid and stand-alone Dickson designs require 8.3 μs and 8.375 μs respectively. Consequently, the serial-parallel charge pump is 33% faster than the other two designs. However, it is important to note that various strategies exist to reduce charge time of Dickson charge pumps with capacitive loads [27], [28].

A performance comparison of high-voltage generation designs is shown in Table 1. The maximum output voltage varies significantly for the different designs, mainly due to technology limitations or application requirements. In comparison to other designs, the charge pump presented here has the most well-rounded design, excels in multiple aspects, and provides very high efficiency in a small chip area.

VI. DISCUSSION

Depending on different system constraints, the charge pump design proposed here can be adjusted to improve its performance. The regulating circuit between the cross-coupled and serial-parallel stages can be removed if the two branches of the cross-coupled pump are sized differently and the whole pump is driven by the same frequency clock. This would improve the overall efficiency and power consumption but would increase the size of the flying capacitors in the first stage and, thus, the total chip area.

Furthermore, the design at present is intended to operate at a small, but continuous current. A body diode in the cross-coupled pump exists together with a high-voltage nLDMOS and a Schottky diode in the serial-parallel stages. A current path from the input to the output is created if the output voltage drops below the supply voltage. As a result, in alternative applications, where disabling the charge pump for extended duration is needed, an additional wide pMOS at the input of the cross-coupled stage can be included.

In applications with external capacitors used to decrease the operational frequency and the total power consumption of the charge pump, the hybrid implementation is even more beneficial. Due to its low maximum flying capacitor voltage requirements, larger external capacitors can be used for the same packaging size. Parasitic effects are also minimised,

improving parasitic losses in the serial-parallel stages and overall efficiency further.

Finally, the Schottky diodes used in the serial-parallel charge pump can be replaced by circuit alternatives: the first diode between the stages can be a diode-connected device with an appropriately biased deep n-well. The second diode can be replaced by an actively switched circuit, provided auxiliary circuit power consumption is not an issue.

VII. CONCLUSION

A hybrid charge pump design for high-voltage and small chip area constraints has been presented. It comprises a zero-reversion loss cross-coupled charge pump and a new, self-biased serial-parallel charge pump design used in tandem. The design achieves high area savings of 60% for the serial-parallel stages with very little efficiency loss in comparison to a standard Dickson charge pump, as well as 33% faster transient performance. Possible adjustments may improve and taper the proposed design for applications where high levels of integration and fast as well as efficient high voltage generation is required.

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