IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received May 22, 2021, accepted June 6, 2021, date of publication June 23, 2021, date of current version June 30, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3090472

Methodology for the Simulation of the Variability of MOSFETs With Polycrystalline High-k Dielectrics Using CAFM Input Data

A. RUIZ[1], C. COUSO[1], N. SEOANE[2], M. PORTI[1], (Member, IEEE), A. J. GARCÍA-LOUREIRO[2,3], (Member, IEEE), AND M. NAFRIA[1], (Senior Member, IEEE)

[1]Electronic Engineering Department, Universitat Autònoma de Barcelona, 08193 Barcelona, Spain
[2]CITIUS, Universidade de Santiago de Compostela, 15782 Santiago de Compostela, Spain
[3]Department of Electronics and Computer Science, Universidade de Santiago de Compostela, 15782 Santiago de Compostela, Spain

Corresponding author: A. Ruiz (ana.ruiz@uab.cat)

This work was supported in part by the AEI/FEDER and UE under Project TEC2016-75151-C3-R, Project PID2019-103869RB/AEI/, Project 10.13039/501100011033, Project PID2019-104834GB-I00, and Project GRC ED431C 2018/19; and in part by the Xunta de Galicia and FEDER under Project ED431F 2020/08. The work of N. Seoane was supported by the Spanish Ministry of Science, Innovation and Universities under Grant RYC-2017-23312.

ABSTRACT In this work, a simulation methodology, whose inputs are Conductive Atomic Force Microscope (CAFM) experimental data, is proposed to evaluate the impact of nanoscale variability sources related to the polycrystallization of high-k dielectrics (i.e., oxide thickness, t_{ox}, and charge density, ρ_{ox}, fluctuations in the nanometer range) on the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) variability. To simulate this variability, a Thickness And Charge MAp Generator (TACMAG) has been developed and used in combination with an in-house-built 3D device simulator (VENDES). From CAFM experimental data (topography and current) obtained on a small area of a given polycrystalline dielectric, the TACMAG generates a high amount of t_{ox} and ρ_{ox} configurations of the gate dielectric, with identical statistical characteristics to those experimentally measured. These dielectrics are then introduced into the device simulator, with which the impact of the t_{ox} and ρ_{ox} fluctuations in the dielectric on the variability of MOSFETs (i.e., threshold voltage) is analyzed. Finally, the impact of different nanoscale parameters, such as the Grain size and Grain Boundaries depth (of polycrystalline dielectrics) on such variability has been evaluated.

INDEX TERMS CAFM, high-k, MOSFET variability, polycrystalline dielectric, defect density, 3D device simulations.

I. INTRODUCTION

The continuous scaling of Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) devices has driven the exploration of new materials [1]. For instance, to limit the gate leakage current, ultra-thin Silicon Dioxide (SiO_2) gate oxide has been replaced by high-k dielectrics [2]. However, some high-k materials show a polycrystalline structure [3], [4], which could affect the electrical properties of scaled devices [5] by increasing the leakage current and the device-to-device variability. Since high-k polycrystallization takes place at the nanometer scale [4], Conductive Atomic Force Microscopy (C-AFM) has been demonstrated to be a very powerful technique to evaluate at the suitable scale the morphological and electrical properties [6]–[10] of polycrystalline high-k dielectrics [11]–[15]. As an example, it has been found that in some polycrystalline Hafnium Dioxide (HfO_2) layers, the gate leakage current mainly flows through grain boundaries (GBs) [16], where a reduced oxide thickness (t_{ox}) was measured [3]. Moreover, the presence of defects has been observed at the GBs, which were associated to an excess of oxygen vacancies [3], [16].

Traditionally, due to the lack of experimental data, variability studies are done via the implementation of physical models that mimic the real behavior of the sources of fluctuations [5], [17], [18]. However, more recently a new methodology was proposed in [11]. It consisted in the simulation (using Technology Computer-Aided Design,

The associate editor coordinating the review of this manuscript and approving it for publication was Kalyan Koley.

This work is licensed under a Creative Commons Attribution-NonCommercial-NoDerivatives 4.0 License.
For more information, see https://creativecommons.org/licenses/by-nc-nd/4.0/

TCAD [19]) of the I-V curves of MOSFETs whose gate oxide properties were directly determined from experimental data. In this way, it was possible to better link variability sources at the nanoscale with the variability of figures of merit of MOSFETs. In particular, a CAFM was used to measure topographical and current maps of polycrystalline high-k dielectrics (from which nanoscale t_{ox} and charge density, ρ_{ox} maps were obtained [11]) and a simulator was used to evaluate their impact on the MOSFET threshold voltage (V_{th}). However, in that work, a statistical analysis was not possible. Only small regions of a particular sample were measured, so that the number of MOSFETs instances available for the analysis of the variability of V_{th} and ON and OFF currents (I_{on} and I_{off}) was rather limited. In addition, the complete evaluation of the impact of the different parameters that describe the polycrystallization of high-k dielectrics (as the grain size, Grain Boundaries depth and/or width, etc) was not allowed. On one hand, because samples obtained with other growth parameters (which result in different polycrystallinity properties) are not always available. On the other, because it would be necessary a lot of experimental measurements, which is very expensive and time consuming.

The focus of this work is to propose a complete simulation flow to statistically evaluate the impact of polycrystalline high-k dielectrics on the MOSFET variability, starting from experimental nanoscale data obtained with a C-AFM. With the proposed methodology, less experimental measurements and samples with different characteristics are needed, reducing the cost and time of such analysis. At this point, only the high-k polycristallinity is considered as variability source, but it could be afterwards combined with others to investigate their global effect on the device [20].

II. EXPERIMENTAL

A. SET UP AND DEVICE STRUCTURE

Nanoscale data, that is, t_{ox} and ρ_{ox} and their fluctuations in the nanometer range, were obtained with CAFM on a sample containing a 5.3 nm thick HfO_2 film deposited by Atomic Layer Deposition (ALD) on a 0.7 nm thick SiO_2 layer. The average thickness of both layers was measured by X-Ray Reflectivity. The gate stack was grown on a Si epitaxial P-substrate. With the aim of studying the impact of the polycrystalline dielectric structure on the MOSFET device variability, an annealing process was carried out at 1000 °C, which lead to the polycrystallization of the high-k layer. The presence of the SiO_2 layer was taken into account during the TCAD simulations, as reported in [11]. However, SiO_2 charges and t_{ox} fluctuations in SiO_2 were considered to be negligible when compared to those linked to the polycrystalline high-k dielectric. This is justified by the fact that SiO_2 is not polycrystalline and because the amount of charges is expected to be larger in HfO_2 than in SiO_2. So, the measured t_{ox} and ρ_{ox} fluctuations are assumed to be related to the polycrystalline high-k.

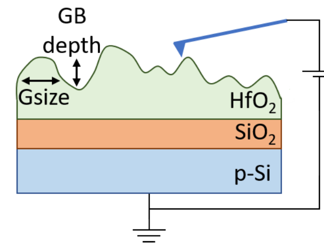

FIGURE 1. Schematic of the set up and device structure.

Figure 1 shows a schematic of the CAFM experimental set up. Note that no top electrode is used. Actually, the tip of the CAFM plays the role of the top electrode, defining a Metal-Oxide-Semiconductor structure whose size is determined by the tip-sample contact area, which is ~100nm^2 [21]. With this experimental configuration, morphological and current maps of different kinds of materials (as high-k dielectrics [12], [13], [22], [23]) can be measured with a nanometer resolution. Current maps correspond to the x-y spatial distribution of the tunneling currents flowing between the gate and the substrate, through the dielectric layer.

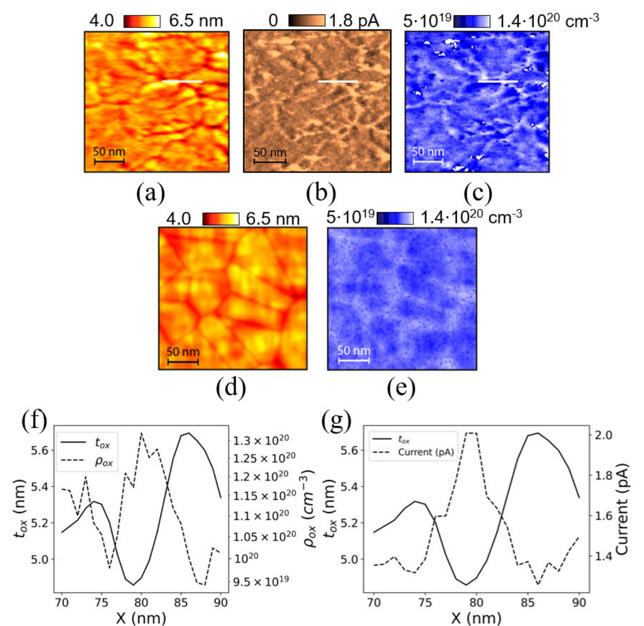

FIGURE 2. Morphological (a) and current (b) maps obtained at $V_G = 6.5V$ on a HfO_2/SiO_2/p-Si structure (230 nm x 230 nm). (c) corresponds to the charge density map estimated from (a) and (b). The white line highlights a GB (depression in the morphological image), which shows higher current and charge density than that observed in the Grains (see profiles along the white line in (f) and (g)). Generated morphological (d) and charge density (e) maps obtained with TACMAG.

B. CAFM EXPERIMENTAL DATA

Figures 2a and 2b show, respectively, an experimental morphological and current map obtained with a CAFM in vacuum and using a diamond-coated tip. The current map was obtained at 6.5V, because it was the minimum voltage at which current above the noise level of the setup was

measured. From both maps, the corresponding charge density map (Fig. 2c) has been estimated using the methodology shown in [11]. It can be observed that there is a clear correlation between the three images. Higher currents and charge densities are measured at GBs (deeper areas in the morphological map). These larger values are assumed to be related to oxygen vacancies by incomplete atomic bonds between hafnium and oxygen [24], [25]. As examples, profiles of the morphological, current and ρ_{ox} maps through a particular GB (highlighted in the images) are shown in Fig. 2f-g. Note that direct information about the oxide thickness t_{ox} cannot be obtained from the morphological image. This is because t_{ox} depends not only on the characteristics of the scanned top (dielectric/gate) interface (Fig. 2a), but also on that of the dielectric/substrate interface, and this information is not available in this kind of experiment. However, Fig. 2a suggests that t_{ox} is smaller at the grain boundaries [26], [27]. Actually, t_{ox} at each pixel of the surface of Fig. 2a was estimated [11] by assuming that the average thickness of the oxide layer, 5.3nm, corresponds to the average height of the morphological map. Any height deviation with respect to the morphological average at any site of Fig. 2a has been attributed to a deviation from the average t_{ox} of the same value. Then, any morphological map can be interpreted also as a t_{ox} map, as it will be done from now on.

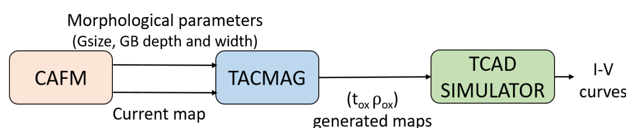

FIGURE 3. Flow diagram showing the different steps of the simulation methodology.

III. SIMULATION TOOLS

The proposed simulation methodology is based on two independent simulators, which are executed sequentially. Fig 3 shows the complete flow of data, covering from the experimental information obtained with CAFM to the analysis of the variability of MOSFETs. First, the TACMAG software (Thickness And Charge MAp Generator) is used, with which multiple (t_{ox}, ρ_{ox}) maps of gate oxides are generated (output) from the experimental morphological and current maps measured with CAFM (input). Secondly, a homemade Semiconductor Device Simulator is used, which takes the output (t_{ox}, ρ_{ox}) maps of TACMAG as input data and simulates the MOSFET electrical characteristics. As a result, the impact of the nanoscale fluctuations of t_{ox} and ρ_{ox} in the dielectric on the device I-V characteristics and the device-to device variability in MOSFETs can be evaluated. Both simulators are described in detail in the following sections.

A. THICKNESS AND CHARGE MAP GENERATOR (TACMAG)

The core of the Thickness And Charge MAp Generator (TACMAG) was partially developed in [28]. In the generator developed in [28], from the AFM measurement of morphological maps of a polycrystalline sample, 3 Dimension (3D) topographical maps could be reproduced with the same statistical morphological characteristics as the experimental sample under study [28]. Moreover, in [11], from pairs of experimental morphological and current maps obtained with CAFM (on the same area), the local charge density was also calculated at each position of the gate oxide. The present work, however, goes one step further, and improves and develops new capabilities of that simulator, called from now on TACMAG, which are necessary to evaluate the impact of the nanoscale properties on the device variability.

On one hand, in order to optimize the generation of morphological maps, in the new version of the generator, that is, in TACMAG, the methodology used to statistically reproduce the sample morphology has been improved by using the Poisson-Voronoi diagrams, which are commonly used to generate polycrystalline grain structures [29]–[31]. Implementing this new technique, the inputs needed to create the grain structure of new samples are reduced, simplifying the map generation. Now, only the grain size (Gsize), GB width and depth (and their corresponding statistics) are necessary, which are easily obtained from experimental data (Fig. 2a). Fig. 2d shows an example of a generated morphological map whose statistical parameters are the same as those that describe Fig. 2a.

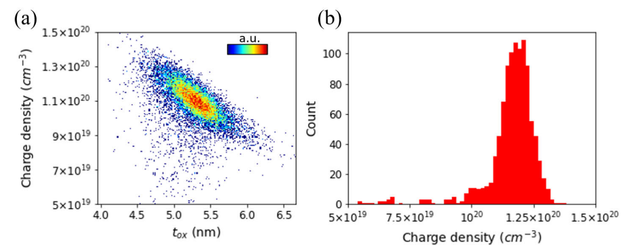

FIGURE 4. (a) ρ_{ox} values calculated from Fig. 2a and 2b, and shown in Fig. 2c, as a function of t_{ox} (Fig. 2a) for all the pixels of Fig. 2a and 2c. The histogram on (b) shows the $\rho_{ox}(t_{ox})$ distribution for a t_{ox} = 5nm (interval between 4.95 and 5.05 nm).

On the other hand, the new version of the generator (TACMAG) has also been extended to generate 2D charge density maps (i.e., the inputs of the Device simulator). To do that, first of all, from morphological and current maps experimentally obtained with CAFM (Fig. 2a and b), we use the methodology shown in [11] to calculate the corresponding ρ_{ox} map (Fig. 2c). Fig. 4a shows the calculated ρ_{ox} values (Fig. 2c) as a function of t_{ox} (Fig. 2a) for all the pixels of Fig. 2a and 2c. Note that there seems to be a correlation between t_{ox} and its corresponding charge density (statistically, higher densities were found at GBs, which have smaller thicknesses). However, this relation is not univocal: for a given t_{ox}, a distribution of ρ_{ox} has been found. Fig. 4b also shows an example of a statistical distribution of charge for t_{ox} = 5 nm (interval between 4.95 and 5.05 nm). The $\rho_{ox}(t_{ox})$ statistical distributions have been determined and have been used as an input of the TACMAG to generate (t_{ox}, ρ_{ox}) maps of the dielectric. That is, for a given pixel of a generated morphological map (characterized by a given t_{ox}),

the ρ_{ox} value has been determined by applying Montecarlo methods, considering the ρ_{ox} distribution found for that value of t_{ox}. As an example, Fig. 2e shows the generated ρ_{ox} map obtained for the morphological map in Fig. 2d.

So, to sum up this section, from the input morphological parameters (Grain size, GB width and depth and their corresponding statistics obtained from morphological maps) and current maps obtained with CAFM, TACMAG calculates the charge density distributions (ρ_{ox}, which depends on t_{ox}), and provides (t_{ox}, ρ_{ox}) maps at the output (Fig. 3).

B. 3D DEVICE SIMULATOR

To evaluate the impact of the nanoscale t_{ox} and ρ_{ox} fluctuations in polycrystalline dielectrics on the device variability of MOSFETs, a 3D in-house built parallel drift-diffusion (DD) Device Simulator (named VENDES) [19] was used, which allows to obtain the I_G-V_D characteristics of MOSFETs. The finite-element method (FEM) has been applied to discretize the simulation domain, which allows the simulation of complex device shapes with great flexibility. In addition, the use of FEM-based meshes allows to easily incorporate and model non-uniform effects (such as variability sources) affecting the device, that might require the deformation of the structure. On every node of the three-dimensional tetrahedral mesh, the classical electrostatic potential is obtained via the solution of the Poisson equation. In order to incorporate quantum mechanical corrections, this classical potential is corrected through the density-gradient (DG) approach. To model the transport inside the semiconductor, the quantum-corrected electrostatic potential is coupled with the current continuity equation for electrons, to obtain the electron current density that flows inside the device. To account for the carrier transport in the MOSFET device, VENDES incorporates the Caughey-Thomas doping dependent electron mobility model [32], to describe low electric field transport, coupled with perpendicular and lateral electric field models [33], that represent high field carrier transport. A more detailed description of the simulation methodology can be found in [19]. This 3D DD-DG simulator has been widely employed in the modelling of different sources of variability affecting semiconductor devices, such as random dopants [34], line-edge roughness [35], [36], or grains in the metal gate [34], [35], [37], [38].

In this work, this simulator has been used to evaluate the impact of high-k dielectric polycrystallization on the V_{th} variability of MOSFETs. With this purpose, a Width (W) x Length (L) = 50 × 50 nm^2 gate area n-type Si MOSFET with a HfO_2/SiO_2 gate stack was considered as a test device. The device dimensions and doping values were obtained from the constant field scaling [39] of a n-type 67 nm effective gate length MOSFET that was calibrated against experimental data [37]. To simulate the Drain current vs. Gate Voltage (I_D-V_G) curves of different devices, nanoscale (t_{ox}, ρ_{ox}) dielectric maps with a 50 × 50 nm^2 size (the area of the gate region), extracted from Fig. 2, were considered as inputs of the Device Simulator. The introduced maps can be either directly measured (i.e, 50 × 50 nm^2 portions of Fig. 2a and 2c) or generated (in Fig. 2d-e).

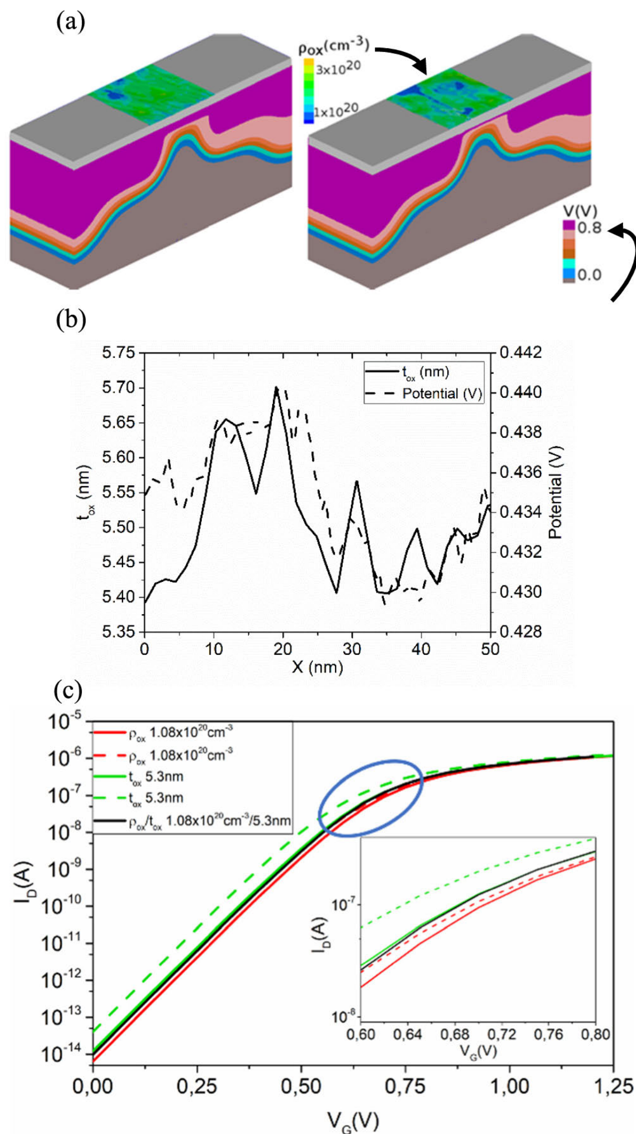

FIGURE 5. (a) Electrostatic potential inside the 50 × 50 nm^2 MOSFET device for the two particular configurations that produce the largest (left) and lowest (right) drain currents (at $V_G = 0.6$ V and $V_D = 0.05$ V) when considering both ρ_{ox} and t_{ox} fluctuations in the device gate. (b) Example of electrostatic potential in the channel (dashed line) and t_{ox} profile (continuous line), (c) I_D-V_G characteristics simulated at $V_D = 50$ mV for the two configurations shown in (a) when different variability sources are analyzed. Red curves correspond to the simulated I_D-V_G curves of devices with dielectrics with constant $\rho_{ox} = 1.08 \times 10^{20}$ cm^{-3} and with the t_{ox} fluctuations taken from (a). Green curves correspond to the simulated I_D-V_G curves of devices with dielectrics with constant $t_{ox} = 5.3$ nm and with the ρ_{ox} fluctuations taken from (a). Black curve corresponds to a device with constant ρ_{ox} and t_{ox} (same values as for the two other considered cases). The inset corresponds to a zoom of the I-V curves inside the circle, showing V_G in the 0.6V to 0.8V range.

As simulation example, Fig. 5a shows a 3D view of the electrostatic potential (cross section) and charge density (top view) for the two device configurations that produce the largest (left figure) and lowest (right figure) drain currents

(at $V_G = 0.6$ V and $V_D = 0.05$ V) when considering both ρ_{ox} and t_{ox} fluctuations in the device gate. The t_{ox} maps of both configurations are not shown, for simplicity. Fig 5b shows, as example, a 1D thickness profile of the high-k dielectric (continuous line). It has been extracted in the center of the channel perpendicular to the transport direction. The corresponding electrostatic potential inside the channel is also plotted (dashed line). Note that the potential is not constant, but depends on the thickness fluctuations. In this case, in those regions with smaller thickness (associated to GBs), a lower potential is found. Since the presence of GBs is related to the polycrystallization of the materials, the results demonstrate that polycrystalization clearly affects the potential distribution in the channel. Fig. 5c shows the I_D-V_G curves at $V_D = 50$ mV for the MOSFET configurations of Fig. 5a with different gate oxides characteristics. The inset corresponds to a zoom of the same plot, to better display the differences among the different I_D-V_G. curves. First, the impact of t_{ox} and ρ_{ox} fluctuations have been separately evaluated, as unique nanoscale variability source. Red I_D-V_G curves in Fig. 5c correspond to two particular devices, characterized by gate dielectrics with constant $\rho_{ox} = 1.08 \times 10^{20}$ cm^{-3} (average charge density estimated from Fig. 2c). The t_{ox} fluctuations were introduced by considering the 50×50 nm^2 regions of Fig. 5a. Green I_D-V_G curves in Fig. 5c correspond to two particular examples of devices with constant $t_{ox} = 5.3$ nm (average thickness) and two 50×50 nm^2 ρ_{ox} maps corresponding to the configurations of Fig. 5a. Finally, both sources are considered simultaneously, i.e., fluctuations in both, ρ_{ox} and t_{ox} parameters. The morphology of the dielectric corresponds to that of Fig. 5a, with charge distributions following the same spatial pattern (for clarity, the resulting curves are not shown in Fig. 5). As reference, the I_D-V_G curve of the device with constant $\rho_{ox} = 1.08 \times 10^{20}$ cm^{-3} and $t_{ox} = 5.3$ nm has also been plotted in Fig. 5c (black curve).

The two I_D-V_G curves of each set of simulated devices show different conduction levels (see Fig. 5c and the inset), which correspond to different V_{th} values. To extract V_{th}, a constant current criterion was used. V_{th} was chosen as the gate bias for which a drain current of 1.4 A/m was obtained. With this criterion, V_{th} is 0.664 V/ 0.675 V when ρ_{ox} is constant (red curves), 0.606 V / 0.654 V when t_{ox} is constant (green curves) and 0.628 V / 0.678 V when t_{ox} and ρ_{ox} fluctuations are considered, respectively. The V_{th} of the device with constant t_{ox} and ρ_{ox} is 0.656 V (black curve). These results indicate, first, that ρ_{ox} and t_{ox} fluctuations lead to different MOSFET electrical properties, and, second, that their impact changes when considered individually or combined. Therefore, the proposed simulation methodology can detect and evaluate the differences in their impact. It is important to emphasize that Fig 5c shows two particular cases, therefore they do not correspond to a statistical analysis, which will be shown in next sections. But before using our simulation tools to evaluate in more detail the impact of the high-k polycrystallization on MOSFETs V_{th} variability, the TACMAG results representativeness will be first verified.

C. TACMAG VERIFICATION

To verify that TACMAG is able to generate statistically representative (t_{ox}, ρ_{ox}) maps of the sample under study, the V_{th} variability of MOSFETs whose dielectric is described by generated (t_{ox}, ρ_{ox}) maps has been compared to that obtained when experimental data are used. In particular, from images as those shown in Fig. 2, 100 different 50×50 nm^2 (t_{ox}, ρ_{ox}) experimental (obtained from images like those shown in Fig. 2a-c) and 100 generated maps (obtained with TACMAG, as in Fig. 2d-e) were introduced into the Device Simulator to set the gate oxide properties of the MOSFETs, so that an ensemble of 100 different devices were analyzed for each case [26].

In order to verify the goodness of the TACMAG results for each of the considered variability sources (t_{ox} and ρ_{ox}), 3 different cases have been evaluated. First, t_{ox} is the only source of variability (being ρ_{ox} constant and equal to the average charge density found from Fig. 2c, that is 1.08×10^{20} cm^{-3}), second, ρ_{ox} is the only source of variability (being t_{ox} constant and equal to 5.3 nm, i.e. the measured average thickness of the sample) and, third, both variability sources are combined. For all the devices, the I_D-V_G characteristics were simulated and V_{th} was estimated. A statistical analysis of V_{th} (mean and standard deviation, σV_{th}) for the three cases has been done and the results are shown in Table 1. Note that, for the three cases, the statistics of the devices with experimentally obtained and simulated dielectric are very similar. In particular, for a 100 devices sample size, the difference between σV_{th} (indicative of the V_{th} variability) of both kinds of devices is <2 mV (representing, for example, an error of $\sim$7.7% for the case when both variability sources are considered). For the average V_{th}, for the same case, a difference of 17 mV is found, which corresponds to an error of 2.6%. These results indicate that the maps obtained by TACMAG (both, t_{ox} and ρ_{ox}) are representative of the sample under analysis. Therefore, the results demonstrate that the proposed simulation methodology and, in particular TACMAG, can be used for an accurate analysis of MOSFET variability.

TABLE 1. Average and standard deviation of V_{th} obtained from 100 devices with the device simulator, when the gate oxide characteristics have been set from experimental data (first row) and maps generated with TACMAG (second row). The different columns show the impact of the different nanoscale variability sources (t_{ox} and/or ρ_{ox}).

	V_{th} (V)		
	Only t_{ox}	Only ρ_{ox}	t_{ox} and ρ_{ox}
Experimental	0.681±0.004	0.640±0.028	0.650±0.012
Generated	0.680±0.005	0.654±0.030	0.667±0.013

IV. CASE OF STUDY: IMPACT OF THE HfO_2 POLYCRYSTALLIZATION ON THE VTH VARIABILITY

In this section, the methodology described in Section III has been used to evaluate in more detail the impact of the polycrystallization of the HfO_2 layer on the V_{th} variability of MOSFETs, as an example. Two cases of study will be considered. In both cases, since the aim is simply to show the capabilities of the proposed methodology, only 100 devices have been simulated, to reduce the simulation time. With this sample size, the relative standard error is around 5% (see section III.C). To reduce this error and obtain more accurate values of V_{th} and σV_{th} for a given gate dielectric, the proposed methodology could be extended to a larger number of devices by simply generating enough t_{ox} and ρ_{ox} maps with TACMAG.

A. CORRELATION BETWEEN t_{ox} AND ρ_{ox} ON THE IMPACT ON V_{th} VARIABILITY

We have started by analyzing the impact of t_{ox} and ρ_{ox} fluctuations on V_{th}. Remember that in Fig. 4, a correlation between t_{ox} and ρ_{ox} (at the nanoscale) was observed. Therefore, one could wonder if, when analyzing their impact on V_{th} (at device level), the impact of both variability sources is (or not) somehow correlated too. Taking advantage of the versatility and capabilities of our simulation tools, the impact of both variability sources has been studied individually and when they are combined. In particular, we have considered for this analysis the data in Table 1, second row, where V_{th} and σV_{th} were determined from the t_{ox} and ρ_{ox} maps generated with TACMAG. Note that, regarding the average value of V_{th}, t_{ox} fluctuations have a higher impact (V_{th} increases from 0.657 V for the reference case to 0.680 V) than ρ_{ox} variations (in this case it remains almost equal, changing only from 0.657 V to 0.654 V). Regarding the standard deviation, when both variability sources are analyzed independently, σV_{th} due to ρ_{ox} (30 mV) is 6 times larger than that due to t_{ox} only (5 mV). So, for the case of the sample analyzed in this work, charge density fluctuations introduce larger V_{th} variability than those related to the gate oxide morphology. However, note also that when both variability sources are combined, the V_{th} deviation is in between those obtained when the two variability sources are considered separately. In particular, the global V_{th} deviation does not correspond to the expected addition of independent variability sources, but it is reduced when compared with the impact of ρ_{ox}. These data suggest that, on one hand, ρ_{ox} and t_{ox} impacts on V_{th} are not independent (as suggested in Fig 4) and, on the other, t_{ox} and ρ_{ox} fluctuations are somehow compensated.

We have investigated the correlation between ρ_{ox} and t_{ox} and its impact on V_{th} in more detail. Figure 6 shows the probability plot (color scale), obtained from the data shown in Table 1 (second row, generated maps, first and second columns) of finding devices with V_{th}'s related to t_{ox} variation only (X-axis) and V_{th}'s related to ρ_{ox} variation only (Y-axis). Note that, for a given value of V_{th} in the X axis (i.e., only t_{ox} fluctuations), a distribution of different V_{th} values in the Y axis (i.e., only ρ_{ox} variations) is observed. The inclination of the obtained probability plot suggests that both variability sources are not independent when analyzing their impact on the V_{th} of devices. To quantify this correlation, the data shown in Fig. 6 has been fitted to a bivariate equation (equation 1), being σ_x and σ_y the standard deviation found for the case when only t_{ox} or ρ_{ox} fluctuations were taken into account (that is, 0.005 and 0.030 V, respectively), μ_x and μ_y the average V_{th} (0.680 and 0.654 V, respectively) and ρ the correlation coefficient. Leaving ρ as free parameter, R-square = 0.85, demonstrating that our data can be really fitted to a bivariate

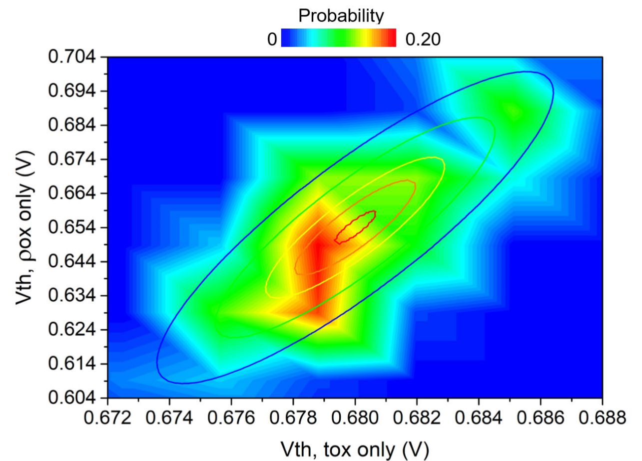

FIGURE 6. Probability (color scale) of finding devices as a function of the V_{th} linked to t_{ox} fluctuations only (X-axis) and V_{th} linked to ρ_{ox} variations only (Y-axis).

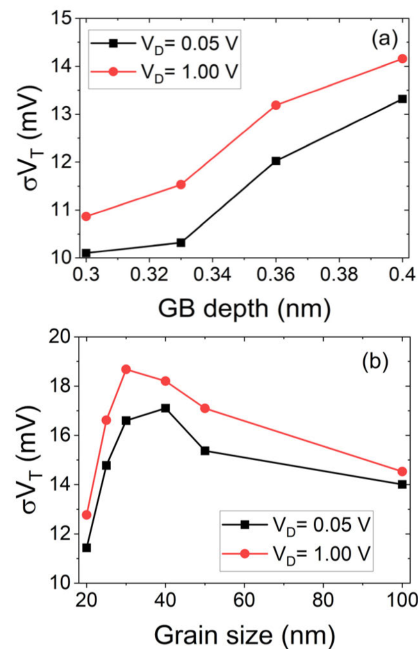

FIGURE 7. Particular examples of how morphological parameters involved in polycrystalline high-k dielectrics affect the V_{th} variability of MOSFETs at 0.05 and 1.0 V drain biases. (a) and (b) show, respectively, the V_{th} deviation for different values of the GB depth (a) and grain size (b).

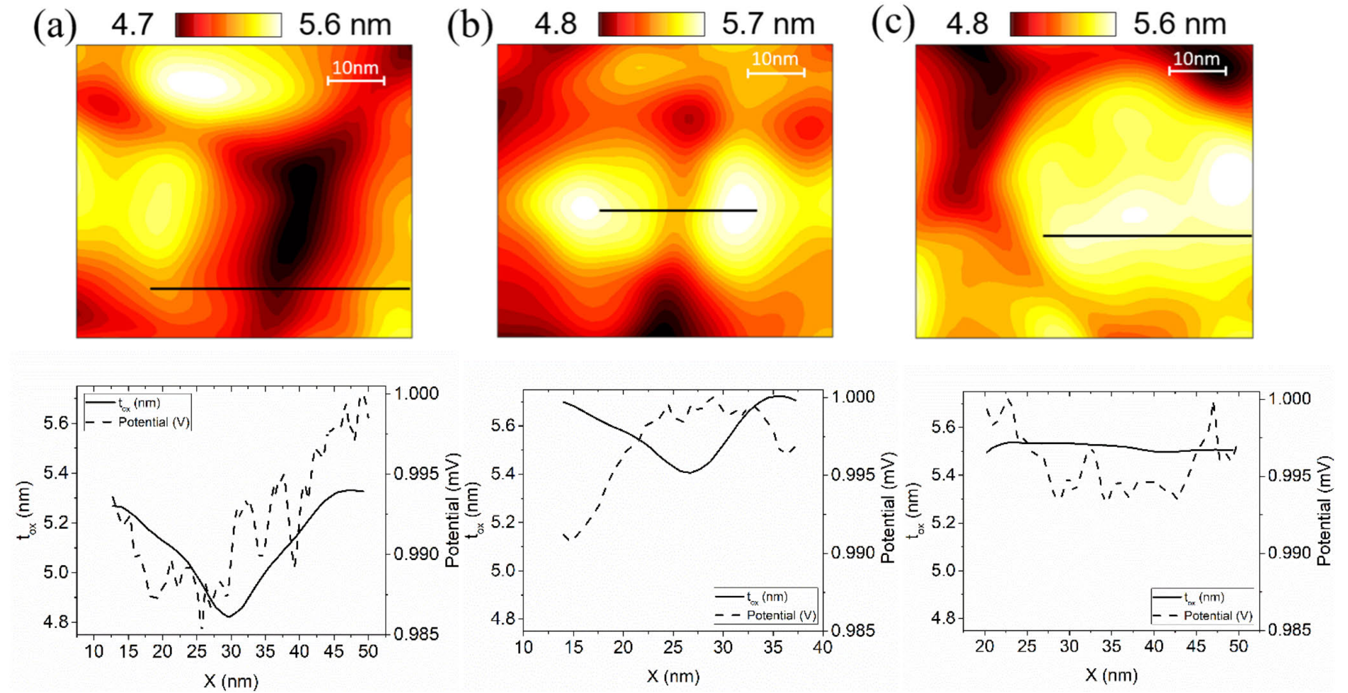

FIGURE 8. t_{ox} **maps of different gate oxide configurations including (a) a deep GB, (b) a shallow GB between two Grains and (c) a big grain. In all cases, the electrostatic potential (dashed line) and** t_{ox} **profile (continuous line) along the black lines indicated in the maps are shown below.**

equation. The best fitting was for $\rho = 0{,}79$, which indicates that both sources of variability are correlated.

$$f(x, y) = \frac{1}{2\pi\sigma_X\sigma_Y\sqrt{1-\rho^2}} \times \exp\left(-\frac{1}{2\left(1-\rho^2\right)}\left[\frac{(x-\mu_X)^2}{\sigma_X^2}+\frac{(y-\mu_Y)^2}{\sigma_Y^2} - \frac{2\rho\,(x-\mu_X)\,(y-\mu_Y)}{\sigma_X\sigma_Y}\right]\right) \tag{1}$$

These results clearly demonstrate that in the HfO_2 layer studied in this work, the correlation between the polycrystalline morphology and the charge density (higher at GBs, already observed in Fig. 2 and [11]) implies that when considered together as variability sources (as it happens in real devices), the V_{th} variability does not correspond to the addition of the associated variabilities but, in our case, is smaller than the one observed when only ρ_{ox} is considered. Therefore, the main conclusion of this section is that, although other variability sources affecting MOSFETs may be studied independently [20], [40], variability sources affecting the polycrystalline gate oxides are correlated and cannot be studied as independent statistical variables if an accurate analysis has to be performed.

B. IMPACT OF GRAIN SIZE AND GB DEPTH ON THE V_{th} VARIABILITY

One of the main characteristics of TACMAG is that, thanks to the possibility of generating (ρ_{ox}, t_{ox}) maps without the need of fabricating new samples, such variability sources and, in particular, the different parameters on which they depend (as, for example, Grain size, GB depth or width and/or charge density distribution), can be changed and analyzed independently. In this section, as another example of the proposed methodology capabilities, we have evaluated the impact of some morphological parameters associated to the high-k polycrystallization of the analyzed sample (as the GB depth and grain size) on the V_{th} variability (that is, on σV_{th}) of MOSFETs.

Fig. 7 shows the σV_{th} obtained for a set of one hundred 50×50 nm^2 MOSFET devices for different GB depths (a) and grain sizes (b) at both low (0.05 V) and high (1.0 V) drain biases. In all cases, smaller average value of V_{th} were obtained for higher V_D (not shown). However, since we are interested in the analysis of the variability, we have focused our analysis on σV_{th}. Note in Fig. 7a that σV_{th} increases as the GB depth rises, as expected: an increase of the GB depth leads to a higher inhomogeneity in t_{ox} and ρ_{ox}, which clearly affects the V_{th} variability. However, when the Grain size (Gsize) is considered as parameter, the V_{th} trend is different. Note in Fig. 7b that σV_{th} reaches the largest value when Gsize is smaller than the channel length of the MOSFET and depends on V_D. In any case, from that maximum value, when Gsize is reduced/increased, σV_{th} decreases. When the Gsize is much smaller than the MOSFET dimensions, every device contains a large amount of grains and, therefore, their impact on the V_{th} variability is averaged, leading to small values of σV_{th}. On the other hand, when Gsize is larger than the MOSFETs dimensions, many MOSFETs could contain

only one single crystal, increasing the homogeneity of the gate oxide characteristics and, therefore, reducing the V_{th} variability, as it is also observed in Fig. 7. For grain sizes comparable to the channel length the variability could be related to the inhomogeneity of the grain properties, since the thickness and charge in the grain are not homogeneous. Moreover, the V_{th} may be affected by the particular position of the grain in the channel. A combination of all these factors will determine the particular position of the variability maximum for a particular bias.

From a nanoscale point of view, the dependence of the MOSFET V_{th} variability on the GB depth and Gsize could be explained taking into account the nanoscale properties of the gate oxide (t_{ox} and ρ_{ox}) and how they affect the electrostatic potential in the channel (Fig. 5b). As an example, Fig. 8a-c shows different t_{ox} configurations and the corresponding t_{ox} and electrostatic potential profile measured along the highlighted lines.

Since the average value of the electrostatic potential depends on the position along the channel and, in our case, only relative variations are meaningful, in the three cases, the maximum value has been associated to 1000 mV and just relative variations with respect to this maximum have been considered. Note in Fig. 8a that a very deep GB (~0.5 nm deep, dark area in the image) is analyzed. Fig. 8b shows two small grains with a shallow GB between them (~0.3 nm deep). Finally, Fig. 8c corresponds to a big grain, which is quite homogeneous (t_{ox} variations are in the range of <0.1 nm). If we compare the t_{ox} variations in the three images with the electrostatic potential fluctuations along the profile, values of ~15, 9 and 6 mV are measured in Fig. 8a, b and c respectively. Moreover, in Fig. 8a, where a deep GB is detected, a clear correlation between the electrostatic potential and t_{ox} is registered. Therefore, these results indicate that the morphological parameters associated to the high-k polycrystallization (as the GB depth and Gsize) affect the electrostatic potential in the channel: the higher the t_{ox} fluctuations, the higher the potential variations. Since the electrostatic potential along the channel determines the global electrical properties of the MOSFET, these results would explain why, the higher the fluctuation in t_{ox} and ρ_{ox}, the higher the variability observed in V_{th}.

V. CONCLUSION

To conclude, a simulation methodology has been proposed to evaluate the impact of nanoscale variability sources related to the polycrystallization of gate dielectrics on the variability of MOSFET devices. With this purpose, a Thickness And Charge MAp Generator (TACMAG) has been developed and used in combination with a semiconductor device simulator. CAFM experimental data, i.e., dielectric morphology and current, are the inputs to the TACMAG and the outputs are thickness and charge density maps of the dielectric. The TACMAG tool has been tested by comparing the V_{th} variability of MOSFETs whose gate oxide characteristics were determined either from the use of the TACMAG generator or measured with CAFM. The results show that the proposed methodology can be reliably used to evaluate the impact of the nanoscale t_{ox} and ρ_{ox} fluctuations of polycrystalline dielectrics on the device threshold voltage variability.

As a particular example, the developed simulation tools have been used to evaluate the impact of the t_{ox} and ρ_{ox} fluctuations of a HfO_2 polycrystalline layer on the V_{th} variability of MOSFETs. The results show that, at least for the case of the sample analyzed in this work, ρ_{ox} fluctuations have a higher impact on σV_{th} than the t_{ox} variations. Moreover, the impact of t_{ox} and ρ_{ox} fluctuations on V_{th} are correlated and can be described by a bivariate equation. When combined, both variability sources are somehow compensated, being the global σV_{th} smaller than that caused individually by ρ_{ox} fluctuations. Therefore, our results show that, for an accurate analysis of the impact of the high-k polycrystallization on the V_{th} variability and for a more realistic approach to real devices, the gate oxide morphology and ρ_{ox} cannot be considered independent variability sources.

Although the proposed methodology has been applied to a particular high-k dielectric, it can be extended to any other kind of polycrystalline structure. Moreover, since the input parameters are related with the morphological and electrical characteristics of the dielectric (Gsize, GB depth, charge density...), they can be easily changed, allowing also to evaluate their impact without the need of fabricating and measuring new samples and, therefore, reducing the cost and time of such analysis.

REFERENCES

[1] J. Robertson and R. M. Wallace, "High-K materials and metal gates for CMOS applications," *Mater. Sci. Eng., R, Rep.*, vol. 88, pp. 1–41, Feb. 2015.

[2] J. Robertson, "High dielectric constant gate oxides for metal oxide Si transistors," *Rep. Prog. Phys.*, vol. 69, no. 2, pp. 327–396, Feb. 2006.

[3] V. Iglesias, M. Porti, M. Nafría, X. Aymerich, P. Dudek, T. Schroeder, and G. Bersuker, "Correlation between the nanoscale electrical and morphological properties of crystallized hafnium oxide-based metal oxide semiconductor structures," *Appl. Phys. Lett.*, vol. 97, no. 26, Dec. 2010, Art. no. 262906.

[4] K. Shubhakar, N. Raghavan, S. S. Kushvaha, M. Bosman, Z. R. Wang, S. J. O'Shea, and K. L. Pey, "Impact of local structural and electrical properties of grain boundaries in polycrystalline HfO_2 on reliability of SiO_X interfacial layer," *Microelectron. Rel.*, vol. 54, nos. 9–10, pp. 1712–1717, Sep. 2014.

[5] X. Wang, A. R. Brown, N. Idris, S. Markov, G. Roy, and A. Asenov, "Statistical threshold-voltage variability in scaled decananometer bulk HKMG MOSFETs: A full-scale 3-D simulation scaling study," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2293–2301, Aug. 2011.

[6] Y.-L. Wu, J.-J. Lin, B.-T. Chen, and C.-Y. Huang, "Position-dependent nanoscale breakdown characteristics of thin silicon dioxide film subjected to mechanical strain," *IEEE Trans. Device Mater. Rel.*, vol. 12, no. 1, pp. 158–165, Mar. 2012.

[7] U. Celano, Y. Y. Chen, D. J. Wouters, G. Groeseneken, M. Jurczak, and W. Vandervorst, "Filament observation in metal-oxide resistive switching devices," *Appl. Phys. Lett.*, vol. 102, no. 12, Mar. 2013, Art. no. 121602.

[8] W. Frammelsberger, G. Benstetter, J. Kiely, and R. Stamp, "C-AFM-based thickness determination of thin and ultra-thin SiO_2 films by use of different conductive-coated probe tips," *Appl. Surf. Sci.*, vol. 253, no. 7, pp. 3615–3626, Jan. 2007.

[9] M. Rommel, J. D. Jambreck, M. Lemberger, A. J. Bauer, L. Frey, K. Murakami, C. Richter, and P. Weinzierl, "Influence of parasitic capacitances on conductive AFM I-V measurements and approaches for its reduction," *J. Vac. Sci. Technol. B, Nanotechnol. Microelectron., Mater., Process., Meas., Phenomena*, vol. 31, no. 1, Jan. 2013, Art. no. 01A108.

[10] T. Erlbacher, V. Yanev, M. Rommel, A. J. Bauer, and L. Frey, "Gate oxide reliability at the nanoscale evaluated by combining conductive atomic force microscopy and constant voltage stress," *J. Vac. Sci. Technol. B, Nanotechnol. Microelectron., Mater., Process., Meas., Phenomena*, vol. 29, no. 1, Jan. 2011, Art. no. 01AB08.

[11] C. Couso, M. Porti, J. Martin-Martinez, A. J. Garcia-Loureiro, N. Seoane, and M. Nafria, "Local defect density in polycrystalline high-K dielectrics: CAFM-based evaluation methodology and impact on MOSFET variability," *IEEE Electron Device Lett.*, vol. 38, no. 5, pp. 637–640, May 2017.

[12] V. Yanev, M. Rommel, M. Lemberger, S. Petersen, B. Amon, T. Erlbacher, A. J. Bauer, H. Ryssel, A. Paskaleva, W. Weinreich, C. Fachmann, J. Heitmann, and U. Schroeder, "Tunneling atomic-force microscopy as a highly sensitive mapping tool for the characterization of film morphology in thin high-K dielectrics," *Appl. Phys. Lett.*, vol. 92, no. 25, Jun. 2008, Art. no. 252910.

[13] K. Murakami, M. Rommel, B. Hudec, A. Rosová, K. Hušeková, E. Dobročka, R. Rammula, A. Kasikov, J. H. Han, W. Lee, S. J. Song, A. Paskaleva, A. J. Bauer, L. Frey, K. Fröhlich, J. Aarik, and C. S. Hwang, "Nanoscale characterization of TiO_2 films grown by atomic layer deposition on RuO_2 electrodes," *ACS Appl. Mater. Interfaces*, vol. 6, no. 4, pp. 2486–2492, Feb. 2014.

[14] V. Iglesias, M. Lanza, K. Zhang, A. Bayerl, M. Porti, M. Nafría, X. Aymerich, G. Benstetter, Z. Y. Shen, and G. Bersuker, "Degradation of polycrystalline HfO_2-based gate dielectrics under nanoscale electrical stress," *Appl. Phys. Lett.*, vol. 99, no. 10, Sep. 2011, Art. no. 103510.

[15] A. Bayerl, M. Lanza, M. Porti, M. Nafria, X. Aymerich, F. Campabadal, and G. Benstetter, "Nanoscale and device level gate conduction variability of high-K dielectrics-based metal-oxide-semiconductor structures," *IEEE Trans. Device Mater. Rel.*, vol. 11, no. 3, pp. 495–501, Sep. 2011.

[16] G. Bersuker, D. C. Gilmer, D. Veksler, P. Kirsch, L. Vandelli, A. Padovani, L. Larcher, K. McKenna, A. Shluger, V. Iglesias, M. Porti, and M. Nafría, "Metal oxide resistive memory switching mechanism based on conductive filament properties," *J. Appl. Phys.*, vol. 110, no. 12, Dec. 2011, Art. no. 124518.

[17] G. Leung and C. O. Chui, "Variability impact of random dopant fluctuation on nanoscale junctionless FinFETs," *IEEE Electron Device Lett.*, vol. 33, no. 6, pp. 767–769, Jun. 2012.

[18] Y. Li, C.-H. Hwang, T.-Y. Li, and M.-H. Han, "Process-variation effect, metal-gate work-function fluctuation, and random-dopant fluctuation in emerging CMOS technologies," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 437–447, Feb. 2010.

[19] N. Seoane, D. Nagy, G. Indalecio, G. Espiñeira, K. Kalna, and A. García-Loureiro, "A multi-method simulation toolbox to study performance and variability of nanowire FETs," *Materials*, vol. 12, no. 15, p. 2391, Jul. 2019.

[20] G. Roy, A. R. Brown, F. Adamu-Lema, S. Roy, and A. Asenov, "Simulation study of individual and combined sources of intrinsic parameter fluctuations in conventional nano-MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 3063–3069, Dec. 2006.

[21] M. Porti, M. Nafría, and X. Aymerich, "Current limited stresses of SiO_2 gate oxides with conductive atomic force microscope," *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 933–940, Jun. 2003.

[22] L. Aguilera, M. Porti, M. Nafria, and X. Aymerich, "Charge trapping and degradation of HfO_2/SiO_2 MOS gate stacks observed with enhanced CAFM," *IEEE Electron Device Lett.*, vol. 27, no. 3, pp. 157–159, Mar. 2006.

[23] M. Lanza, V. Iglesias, M. Porti, M. Nafria, and X. Aymerich, "Polycrystallization effects on the nanoscale electrical properties of high-K dielectrics," *Nanosc. Res. Lett.*, vol. 6, no. 1, pp. 1–9, Jan. 2011.

[24] O. Pirrotta, L. Larcher, M. Lanza, A. Padovani, M. Porti, M. Nafría, and G. Bersuker, "Leakage current through the poly-crystalline HfO_2: Trap densities at grains and grain boundaries," *J. Appl. Phys.*, vol. 114, no. 13, Oct. 2013, Art. no. 134503.

[25] K. McKenna and A. Shluger, "The interaction of oxygen vacancies with grain boundaries in monoclinic HfO_2," *Appl. Phys. Lett.*, vol. 95, no. 22, Nov. 2009, Art. no. 222111.

[26] A. Asenov, A. R. Brown, G. Roy, B. Cheng, C. Alexander, C. Riddet, U. Kovac, A. Martinez, N. Seoane, and S. Roy, "Simulation of statistical variability in nano-CMOS transistors using drift-diffusion, Monte Carlo and non-equilibrium Green's function techniques," *J. Comput. Electron.*, vol. 8, nos. 3–4, pp. 349–373, Sep. 2009.

[27] K. Murakami, M. Rommel, V. Yanev, A. J. Bauer, and L. Frey, "Current voltage characteristics through grains and grain boundaries of high-K dielectric thin films measured by tunneling atomic force microscopy," *AIP Conf. Proc.*, vol. 1395, pp. 134–138, Nov. 2011.

[28] C. Couso, M. Porti, J. Martin-Martinez, V. Iglesias, M. Nafria, and X. Aymerich, "Conductive-AFM topography and current maps simulator for the study of polycrystalline high-K dielectrics," *J. Vac. Sci. Technol. B, Nanotechnol. Microelectron., Mater., Process., Meas., Phenomena*, vol. 33, no. 3, May 2015, Art. no. 031801.

[29] A. Leonardi, P. Scardi, and M. Leoni, "Realistic nano-polycrystalline microstructures: Beyond the classical Voronoi tessellation," *Phil. Mag.*, vol. 92, no. 8, pp. 986–1005, Mar. 2012.

[30] Z. Fan, Y. Wu, X. Zhao, and Y. Lu, "Simulation of polycrystalline structure with Voronoi diagram in Laguerre geometry based on random closed packing of spheres," *Comput. Mater. Sci.*, vol. 29, no. 3, pp. 301–308, Mar. 2004.

[31] G. Indalecio, A. J. García-Loureiro, M. Aldegunde, and K. Kalna, "3D simulation study of work-function variability in a 25 nm metal-gate FinFET with curved geometry using Voronoi grains," in *Proc. 17th Int. Conf. Simul. Semiconductor Processes Devices*, Sep. 2012, pp. 149–152.

[32] D. M. Caughey and R. E. Thomas, "Carrier mobilities in silicon empirically related to doping and field," *Proc. IEEE*, vol. 55, no. 12, pp. 2192–2193, Dec. 1967.

[33] K. Yamaguchi, "Field-dependent mobility model for two-dimensional numerical analysis of MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-26, no. 7, pp. 1068–1074, Jul. 1979.

[34] N. Seoane, G. Indalecio, E. Comesana, A. J. Garcia-Loureiro, M. Aldegunde, and K. Kalna, "Three-dimensional simulations of random dopant and metal-gate workfunction variability in an $In_{0.53}Ga_{0.47}As$ GAA MOSFET," *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 205–207, Feb. 2013.

[35] N. Seoane, G. Indalecio, M. Aldegunde, D. Nagy, M. A. Elmessary, A. J. Garcia-Loureiro, and K. Kalna, "Comparison of fin-edge roughness and metal grain work function variability in InGaAs and Si FinFETs," *IEEE Trans. Electron Devices*, vol. 63, no. 3, pp. 1209–1216, Mar. 2016.

[36] G. Espineira, D. Nagy, G. Indalecio, A. J. Garcia-Loureiro, K. Kalna, and N. Seoane, "Impact of gate edge roughness variability on FinFET and gate-all-around nanowire FET," *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 510–513, Apr. 2019.

[37] A. J. García-Loureiro, K. Kalna, and A. Asenov, "Intrinsic fluctuations induced by a high-K gate dielectric in sub-100 nm Si MOSFETs," *AIP Conf. Proc.*, vol. 780, no. 1, pp. 239–242, 2005.

[38] A. J. Garcia-Loureiro, N. Seoane, M. Aldegunde, R. Valin, A. Asenov, A. Martinez, and K. Kalna, "Implementation of the density gradient quantum corrections for 3-D simulations of multigate nanoscaled transistors," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 30, no. 6, pp. 841–851, Jun. 2011.

[39] R. H. Dennard, F. H. Gaensslen, H.-N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE J. Solid-State Circuits*, vol. SSC-9, no. 5, pp. 256–268, Oct. 1974.

[40] N. Seoane, G. Indalecio, D. Nagy, K. Kalna, and A. J. Garcia-Loureiro, "Impact of cross-sectional shape on 10-nm gate length InGaAs FinFET performance and variability," *IEEE Trans. Electron Devices*, vol. 65, no. 2, pp. 456–462, Feb. 2018.