IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received May 21, 2021, accepted June 10, 2021, date of publication June 21, 2021, date of current version June 29, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3090956

Capacitive Modeling of Cylindrical Surrounding Double-Gate MOSFETs for Hybrid RF Applications

NAVEENBALAJI GOWTHAMAN, (Member, IEEE), AND VIRANJAY M. SRIVASTAVA, (Senior Member, IEEE)
Department of Electronic Engineering, Howard College, University of KwaZulu-Natal, Durban 4041, South Africa
Corresponding author: Naveenbalaji Gowthaman (dr.gnb@ieee.org)

ABSTRACT The advancements in semiconductor technology greatly impact the growth of hybrid VLSI devices and components. The nanometer technology has been possibly executed due to the enhancement of the scaling factor of the MOSFETs. Since the MOSFETs play a vital role in building dense devices, it also has several research insights with various semiconductor materials with high-ꞓ dielectrics. The high-ꞓ dielectric material in place of the conventional oxide layer in the MOSFET design results in improved performance by reducing the Short Channel Effects (SCEs). In this research work, an analytical model of the lightly doped Cylindrical Surrounding Double-Gate (CSDG) MOSFET has been realized. The capacitive modeling has been done for this cylindrical structure. This modeling has been analyzed for all operating regions of the transistors, capacitance estimation, and electrical field dependence on the capacitance. The results have been compared with the previous research and tabulated. It has been observed that the transconductance (G_m) values have been raised to $0.0106\ S/\mu m$ from $0.000645\ S/\mu m$ with the inclusion of 2D electron gas in the core of CSDG MOSFET. This novel model occupies less area on the board, and routing is more accessible than the conventional DG MOSFET design. The overall results have been following the agreement in terms of accuracy, area tradeoff, and high speed, making the novel model suitable for high-frequency/RF applications.

INDEX TERMS CSDG MOSFET, cylindrical structure, double-gate (DG) MOSFET, high-ꞓ dielectric, microelectronics, nanotechnology, VLSI.

I. INTRODUCTION

Designing an Integrated Circuit (IC) or high-speed semiconductor devices requires a set of protocols or regulations for its series of functionalities-photo-lithography, etching, ion implantation, atomic layer deposition, metal and contact creation, etc. [1]–[3]. The MOSFET design involves these functions and had been performed by a group of marketable entities. The double-gate model is extended as Cylindrical Surrounding Double-Gate (CSDG) MOSFET to get three-dimensional controllability and scalability in the nanometer regime. The proposed model has been described as single analytical expressions as in cylindrical dimension as the conventional DG MOSFET is revolved along the axis outside the second gate. This revolution creates the bottom gate as the inner gate in the CSDG MOSFET design. The scaling of the gate terminal length has been promising research in the CSDG MOSFET structures [4]. The proposed model makes the transistor immune to Short Channel Effects (SCEs) and highly controllable due to the cylindrical structure. Doping acts as a significant factor in the CSDG MOSFETs since the lightly doped or undoped channel is the preferred overdoped material [4], [5]. This doped material has high fluctuations, which result in poor mobility and threshold voltage (V_T) variations [6].

The CSDG MOSFETs have been experimented with in previous research, but to calculate the actual performance of the CSDG MOSFETs, capacitance modeling and electrical field estimation for the same is required. The drain current models were established in recent works in the nanometer regime [7]–[11], which concentrates only on the long channel models [5], [12]. Hence, capacitance modeling with good accuracy of transconductance and electrical field in the cylindrical structure is essential for the accurate designing of CSDG MOSFETs.

Takagi and Takenaka [12] proposed a fabrication technique of the InGaAs ultrathin body channels on large size Si wafers. Also, the effectiveness of III-V materials on TFETs

The associate editor coordinating the review of this manuscript and approving it for publication was Yue Zhang.

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/

through the enhancement of tunneling probability has been demonstrated. Yu *et. al.* [13] have evaluated monolithic 3-D logic circuits and 6T SRAMs composed of InGaAs-n/Ge-p ultra-thin-body CSDG MOSFETs by considering inter-layer coupling through the TCAD mixed-mode model. Their work indicates that monolithic 3-D InGaAs/Ge logic circuits provide equal leakage and better delay performance compared with planar 2-D structure through the optimized 3-D layout. Rodwell *et. al.* [14] reviewed the development of In(Ga)As-channel DG MOSFETs. The InAs and InGaAs channels, combined with thin gate dielectrics, provide high transconductance, but Off-state leakage can be high due to band-band tunneling currents. This leakage is reduced through thin $2.5\ nm - 3\ nm$ channels and InGaAs or InP vertical field spacers in the raised source and drain. Kanale and Baliga [15] demonstrated the BaSIC (DMM) topology to improve the short-circuit time for a $1.2\ kV$ SiC power MOSFET product from $4.8\ \mu s$ to $7.9\ \mu s$ with a $17\ \%$ increase in on-state resistance by utilizing a commercially available $100\ V$ rated Gate-Source-Shorted (GSS) Si Depletion-Mode power MOSFET (DMM). The optimization of the Si GSS-DMM was discussed to achieve superior performance, namely larger short-circuit time with less increase in ON-resistance. Akbar *et. al.* [16] advanced using Deep Learning (DL) algorithms in the design of cylindrical surrounding MOSFET, device simulation for gate-all-around silicon nanowire MOSFETs to predict electrical characteristics of device induced by work function fluctuation. Notably, the DL approach can extract crucial electrical characteristics of a complicated device accurately with *a 2 %* error in a cost-effective manner computationally.

In this research work, the exact cylindrical capacitive model of the CSDG MOSFETs has been developed to eradicate SCEs and provide stability, scalability, a better routing facility on board. The drain current equation has been modified for cylindrical structure, which is valid for all operating regions. The lightly doped channel is most suitable for the CSDG MOSFET design [17]–[21]. The model starts with developing the current equation for the Double-Gate (DG) MOSFET and extends to the nanometer region for the CSDG MOSFET by substituting the equivalent parameters for the cylindrical structure [22]. This proposed model has been validated using the results extracted from the electronic device simulator and also using predictive model values. The quantum energy coefficients have not been covered in this model as the threshold voltage drops rounded up in the quantum correction, which is important only in Silicon-based devices with lower than $10\ nm$ thickness [23]–[25]. The capacitance estimation has been done using the conventional DG MOSFET constraints and expanded to the cylindrical structure with the electrical field model in the oxide layer [26], considering the thickness of the oxide layer [27]. It has been maintained at less than $10\ nm$ for semiconductor material alloys [28], [29].

This research paper has been organized as follows: Section II models the CSDG MOSFET using the capacitance (electrical field associated) with high-ƙ dielectric material between the gate and the channel. Also, this section deals with the effect of channel doping. Section III describes the current modeling of the proposed MOSFET. Section IV elaborates on the capacitive model. Section V supports the proposed model with quantitative and qualitative results followed by the discussions to enhance the performance of the CSDG MOSFET. Finally, Section VI concludes the work with confirmed results and also provides future considerations.

II. STRUCTURAL ANALYSIS OF PROPOSED CSDG MOSFET MODEL

The functional unit in the design of CSDG MOSFET is the two-dimensional double-gate MOSFET that is shown in fig. 1. Here in fig. 1 (dimensions, in nm), the green color block represents the substrate material, the royal blue block shows the outer gate terminal, and the light blue depicts the inner gate terminal. The red color is the spacer material. The yellow color of the DG MOSFET shows the oxide layer where a high-ƙ (kappa) dielectric has been introduced. The purple color shows the contacts at the source and drain terminals. To design an efficient CSDG in three-dimension, the 2-D DG MOSFET has been revolved along the axis outside the second/internal gate terminal. This makes the proposed design reflect three-dimension as CSDG MOSFET as shown in fig. 2(a). The cross-sectional view of the proposed CSDG MOSFET is represented as isometric and plane view in fig. 2(b).

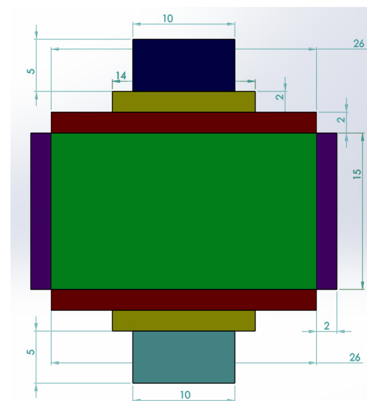
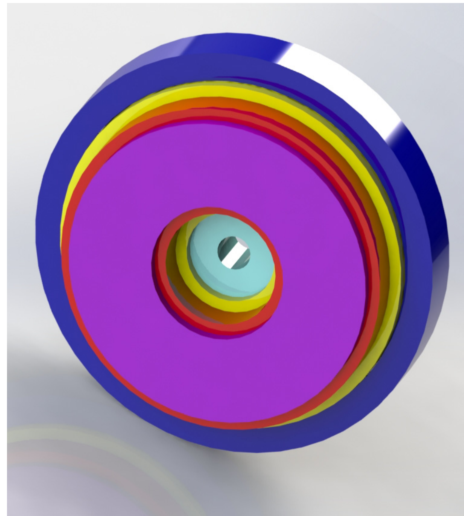


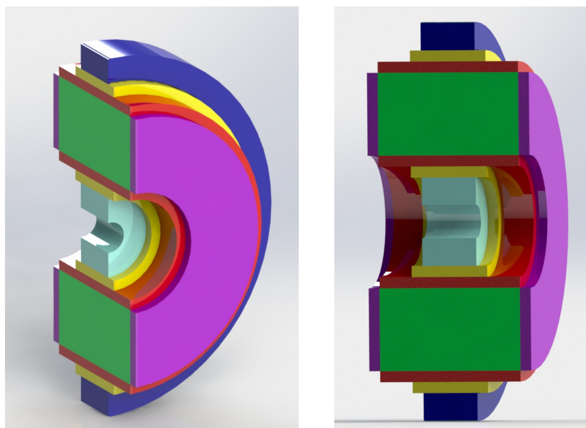
FIGURE 1. The dimensions (in nm) of the 2D structure of the double-gate MOSFET.

The most significant challenges in the design of the CSDG MOSFET are the account of capacitances and transconductances [30], [31]. This cylindrical structure constitutes the capacitance between the concentric walls created by the inner gate terminal and the channel inside the bulk separated by the spacer layer. In this analysis, the structural parameters (as in Table 1) of the cylindrical-shaped MOSFET are considered. The electrical field stored in the capacitor is derived using the energy stored by charge accumulation in the CSDG MOSFET [32]–[34].

The CSDG MOSFET design has been analyzed using the capacitive model derived in the following section.



(a) The isometric view



(b) Cross-sectional view

FIGURE 2. **The proposed CSDG MOSFET. The double-gate MOSFET is rotated around the axis outside/below the lower gate to get the cylindrical-shaped CSDG MOSFET.**

This enables the proposed MOSFET suitable for the application such as low power RF device design, industrial automation, and consumer electronics [35]–[37]. The oxide capacitive effect has been analyzed using the energy stored in the concentric cylindrical walls, which constitutes the electrical field [38].

III. CURRENT MODELING FOR CSDG MOSFET

The current passing through the device is commonly termed as ON-current and the current passing through the insulator or the high-ƙ dielectric material is termed as the leakage current [39]. In the MOSFET ON state, the current flowing between the source and drain terminals is often referred to as the on-current [40], [41]. Here, the MOSFET current equation has been derived for the cylindrical structure and applied to model the cylindrical surrounding double-gate MOSFET.

For n-channel MOSFET, the current equations [5]–[8], [42] can be given as (1), shown at the bottom of the page.

For p-channel MOSFET, the current equations [5]–[8], [42] can be given as (2), shown at the bottom of the page.

The transistors with multiple threshold voltages (V_t) has been in need to design low power circuit in nanometer and its optimization. Channel doping plays a significant role in designing low-power circuits with higher mobility and controllability [43]. The use of intrinsic channel material is avoided in recent research to increase mobility and lower dopant fluctuations, reducing controllability. However, to fabricate multi-gate terminals in a single structure, enough doping has to be used to stay in the active operating region. With a lower amount of inversion charge carriers or minimum gate voltages, the depletion charge due to low V_g is appreciable in non-zero energy across the channel length [44]. The intrinsic material has zero initial energy, and the potential was observed to be constant in the active region. The doping increases the operating range such as in the case of DG MOSFET, doping exhibits linear electric field and an acute drop of potential in the center of the channel.

The charge inversion is acquired along with the interface layer and accumulates close to this layer at very minimum gate voltages [17], [45]. Similar structures can be used in the cylindrical structure as well in the parabolic field is set up at very minimum gate voltages in the cylindrical coordinate. The positions of the charge accumulated in the concentric cylinders have been fixed inside the centroid position, which can be used to modify the effective capacitance expression as in (3). The capacitance is the combination of the capacitance connected series, gate capacitance, and the oxide capacitance, channel capacitance components due to the centroid point chosen inside the cylindrical structures [7], [16], [46]. For a cylindrical surrounding double-gate MOSFET is given

$$\left.\begin{array}{lll} \mathrm{I_{DS}} = 0 & \text{for} & \mathrm{V_{GS}} < \mathrm{V_T} \\ \mathrm{I_{D(linear)}} = \dfrac{\mu_n}{2}.\mathrm{C_{ox}}.\dfrac{\mathrm{W}}{\mathrm{L}}\left[2\left(\mathrm{V_{GS}} - \mathrm{V_T}\right).\mathrm{V_{DS}} - \mathrm{V_{DS}^2}\right] & \text{for} & \left(\mathrm{V_{GS}} \geq \mathrm{V_T}\right) \& \left(\mathrm{V_{DS}} < \mathrm{V_{GS}} - \mathrm{V_T}\right) \\ \mathrm{I_{D(saturation)}} = \dfrac{\mu_n}{2}.\mathrm{C_{ox}}.\dfrac{\mathrm{W}}{\mathrm{L}}\left(\mathrm{V_{GS}} - \mathrm{V_T}\right)^2\left(1 + \lambda \mathrm{V_{DS}}\right) & \text{for} & \mathrm{V_{GS}} \geq \mathrm{V_T} \end{array}\right\} \quad (1)$$

$$\left.\begin{array}{lll} \mathrm{I_{DS}} = 0 & \text{for} & \mathrm{V_{GS}} < \mathrm{V_T} \\ \mathrm{I_{D(linear)}} = \dfrac{\mu_p}{2}.\mathrm{C_{ox}}.\dfrac{\mathrm{W}}{\mathrm{L}}\left[2\left(\mathrm{V_{GS}} - \mathrm{V_T}\right).\mathrm{V_{DS}} - \mathrm{V_{DS}^2}\right] & \text{for} & \left(\mathrm{V_{GS}} \geq \mathrm{V_T}\right) \& \left(\mathrm{V_{DS}} < \mathrm{V_{GS}} - \mathrm{V_T}\right) \\ \mathrm{I_{D(saturation)}} = \dfrac{\mu_p}{2}.\mathrm{C_{ox}}.\dfrac{\mathrm{W}}{\mathrm{L}}\left(\mathrm{V_{GS}} - \mathrm{V_T}\right)^2\left(1 + \lambda \mathrm{V_{DS}}\right) & \text{for} & \mathrm{V_{GS}} \geq \mathrm{V_T} \end{array}\right\} \quad (2)$$

as follows, in general, for cylindrical structures, cylindrical capacitance per unit length is often expressed as:

$$\frac{C}{L_c} = \frac{2\pi k\varepsilon_0}{\ln\left(\frac{b}{a}\right)} \tag{3}$$

Thereafter, the capacitance modeling has been executed for the proposed CSDG MOSFET using the (1) and (2). The CSDG MOSFET delivers a cylindrical capacitance between the gate and conducting material. There exists an oxide layer that acts as a dielectric material [47].

Hence, this setup constitutes a concentric cylindrical capacitor between the layers of the transistor [38], [42]. The concentric cylindrical capacitance is similar to the parallel plate capacitor with the cylindrical coordinates. The cylindrical capacitance parameters of (3) are substituted in (1) and (2), forming the (4) and (5), respectively. For n-channel CSDG MOSFET, the drain current can be expressed as (4), shown at the bottom of the page.

For *p-channel CSDG-MOSFET*, the drain current can be given as (5), shown at the bottom of the page.

IV. EXTENSIVE CAPACITIVE MODELING

In this modeling, the capacitance effect has been calculated for the two-dimensional structure initially, and then it has been extended to the cylindrical structure. The CSDG MOSFET has complex capacitance expressions, which are modeled using the electrical field in the cylinder and the energy stored in the concentric sheets of the cylinder (area between gate and the channel separated by a high-ķ dielectric, acts as a concentric capacitor inside the CSDG MOSFET) [48], [49]. The high-ķ dielectric material acts as a vital modeling capacitance parameter in the CSDG MOSFET paradigm [9], [12].

The proposed CSDG structure is a cylindrical form, and modeling of a cylinder is essential to model for the same. Customarily, the cylindrical capacitance of the CSDG MOSFET is expressed as:

$$C_{ox_cyl} = k\varepsilon_{ox}\frac{A_{cap}}{d} \tag{6}$$

where the area of the cylindrical structure is given by:

$$A_{cyl} = 2\pi r^2 + h(2\pi r) \tag{7}$$

The cylindrical capacitance of the oxide layer (preferably high-ķ dielectric material) in the CSDG MOSFET is given by (6). This capacitor has become a dielectric cylindrical capacitor of area A_{cap}:

$$A_{cap} = A_{c1} - A_{c2} \tag{8}$$

The area of the two cylindrical structures has to be calculated and after subtracting the area of the cylinder having a smaller radius (inner, b) from the area of a cylinder having a larger radius (outer, a), it gives the exact area of the capacitor dielectric material. It has been used to calculate the effect of the high-ķ dielectric material in the construction in the CSDG MOSFETs [50]. The outer and inner cylinder's area is denoted as A_{c1} and A_{c2}.

$$\left.\begin{aligned} A_{c1} &= 2\pi r_{c1}^2 + h(2\pi r_{c1}) \\ A_{c2} &= 2\pi r_{c2}^2 + h(2\pi r_{c2}) \end{aligned}\right\} \tag{9}$$

Substituting (9) in (8) as

$$A_{cap} = \left[2\pi r_{c1}^2 + h(2\pi r_{c1})\right] - \left[2\pi r_{c2}^2 + h(2\pi r_{c2})\right] \tag{10a}$$

Therefore,

$$A_{cap} = 2\pi\left[\left(r_{c1}^2 - r_{c2}^2\right) + h(r_{c1} - r_{c2})\right] \tag{10b}$$

Cylindrical capacitance can be given as,

$$\begin{aligned} C_{ox_cyl} &= k\varepsilon_0\frac{A}{d} = k\varepsilon_0\frac{2\pi\left[\left(r_{c1}^2 - r_{c2}^2\right) + h(r_{c1} - r_{c2})\right]}{d} \\ &= \frac{2\pi k\varepsilon_0}{d}\left[\left(r_{c1}^2 - r_{c2}^2\right) + h(r_{c1} - r_{c2})\right] \end{aligned} \tag{11}$$

The capacitance in the cylindrical structure is the function of the radii of the inner (*a*) and the outer (*b*) cylinders. The expression as in (11) shows the capacitance due to the oxide layer between the gate and channel materials.

A. ELECTRICAL FIELD IN THE CAPACITOR OF CSDG MOSFET

In general, energy stored in the capacitor is given as E_{cap}:

$$E_{cap} = \frac{1}{2}C_{ox_cyl}.V^2 \tag{12}$$

$$\left.\begin{aligned} I_{D(linear)} &= \frac{\mu_n\pi k\varepsilon_{ox}}{\ln\left(\frac{b}{a}\right)}\frac{W}{L}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] && \text{for} \quad (V_{GS} \geq V_T)\,\&\,(V_{DS} < V_{GS} - V_T) \\ I_{D(saturation)} &= \frac{\mu_n\pi k\varepsilon_{ox}}{\ln\left(\frac{b}{a}\right)}\frac{W}{L}\left[(V_{GS} - V_T)^2(1 + \lambda V_{DS})\right] && \text{for} \quad V_{GS} \geq V_T \end{aligned}\right\} \tag{4}$$

$$\left.\begin{aligned} I_{D(linear)} &= \frac{\mu_p\pi k\varepsilon_{ox}}{\ln\left(\frac{b}{a}\right)}\frac{W}{L}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] && \text{for} \quad (V_{GS} \geq V_T)\,\&\,(V_{DS} < V_{GS} - V_T) \\ I_{D(saturation)} &= \frac{\mu_p\pi k\varepsilon_{ox}}{\ln\left(\frac{b}{a}\right)}\frac{W}{L}\left[(V_{GS} - V_T)^2(1 + \lambda V_{DS})\right] && \text{for} \quad V_{GS} \geq V_T \end{aligned}\right\} \tag{5}$$

Substituting (11) in (12) and after reduction will give:

$$E_{cap_cyl} = \frac{\pi k \varepsilon_0 V^2}{d}\left[\left(r_{c1}^2 - r_{c2}^2\right) + h\left(r_{c1} - r_{c2}\right)\right] \quad (13)$$

An electric field in the cylindrical capacitor within the cylinder is expressed as:

$$\left.\begin{aligned} E &= \frac{V}{d} = \frac{\mu_0}{2\pi R^2}\cdot\frac{\mu_n \pi k \varepsilon_0}{\ln\left(\frac{b}{a}\right)}\cdot\frac{W}{L}\left[2\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^2\right] \\ E &= -\frac{\mu_0 \mu_n k \varepsilon_0}{2R^2}.\ln\left(\frac{a}{b}\right)\cdot\frac{W}{L}\left[2\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^2\right] \end{aligned}\right\} \quad (14)$$

The electrical field is inversely proportional to the radius of the three-dimensional cylindrical structure. As shown in (14), the expression for the electric field is applied in the following section to derive the electric field associated with the oxide layer. This gate oxide layer acts as a dielectric material. So, the entire design comprises a concentric cylindrical capacitor between the layers of the CSDG MOSFET. The concentric cylindrical capacitance is similar to the parallel plate capacitor but with the cylindrical coordinates [51]–[53]. Hence, the modeling of this electric field plays a significant role in analyzing the capacitive effect and the energy stored in the MOSFET.

B. COMPREHENSIVE ELECTRICAL FIELD IN THE OXIDE LAYER

An electric field in the inner cylindrical capacitor with uniform current density is expressed as:

$$\left.\begin{aligned} E_{inner} &= -\frac{\mu_0 \mu_n k \varepsilon_0}{2r}.\ln\left(\frac{a}{b}\right)\cdot\frac{W}{L}\left[2\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^2\right] \\ E_{outer} &= \frac{\mu_0 \mu_n k \varepsilon_0}{r}.\ln\left(\frac{a}{b}\right)\cdot\frac{W}{L}\left[2\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^2\right] \end{aligned}\right\} \quad (15)$$

The total electric field of the cylindrical structure of the oxide layer is given by the expression after reduction (14) gives the electric field associated with the oxide layer of the cylindrical capacitor.

The expression for the electric field in the oxide layer of CSDG MOSFET is given as:

$$\left.\begin{aligned} E_{ox} &= E_{inner} + E_{outer} \\ E_{ox} &= \left\{-\frac{\mu_0 \mu_n k \varepsilon_0}{2r}.\ln\left(\frac{a}{b}\right)\cdot\frac{W}{L}\left[2\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^2\right]\right\} \\ &+ \left\{\frac{\mu_0 \mu_n k \varepsilon_0}{r}.\ln\left(\frac{a}{b}\right)\cdot\frac{W}{L}\left[2\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^2\right]\right\} \\ E_{ox} &= \frac{1}{2r}\mu_0 \mu_n k \varepsilon_0.\ln\left(\frac{a}{b}\right)\cdot\frac{W}{L}\left[2\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^2\right] \end{aligned}\right\} \quad (16)$$

Here, the expression, E_{ox} provides the reduced form of the electric field associated with the cylindrical capacitor with a high-ƙ dielectric material between two concentric cylindrical structures.

This analysis has been further divided into following sections:

a. For CSDG MOSFET, $a = r_{c1}; b = r_{c2}$, in (15), the energy stored in the oxide layer becomes,

$$E_{ox} = \frac{1}{2r}\mu_0 \mu_n k \varepsilon_0.\ln\left(\frac{r_{c1}}{r_{c2}}\right) \cdot\frac{W}{L}\left[2\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^2\right] \quad (17)$$

b. For $r_{c1} = r_{c2} = R$

$$E_{cap_cyl} = \frac{\pi k \varepsilon_0 V^2}{d} V^2/cm \quad (18)$$

c. For p-type CSDG MOSFET, $a = r_{c1}$; $b = r_{c2}$ in Eq. (15)

$$E_{ox} = -\frac{\mu_0 \mu_p \varepsilon_0 k}{2R^2}.\ln\left[\frac{r_{c1}}{r_{c2}}\right] \cdot\frac{W}{L}.\left[2\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^2\right] \quad (19)$$

The small-signal model of capacitance at the gate terminal with lightly doped channel and the high-ƙ dielectric material in CSDG MOSFET (as in fig. 1) (Gate length = *10 nm*, t_{ox} = *2 nm*, and L = *30 nm)* has been simulated using electronic simulator.

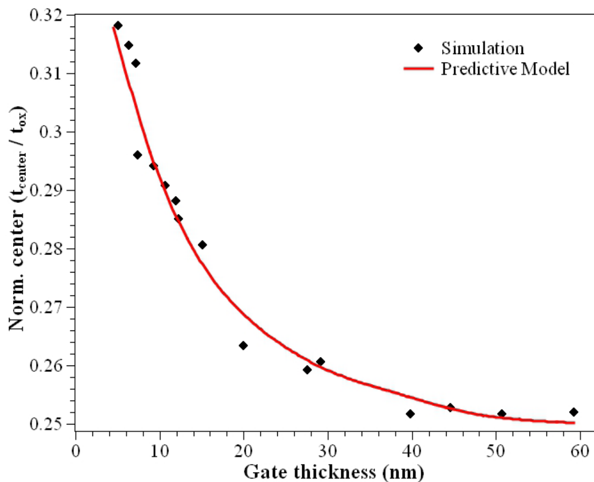
The device has been used in the nanometer range in the linear region to record the capacitance values (drain voltage, $V_{ds} = 50\ mV$) and compared them with the predictive model. The resulted model predicts and effectively calculates the gate capacitances. As the centroid approaches the interface layer when the gate voltage is increased, the gate capacitance also rises to its maximum.

V. RESULTS AND DISCUSSIONS

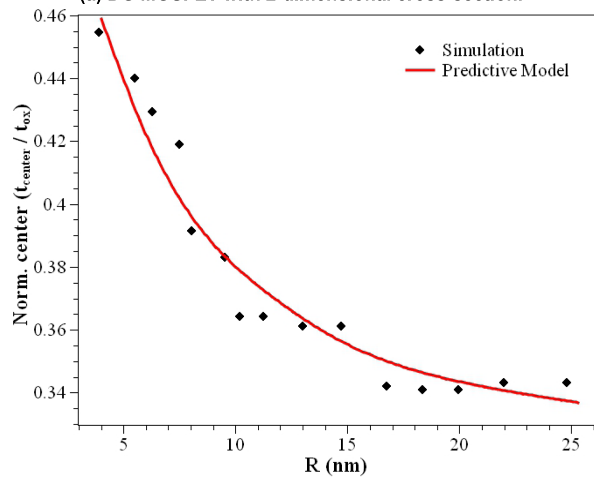
The cylindrical model has been simulated using the electronic simulator and the results have been compared with the Predictive Technology Model (PTM) values.

The center of the cylindrical structure was extracted from the simulation results and the charge density distribution graphs were plotted as in fig. 3(a) double-gate and 3(b) cylindrical surrounding double-gate MOSFET, respectively. The exponential values of the results are in good agreement with the predicted values.

The simulated result is submissive in order with the recorded values. The MOSFET behaves submissively to the conventional planar structure. The predicted values of gate thickness for DG MOSFET below *12 nm* possess the normalized center (t_{center}/t_{ox}) with *0.31825, 0.29075*, and *0.0.285125* for *5 nm, 10 nm*, and *12 nm*, respectively. But in order of higher thickness, it has been observed to be from *0.280625* to *0.252125* for *25 nm* and *60 nm*, respectively. The experimented simulation was carried out and it showed agreement to the predicted values. The simulation result for *60 nm* gate thickness provides a normalized center of *0.25025* that is nearer to the predicted values. The predicted value and the electronic device simulated values are in perfect agreement that states that the capacitive model proposed has been satisfied. The increment in the gate voltage provides



(a) DG MOSFET with 2-dimensional cross-section.



(b) CSDG MOSFET with cylindrical cross-section.

FIGURE 3. **Charge along the center of the cylindrical structure has a dependence on dimensions of the MOSFET with simulated values and predictive model.**

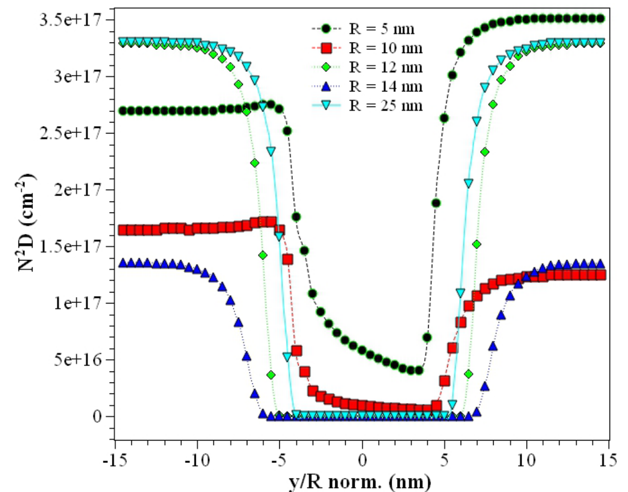


FIGURE 4. **Simulated charge density distribution along the length of the channel in the diameter of the CSDG MOSFET structure in the subthreshold operating region for various radii.**

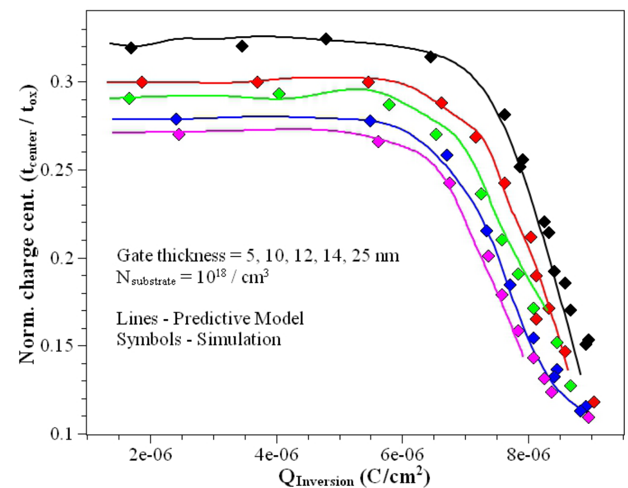


FIGURE 5. **The cylindrical center for the charge has been shifted towards the interface between the gate and the oxide layer.**

the development of the charge carrier accumulation along the channel length, which increases the chance of band bending towards the interface between the gate and the channel. The charge density distribution is shown in fig. 4 to depict the various radii of the cylindrical structure of the proposed MOSFET. The novel model can be used in hybrid RF applications and also introduced to the different configurations of heterostructures.

The predictive model of the MOSFET has been used to find the charge center in the cylinder, which has been in agreement with the proposed analytical model as shown in fig. 5. This shows the exact location of the center for various radii of the proposed CSDG MOSFET. This design can be used to design complex electronic devices like high-precision hybrid RF devices.

The value of the charge density distribution has been analyzed for various radii of the CSDG MOSFET, which states the proposed model is working successfully in all regions of operations satisfying the desired outputs. The core of the cylindrical surrounding double-gate MOSFET plays a major role in improving the transconductance parameter. Initially, the core of the CSDG MOSFET has been designed without any material that shows reduced improvement. The two-dimensional electron gas (2DEG) has been added as core material to enhance the electron transmission inside the core. This improves the velocity of the electrons in the inner gate material. So, the transconductance in the active region has been improved well and it is more submissive to the CSDG MOSFET without 2D electron gas. The transconductance values have been improved with the inclusion of 2D electron gas in the core inside the inner gate cylinder.

At normal room temperature, $V_d = 0.167\ V$, it has been observed that the transconductance (G_m) values have been raised to *0.0106* $S/\mu m$ from *0.000645* $S/\mu m$ without and with 2D electron gas respectively. The value of

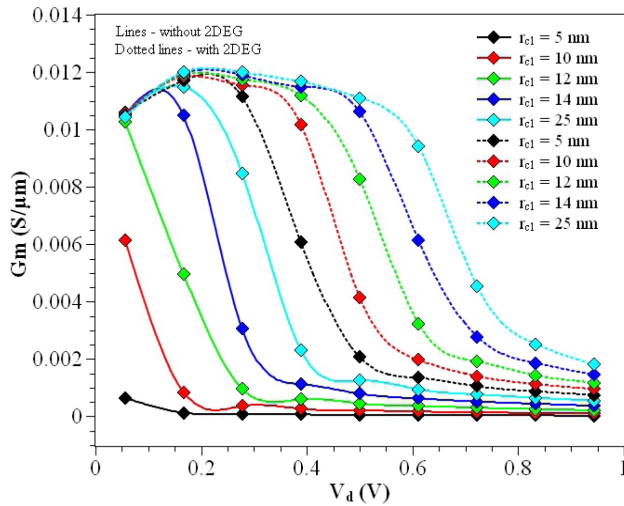


FIGURE 6. The transconductance values range for various radii of the inner cylindrical structure showing the effect of the 2D electron gas in the core of the proposed CSDG MOSFET.

TABLE 1. Parameters used for capacitance modeling.

Symbol	Description of the parameters used
A_{cap}	Area of the cylindrical capacitance
A_{cyl}	Area of the cylinder structure
A_{c1}, A_{c2}	Area of the outer, and inner cylindrical capacitor
a, b	The outer, and inner radius of the cylindrical capacitor
C_{ox}	The specific capacitance of the gate oxide
C_{ox_cyl}	The cylindrical capacitance (CSDG)
d	Unit length of the capacitor
E_{cap}	Energy stored in the capacitor
E_{cap_cyl}	Energy stored in the cylindrical capacitor (CSDG)
E_{inner}	Energy stored in the inner cylinder
E_{outer}	Energy stored in the outer cylinder
h	Height of the cylindrical capacitor (CSDG)
L	The gate length of the transistor
L_c	Unit length of the capacitor
r	The radius of the cylindrical capacitor (General)
r_{c1}, r_{c2}	The outer, and inner radius of the CSDG
R	Effective radius rc1<R<rc2
V_{GS}	Gate to Source voltage
W	The width of the transistor
ε_0	The permittivity of free space
ε_{ox}	The relative permittivity of the gate oxide
λ	Channel length modulation
μ_n	The electron mobility of the transistor substrate (n-type)
μ_p	The hole mobility of the transistor substrate (p-type)

transconductance has been improved from $0.000208\ S/\mu m$ to $0.00415\ S/\mu m$ at $V_d = 0.5\ V$ for the radius of *10 nm*. For a greater impact, the usage of electron gas has been showing a considerable amount of improvement in the G_m values for the radii of the proposed CSDG MOSFET. Hence, the modeled CSDG MOSFET has been appropriate to work in hybrid RF devices and most suitable for designing consumer electronic devices.

VI. CONCLUSION AND FUTURE RECOMMENDATIONS

In this research work, an analytical capacitive model for the cylindrical surrounding double-gate MOSFET had been proposed. It has been validated in all the operating regions of the transistor. The lightly doped cylindrical structure is capable of performing characteristics in the linear active region. The overall results show very well submissive than the conventional MOSFET. A compact analytical capacitive model for the cylindrical structure had been analyzed with a three-dimensional cylindrical structure. The simulations provide agreement with the proposed CSDG MOSFET with the parametric evaluation with the cylindrical MOSFET and the energy stored in a cylindrical structure, electrical field associated with that.

In the future, the CSDG with heterostructures can be developed to provide high electron mobility inside the channel. The three-dimensional design can be improved in the electron velocity by applying a high-ƙ dielectric along with the arbitrary alloy of semiconductor materials. A further study can be carried out to improve I_{ON}/I_{OFF} ratio.

APPENDIX

See Table 1.

REFERENCES

[1] (2013). *International Technology Roadmap for Semiconductors*. [Online]. Available: https://www.public.itrs.net

[2] B. Duan, S. Xue, X. Huang, and Y. Yang, "Novel Si/SiC heterojunction lateral double-diffused metal oxide semiconductor with SIPOS field plate by simulation study," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 114–120, Dec. 2021.

[3] P. Ghosh, S. Haldar, R. S. Gupta, and M. Gupta, "An analytical drain current model for dual material engineered cylindrical/surrounded gate MOSFET," *Microelectron. J.*, vol. 43, no. 1, pp. 17–24, Jan. 2012.

[4] V. M. Srivastava, "Scaling effect on parameters of HfO_2 based CSDG MOSFET," *Int. J. Eng. Technol.*, vol. 9, no. 2, pp. 420–426, Apr./May 2017.

[5] H.-J. Yang and Q.-Y. Feng, "Design novel structure of high-voltage MOSFET with double-trench gates," in *Proc. Photon. Electromagn. Res. Symp. (PIERS)*, Rome, Italy, Jun. 2019, pp. 1012–1017.

[6] J. Sharma, R. Pandey, and A. D. D. Dwivedi, "Design and device characteristic analysis of a triple material double gate (TMDG) strained channel MOSFET," in *Proc. 3rd Int. Conf. Workshops Recent Adv. Innov. Eng. (ICRAIE)*, Jaipur, India, Nov. 2018, pp. 1–4.

[7] W. M. Arden, "The international technology roadmap for semiconductors—Perspectives and challenges for the next 15 years," *Current Opinion Solid State Mater. Sci.*, vol. 6, no. 5, pp. 371–377, Oct. 2002.

[8] J. An and S. Hu, "Heterojunction diode shielded SiC split-gate trench MOSFET with optimized reverse recovery characteristic and low switching loss," *IEEE Access*, vol. 7, pp. 28592–28596, Feb. 2019.

[9] M. Shunqukela and V. M. Srivastava, "Dielectric material (HfO_2) effect on the surface potential for CSDG MOSFET," in *Proc. 8th IEEE Int. Conf. Comput. Commun. Informat. (ICCCI)*, Coimbatore, India, Jan. 2018, pp. 135–139.

[10] N. Gowthaman and V. M. Srivastava, "Analysis of n-type double-gate MOSFET (at nanometer-scale) using high-*K* dielectrics for high-speed applications," in *Proc. 44th Int. Spring Seminar Electron. Technol. (ISSE)*, Dresden, Germany, May 2021, pp. 1–5.

[11] J. Jeong, S. K. Kim, J. Kim, D.-M. Geum, J. Park, J.-H. Jang, and S. Kim, "Stackable InGaAs-on-insulator HEMTs for monolithic 3-D integration," *IEEE Trans. Electron Devices*, vol. 68, no. 5, pp. 2205–2211, May 2021.

[12] S. Takagi and M. Takenaka, "III–V MOS device technologies for advanced CMOS and tunneling FET," in *Proc. Compound Semiconductor Week (CSW), Includes 28th Int. Conf. Indium Phosph. Rel. Mater. (IPRM) 43rd Int. Symp. Compound Semiconductors (ISCS)*, Toyama, Japan, Jun. 2016, pp. 1–2.

[13] K.-C. Yu, M.-L. Fan, P. Su, and C.-T. Chuang, "Evaluation of monolithic 3-D logic circuits and 6T SRAMs with InGaAs-n/Ge-p ultra-thin-body MOSFETs," *IEEE J. Electron Devices Soc.*, vol. 4, no. 2, pp. 76–82, Mar. 2016.

[14] M. J. Rodwell, C. Y. Huang, S. Lee, V. Chobpattana, B. Thibeault, W. Mitchell, S. Stemmer, and A. Gossard, "Record performance InGaAs MOSFETS targeting ITRS high performance and low-power logic," *ECS Trans.*, vol. 66, no. 4, pp. 135–140, May 2015.

[15] A. Kanale and B. J. Baliga, "Theoretical optimization of the Si GSS-DMM device in the BaSIC topology for SiC power MOSFET short-circuit capability improvement," *IEEE Access*, vol. 9, pp. 70039–70047, May 2021.

[16] C. Akbar, Y. Li, and W.-L. Sung, "Deep learning algorithms for the work function fluctuation of random nanosized metal grains on gate-all-around silicon nanowire MOSFETs," *IEEE Access*, vol. 9, pp. 73467–73481, May 2021.

[17] J. J. Gu, X. W. Wang, J. Shao, A. T. Neal, M. J. Manfra, R. G. Gordon, and P. D. Ye, "III-V gate-all-around nanowire MOSFET process technology: From 3D to 4D," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2012, pp. 23.7.1–23.7.4.

[18] W. Zhang, X. Wang, M. S. A. Dahidah, G. N. Thompson, V. Pickert, and M. A. Elgendy, "An investigation of gate voltage oscillation and its suppression for SiC MOSFET," *IEEE Access*, vol. 8, pp. 127781–127788, Jul. 2020.

[19] J. Zhang, H. Wu, J. Zhao, Y. Zhang, and Y. Zhu, "A resonant gate driver for silicon carbide MOSFETs," *IEEE Access*, vol. 6, pp. 78394–78401, Dec. 2018.

[20] M. Jin, Q. Gao, Y. Wang, and D. Xu, "A temperature-dependent SiC MOSFET modeling method based on MATLAB/simulink," *IEEE Access*, vol. 6, pp. 4497–4505, Nov. 2018.

[21] Y. Kang, H. Kim, J. Lee, Y. Son, B.-G. Park, J. D. Lee, and H. Shin, "Modeling of polysilicon depletion effect in recessed-channel MOSFETs," *IEEE Electron Device Lett.*, vol. 30, no. 12, pp. 1371–1373, Dec. 2009.

[22] M. A. Uchechukwu and V. M. Srivastava, "Channel length scaling pattern for cylindrical surrounding double-gate (CSDG) MOSFET," *IEEE Access*, vol. 8, pp. 121204–121210, Jul. 2020.

[23] S. K. Saha, "Compact MOSFET modeling for process variability-aware VLSI circuit design," *IEEE Access*, vol. 2, pp. 104–115, Feb. 2014.

[24] K. Ganapathi, Y. Yoon, and S. Salahuddin, "Analysis of InAs vertical and lateral band-to-band tunneling transistors: Leveraging vertical tunneling for improved performance," *Appl. Phys. Lett.*, vol. 97, no. 3, Jul. 2010, Art. no. 033504.

[25] G. N. Balaji, S. C. Pandian, and D. Rajesh, "Fast test pattern generator using ATALANTA M 2.0," *Asian J. Res. Social Sci. Hum.*, vol. 7, no. 2, pp. 721–729, Feb. 2017.

[26] J. Mo, E. Lind, and L.-E. Wernersson, "InP drain engineering in asymmetric InGaAs/InP MOSFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 501–506, Feb. 2015.

[27] J. Mo, E. Lind, and L.-E. Wernersson, "Asymmetric InGaAs/InP MOSFETs with source/drain engineering," *IEEE Electron Device Lett.*, vol. 35, no. 5, pp. 515–517, May 2014.

[28] X. Zhang, H. Guo, H.-Y. Lin, Ivana, X. Gong, Q. Zhou, Y.-R. Lin, C.-H. Ko, C. H. Wann, and Y.-C. Yeo, "Reduction of off-state leakage current in $In_{0.7}Ga_{0.3}As$ channel n-MOSFETs with self-aligned Ni-InGaAs contact metallization," *Electrochem. Solid-State Lett.*, vol. 14, no. 5, pp. H212–H214, 2011.

[29] P.-C. Chang, C.-J. Hsiao, F. J. Lumbantoruan, C.-H. Wu, Y.-K. Lin, Y.-C. Lin, S. M. Sze, and E. Y. Chang, "InGaAs junctionless FinFETs with self-aligned Ni-InGaAs S/D," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 856–860, Jul. 2018, doi: 10.1109/JEDS.2018.2859811.

[30] Y. Xuan, Y. Q. Wu, H. C. Lin, T. Shen, and P. D. Ye, "Submicrometer inversion-type enhancement-mode InGaAs MOSFET with atomic-layer-deposited Al_2O_3 as gate dielectric," *IEEE Electron Device Lett.*, vol. 28, no. 11, pp. 935–938, Nov. 2007.

[31] R. Chau, S. Datta, and A. Majumdar, "Opportunities and challenges of III–V nanoelectronics for future high-speed, low-power logic applications," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp.*, Palm Springs, CA, USA, Oct. 2005, pp. 1–4.

[32] W.-S. Cho, M. Luisier, D. Mohata, S. Datta, D. Pawlik, S. L. Rommel, and G. Klimeck, "Full band atomistic modeling of homo-junction InGaAs band-to-band tunneling diodes including band gap narrowing," *Appl. Phys. Lett.*, vol. 100, no. 6, Feb. 2012, Art. no. 063504.

[33] V. M. Srivastava and G. Singh, *MOSFET Technologies for Double-Pole Four-Throw Radio-Frequency Switch*. Cham, Switzerland: Springer, Oct. 2013.

[34] Q. Smets, D. Verreck, A. S. Verhulst, R. Rooyackers, C. Merckling, M. Van De Put, E. Simoen, W. Vandervorst, N. Collaert, V. Y. Thean, B. Sorée, G. Groeseneken, and M. M. Heyns, "InGaAs tunnel diodes for the calibration of semi-classical and quantum mechanical band-to-band tunneling models," *J. Appl. Phys.*, vol. 115, no. 18, May 2014, Art. no. 184503.

[35] S. K. Dargar and V. M. Srivastava, "Design of double-gate tri-active layer channel based IGZO thin-film transistor for improved performance of ultra-low-power RFID rectifier," *IEEE Access*, vol. 8, pp. 194652–194662, Oct. 2020.

[36] G. Dewey, B. Chu-Kung, R. Kotlyar, M. Metz, N. Mukherjee, and M. Radosavljevic, "I–V field effect transistors for future ultra-low power applications," in *Proc. Symp. VLSI Technol. (VLSIT)*, Honolulu, HI, USA, Jun. 2012, pp. 45–46.

[37] S. Takagi and M. Takenaka, "Ge/III–V MOS device technologies for low power integrated systems," in *Proc. 45th Eur. Solid State Device Res. Conf. (ESSDERC)*, Graz, Austria, Sep. 2015, pp. 20–25.

[38] K. K. Bhuwalka, Z. Wu, H.-K. Noh, W. Lee, M. Cantoro, Y.-C. Heo, S. Jin, W. Choi, U. Kwon, S. Maeda, K.-H. Lee, and Y.-K. Park, "$In_{0.53}Ga_{0.47}As$-based nMOSFET design for low standby power applications," *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 2816–2823, Sep. 2015.

[39] Y. Mishima, T. Kanazawa, H. Kinoshita, E. Uehara, and Y. Miyamoto, "InGaAs tri-gate MOSFETs with MOVPE regrown source/drain," in *Proc. 72nd Device Res. Conf.*, Santa Barbara, CA, USA, Jun. 2014, pp. 121–122.

[40] V. M. Srivastava, K. S. Yadav, and G. Singh, "Design and performance analysis of cylindrical surrounding double-gate MOSFET for RF switch," *Microelectron. J.*, vol. 42, no. 10, pp. 1124–1135, Oct. 2011.

[41] S. Lee, C.-Y. Huang, A. D. Carter, J. J. M. Law, D. C. Elias, V. Chobpattana, B. J. Thibeault, W. Mitchell, S. Stemmer, A. C. Gossard, and M. J. W. Rodwell, "High transconductance surface channel $In_{0.53}Ga_{0.47}As$ MOSFETs using MBE source-drain regrowth and surface digital etching," in *Proc. Int. Conf. Indium Phosph. Rel. Mater. (IPRM)*, Kobe, Japan, May 2013, pp. 1–2, doi: 10.1109/ICIPRM.2013.6562630.

[42] T. Kanazawa, K. Wakabayashi, H. Saito, R. Terao, T. Tajima, S. Ikeda, Y. Miyamoto, and K. Furuya, "Submicron InP/InGaAs composite channel MOSFETs with selectively regrown N^+-source/drain buried in channel undercut," in *Proc. 22nd Int. Conf. Indium Phosph. Rel. Mater. (IPRM)*, Takamatsu, Japan, Jun. 2010, pp. 37–40.

[43] H. Kinoshita, N. Kise, A. Yukimachi, T. Kanazawa, and Y. Miyamoto, "Operation of 16-nm InGaAs channel multi-gate MOSFETs with regrown source/drain," in *Proc. Compound Semiconductor Week (CSW), Includes 28th Int. Conf. Indium Phosph. Rel. Mater. (IPRM) 43rd Int. Symp. Compound Semiconductors (ISCS)*, Toyama, Japan, Jun. 2016, pp. 1–2.

[44] M. Egard, L. Ohlsson, M. Ärlelid, K.-M. Persson, M. Borg, F. Lenrick, R. Wallenberg, E. Lind, and E. L. Wernersso, "High-frequency performance of self-aligned gate last surface channel $In_{0.53}Ga_{0.47}As$ MOSFET," *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 369–371, Mar. 2012.

[45] M. Passlack, "Off-state current limits of narrow bandgap MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 11, pp. 2773–2778, Nov. 2006.

[46] Z. Gong, H. Chang, S. Wang, Y. Li, B. Sun, and H. Liu, "Simulation study of an enhancement-mode n-type InGaAs MOSFETs with a low zero bias off-current," in *Proc. IEEE Int. Nanoelectron. Conf. (INEC)*, Chengdu, China, May 2016, pp. 1–2.

[47] J. Lin, D. A. Antoniadis, and J. A. D. Alamo, "Physics and mitigation of excess OFF-state current in InGaAs quantum-well MOSFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 5, pp. 1448–1455, May 2015.

[48] J. Lin, D. A. Antoniadis, and J. A. D. Alamo, "Off-state leakage induced by band-to-band tunneling and floating-body bipolar effect in InGaAs quantum-well MOSFETs," *IEEE Electron Device Lett.*, vol. 35, no. 12, pp. 1203–1205, Dec. 2014.

[49] S. Kim, J. D. Song, M. A. Alam, H.-J. Kim, S. K. Kim, S. Shin, J.-H. Han, D.-M. Geum, J.-P. Shim, S. Lee, H. Kim, and G. Ju, "Highly stable self-aligned Ni-InGaAs and non-self-aligned Mo contact for monolithic 3-D integration of InGaAs MOSFETs," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 869–877, Mar. 2019, doi: 10.1109/JEDS.2019.2907957.

[50] J. Villa, I. Ramiro, J. M. Ripalda, I. Tobías, P. García-Linares, E. Antolin, and A. Martí, "Contribution to the study of sub-bandgap photon absorption in quantum dot InAs/AlGaAs intermediate band solar cells," *IEEE J. Photovolt.*, vol. 11, no. 2, pp. 420–428, Mar. 2021.

[51] R. J. W. Hill, D. A. J. Moran, X. Li, H. Zhou, D. Macintyre, S. Thoms, A. Asenov, P. Zurcher, K. Rajagopalan, J. Abrokwah, R. Droopad, M. Passlack, and I. G. Thayne, "Enhancement-mode GaAs MOSFETs with an $In_{0.3}Ga_{0.7}As$ channel, a mobility of over 5000 cm^2/V·s, and transconductance of over 475 μS/μm," *IEEE Electron Device Lett.*, vol. 28, no. 12, pp. 1080–1082, 27 Dec. 2007.

[52] D. Sen, B. Goswami, A. Dey, P. Saha, and S. K. Sarkar, "Impact of self-heating and nano-gap filling factor on AlGaAs/GaAs junction-less DG-MOSFET based biosensor for early stage diagnostics," in *Proc. IEEE Region 10 Symp. (TENSYMP)*, Dhaka, Bangladesh, Jun. 2020, pp. 662–665.

[53] M. Allaei, M. Shalchian, and F. Jazaeri, "Modeling of short-channel effects in GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 67, no. 8, pp. 3088–3094, Aug. 2020.

NAVEENBALAJI GOWTHAMAN (Member, IEEE) was born in Kumbakonam, India, in 1990. He received the B.E. degree in electronics and communication engineering and the M.E. and Ph.D. degrees in VLSI design from Anna University, Tiruchirappalli, India, in 2011, 2013, and 2019, respectively.

He has worked for VLSI circuit design using electronic simulators. He is currently a Postdoctoral Research Scholar with the Department of Electronic Engineering, Howard College, University of KwaZulu-Natal, Durban, South Africa. He has more than seven years of teaching and research experience in VLSI design, microprocessors, and microcontrollers. He has supervised various bachelor's and master's projects. He has authored and coauthored more than 100 technical offerings, including articles in international refereed journals, book chapters, and international/national conferences. He has co-edited the book *Advanced Controllers for Smart Cities – An Industry 4.0 Perspective* (Springer Nature, Switzerland AG), which presents applications of advanced microcontrollers that can control large systems and devices. His research interests include cylindrical surrounding double-gate MOSFETs, low power VLSI circuits, testing of VLSI circuits, and digital electronics.

Dr. Gowthaman has become an Active Member of the IEEE Smart Grid and Smart City Community and the India Chapter. He is also a member of ISTE, India (LM'17); IETE, India (LM'17); and IAENG (M'15). He was a recipient of the Best Teaching Faculty, in 2017; the Innovative Research and Dedicated Teaching Professional Award, in 2018; the Young Scientist Award, in 2018, the Outstanding Researcher Award, in 2018; and the Bright Engineer Award, in 2019. He is an Associate Editor and a Reviewer in various peer-review journals, including IET and Springer.

VIRANJAY M. SRIVASTAVA (Senior Member, IEEE) received the bachelor's degree in electronics and instrumentation engineering, in 2002, the master's degree in VLSI design, in 2008, and the Ph.D. degree in RF microelectronics and VLSI design, in 2012.

He has worked on the fabrication of devices and the development of circuit design. He is currently working with the Department of Electronic Engineering, Howard College, University of KwaZulu-Natal, Durban, South Africa. He has more than 19 years of teaching and research experience in the area of VLSI design, RFIC design, and analog IC design. He has supervised various bachelor's, master's and doctorate theses. He is a Professional Engineer of ECSA, South Africa. He is the author/coauthor of more than 270 scientific contributions, including articles in international refereed journals and conferences and also the author of various books.

Dr. Srivastava is a Life Member of IEEE-HKN, a Senior Member of SAIEE, and a member of IET and IITPSA. He has worked as a reviewer for several journals and conferences, both national and international.